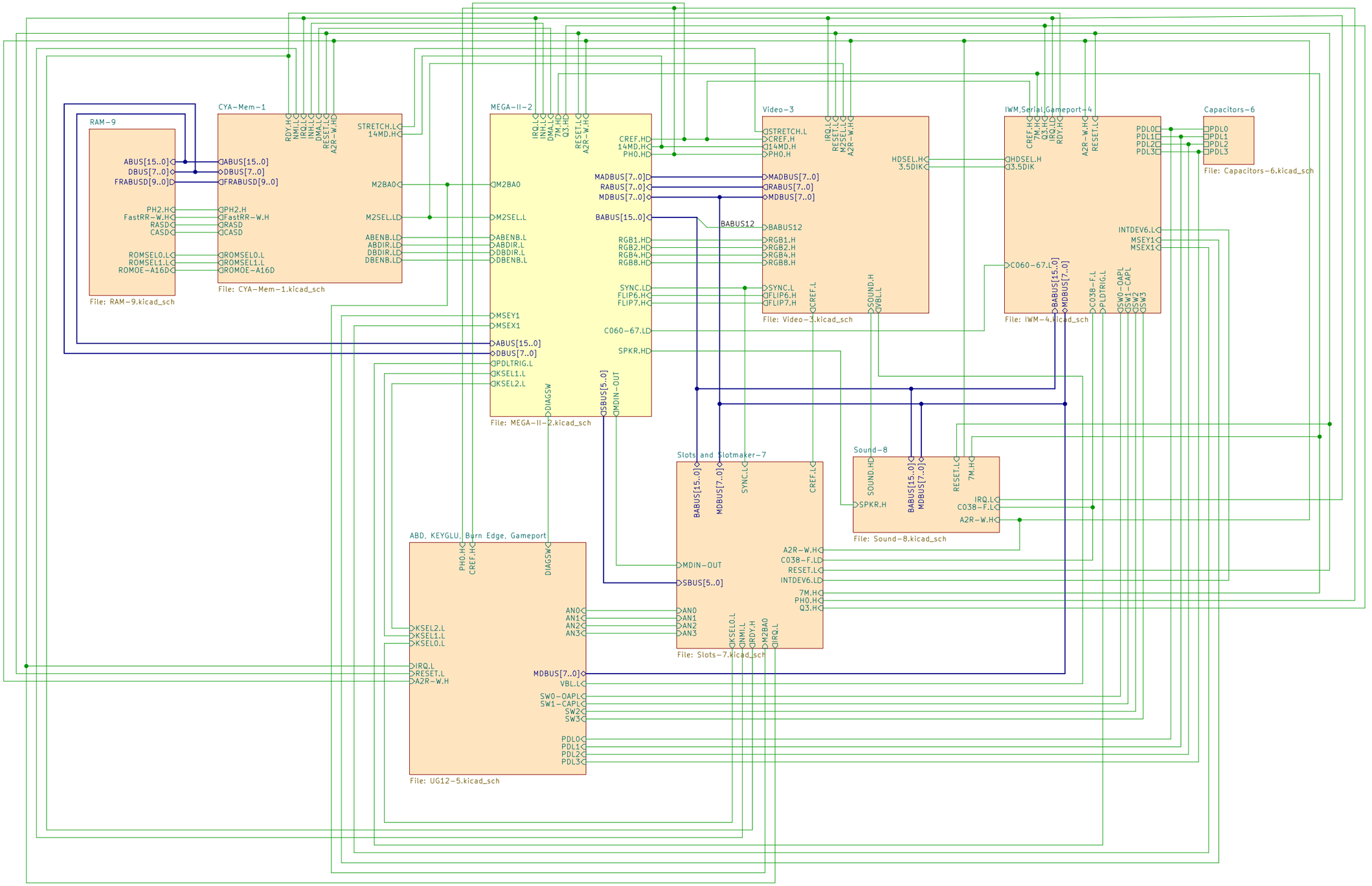


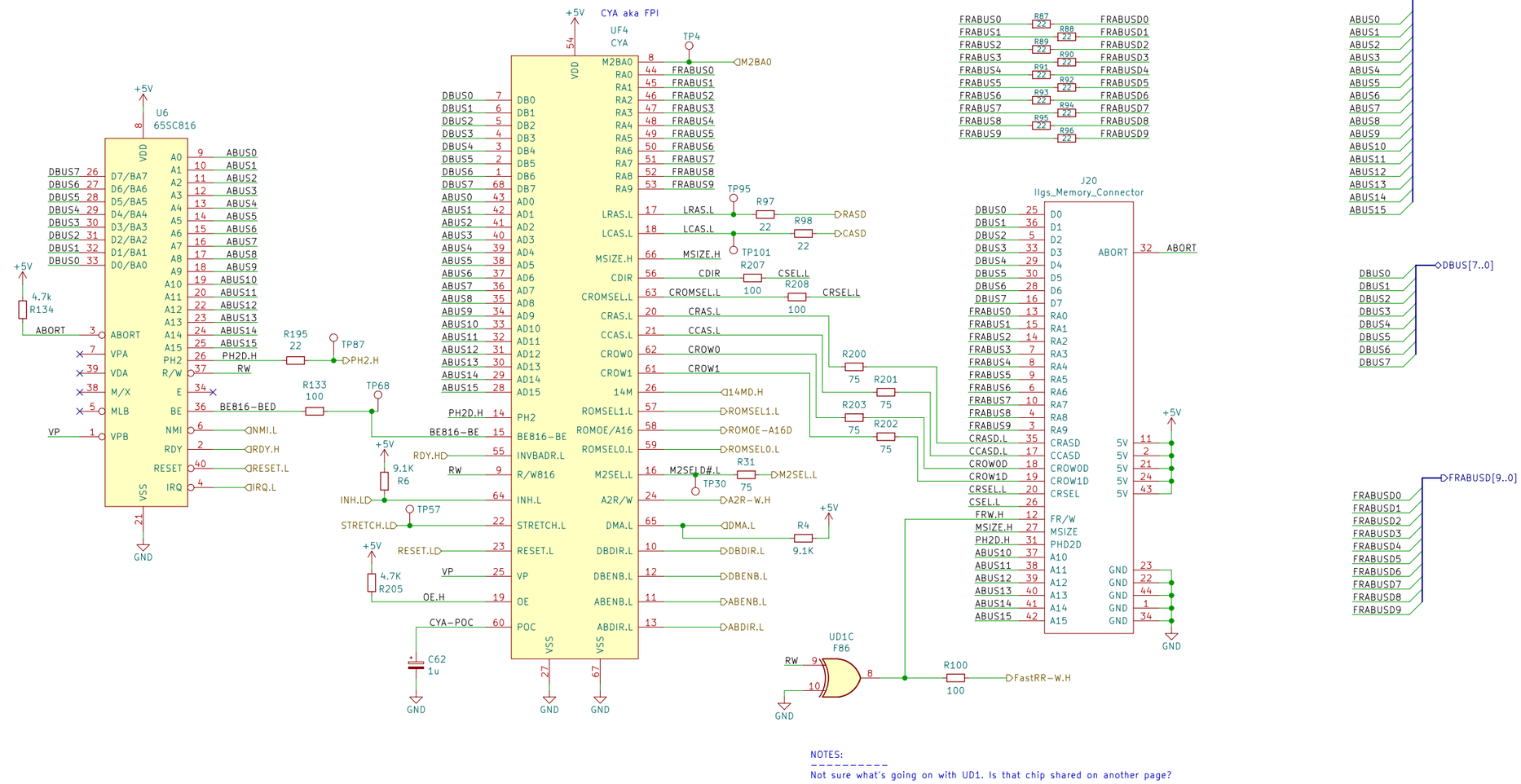
Redrawn by james@baldengineer

bald.ee/bitpreserve

Sheet: /
File: IIgs Schematic.kicad_sch

Title: Apple IIgs ROM3 / 1 Mb

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 1/10



Redrawn by james@baldengineer
ROM3 / 1 Mb Ilgs
bald.ee/bitpreserve

Sheet: /CYA-Mem-1/
File: CYA-Mem-1.kicad_sch

Title: CPU and Fast Memory Controller (CYA)

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 2/10

KSEL0.LD KSEL0.L TP28
KSEL1.LD KSEL1.L TP14
KSEL2.LD KSEL2.L TP29

UG12
M50741
Mitsubishi 740 Microcontroller
(6502 based)
for ADB

RP1
2.2K
UI12-16
UI12-15
UI12-14
UI12-13
UI14-35
UI14-34

RP2
2.2K
UI12-19
UI12-12
UI12-11
UI12-10
UI12-9
UI12-8
UI12-6
UI12-5
UI12-4

R151 4.7k
RR152 4.7k
SW1-CAPL
SW0-OAPL
CP-CNTL

UI12
KEYGLU
No Power or GND Pins?
Does KEYGLU also do matrix decoding?!
(For the Apple IIe Keyboard connector)
MDBUS[7..0]
MDBUS0
MDBUS1
MDBUS2
MDBUS3
MDBUS4
MDBUS5
MDBUS6
MDBUS7
IRQ.LD
A2R-W.HD
PH0.HD
RESET.LD
VBL.LD
TP76
TP77

S1
CP-CNTL
R217 4.7k

J23
Edge Conn Burn-In
SW0-OAPL
DIAGSW
AN1
AN0
-12V
+12V
-5V

CR2
1N914
R105 200k
R105-2
CREF.H
CREF.HD
TP74
C39 1u

J21
Game-IO
SW0-OAPL
SW1-CAPL
SW2
R117 4.7K
STB.L
PDL0
PDL2
AN0
AN1
AN2
AN3
PDL1
PDL3
PDL1
SW3

J18
Apple Desk Top Bus
L2-1
L2-2
L2-3
SHLD
GNDPWR
BC91 10n
L2
D-15C
L2-8
R107 470
2N3904 Q4
Q4-1
R108 4.7K
ADB
TP83
TP78
R150 4.7K

Redrawn by james@baldengineer
ROM3 / 1 Mb IIgs
bald.ee/bitpreserve
Sheet: /ABD, KEYGLU, Burn Edge, Gameport/
File: UG12-5.kicad_sch

Title: UG12, Keyboard GLU, Burn-In, Gameport

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 3/10

UJ5-1, UJ5-19, UI5-1, UI5-19 refer to buffer locations on 256k schematic!

ABUSxx – Address bus from CPU
DBUSxx – Data bus from CPU
BABUSxx – Buffered Address Bus to MEGA II
RABUSx – DRAM Row/Column Bus
SBUS – Slot Selector

MDBUS – Main Data Bus
ADBUS – Aux Data Bus
MADBUS – Muxed(?) Aux Data Bus

NOTE: All of these data busses only exist on 1MB board.
On 256kb Board there is only: ABUS, DBUS, MDBUS, and ADBUS.

RGBx = 4-bit linear-weighted binary value that gets decoded by VGC

MDIN-OUT controls Main Data on Slots

SERVIDEO = Test Signal. Composite w/out Sync

256k: UM4-14, UM4-10
1M: UK4-14, UK4-10

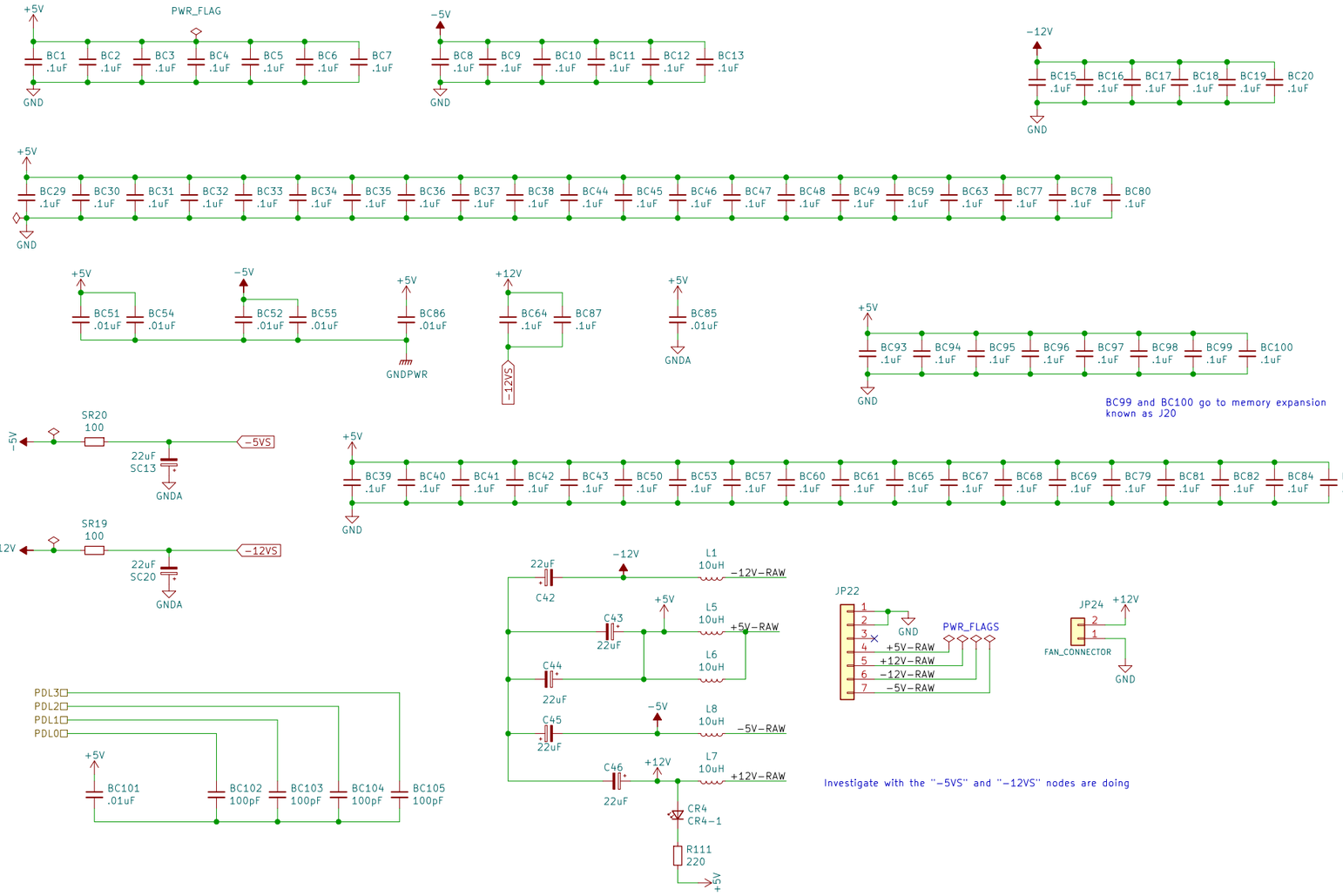
TIL the Apple II memory map is a nightmare. "Thanks" Woz! J/K You're awesome! -James

Redrawn by james@baldengineer
ROM3 / 1 Mb IIgs
bald.ee/bitpreserve

Sheet: /MEGA-II-2/
File: MEGA-II-2.kicad_sch

Title: MEGA-II for IIgs ROM3

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 4/10



Redrawn by james@baldengineer
ROM3 / 1 Mb Ilgs
bald.ee/bitpreserve

Sheet: /Capacitors−6/
File: Capacitors−6.kicad_sch

Title: Capacitors (and Power Connector)

Size: A3	Date: 2023−01−28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 5/10

RABUS[7..0]
RABUS0
RABUS1
RABUS2
RABUS3
RABUS4
RABUS5
RABUS6
RABUS7

MDBUS[7..0]
MDBUS0
MDBUS1
MDBUS2
MDBUS3
MDBUS4
MDBUS5
MDBUS6
MDBUS7

MADBUS[7..0]
MADBUS7
MADBUS6
MADBUS5
MADBUS4
MADBUS3
MADBUS2
MADBUS1
MADBUS0

MDBUSx goes back to MEGA-II

STRETCH:
Every 65 clocks, A2 must have 1 longer clock period. For each Horizontal line.

All clocks derived from 28.636360 MHz Xtal

VGC generates 14M
Mega-II generates all other clocks

C30 56p
R106 100
OS1 28.636360 MHz
+5V
UH2-43
SYNC.LD
TP160
R30 1k

UF2+5V
VGC
C61 1000u
GND

VIDx - 12-bit binary values for RGB

RP3
MADBUS0
MADBUS1
MADBUS2
MADBUS3
MADBUS4
MADBUS5
MADBUS6
MADBUS7
VADBUS0
VADBUS1
VADBUS2
VADBUS3
VADBUS4
VADBUS5
VADBUS6
VADBUS7

RP4
RABUS0
RABUS1
RABUS2
RABUS3
RABUS4
RABUS5
RABUS6
RABUS7
VRABUS0
VRABUS1
VRABUS2
VRABUS3
VRABUS4
VRABUS5
VRABUS6
VRABUS7

UC2
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
R/W
STRETCH
FLIP7
FLIP6
14M
RGB1
RGB2
RGB4
RGB8
M2SEL/CA
SYNC
PH0
IRQ
28M
RESET
HDSEL
A12
EXTIRQ
TEST
POC
VDD
VSS
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VID7
VID8
VID9
VID10
VID11
COMP/SYN
MONO/COLOR
VBL
CLKCS
DATA
CLK
1SEC
3.5DIK

MDBUS0
MDBUS1
MDBUS2
MDBUS3
MDBUS4
MDBUS5
MDBUS6
MDBUS7
A2R-W.H
STRETCH.L
FLIP7.H
FLIP6.H
14M.H
RGB1.H
RGB2.H
RGB4.H
RGB8.H
M2SEL.LD
PH0.H
IRQ.LD
28M
RESET.LD
HDSEL.HD
BABUS12
UH2-40
U18TEST
UH2-44
A2R-W.H
STRETCH.L
MONO-COLOR
VBL.L
TP5
UG3-5
UG3-6
UG3-7
UG3-1
3.5DIK
COMP-SYN

TP189
R206 75
14MD.H
TP93
R196 4.7k
R11 1k
TP112
C59 1u

H2, H3, and H4 form DAC for RGB video

H2
H3
H4
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VID7
VID8
VID9
VID10
VID11
H2-6
H2-1
H3-6
H3-1
H4-6
H4-1

H1
-5V
+5V
IN1
IN2
IN3
SYNCIN
OUT1
OUT2
OUT3
GND
H2-1
H3-1
H4-1
COMP-BLUE
COMP-GREEN
COMP-RED
C32 33p
C31 33p
C29 33p
COMP-SYN

Q3
2n3904
+12V
TP127
R114 220
R114-1
R114-2
L12 1.5u
COMSYNC
R10 1.5K

J10
Video Connector
COMP-RED
COMSYNC
COMP-GREEN
COMP-BLUE
1.245V
SOUND.HD
R54-2
C100 120p
C101 120p
C102 120p

TP61
TP59
R17-1
C23 56p
R17 1k
UC2-13
C18 27p
R13 1k
R13-1
Q2-3
R14 1k
TP60
C19 .001u
UC2-10
R193 100
R14-2
C60 22u
GNDREF
+12V
+5V
TP58
R191 4.7k
C17 0.1u
MONO-COLOR
Q1 2n3904
R12 220
Q2 2n3904

TP26
CREF.HD
CREF.L
UE7B 74LS02
R15 1.5k
C33 220p
UC2-17
R135-1
R135 470
TP67

NOTE: Place the two inductors, L3 and L4 at right angles to each other

L3-1
L3 10u
L4-1
L4 10u
C3 18p
C1 56p
C2 18p
R18 470
+12V
UC2-6
UC2-8
H4-6
H3-6
H2-6
C22 22u
C21 22u
C20 22u
UC2-3
UC2-4
UC2-5
UC2
B
G
R
GND
+12V
SEL
CHROME
NC
UB2
MC1377
2 COMP-SYN
(pin 2 label not from schematic)
20 UC2-20
9 UC2-9
16 UC2-16
1
UC2-13
UC2-10
UC2-17
UC2-11
UC2-12
UC2-7
UC2-19
R19 470
R138
R9 100
220
R16 51k
C7 0.1u
C8 1n
C9 0.1u
C11 0.01u
C10 0.1u
C12 0.01u
C6 1000u
6.3V
R54-1
R54 75
R54-2
R8 75
R8-2
TF1
J11-1
J11
RCA MONO OUT

TP214 VADBUS1
TP212 VADBUS3
TP210 VADBUS5
TP208 VADBUS7
TP215 VADBUS0
TP213 VADBUS2
TP211 VADBUS4
TP209 VADBUS6

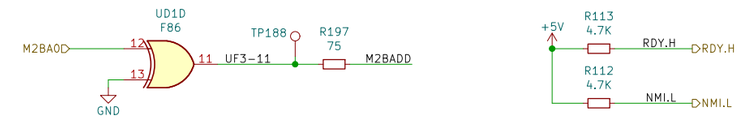
TP201 VRABUS1
TP204 VRABUS3
TP206 VRABUS5
TP200 VRABUS7
TP202 VRABUS0
TP203 VRABUS2
TP205 VRABUS4
TP207 VRABUS6

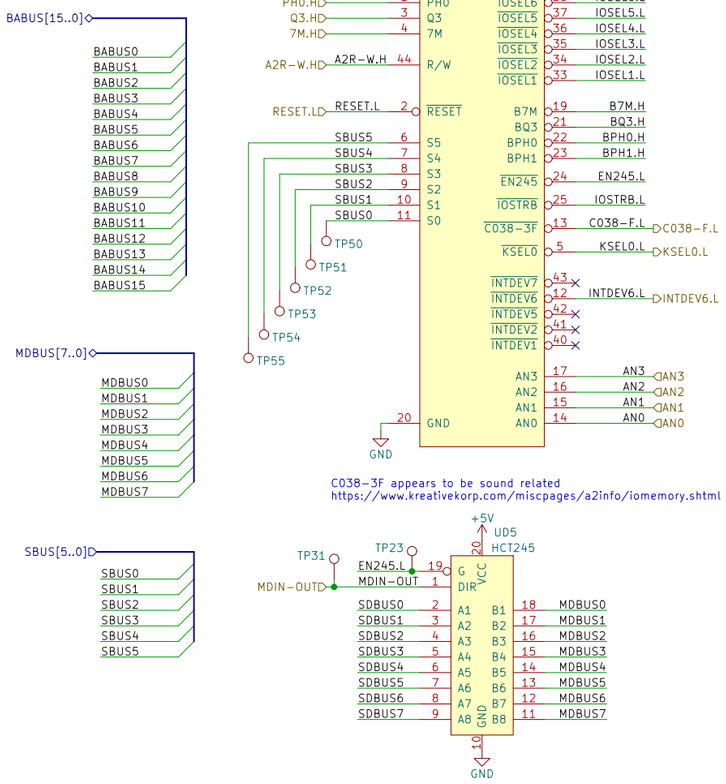
TP99
TP100
R75 1k
R75-2
CR5 1N914
CR3 1N914
PWR_FLAG
B1 Lithium Batt
C38 0.1u
UD4
SERCLK
EN
DATA
CLK
1SEC
VCC
XIN
XOUT
GND
UG3-5
UG3-6
UG3-7
UG3-1
UG3-2
UG3-3
C37 10p
Y1 32.768 kHz
C36 33p
R192 4.7k
R118 4.7k

Redrawn by james@baldengineer
ROM3 / 1 Mb IIgs
bald.ee/bitpreserve
Sheet: /Video-3/
File: Video-3.kicad_sch

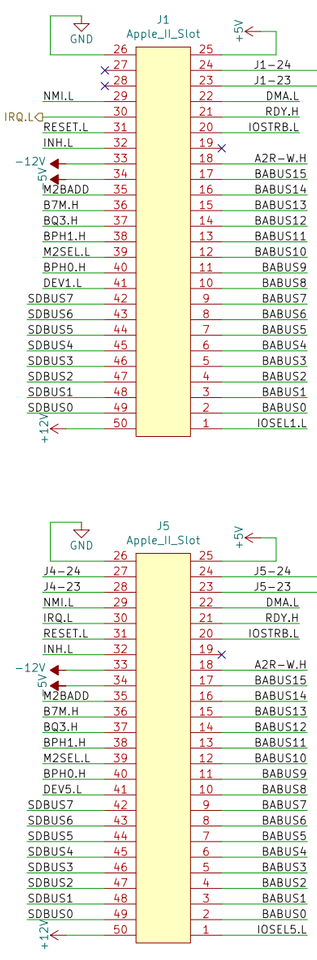
Title: VGA, Digital RGB, and Composite

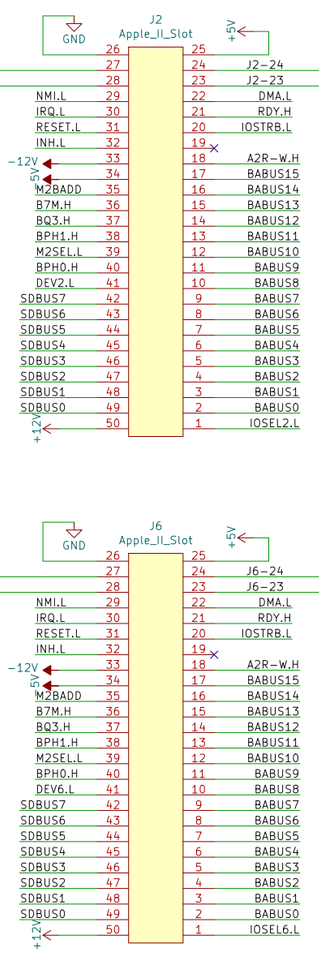
Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 6/10

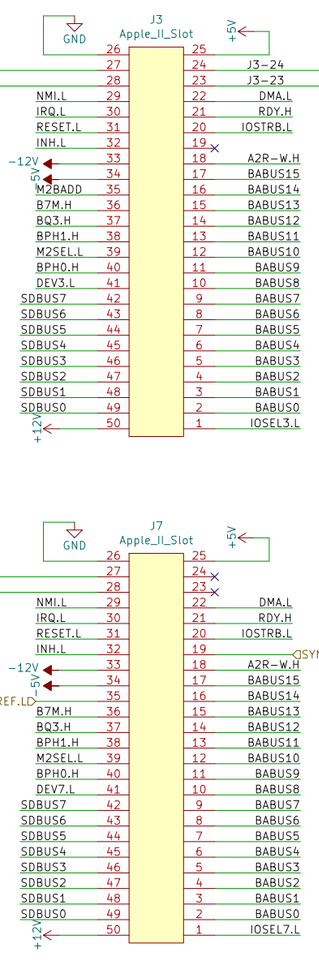


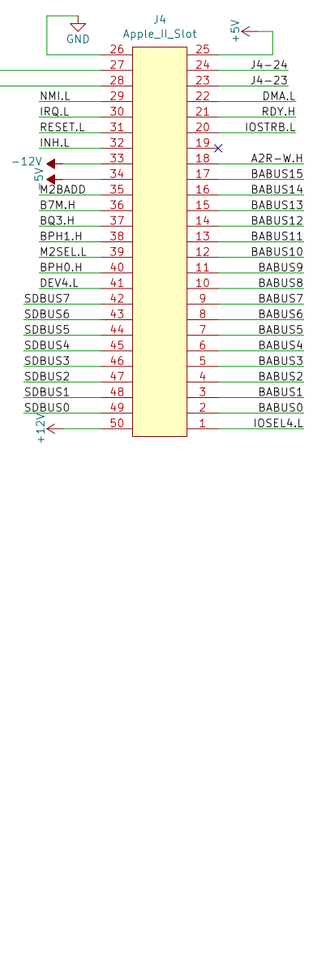


C038-3F appears to be sound related
https://www.kreativekorp.com/miscpages/a2info/iomemory.shtml









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ROM3 / 1 Mb IIgs
bald.ee/bitpreserve

Sheet: /Slots and Slotmaker-7/
File: Slots-7.kicad_sch

Title: Slot and Slotmaker

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 7/10

BABUS[15..0]
BABUS0
BABUS1
BABUS2
BABUS3
MDBUS[7..0]
MDBUS0
MDBUS1
MDBUS2
MDBUS3
MDBUS4
MDBUS5
MDBUS6
MDBUS7
Note: PH0 and PH2 refer to stepper phases, and not the 6502/816 clocks!
UC5
IWM
+5V
GND
SENSE
RDATA
WDAT
WREQ
PH3
PH2
PH1
PH0
EN1
EN2
R32 22
R33 22
R34 22
R35 22
R36 22
R37 22
R38 22
R39 22
J8-19
J8-15
J8-14
J8-13
J8-12
J8-11
J8-17
J8-9
TP163
TP164
TP162
TP161
TP165
TP166
TP167
TP168
J8
-12V
3.5DIK
HDSEL.H
TP111
TP153
R120 470
R190 470
J8-4
J8-16
UC12
AM26LS32
H5A
RC4300
MSEX1
UE15-21
UE15-22
UC15-2
UC15-1
UC15-15
UC15-7
RXDA.H
RXDA.L
HSKIA.H
GPIA.H
Serial 1
J15
J15-1
HSKIA.H
J15-3
GAME.GND
RXDA.L
J15-6
GPIA.H
RXDA.H
L10 10u
UB13
26LS30
H5B
UE15-16
UE15-20
UE15-19
UB15-15
UB15-14
UB15-10
J15-6
J15-3
J15-1
7M.H
Q3.H
INTDEV6.L
TP3
TP27
UD12A
74LS74
UD12B
74LS74
RESET.L
DRES.H
RDY.HD
IRQ.L
UE7A
74LS02
A2R-W.HD
UD14-4
UF9-1
GND
TP73
TP117
TP116
U13B
74LS51
U13A
74LS51
TP70
TP71
TP69
UE7D
74LS02
UE7C
74LS02
BABUS2
C038-F.L
TP118
TP72
UF9-88
UE15-38
UF13
8530L
IRQ.L
UE15-40
UE15-41
UE15-38
CREF.H
UE15-13
BABUS0
BABUS1
MDBUS0
MDBUS1
MDBUS2
MDBUS3
MDBUS4
MDBUS5
MDBUS6
MDBUS7
RXDA.H
DCDA.H
CTSA.L
TRXCA.L
TXDA.H
RTSA.L
DTR/REQA.L
RXDB.H
CTSB.L
TRXCB.L
DCDB.L
TXDB.H
RTSB.L
DTR/REQB.L
UE15-22
UE15-21
UE15-16
UE15-20
UE15-19
UE15-25
UE15-24
UE15-29
UE15-26
UE15-27
MSEX1
MSEY1
Y2
3.6864 MHz
UC13
AM26LS32
H6A
RC4300
UC16-2
UC16-1
UC16-15
UC16-7
RXDB.H
RXDB.L
HSKIB.H
GPIB.H
Serial 2
J16
J16-1
HSKIB.H
J16-3
GAME.GND
RXDB.L
J16-6
GPIB.H
RXDB.H
UB14
26LS30
H6B
UB16-15
UB16-14
UB16-10
J16-6
J16-3
J16-1
UD7
HCT251-Ilgs
C060-67.L
TP10
TP15
TP16
TP17
TP18
SW2
SW3
R2 200K
R1 200K
R86 1K
R85 1K
R84 1K
R83 1K
SW3
SW0-OAPL
SW1-CAPL
CP0.H
CP1.H
CP2.H
CP3.H
MDBUS7
UD6
NE558
PLDTRIG.L
TP11
TRIGGERS
PDL0
PDL1
PDL2
PDL3
R79 100
R80 100
R81 100
R82 100
UE8-2
UE8-15
UE8-10
UE8-7
UE8-4
C28 .1u
TP66
TP62
TP63
TP64
TP65
C24 .022u
C25 .022u
C26 .022u
C27 .022u
J9
Game Port
SW1-CAPL
GAME.GND
PDL2
PDL0
SW0-OAPL
PDL1
PDL3
SW2
C34 0.01u
C35 .01u
C34 & C35
Optional
For Impoved EMI
H5, H6 measure to see if they are resistor networks.
(Looks like: https://www.mouser.com/datasheet/2/54/4100R-776985.pdf, thanks midendian42!)
Redrawn by james@baldengineer
ROM3 / 1 Mb Ilgs
bald.ee/bitpreserve
Sheet: /IWM,Serial,Gameport-4/
File: IWM-4.kicad_sch
Title: IWM, Serial, Gameport
Size: A3
Date: 2023-01-28
Rev: 2
KiCad E.D.A. kicad (6.0.11)
Id: 8/10

TP119 TP120 TP121 TP122 TP123

SORABUS0 SR21 220 SNDRAMBUSD0
SORABUS1 SR22 220 SNDRAMBUSD1
SORABUS2 SR23 220 SNDRAMBUSD2
SORABUS3 SR24 220 SNDRAMBUSD3
SORABUS4 SR25 220 SNDRAMBUSD4
SORABUS5 SR26 220 SNDRAMBUSD5
SORABUS6 SR27 220 SNDRAMBUSD6
SORABUS7 SR28 220 SNDRAMBUSD7

TP124 TP125 TP126

MDBUS[7..0]
MDBUS0 MDBUS1 MDBUS2 MDBUS3 MDBUS4 MDBUS5 MDBUS6 MDBUS7

BABUS[15..0]
BABUS0 BABUS1 BABUS2 BABUS3

+5V

UJ7 SOUNDGLU

MDBUS0	48	D0	RA0	38	SORABUS0
MDBUS1	49	D1	RA1	37	SORABUS1
MDBUS2	50	D2	RA2	36	SORABUS2
MDBUS3	51	D3	RA3	35	SORABUS3
MDBUS4	52	D4	RA4	34	SORABUS4
MDBUS5	53	D5	RA5	33	SORABUS5
MDBUS6	54	D6	RA6	32	SORABUS6
MDBUS7	55	D7	RA7	31	SORABUS7
			E	68	SND-E
BABUS1	65	A1	CAS.L	3	SND-CAS
BABUS0	66	A0	RAS.L	2	SND-RAS
			DOC.L	62	SND-DOC
SND-R-W.H	39	R/W.H	SR/W	63	SND-R-W
BABUS2	64	CS.H	7M	6	7M.H
C038-F.LD	61	DEV.L			
SOADBUS0	30	S0	LA0	18	SND-LA0
SOADBUS1	29	S1	LA1	17	SND-LA1
SOADBUS2	28	S2	LA2	16	SND-LA2
SOADBUS3	27	S3	LA3	15	SND-LA3
SOADBUS4	22	S4	LA4	14	SND-LA4
SOADBUS5	21	S5	LA5	9	SND-LA5
SOADBUS6	20	S6	LA6	8	SND-LA6
SOADBUS7	19	S7	LA7	7	SND-LA7
RESET.LD	1	RESET.L	VC0	41	SND-VC0
+5V	67	MODE	VC1	42	SND-VC1
			VC2	43	SND-VC2
			VC3	47	SND-VC3
		VSSA	VSS		
	40			5	

GNDA

SR35 1K
A2R-W.HD
TP169
SC31 56pF

SR6 75K
SR7 36K
SR8 18K
SR9 9.1K
UM12-2
SR72 27K
SC41 22uF
SC42 0.1uF

TP130 TP131 TP132 TP129

+5V

UK5 DRAM64KX4

SNDRAMBUSD0	6	A0	VCC	9	+5V
SNDRAMBUSD1	8	A1			
SNDRAMBUSD2	7	A2			
SNDRAMBUSD3	13	A3			
SNDRAMBUSD4	12	A4			
SNDRAMBUSD5	11	A5			
SNDRAMBUSD6	14	A6			
SNDRAMBUSD7	10	A7			
	5	RAS	IQ0	2	SOADBUS0
	16	CAS	IQ1	3	SOADBUS1
	4	R/W	IQ2	15	SOADBUS2
	1	OE	IQ3	17	SOADBUS3
			VSS	18	GNDA

GNDREF

+5V

UK6 DRAM64KX4

SNDRAMBUSD0	6	A0	VCC	9	+5V
SNDRAMBUSD1	8	A1			
SNDRAMBUSD0	7	A2			
SNDRAMBUSD1	13	A3			
SNDRAMBUSD0	12	A4			
SNDRAMBUSD1	11	A5			
SNDRAMBUSD0	14	A6			
SNDRAMBUSD1	10	A7			
	5	RAS	IQ0	2	SOADBUS4
	16	CAS	IQ1	3	SOADBUS5
	4	R/W	IQ2	15	SOADBUS6
	1	OE	IQ3	17	SOADBUS7
			VSS	18	GNDA

SR38-1 220
SR37-1 220
SR68-1 220
TP140
SND-CAS
SND-RAS
SND-R-W

SND-SIG+
SC21 10p
SR49 3.9K
TP172
UL12B MC34084
UN14-7
GNDA

SC30 10p
SR31 3.9K
SR51 15K
UN14-11
SR30 3.9K
TP85
SR50 3.9K
UL12C MC34084
J25-3

SND-SIG-
SR13 3.9K
SC46 10p
UL12A MC34084
GNDA

TP173
SR32 3.9K
SC32 10p
GNDA

UN12-1

TP143
SR2-1
SC24 1.5n
GNDA

TP145
SR15-1 15K
SC15 3.9n

UN12-6
UL11B TL072
UN12-5
TP149
SC14 220p
GNDA

TP148
SR16 10K
SR16-2
SR43 10K
TP146
SC17 3.9n
UL11A TL072
UN12-1
UN12-3
TP156
SC16 560p
GNDA
TP157

+12V
SR71 200
SR70 200
PWR_FLAG
SC50 470u/16v
GNDA

SC10 .1u
+12V
22u
SC18
PWR_FLAG
GNDA
22u
SC5
GNDA

UN12-1
SR34 470K
SR1-1
SR1 470K
SR53 10K
SD2 MLL5239
CS40 .1u
GNDA
TP170
SC2 22u
UM12-1
UK11 LM3340
UM12-8
UM12-7
UM12-6
SC43 1.8n
GNDA
UM12-2

TP56 TP171
SPKR.HD
SR33 200K
Q5-1
Q5 2n3904
GNDA

SC44 .1u
UM11-2
UK10 LM380N-8
UM11-8
UM11-6
Schematic not clear on SC44, might be 1.0 uf
GNDA

SOUND.H seems to be a "disconnect" for sound on the monitor connector when the earphone is connected. (unsure)

SOUND.H
SR74 1K
SR75 560
GND
22u
SC6
SR12 220
SR73 100
SR12-2
L17
J12-1
SR46 2.7
TP82
SC19 .1u
GNDA
C4 0.1u
J12 PHONEJACK
J12-11 J12-10 J12-1
J17 SPEAKER
GNDA

+5V

UJ12 DOC5503

			VCC	39	+5V
RESET.LD	20	RES	A8/D0	30	SOADBUS0
IRQ.LD	18	IRQ	A9/D1	29	SOADBUS1
	3	CASM	A10/D2	28	SOADBUS2
	40	BS_A16	A11/D3	27	SOADBUS3
SND-E	5	E_CLK	A12/D4	26	SOADBUS4
	4	Q_CLK	D13/D5	25	SOADBUS5
SND-RAS	2	RAS	A14/D6	24	SOADBUS6
SND-DOC	21	CS	A15/D7	23	SOADBUS7
SND-R-W	22	WE			
7M.H	1	CLK	SIG+	15	SND-SIG+
			SIG-	16	SND-SIG-
			CSTRB	6	J25-6
SND-LA0	38	A0	CA0	7	J25-4
SND-LA1	37	A1	CA1	8	J25-5
SND-LA2	36	A2	CA2	9	J25-7
SND-LA3	35	A3	CA3	10	
SND-LA4	34	A4			
SND-LA5	33	A5	VVREF	11	
SND-LA6	32	A6	VOL-	13	UL14-13
SND-LA7	31	A7	WVREF	14	UL14-14
			VLFDBK	12	UL14-12
		VSS	A/D		
	19			17	

-5VS
-5V

GND GNDA
GNDA

J25
J25-1 J25-3 J25-4 J25-5 J25-6 J25-7

UL12D MC34084
UL14-13
SC45 10p
UL14-12
UL14-14
CR1 1N914
SR40 1K
GNDA

NOTE: Analog ground, as shown on this schematic, shall be separate from digital ground. Digital ground will tie into the DOC-5503 (UL14) At one point only, pin 19, and this point will also be the only place where analog ground ties to digital ground.

Redrawn by james@baldengineer
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Sheet: /Sound-8/
File: Sound-8.kicad_sch

Title: Sound

Size: A3	Date: 2023-01-28	**Rev: 2**
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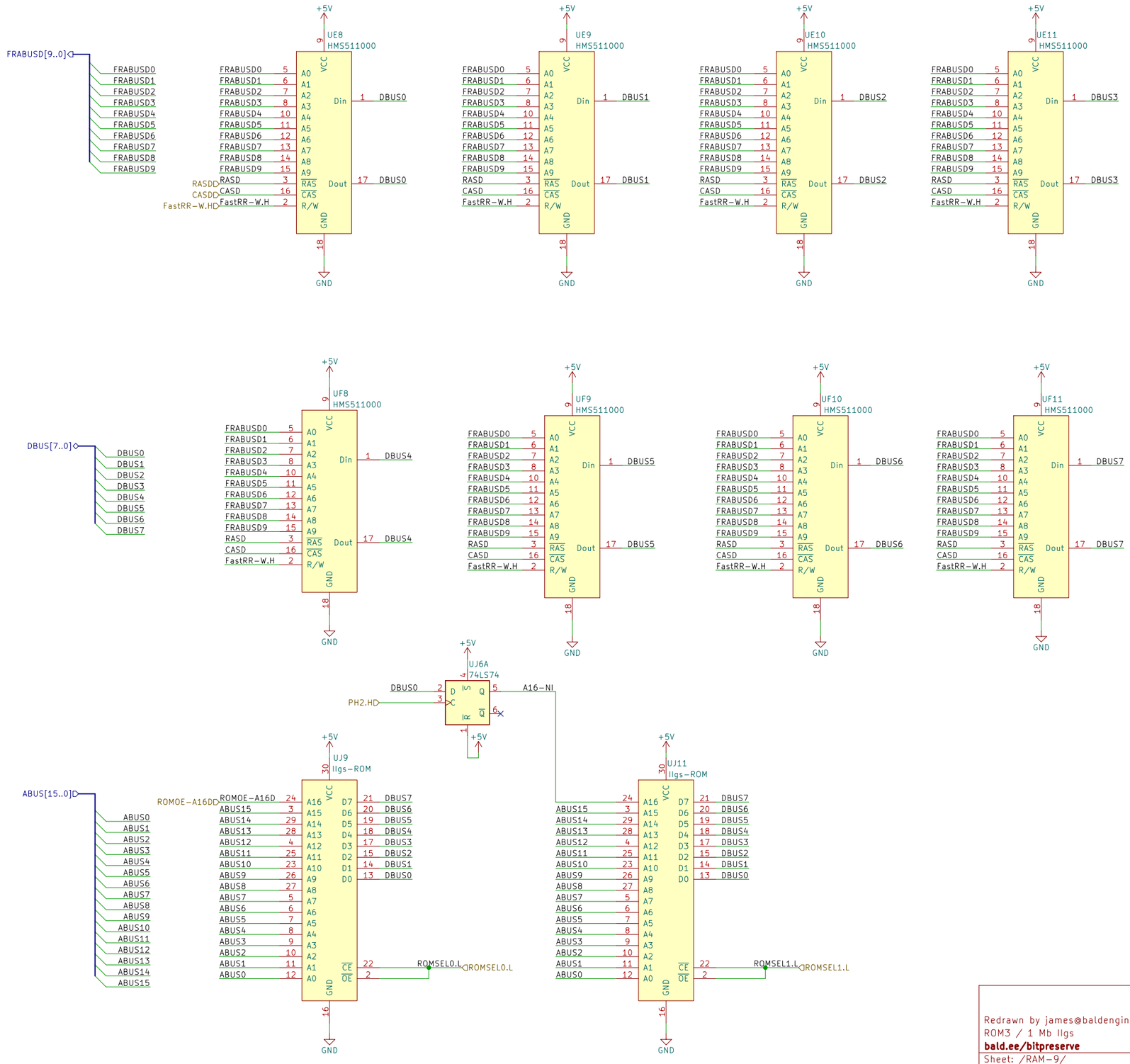

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ROM3 / 1 Mb IIgs
bald.ee/bitpreserve

Sheet: /RAM-9/
File: RAM-9.kicad_sch

Title: RAM

Size: A3	Date: 2023-01-28	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 10/10