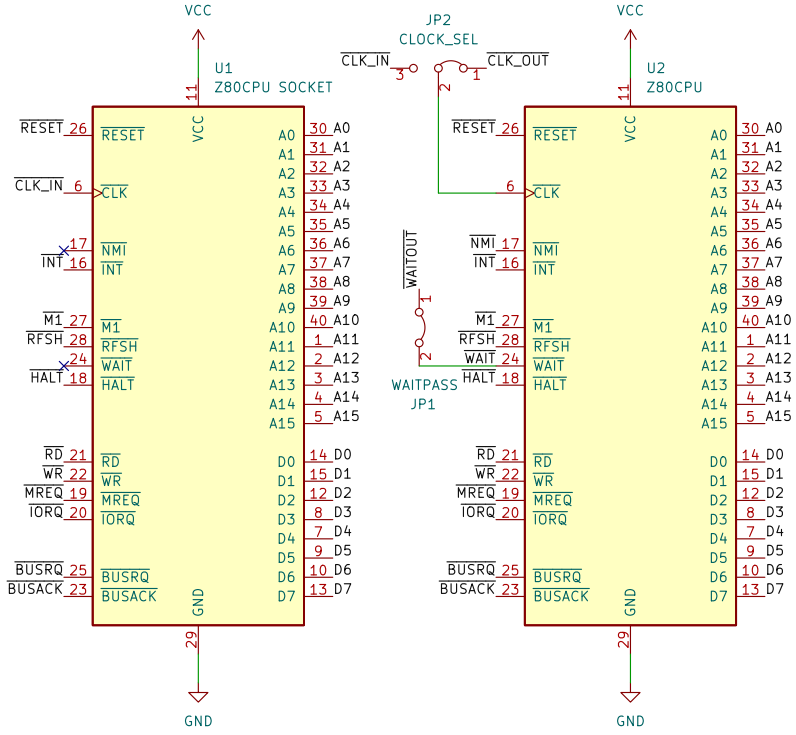
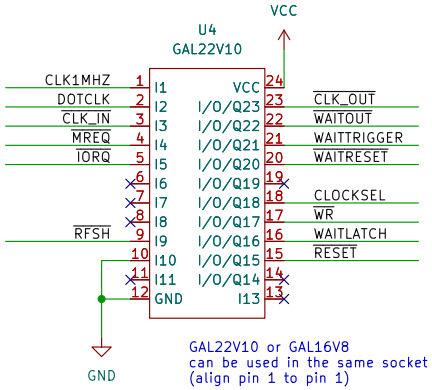
JP1 – when closed pass waitstates from GAL
JP2 – use onboard clock (1–2) or clock from GAL (2–3)
JP3 – GAL option: when closed pass CLK_IN when open pass CLK_OUT to Z80

JP3 should be enough to disable the circuit. If not, then:
1) remove U3 and U4
2) move JP2 to connect pins 1–2
3) open JP1

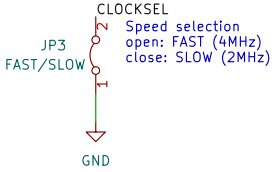
Fast clock is enabled when:
1) JP3 is open
2) JP2 connects pins 1–2
3) JP1 is closed

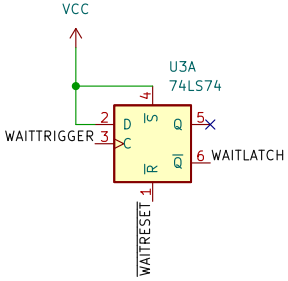


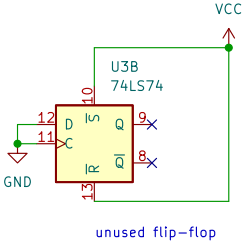
CLK1MHZ from U12 pin 11 (same in C128/D/DCR)
DOTCLK from Expansion port pin 6
NMI is optional, can be left unconnected

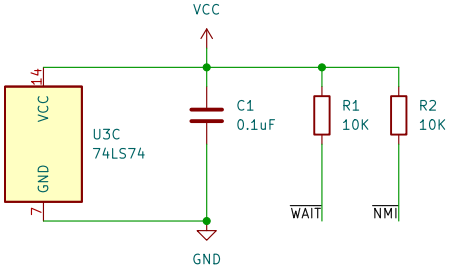


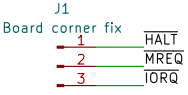
GAL22V10 or GAL16V8
can be used in the same socket
(align pin 1 to pin 1)











This is needed only on C128D equipped with 256K MMU expansion
The MMU daughterboard overlaps Z80 footprint a little and
I had to dremel out last three pins of U1 from this board.
We need corner signals 19/20 (MREQ, IORQ),
HALT can be left unconnected

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YTM Enterprises

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Title: C128 Z80 at 8MHz

Size: A4	Date: 2024-06-01	**Rev: 2**
KiCad E.D.A. kicad (6.0.11)		Id: 1/1