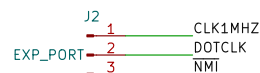


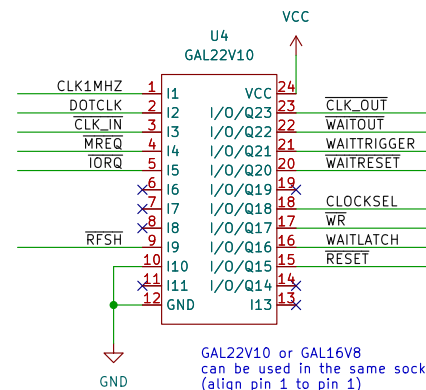
JP1 - when closed pass waitstates from GAL  
 JP2 - use onboard clock (1-2) or clock from GAL (2-3)  
 JP3 - GAL option: when closed pass CLK\_IN when open pass CLK\_OUT to Z80

JP3 should be enough to disable the circuit. If not, then:  
 1) remove U3 and U4  
 2) move JP2 to connect pins 1-2  
 3) open JP1

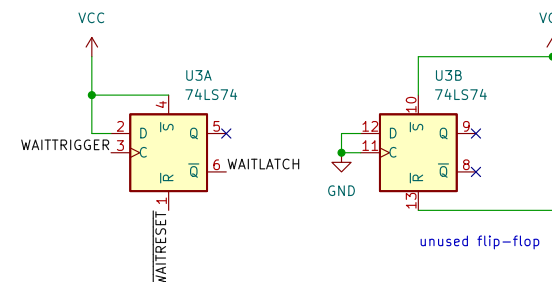
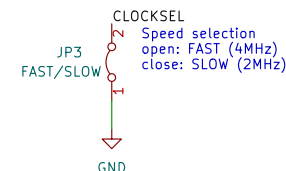
Fast clock is enabled when:  
 1) JP3 is open  
 2) JP2 connects pins 1-2  
 3) JP1 is closed



CLK1MHZ from U12 pin 11 (same in C128/D/DCR)  
 DOTCLK from Expansion port pin 6  
 NMI is optional, can be left unconnected



GAL22V10 or GAL16V8  
 can be used in the same socket  
 (align pin 1 to pin 1)



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 File: z80-dot-gal.kicad\_sch

**Title: C128 Z80 at 8MHz**

Size: A4 Date: 2024-06-01

KiCad E.D.A. kicad (6.0.11)

Rev: 2  
 Id: 1/1