**1- Answer the following question, using NUCLEO manual and datasheet:**

*a. If you need information about the connection within the NUCLEO board (e.g. at which microcontroller pin is LD2 connected?) which document would you use?*

The NUCLEO schematic

*b. At which page of the NUCLEO manual do you find the correspondence of extension connectors pins and microcontroller pins?*

Page 32 of the manual (page 4 of the schematic)

*c. Which is the meaning of different blinking speed and colors of LD1 in the NUCLEO board?*  
LD1 default color is red.

Green color of LD1 indicates that communication is in progress between the PC and the ST-LINK/V2-1

* Slow blinking Red/Off: at power-on before USB initialization
* Fast blinking Red/Off: after the first correct communication between the PC and ST-LINK/V2-1 (enumeration)
* Red LED On: when the initialization between the PC and ST-LINK/V2-1 is complete
* Green LED On: after a successful target communication initialization
* Blinking Red/Green: during communication with the target
* Green On: communication finished and successful
* Orange On: Communication failure

*d. What is the Jumper J6 used for?*

When the jumper is ON, the microcontroller is powered normally (default configuration).  
If the jumper is removed, an ammeter can be connected to measure the STM32 microcontroller consumption.

*e. What is a solder bridge?*

A solder bridge is a connection made during soldering. It is used for configurations which are rarely changed. The user manual shows possible connections and change in configuration obtainable using solder bridges (e.g. configuration of I/Os and power supply pins for compatibility).

*f. What do you have to do if you want to use PH0 and PH1 as normal GPIO?*  
If the external high-speed clock is not used, PF0/PD0/PH0 and PF1/PD1/PH1 are used as GPIOs instead of clocks. The following configuration is needed: SB54 and SB55 ON, SB16 and SB50 (MCO) OFF, R35 and R37 removed.

*g. On your NUCLEO board how is the LSE clock configured? Can you use PC14 and PC15 as normal GPIO?*

The LSE clock is configured as an on-board oscillator.   
Since SB48 and SB49 are open by default according to the datasheet, and the NUCLEO board has R34 and R36, PC14 and PC15 cannot be used as GPIO.

*h. If you want to send/receive data with a virtual serial port (to communicate with a computer), which pins do you select and which solder bridge should be connected/disconnected?*

On the STM32 the USART2 interface is available on PA2 and PA3. The default configuration (SB13 and SB14 ON, SB62 and SB63 OFF) supports virtual COM port for communication between the target STM32 and ST-LINK MCU.

*i. In the NUCLEO board schematics which is the component name of the F401RE microcontroller and of the ST-Link microcontroller?*

The component name referred to F401RE microcontroller is U5, and ST-link is called U2.

*j. Which pin of the morpho connector can be connected to PA6?*

The PIN 13 through SB41 (according to table 29 pag. 58 of the user manual).

**2- Look at the STM32F401RE data-sheet and answer the following questions:**

*a. Which is the meaning of each part of the name STM32F401RE?*

STM: STmicroelectronics

32: 32 bits

F401: Product line

R: 64 pins

E: Flash memory of 512 Kbytes

*b. Which is the package of the STM32F401RE?*

LQFP64 package.

*c. What voltages are allowed as Vdd power supply? Which is the maximum acceptable variations between different pins of Vdd? What is and how is Vbat used?*

* VDD = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through VDD pins. Requires the use of an external power supply supervisor connected to the VDD and PDR\_ON pins.
* VDD = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through VDD pins.
* VBAT = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

The maximum variation is 50 mV.

The VBAT pin allows to power the device from an external battery.

*d. Which is the typical current consumption (order of magnitude)?*

Hundreds of mA.

*e. Which peripherals are connected to AHB1, APB1 and APB2?*

AHB1:

GPIOA, GPIOB, GPIOC, GPIOD, GPIOE, GPIOH, CRC, RCC, Flash interface register, DMA1, DMA2

APB1:

PWR, I2C3, I2C2, I2C1, USART2, I2S3ext, SPI3 / I2S3, SPI2 / I2S2, I2S2ext, IWDG, WWDG, RTC & BKP Registers, TIM5, TIM4, TIM3, TIM2

APB2:

TIM11, TIM10, TIM9, EXTI, SYSCFG, SPI4/I2S4, SPI1, SDIO, ADC1, USART6, USART1, TIM8, TIM1

*f. Which is the difference in terms of clock frequency between APB1 and APB2?*

Internal APB1 clock frequency: from 0 to 40 MHz

Internal APB2 clock frequency: from 0 to 84 MHz

*g. How many channels does the ADC have? How many bits? Which is the maximum sampling frequency (and how is it affected by Vdda)?*

16 channels

12 bits

Maximum sampling frequency: 18MHz for Vdda (1.7V-2.4V) and 36MHz for Vdda (2.4V-2.6V)

*h. What is the Analog Watchdog?*

The analog watchdog is a timer able to generate interrupt signal. Its features allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

*i. Which are the values of the S&H resistance and capacitance?*

Sampling switch resistance: 6 kΩ

Internal sample and hold capacitor 7 pF

*j. Which is the maximum CPU clock frequency?*

84 MHz

*k. Which is the range of operating frequencies of HSE and LSE clocks?*

HSE: 4 MHz – 26 MHz

LSE Only 32.768 kHz

*l. List all the communication interfaces (and also how many of them).*

SPI: 4

I2 : 2

I2: 3

USART: 3

SDIO: 1

*m. Which are the typical clock frequencies for the I2C and SPI interfaces?*

I2C:

Up to three I2C bus interfaces can operate in multimaster and slave modes. They can

Support

* standard mode - up to 100 kHz
* Fast mode - up to 400 kHz

The I2C bus frequency can be increased up to 1 MHz.

SPI:

* Master mode - 42 MHz
* Slave mode – 42 MHz
* Slave transmitter/full-duplex mode – 38 MHz
* Master mode, SPI1/2/3/4 - 21 MHz
* Slave mode, SPI1/2/3/4 - 21 MHz

*n. What is the NVIC? How many priority levels can it mange?*

It’s a device to control interrupts (Nested Vectored Interrupt Controller), it’s able to manage 16 priority levels

*o. How large is the embedded flash memory? And the SRAM memory?*

The devices embed 512 Kbytes of Flash memory available for storing programs and data.

The SRAM has 96 Kbytes which can be accessed (read/write) at CPU clock speed with 0 wait states.

*p. What is the DMA? Which peripherals can use the DMA? How many streams are supported at maximum? What is the circular buffer management?*

The DMA (Direct Memory Access) is a mechanism that enbles peripherals to directly access memory.

The DMA can be used with the main peripherals:

• SPI and I2S

• I 2C

• USART

• General-purpose, basic and advanced-control timers TIMx

• SD/SDIO/MMC host interface

• ADC

Each DMA can support up to 8 streams. The streams are managed with a circular buffer, a buffer connected end to end to itself, so that no specific code is needed when the controller reaches the end of the buffer.

*q. What is the RTC?*

The Real Time Clock. It is an independent BCD timer/counter that uses dedicated

Register to save the second, minute, hour (in 12/24 hour), week day, date, month and year

*r. What is PIN60 in the STM32F401RE?*

Boot0

*s. What is an alternate function? Make some examples.*

An ‘alterante function’ is another function of a pin, different from the GPIO (General Purpose Input/Output).

For example, the pin AF08 can be uses as a USART port.

*t. Which is the maximum source/sink source current of the GPIOs? What are the output voltage levels of GPIOs?*

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed VOL/VOH) except PC13, PC14 and PC15 which can sink or source up to ±3mA. e general values for the current consuptions are Idd= 1,55 μA/MHz allowing maximum I/O toggling up to 84 MHz.

The GPIOs’ voltage leves are 0.4 for the low level and VDD – 0.4 for the high level.

*u. Which is the value of the internal reference voltage?*

Vref should satisfy the condition VDDA-VREF+ < 1.2 V where VDDA is the analog operating voltage.