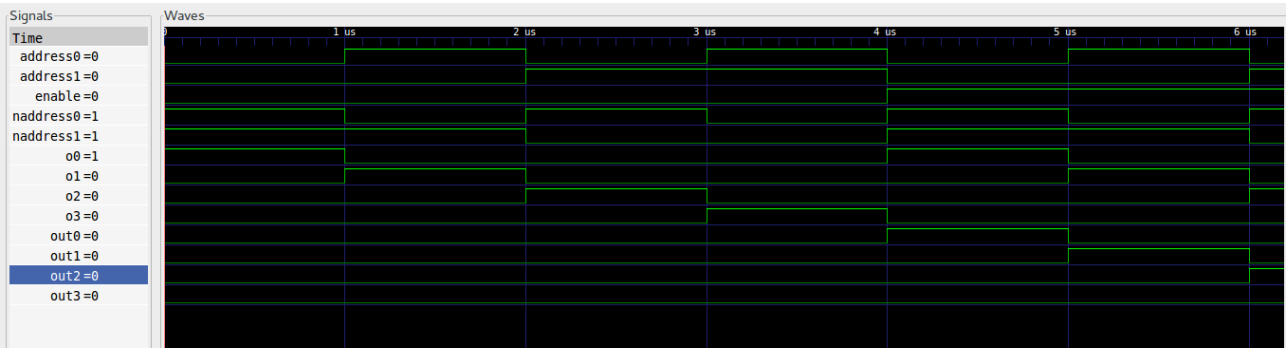
Computer Architecture HW2

Zarin Bhuiyan

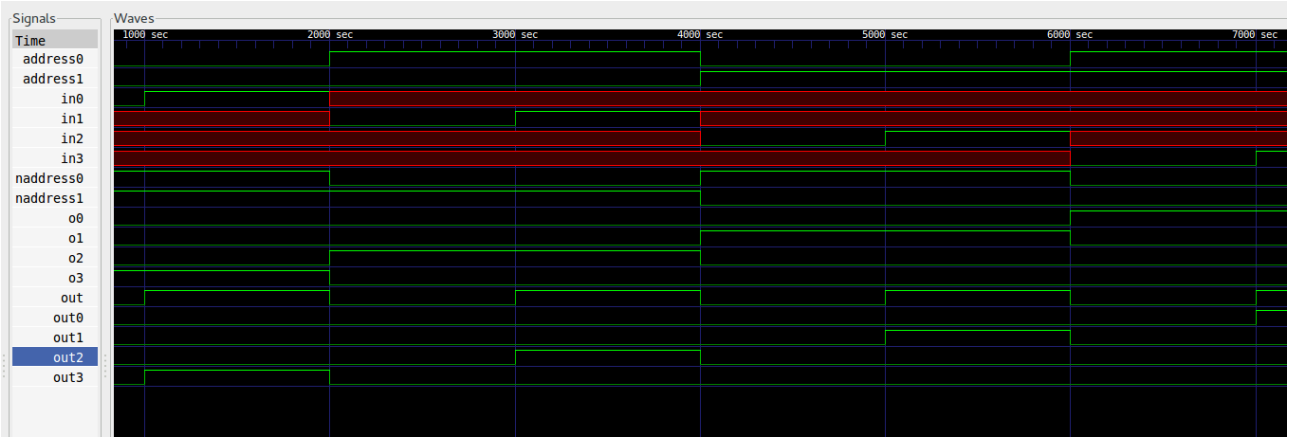
September 22, 2016

Decoder



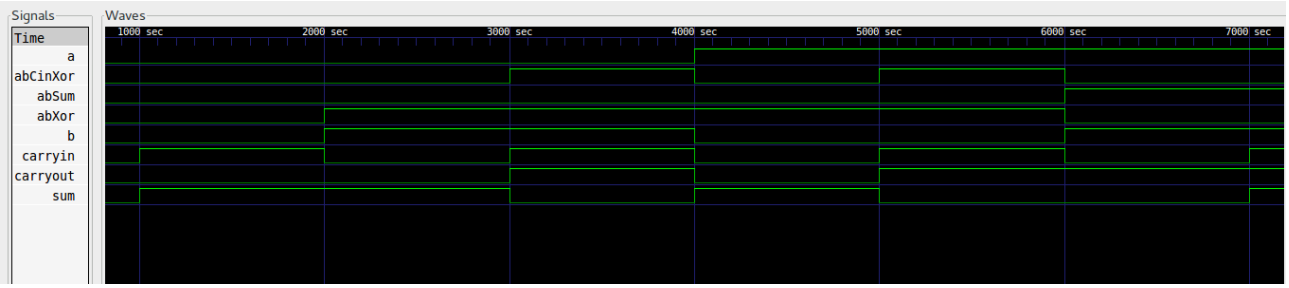
En	A0	A1	O0	O1	O2	O3	Expected Output
0	0	0	0	0	0	0	All false
0	1	0	0	0	0	0	All false
0	0	1	0	0	0	0	All false
0	1	1	0	0	0	0	All false
1	0	0	1	0	0	0	O0 Only
1	1	0	0	1	0	0	O1 Only
1	0	1	0	0	1	0	O2 Only
1	1	1	0	0	0	1	O3 Only

Multiplexer



addr0	addr1	in3	in2	in1	in0	Out	Expected Output
0	0	x	x	x	0	0	0
0	0	x	x	x	1	1	1
1	0	x	x	0	x	0	0
1	0	x	x	1	x	1	1
0	1	x	0	x	x	0	0
0	1	x	1	x	x	1	1
1	1	0	x	x	x	0	0
1	1	1	x	x	x	1	1

Full Adder



A	B	CarryIn	Sum	CarryOut	Expected Output	
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1