# Computer Architecture HW2

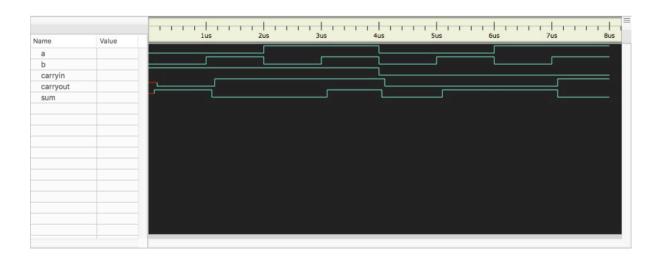
Bill Du

### 1-bit Full Adder:

#### test bench results:

a	b	١	carryin	١	sum	١	carryout	١	Expected carryout/sum	1
0	0	ı	1	ı	1	١	0	ı	0/1	
0	1	ı	1	ı	0	١	1	ı	1/0	
1	0	ı	1	ı	0	١	1	ı	1/0	
1	1	ı	1	ı	1	١	1	ı	1/1	
0	0	ı	0	ı	0	١	0	ı	0/0 I	
0	1	ı	0	ı	1	١	0	ı	0/1	
1	0	ı	0	ı	1	١	0	ı	0/1	
1	1	I	0	I	0	١	1	I	1/0	

## waveform with delay:

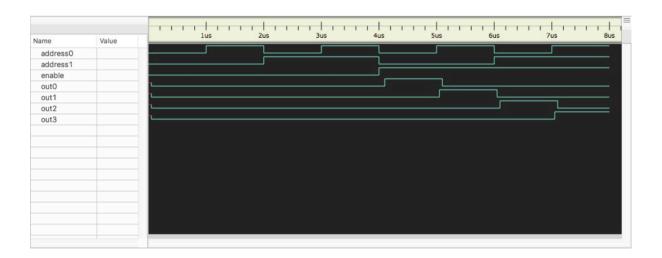


### 2-bit Decoder:

#### test bench results:

En	۸a	۸1	ı	na	01	02	U3	1	Expected Output
	AU	H		00	OT.	UZ.	U3		expected output
0	0	0	ı	0	0	0	0	ı	All false
0	1	0	١	0	0	0	0	ı	All false
0	0	1	١	0	0	0	0	ı	All false
0	1	1	١	0	0	0	0	ı	All false
1	0	0	١	1	0	0	0	ı	00 Only
1	1	0	١	0	1	0	0	ı	01 Only
1	0	1	I	0	0	1	0	I	02 Only
1	1	1	I	0	0	0	1	ı	03 Only

## waveform with delay:



# 4:1 Multiplexer:

### test bench results:

address0	١	address1	ı	in0	١	in1	١	in2	١	in3	١	out	١	Expected	Out I
0	I	0	ı	0	I	X	I	X	ı	X	I	0	I	0	1
0	١	0	ı	1	ı	X	ı	X	ı	X	I	1	I	1	1
0	I	1	ı	1	ı	X	ı	0	ı	X	I	0	I	0	1
0	I	1	ı	1	I	X	I	1	ı	X	I	1	I	1	1
1	I	0	ı	1	ı	0	ı	1	ı	X	I	0	I	0	1
1	I	0	ı	1	ı	1	ı	1	ı	X	I	1	I	1	1
1	I	1	ı	1	ı	1	ı	1	ı	0	ı	0	I	0	1
1	I	1	I	1	I	1	١	1	١	1	I	1	I	1	1

## waveform with delay:

