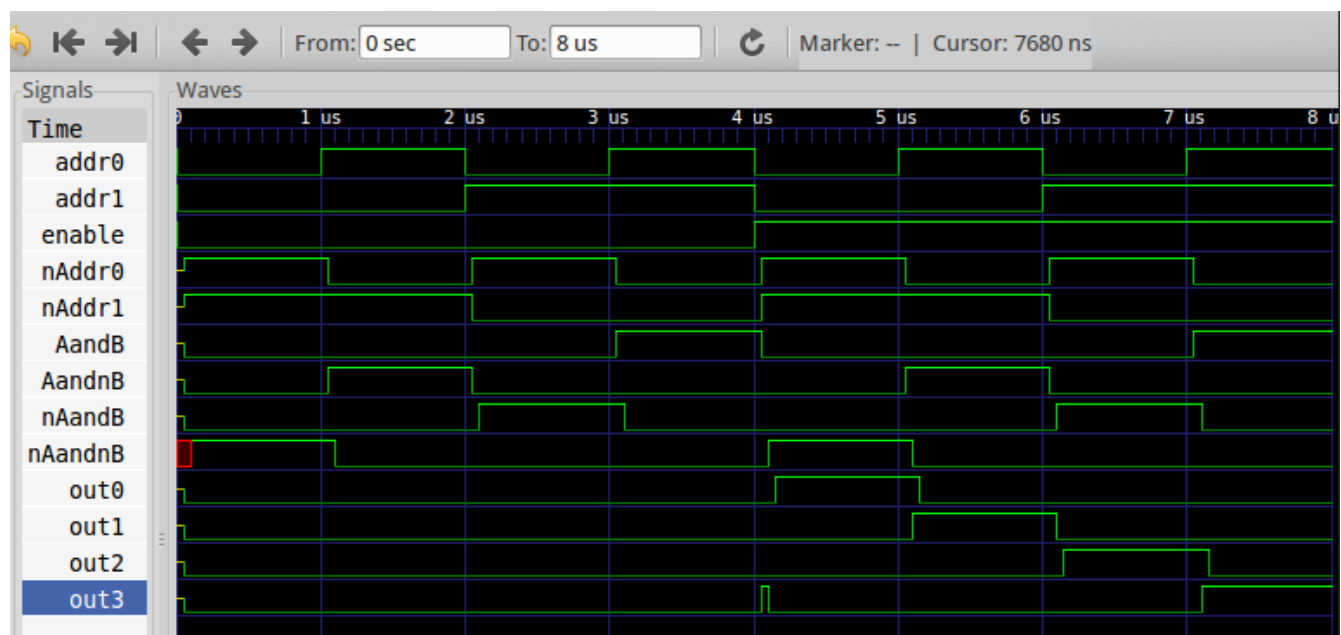


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Homework 2: Verilog Building Blocks

Decoder

```
vagrant@vagrant-ubuntu-trusty-64:~/HW2$ ./decoder
VCD info: dumpfile decoder_trace.vcd opened for output.
En A0 A1 | 00 01 02 03 | Expected Output
0 0 0 | 0 0 0 0 | All false
0 1 0 | 0 0 0 0 | All false
0 0 1 | 0 0 0 0 | All false
0 1 1 | 0 0 0 0 | All false
1 0 0 | 1 0 0 0 | 00 Only
1 1 0 | 0 1 0 0 | 01 Only
1 0 1 | 0 0 1 0 | 02 Only
1 1 1 | 0 0 0 1 | 03 Only
```



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Multiplexer

```
vagrant@vagrant-ubuntu-trusty-64:~/HW2$ ./multiplexer
VCD info: dumpfile multiplexer_trace.vcd opened for output.
S1 S0 | A0 A1 A2 A3 | Out | Expected Out
0 0 | 0 x x x | 0 | 0
0 0 | 1 x x x | 1 | 1
0 1 | x 0 x x | 0 | 0
0 1 | x 1 x x | 1 | 1
1 0 | x x 0 x | 0 | 0
1 0 | x x 1 x | 1 | 1
1 1 | x x x 0 | 0 | 0
1 1 | x x x 1 | 1 | 1
```



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Adder

```
vagrant@vagrant-ubuntu-trusty-64:~/HW2$ ./adder
VCD info: dumpfile adder_trace.vcd opened for output.
A B Ci | S Co | Expected Output
0 0 0 | 0 0 | 0 0
0 0 1 | 1 0 | 1 0
1 0 0 | 1 0 | 1 0
1 0 1 | 0 1 | 0 1
0 1 0 | 1 0 | 1 0
0 1 1 | 0 1 | 0 1
1 1 0 | 0 1 | 0 1
1 1 1 | 1 1 | 1 1
```

