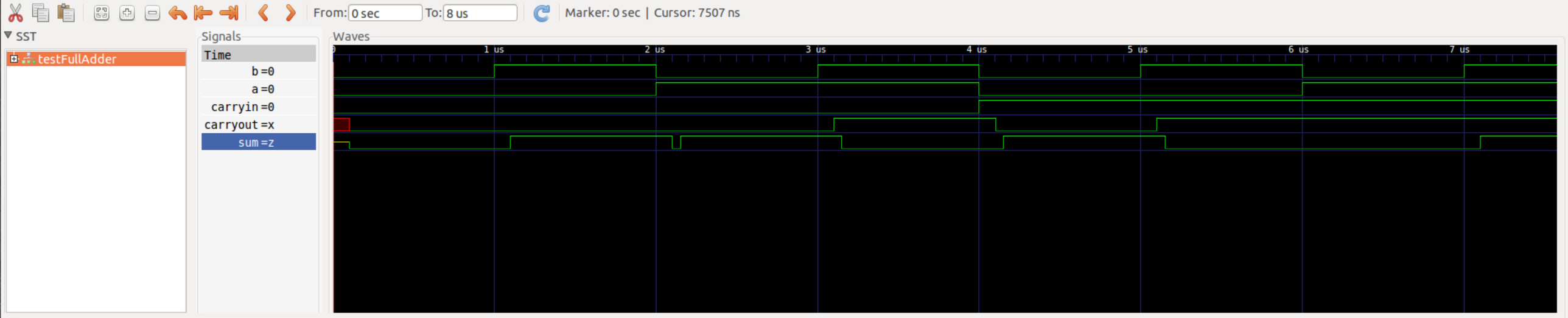

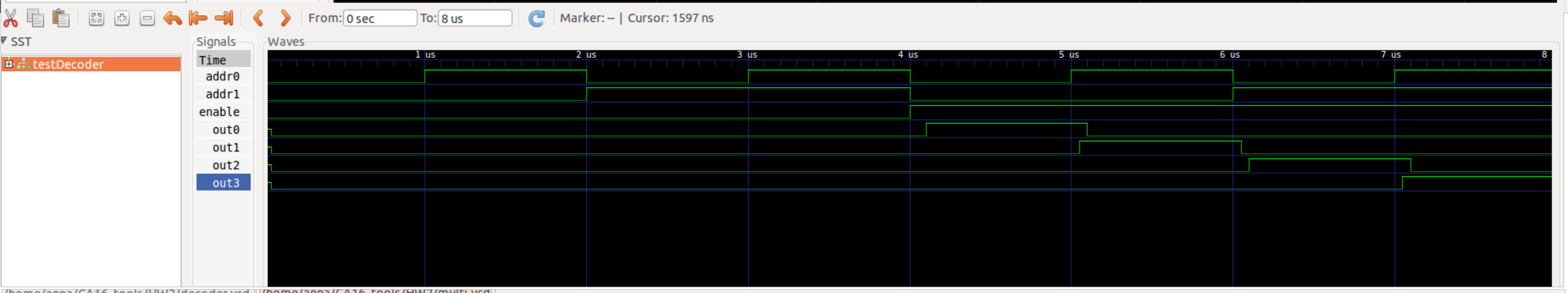

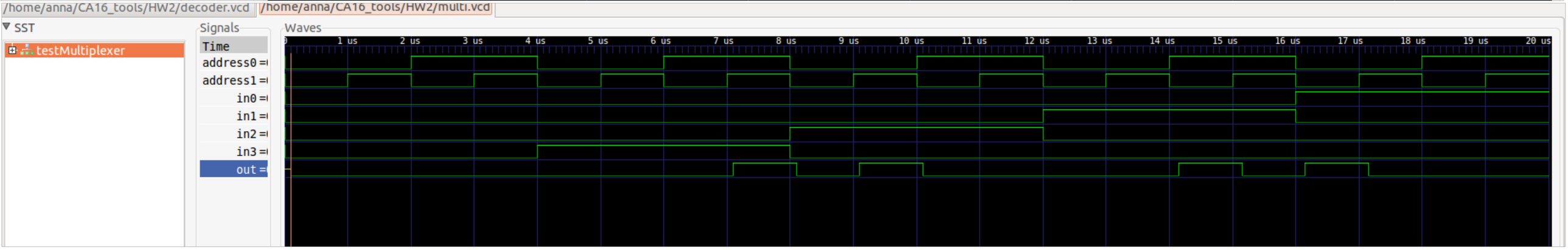


```
anna@A2-B2:~/CA16_tools/HW2$ iverilog -o adder  adder.t.v
anna@A2-B2:~/CA16_tools/HW2$ ./adder
VCD info: dumpfile adder.vcd opened for output.
a b | Cin Cout | sum | Expected Sum | Expected Cout
0 0 |  0    0  |  0  |       0      |      0
0 1 |  0    0  |  1  |       1      |      0
1 0 |  0    0  |  1  |       1      |      0
1 1 |  0    1  |  0  |       0      |      1
0 0 |  1    0  |  1  |       1      |      0
0 1 |  1    1  |  0  |       0      |      1
1 0 |  1    1  |  0  |       0      |      1
1 1 |  1    1  |  1  |       1      |      1
```

```
anna@A2-B2:~/CA16_tools/HW2$ iverilog -o DECODER  decoder.t.v
anna@A2-B2:~/CA16_tools/HW2$ ./DECODER
VCD info: dumpfile decoder.vcd opened for output.
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

```
anna@A2-B2:~/CA16_tools/HW2$ iverilog -o multi  multiplexer.t.v
anna@A2-B2:~/CA16_tools/HW2$ ./multi
VCD info: dumpfile multi.vcd opened for output.
in0 in1 in2 in3 | a1 a2 | out | Expected Output
 0   0   0   0  | 0  0  |  0  |  0
 0   0   0   0  | 0  1  |  0  |  0
 0   0   0   0  | 1  0  |  0  |  0
 0   0   0   0  | 1  1  |  0  |  0
 0   0   0   1  | 0  0  |  0  |  0
 0   0   0   1  | 0  1  |  0  |  0
 0   0   0   1  | 1  0  |  0  |  0
 0   0   0   1  | 1  1  |  1  |  1
 0   0   1   0  | 0  0  |  0  |  0
 0   0   1   0  | 0  1  |  1  |  1
 0   0   1   0  | 1  0  |  0  |  0
 0   0   1   0  | 1  1  |  0  |  0
 0   1   0   0  | 0  0  |  0  |  0
 0   1   0   0  | 0  1  |  0  |  0
 0   1   0   0  | 1  0  |  1  |  1
 0   1   0   0  | 1  1  |  0  |  0
 1   0   0   0  | 0  0  |  1  |  1
 1   0   0   0  | 0  1  |  0  |  0
 1   0   0   0  | 1  0  |  0  |  0
 1   0   0   0  | 1  1  |  0  |  0
```