Computer Architecture HW2

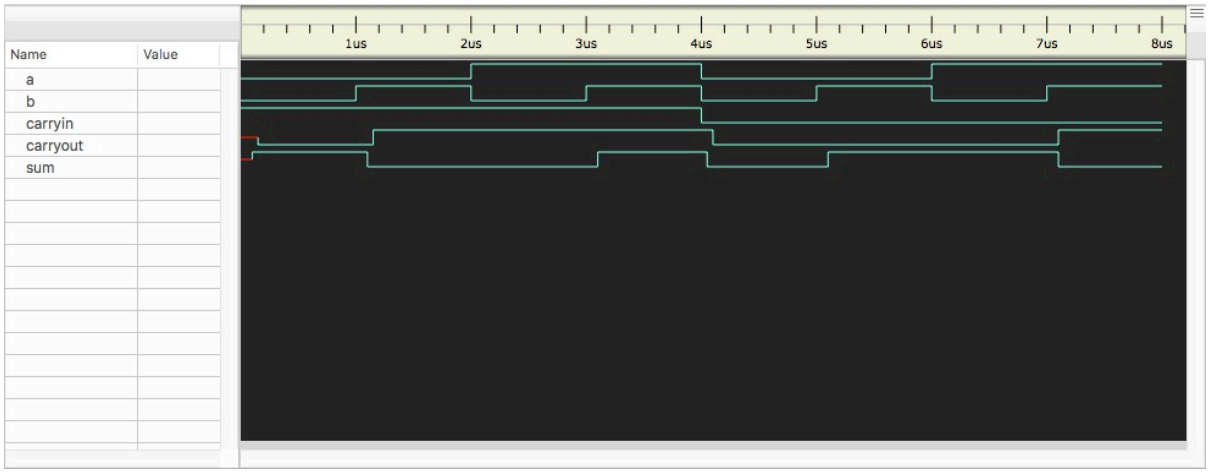
Bill Du

1-bit Full Adder:

test bench results:

a	b	carryin	sum	carryout	Expected carryout/sum
0	0	1	1	0	0/1
0	1	1	0	1	1/0
1	0	1	0	1	1/0
1	1	1	1	1	1/1
0	0	0	0	0	0/0
0	1	0	1	0	0/1
1	0	0	1	0	0/1
1	1	0	0	1	1/0

waveform with delay:

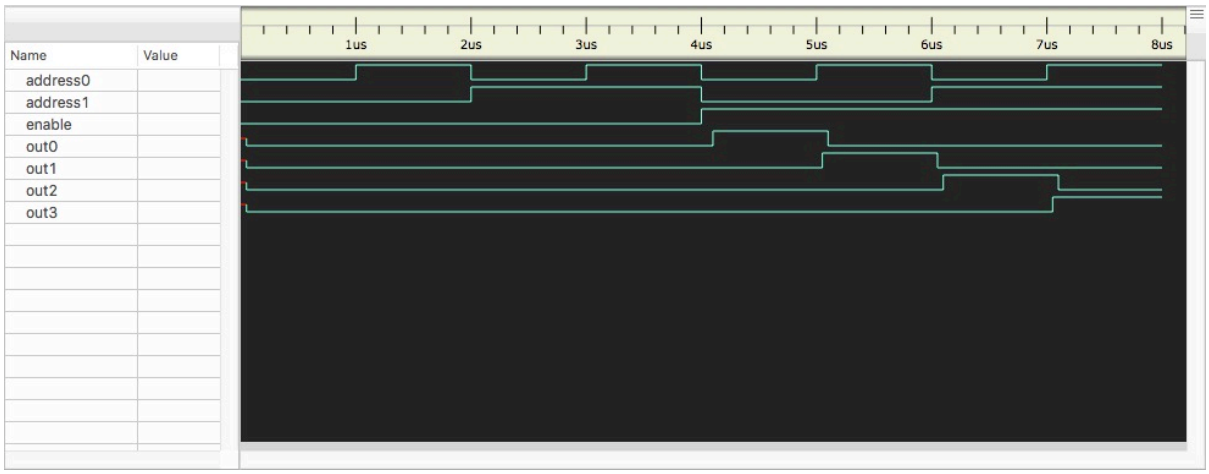


2-bit Decoder:

test bench results:

```
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

waveform with delay:



4:1 Multiplexer:

test bench results:

address0	address1	in0	in1	in2	in3	out	Expected Out
0	0	0	x	x	x	0	0
0	0	1	x	x	x	1	1
0	1	1	x	0	x	0	0
0	1	1	x	1	x	1	1
1	0	1	0	1	x	0	0
1	0	1	1	1	x	1	1
1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1

waveform with delay: