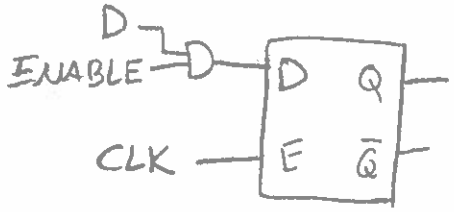
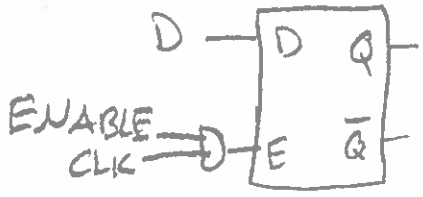
Anisha N

Deliverable 1

D-flip flop with enable, positive edge triggered



D-flip flop where you "gate the clock"



Deliverable 6

The decoder module outputs a high signal to one of the 32 output pins based on a 4 bit address and a 1 bit enable. The behavioral verilog works to output the value of the enable to the appropriate pin. That is - one of the output pins will be high only if the enable is high, and of the enable is low everything will be zero. Each possible combination of the 4 bit address corresponds to an output pin. (The possible values are 0000 to 1111, which is the range 0 to 31). The syntax of << means that the value of enable is shifted over by the value of the address. So if enable is high, the high value is shifted over to the appropriate pin defined by the address.