CompArch Homework 4

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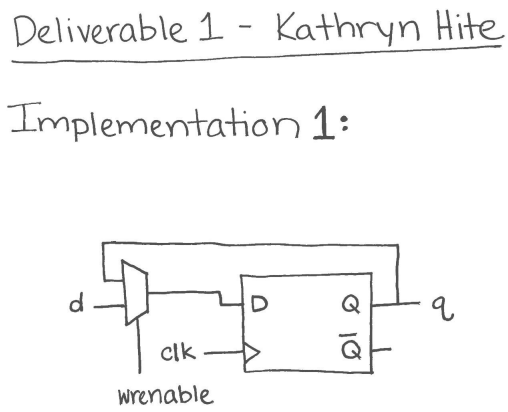
1 Deliverable 1



2 Deliverable 6

The decoder module uses the behavioral Verilog bit shift operator <<. Written in the module, the line is first given the bit string that will be moved, the enable high input in this case, followed by the bit shift operator and then the address number of bits that it will be shifted by. This results in the corresponding one of the 32 outputs becoming high when the decoder is given a high value from the enable input as well as the 4 bit address. Otherwise, every pin will be at 0.