Comparch HW4 Write-Up

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Deliverable 1

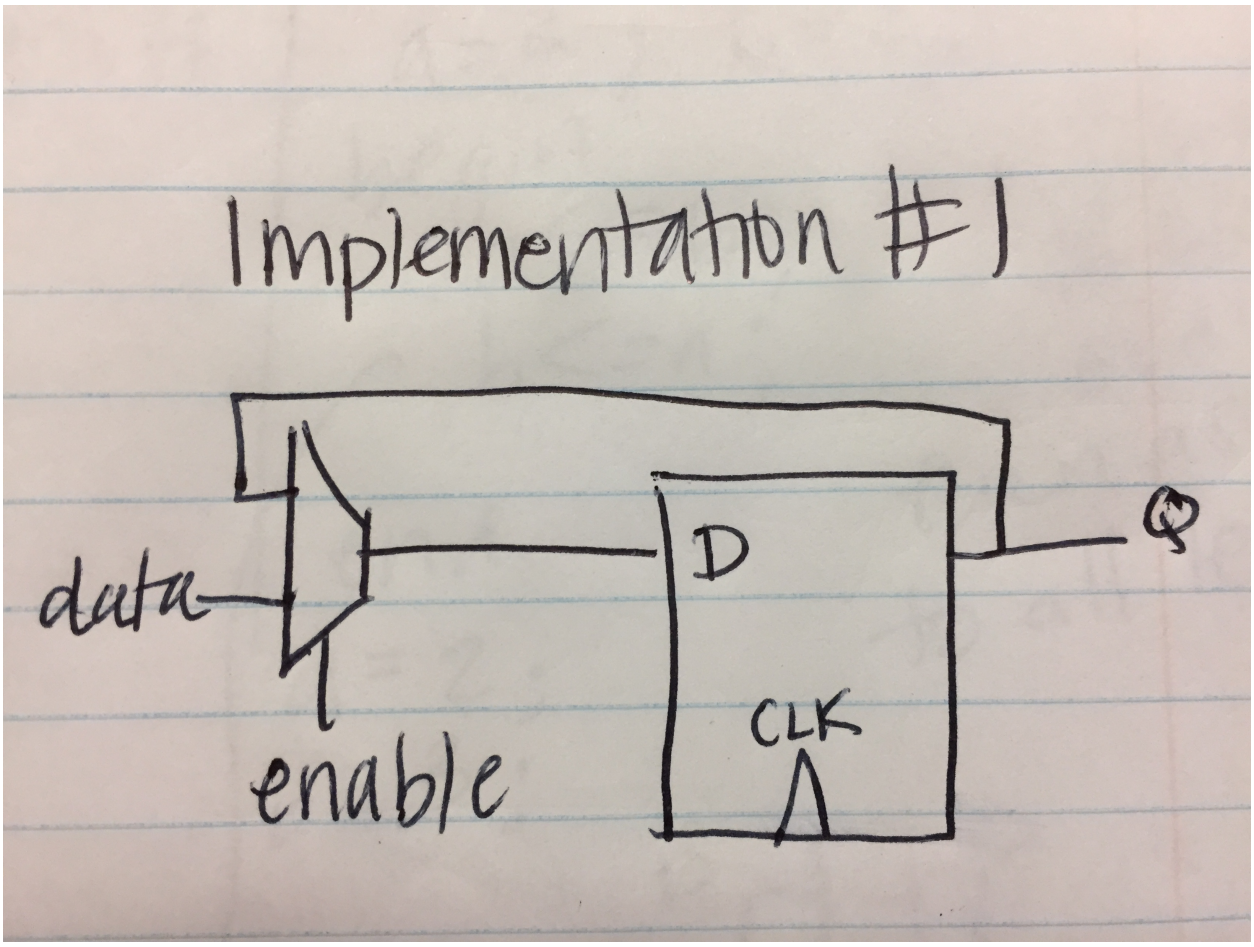

Figure 1: Schematic for implementation #1

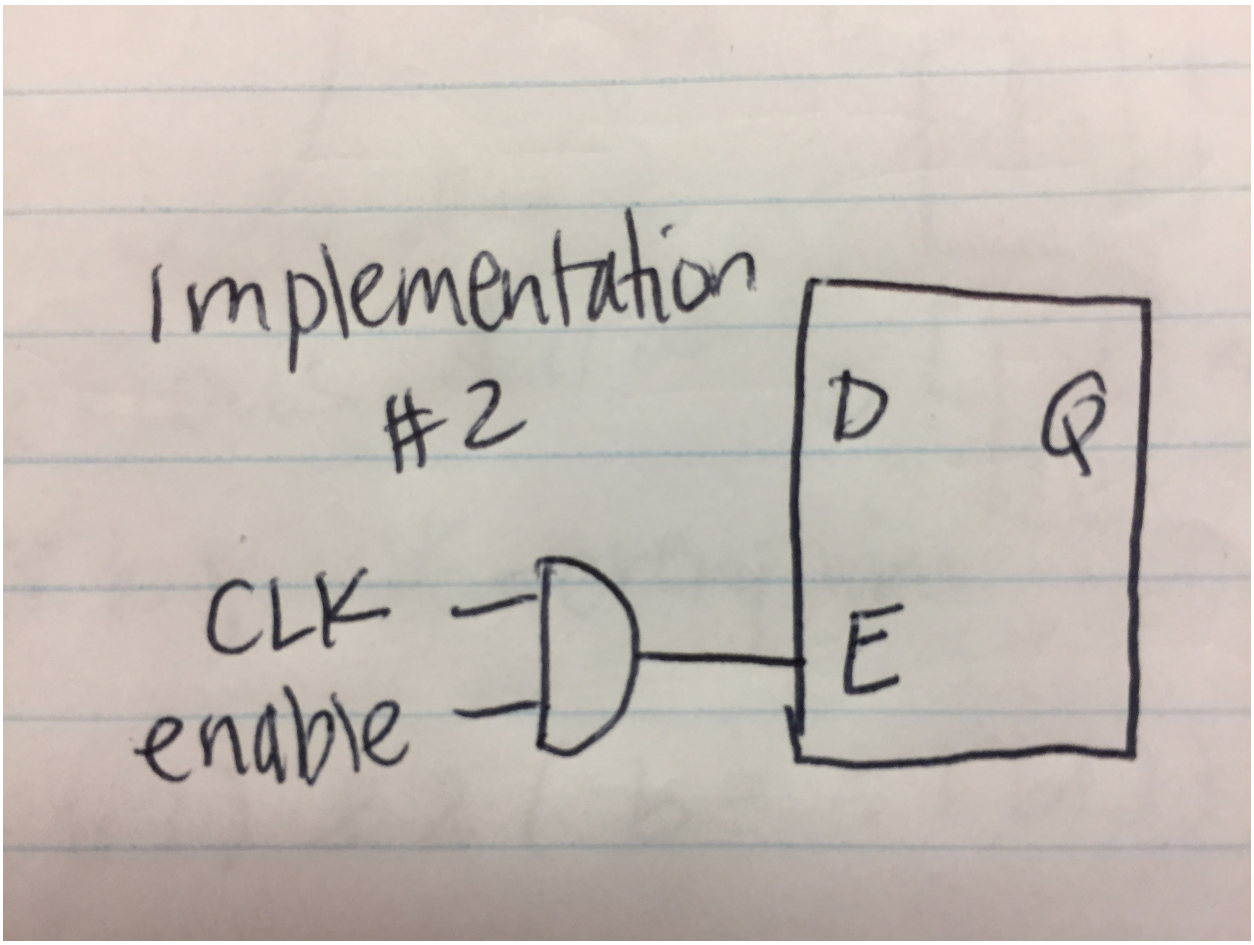

Figure 2: Schematic for implementation #2

Deliverable 6

This decoder (1 to 32, with a 5 bit address), has the output assigned according to a bit shifter. The enable has the data to be shifted to the left, and the address contains the number of single bit shift operations to be performed. Therefore the output has the enable shifted by the amount specified in the address. This allows the output only be in powers of two, like: 00000000000000000000000000000100 (address 3), 00000000000000000000000010000000 (address 8) etc. but it selects only one register file at a time.