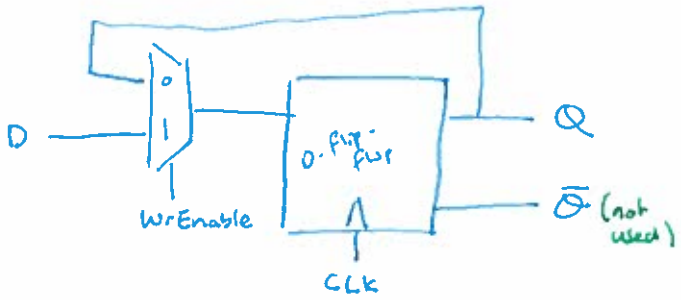
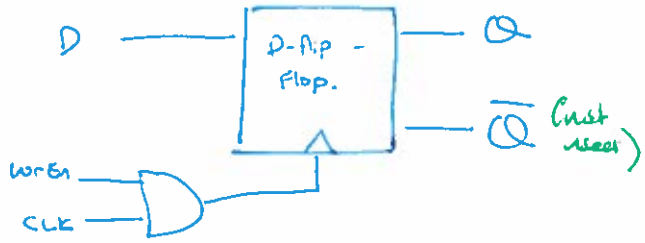
Deliverable 1

Register Implementation # 1.



Register Implementation #2



Deliverable 6

```
module decoder1to32
(
  output[31:0]    out,
  input           enable,
  input [4:0]     address
);

    assign out = enable << address;
endmodule.
```

Given an empty string (in this case of 32 length) we output the following from this decoder.

ex) length = 5

address @ 3
enable 1

enable = 1
Address = $011_2 = 3_{10}$

0	1	0	0	0
4_{10}	3_{10}	2_{10}	1_{10}	0_{10}

First the address will tell which bit of the string (starting @ zero from rightmost bit) where the enable variable will be. For example, if address is 011 and enable is 1, 1 will be the 3rd bit of the output and the rest will be zero.

Basically, we are padding the "enable" variable to the left w/ the number of zeros corresponding to the address. The zeros to the right of "enable" will also be zero.

If enable is zero, the same logic will apply, but it won't really matter because every bit in the output will be zero.