Work Plan 1

Input Conditioner Deliverables (17/10/16)

- Complete module in `inputconditioner.v`
- Test bench `inputconditioner.t.v`
- Test script that executes the test bench and generates wave forms showing the correct operation of your input conditioner.
- Draw a circuit diagram of the structural circuit for the input conditioner. This should be drawn from primitives such as D flip-flops, adders, muxes, and basic gates.
- Time analysis: If the main system clock is running at 50MHz, what is the maximum length input glitch that will be suppressed by this design for a `waittime` of 10?

Background + Circuit diagram: 1hr

Inputconditioner.v module: 3hr

Test bench: 1hr

Debugging: 2hr

Time Analysis: 1hr

Total: 8 hours

Shift Register Deliverables (17/10/16)

- Complete module in `shiftregister.v`
- Test bench in `shiftregister.t.v` demonstrating both modes of operation for the shift register.

Background: 30min

shiftregister.v module: 3hr

Test bench: 1hr

Debugging: 2hr

Total: 6hr 30min

Loading to FPGA (19/10/16)

Create a top-level module and load the shift register and the input conditioners onto the Zybo board

Do at NINJA hours: 2 hours

midpoint.v: 2hours

Film: 10min

Total: 4hr 10min

Midpoint Deliverables

Create module `midpoint.v`, no test bench needed.

Design a test sequence that demonstrates successful operation of this portion of the lab. Provide a short written description of what the test engineer is to do, and what the state of the LEDs should be at each step.

Record a short video (~60 seconds) of your test being executed on the FPGA and submit the link (via Piazza is fine, don't need to push to GitHub). If you are unable to do so, you can schedule a demo with a NINJA.

Have done by: Monday, October 17

Total Estimated Time for Part 1: 18hr 10min

Actual due date: October 20

Work Plan 2

Finite State Machine (24/10/16)

- Implement SPI Memory
- Testing
  Estimated Time: 7hr

SPI Memory (24/10/16)

- Implement SPI Memory
- Address Latch
- Buffer
- Debugging
- Implementation
- Load onto FPGA
  Estimated Time: 5hr

SPI Testing

- Test Strategy
- Test cases check
- Waveform Analysis
- Debugging
  Estimated Time: 3hr

Final Report

Estimated Time: 4hr

Total estimated time for Part 2: 19 hrs