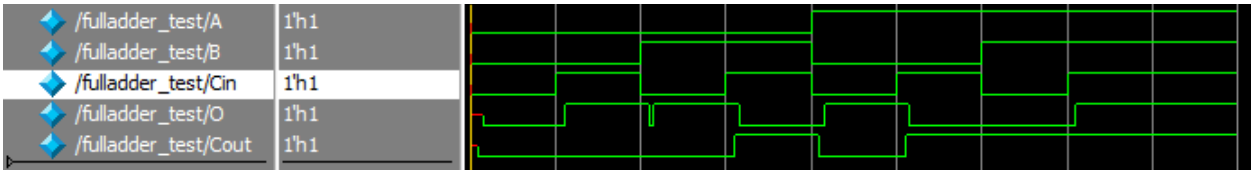
Full Adder

Timing Diagram

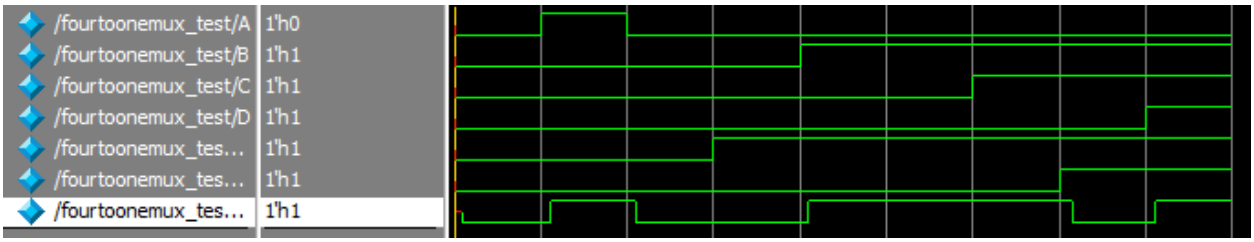


Truth Table

A	B	Cin	O	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Mux

Timing Diagram

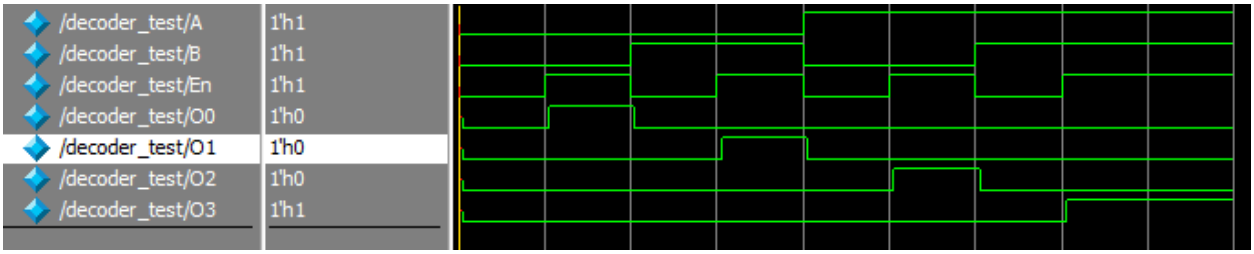


Truth Table

A	B	C	D	Pick0	Pick1	Out
0	0	0	0	0	0	0
1	0	0	0	0	0	1
0	0	0	0	0	0	0
0	0	0	0	1	0	0
0	1	0	0	1	0	1
0	1	0	0	1	0	1
0	1	1	0	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1

Decoder

Timing Diagram



Truth Table

A	B	En	Out3	Out2	Out1	Out0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0