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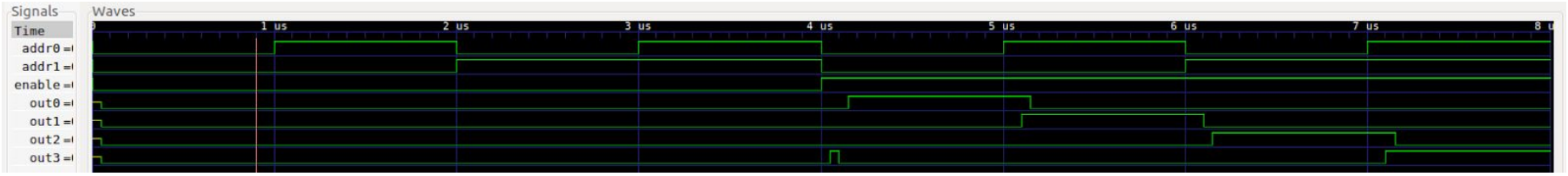
HW 1 Testing and Waveforms

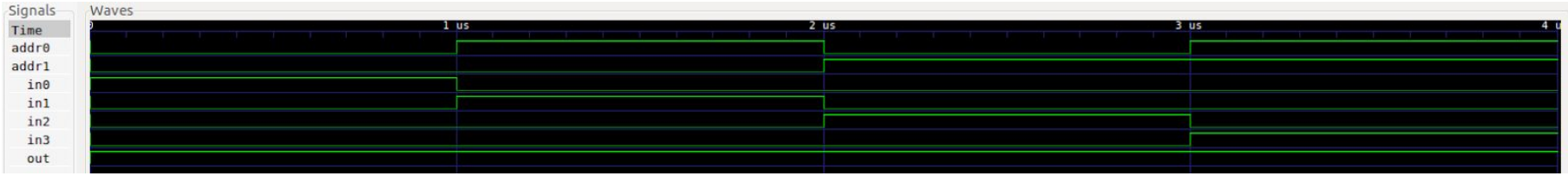
Decoder:

```
youngdp@youngdp:~/HW1/CompArc/HW2$ ./decoder
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```



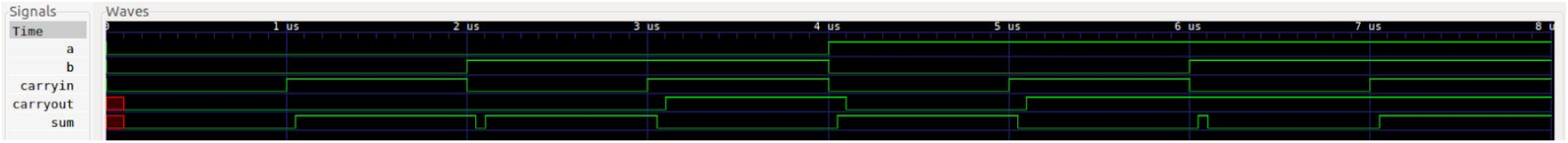
Multiplexer:

```
youngdp@youngdp:~/HW1/CompArc/HW2$ ./multiplexer
A0 A 1| in0 in1 in2 in3 | Out | Expected Output
0  0  |  1   0   0   0  |  1  | O1 Only
1  0  |  0   1   0   0  |  1  | O2 Only
0  1  |  0   0   1   0  |  1  | O3 Only
1  1  |  0   0   0   1  |  1  | O4 Only
```



Adder:

```
youngdp@youngdp:~/HW1/CompArc/HW2$ ./adder
A  B  Cin | Sum  Cout | Expected Output
0  0  0   | 0    0    | 0 0
0  0  1   | 1    0    | 1 0
0  1  0   | 1    0    | 1 0
0  1  1   | 0    1    | 0 1
1  0  0   | 1    0    | 1 0
1  0  1   | 0    1    | 0 1
1  1  0   | 0    1    | 0 1
1  1  1   | 1    1    | 1 1
```



Note:

I did not use any scripts besides the standard methods of compiling and running verilog files:

$ iverilog -o adder adder.t.cv

$ ./adder

Followed by:

$ gtkwave adder.vcd