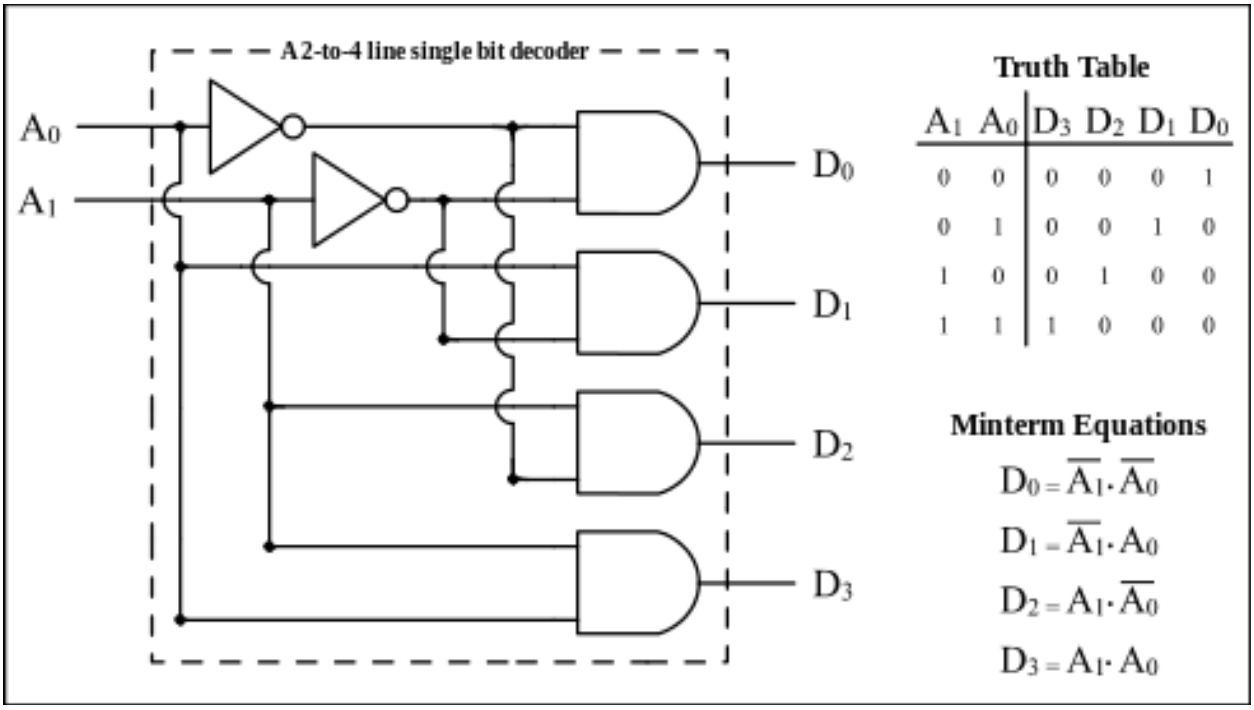
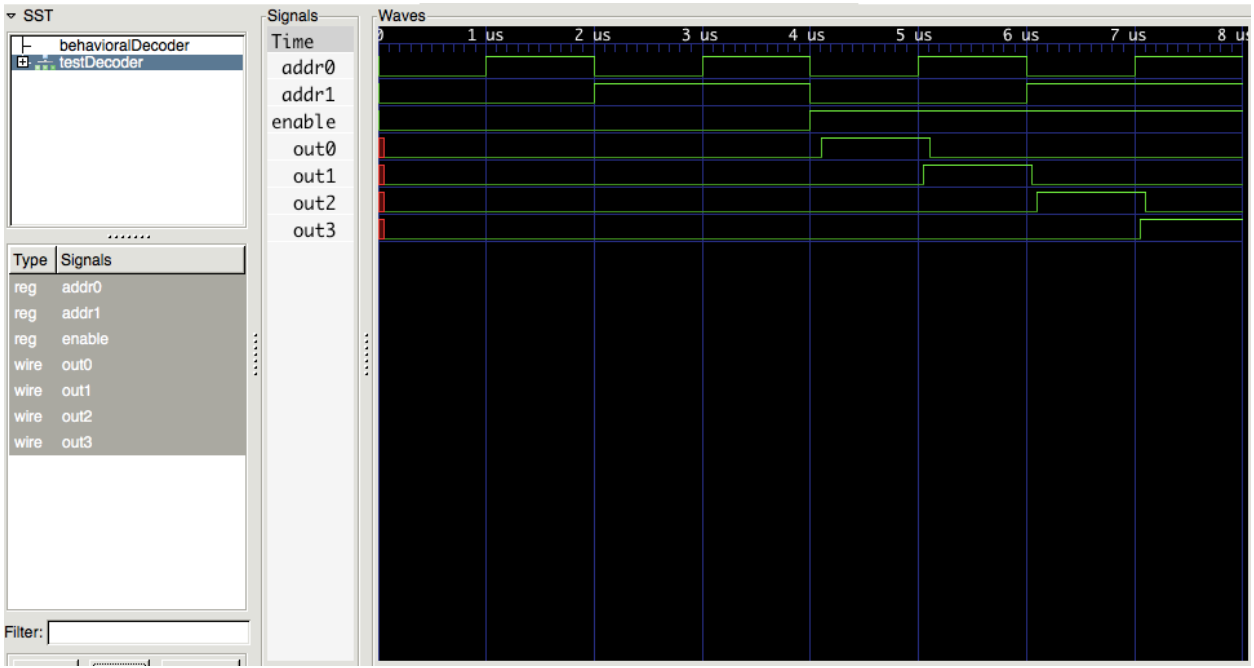
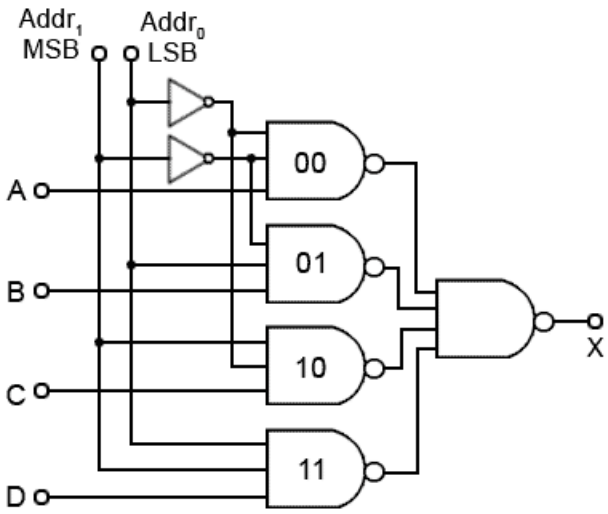
Decoder



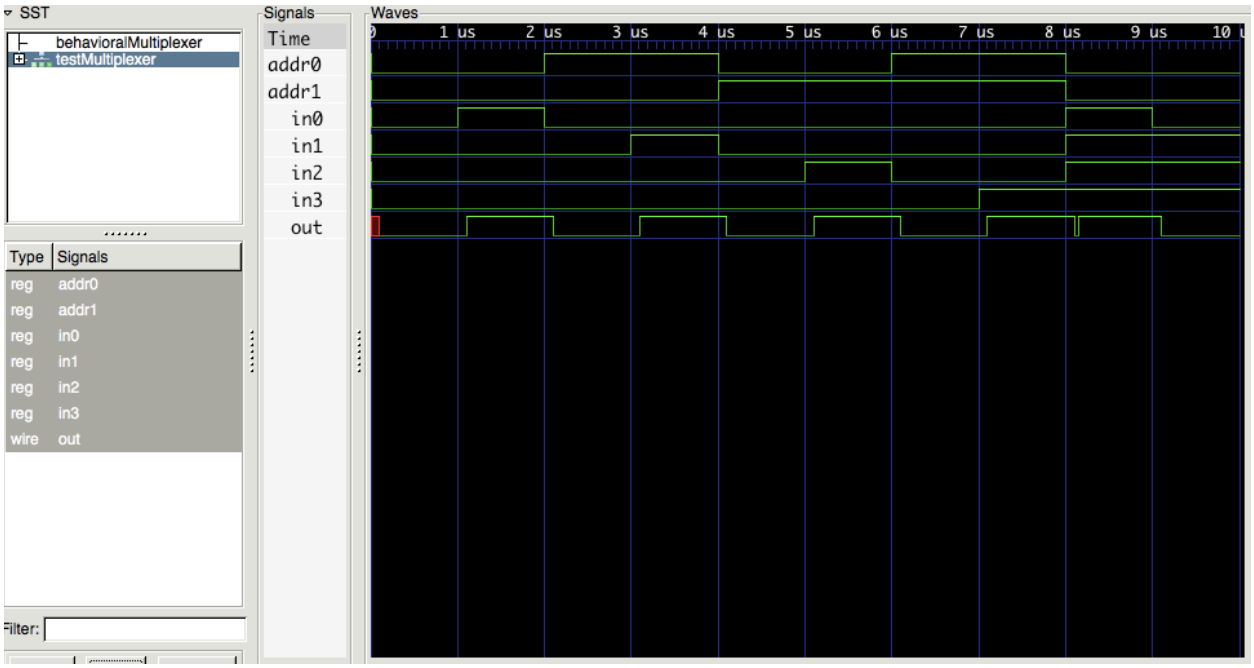
En A0 A1| O0 O1 O2 O3 | Expected Output
0 0 0 | 0 0 0 0 | All false
0 1 0 | 0 0 0 0 | All false
0 0 1 | 0 0 0 0 | All false
0 1 1 | 0 0 0 0 | All false
1 0 0 | 1 0 0 0 | O0 Only
1 1 0 | 0 1 0 0 | O1 Only
1 0 1 | 0 0 1 0 | O2 Only
1 1 1 | 0 0 0 1 | O3 Only



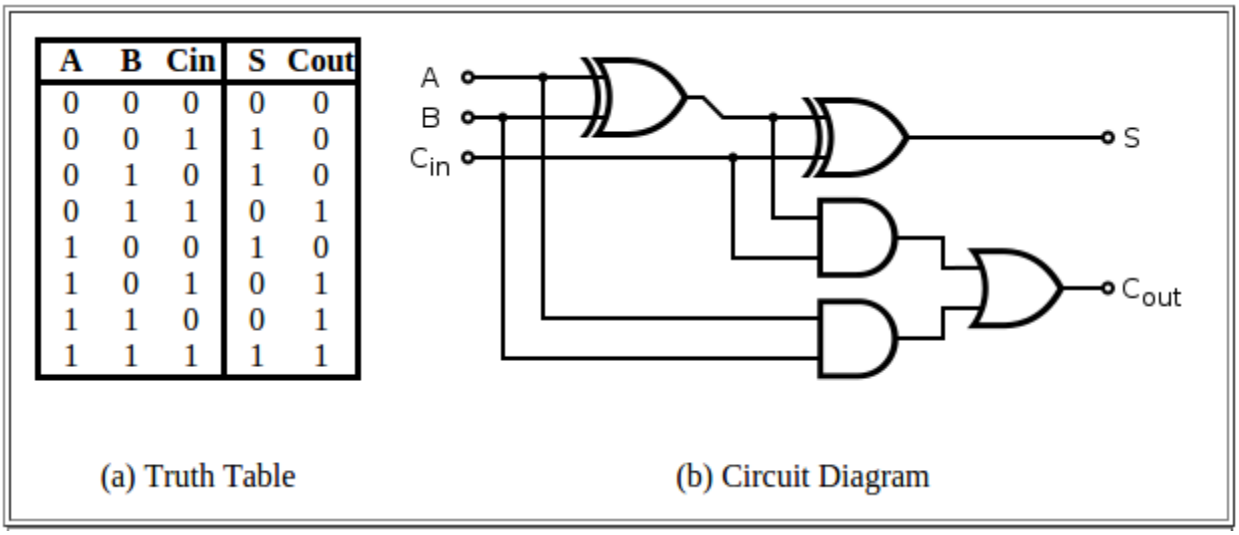
Multiplexer 4-1



A0 A1 O0 O1 O2 O3 | out | Expected Output
0 0 0 0 0 0 | 0 | in0:0
0 0 1 0 0 0 | 1 | in0:1
1 0 0 0 0 0 | 0 | in1:0
1 0 0 1 0 0 | 1 | in1:1
0 1 0 0 0 0 | 0 | in2:0
0 1 0 0 1 0 | 1 | in2:1
1 1 0 0 0 0 | 0 | in3:0
1 1 0 0 0 1 | 1 | in3:1
0 0 1 1 1 1 | 1 | in0:1
0 0 0 1 1 1 | 0 | in0:0
Assume the other inputs work like in0, etc..
Because the logic is symmetric.



Full
A B Cin |S Cout|Expected Output
0 0 0 | 0 0 | 0 0
0 0 1 | 1 0 | 1 0
0 1 0 | 1 0 | 1 0
0 1 1 | 0 1 | 0 1
1 0 0 | 1 0 | 1 0
1 0 1 | 0 1 | 0 1
1 1 0 | 0 1 | 0 1
1 1 1 | 1 1 | 1 1



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Truth Table (b) Circuit Diagram