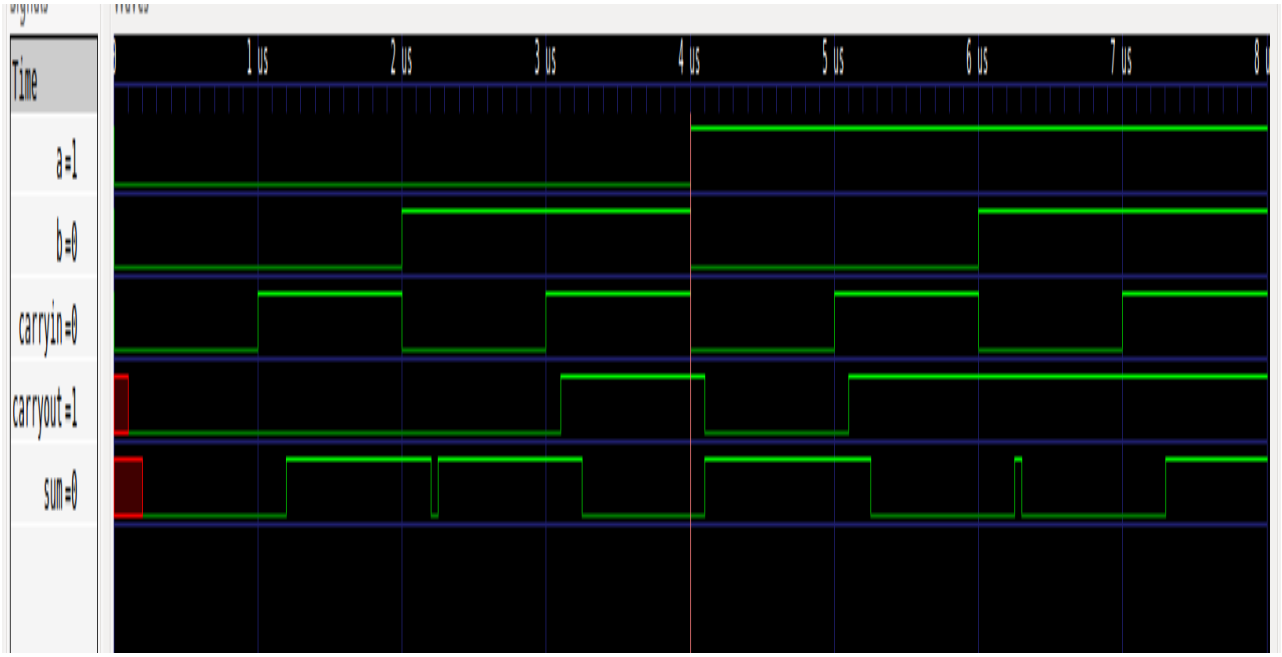
| a | b | carryin | carryout | sum | expected |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 0 |
| 0 | 0 | 1 | 0 | 1 | 0 1 |
| 0 | 1 | 0 | 0 | 1 | 0 1 |
| 0 | 1 | 1 | 1 | 0 | 1 0 |
| 1 | 0 | 0 | 0 | 1 | 0 1 |
| 1 | 0 | 1 | 1 | 0 | 1 0 |
| 1 | 1 | 0 | 1 | 0 | 1 0 |
| 1 | 1 | 1 | 1 | 1 | 1 1 |

Adder truth table showing expected behavior.




Adder waveform showing clear delay of the output.

En A0 A1| O0 O1 O2 O3 | Expected Output

0 0 0 | 0 0 0 0 | All false

0 1 0 | 0 0 0 0 | All false

0 0 1 | 0 0 0 0 | All false

0 1 1 | 0 0 0 0 | All false

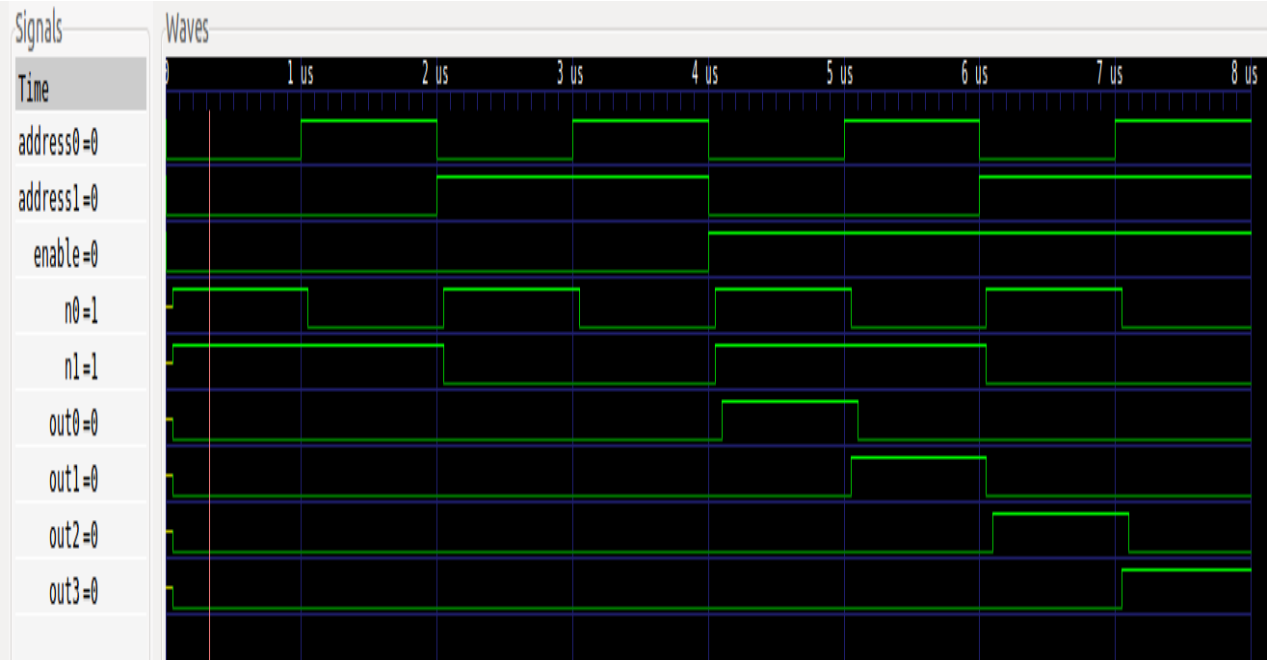
1 0 0 | 1 0 0 0 | O0 Only

1 1 0 | 0 1 0 0 | O1 Only

1 0 1 | 0 0 1 0 | O2 Only

1 1 1 | 0 0 0 1 | O3 Only

Decoder truth table showing expected behavior.




Decoder waveform showing output delay.

Expected Value = in3 for addr = 00

Expected Value = in2 for addr = 01

Expected Value = in1 for addr = 10

Expected Value = in0 for addr = 11

addr0 addr1 | in0 in1 in2 in3 | out

0 0 | 0 0 0 0 | 0

0 0 | 0 0 0 1 | 1

0 0 | 0 0 1 0 | 0

0 0 | 0 0 1 1 | 1

0 0 | 0 1 0 0 | 0

0 0 | 0 1 0 1 | 1

0 0 | 0 1 1 0 | 0

0 0 | 0 1 1 1 | 1

0 0 | 1 0 0 0 | 0

0 0 | 1 0 0 1 | 1

0 0 | 1 0 1 0 | 0

0 0 | 1 0 1 1 | 1

0 0 | 1 1 0 0 | 0

0 0 | 1 1 0 1 | 1

0 0 | 1 1 1 0 | 0

0 0 | 1 1 1 1 | 1

0 1 | 0 0 0 0 | 0

0 1 | 0 0 0 1 | 0

0 1 | 0 0 1 0 | 1

0 1 | 0 0 1 1 | 1

0 1 | 0 1 0 0 | 0

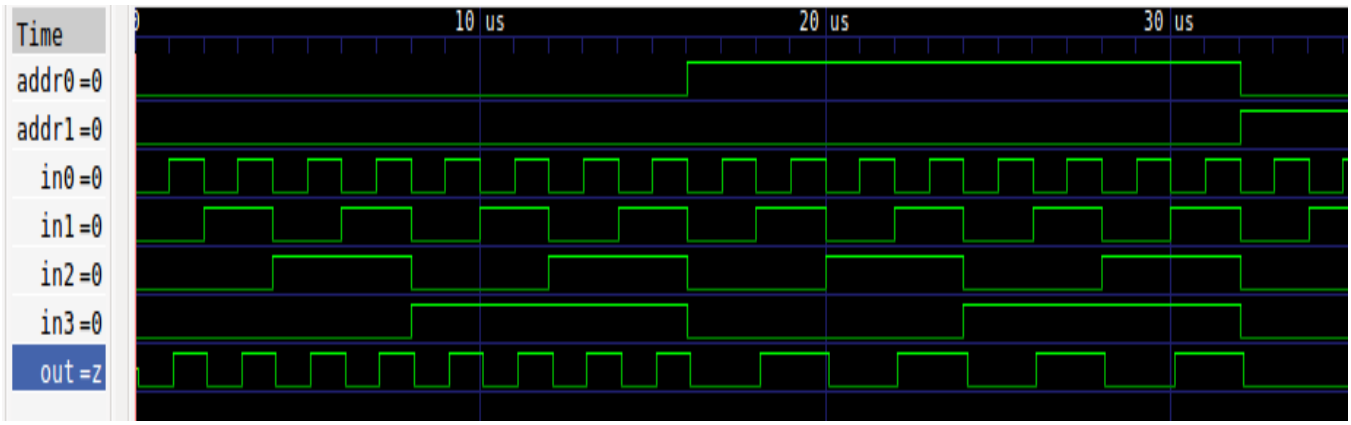
| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | | 1 |

Multiplexer truth table showing expected behavior…note that the above breaks down to this:

| Addr0 | Addr1 | | In0 | In1 | In2 | In3 | | Out |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | | X | X | X | 1 | | 1 |
| 0 | 1 | | X | X | 1 | X | | 1 |
| 1 | 0 | | X | 1 | X | X | | 1 |
| 1 | 1 | | 1 | X | X | X | | 1 |




Multiplexer waveform showing output delay.