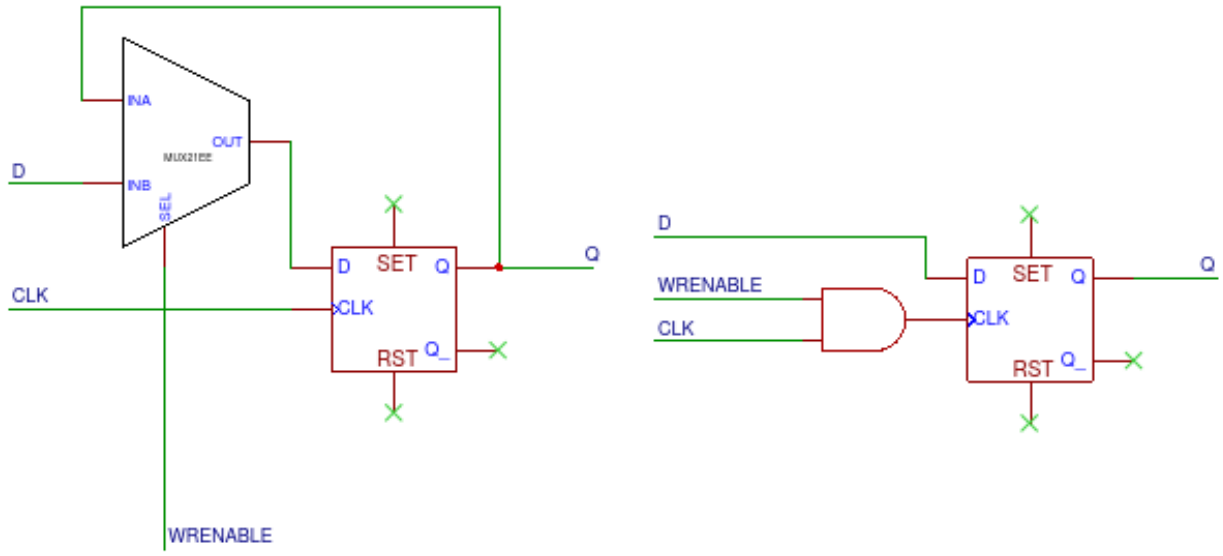
Deliverable 1:




The design on the right is flawed in that it will sometimes set Q in the middle of a clock cycle. If CLK is high and WRENABLE goes high, the DFF will latch the current value of D, regardless of whether or not it is in a glitch state. The design on the left will only ever latch on the rising clock edge, when D is guaranteed to not be in a glitch state.

Deliverable 6:
If enable is 0, enable<<address will always be zero. If enable is 1, enable<<address will be mostly zero, except its addressth bit will be 1. This is exactly the behavior of a decoder. The addressth bit of the output will be equal to 1 if enable is high, otherwise it will be zero. All the other bits of out will always be zero.