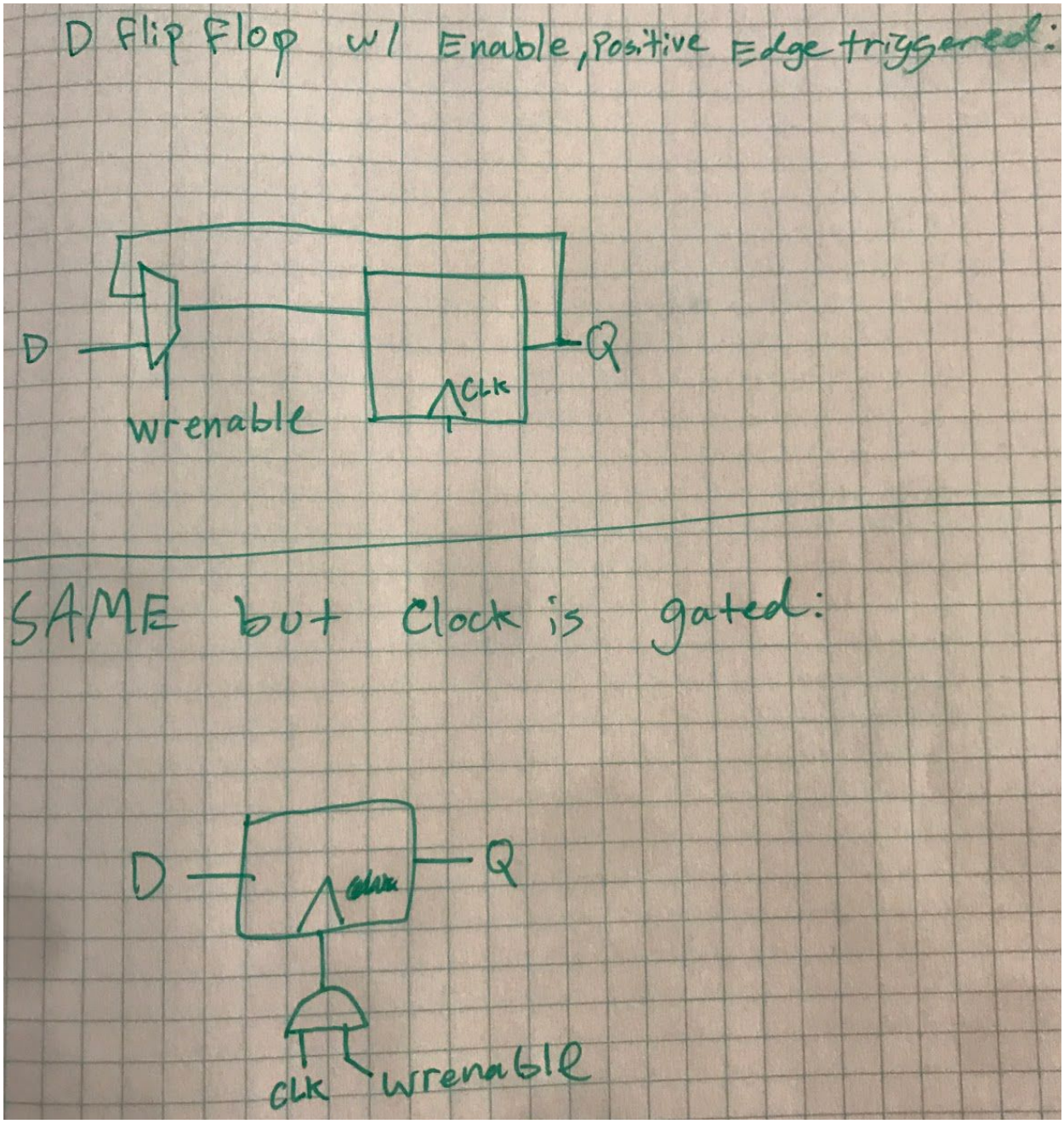
Chris Aring

Computer Architecture: HW 4

Deliverable 1:



Deliverable 2:

`module decoder1to32,` First sets the 0th bit of the **output** to **Enable**(1) and then gets bit-shifted by the value dictated by the 5-bit address wire. This sets the correct address to an **Enable**(1) signal and leaves all the others as a 0.