Joseph Lee, Sam Myers, Bryan Werth

Computer Architecture

Lab 0

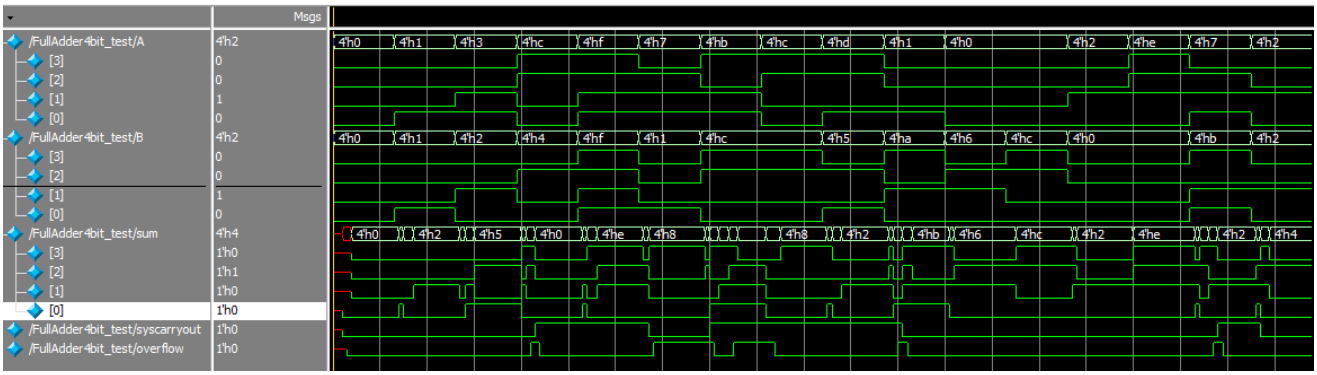

Figure 1. The waveform output for the testbench

The maximum delay for the full four bit adder is 650 ns if the gate delay is 50 ns. For a one bit adder, the maximum delay for the Cout output is 150 ns because in the worst case there are three gates to get the output. Also, the maximum delay for the Sum output is 200 ns because at worst there are four gates between input and output. Given this and the design of the four bit adder as four strung together single bit adders, the worst delay is the sum of the 150 ns Cout delay through three single bit adders followed by a 200 ns delay Sum delay on the last single bit adder (most significant bit). The sum of this is 650 ns.

We were concerned with the following cases, and implemented at least one test for each: two positive numbers without overflow, two positive numbers with overflow, two negative numbers without overflow, two negative numbers with overflow, one negative, one positive with a positive result, one negative, one positive with a negative result, two numbers that sum to the smallest 4-bit value (-8), two numbers that sum to the largest 4-bit value (7), and two zeroes. Theoretically, we would have been satisfied with these nine, but added seven additional tests (each of which falls into one of the above categories) for more coverage.

We didn't have any test case failures. On the FPGA, I tested to make sure the sum output was working. I also tested to make sure that both overflow and carryout were working. For sum, I tested a variety of inputs and checked to make sure the outputs were correct. For overflow and carryout I tested the cases that resulted in all possible versions of the outputs (overflow low and carryout high, overflow low and carryout low, overflow high and carryout low, and overflow high and carryout high). The data path delay of the implemented design in total is 6.656 ns with a 4.406 ns logic delay and a 2.25 ns route delay. The design did not take up a lot of space, as expected. Six of the 17600 slice LUTs were used in the design, all of which were used as logic.