Comparch Lab 2

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1 Input Conditioner

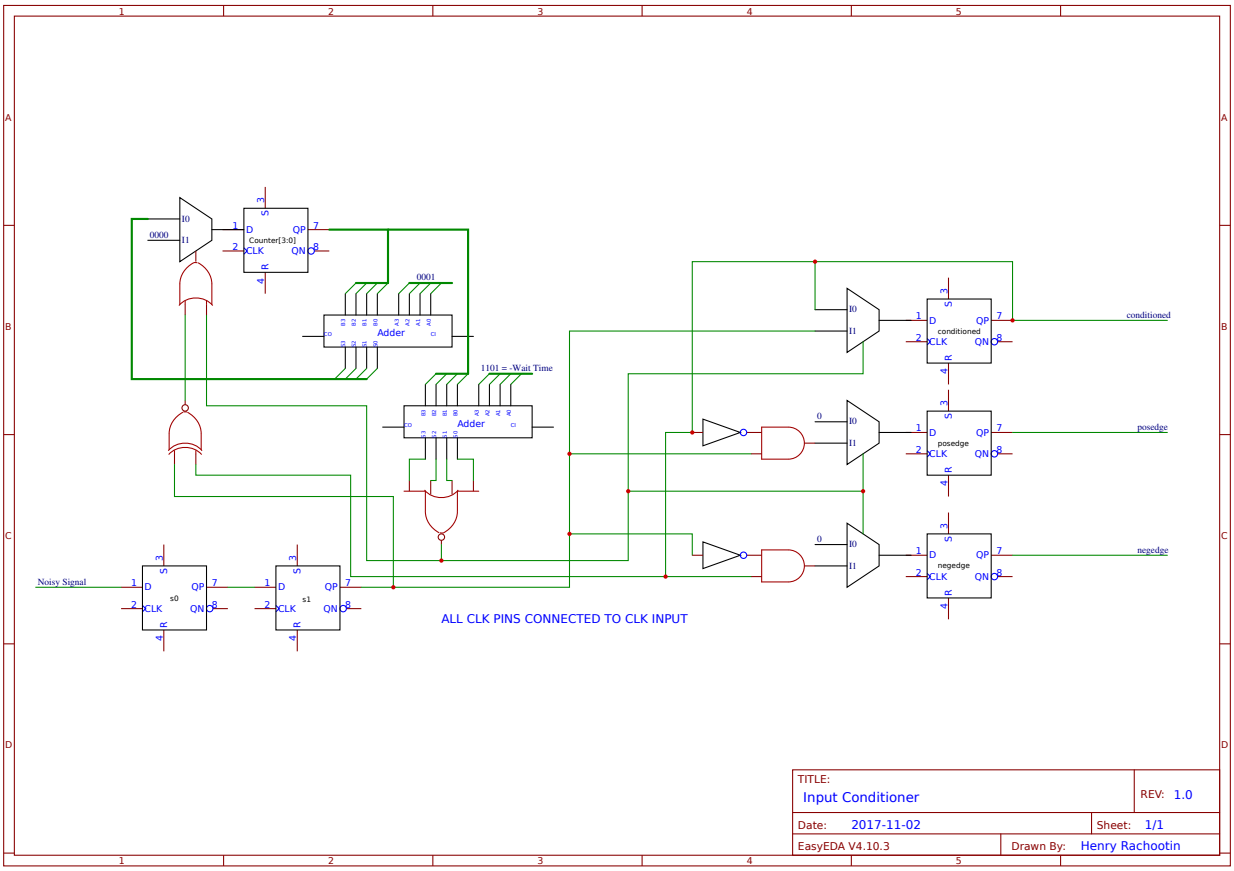
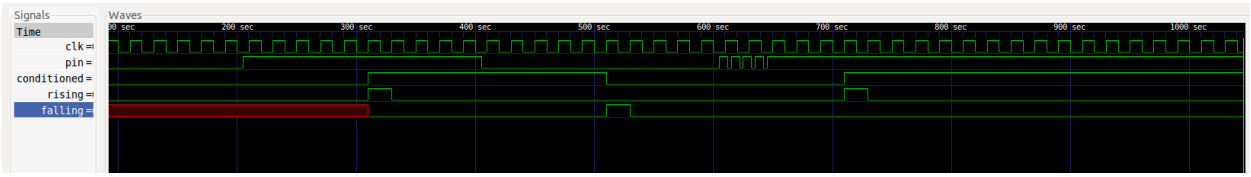


Figure 1: Possible schematic for input conditioner.



With a 50 MHz clock, each clock cycle will take

$$\frac{1}{50MHz} = 20ns$$

for signal to go through to the output, it must be held for at least $waitTime = 10$ clock cycles, or $200ns$. This is how long synchronizer 1 (s1) must be held in order for the output to update. The two clock cycle delay for the input to propagate to synchronizer 1 contributes latency to both the rising and falling (or vice versa) edges, so it will just phase shift the input, and will have no impact on the total glitch suppression time. Glitches less than 200 ns will be suppressed.

2 Shift Register

Testing the shift register was extremely simple. We parallel load 0x00, then test that parallel out and serial out are both 0x00 and 0b0 respectively. Then we serial load 0b11001010, and test that parallel out is that, and that serial out is 0b1. Then we parallel load 0b01010011, and check that serial out is 0b0 and that parallel out is 0b01010011. Then we try to parallel load 0xFF while we serial load 0b0, and verify that the parallel out is 0xFF (parallel load wins) and that serial out is 0b1. By doing these tests, we tested all the functionality of a shift register.

3 SPI Memory Test Bench

There are two main tests that we ran on the SPI memory. The first was a test to make sure that the chip select pin worked. We Tested this by raising the CS pin and checking that output of LIFO was in high impedance ($\mathbb{Z}$) mode. The second test was a read/write test where 0x0F was loaded into buffer 55 and subsequently read to make sure the output was consistent with the input. Since the datamemory was provided we assumed that reading and writing to a single address was exhaustive, however seeing as datamemory did not compile in its shipped state this assumption may have been wrong.