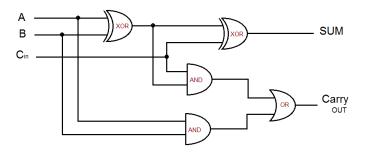
Adder

The full adder is a digital circuit that performs addition of 3 one bit numbers, including a number "carried in", then giving an output "sum" and a number "carried out". Adders connected congruently can perform equations that are more complex.

Α	ì	В	Τ	Cin	Cout	Т	Su	m E	хр	Sum Exp Out
0	Ĺ	0	Ĺ	0	0	Ĺ	0	Ĺ	0	0
0	Ť	0	Ť	1	0	Ĺ	1	Ĺ	1	0
0	Т	1	Т	0	0	П	1	1	1	0
0	Т	1	Т	1	1	П	0	1	0	1
1	Т	0	Т	0	0	П	1	-1	1	0
1	Т	0	Т	1	1	-1	0	1	0	1
1	1	1	Т	0	1	1	0	1	0	1
1	1	1	1	1	1	1	1	1	1	1 1 _



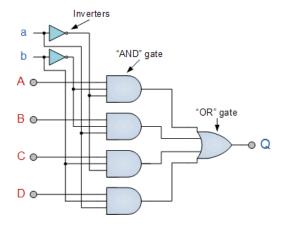
The module is created using 2 XOR gates to find the output, "sum", then 2 AND gates leading into our OR gate giving the carry out output.



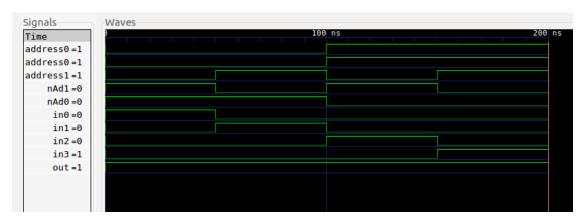
The "CarryIn" input can represent the input from another adder when using adder chains for more complex problems. The "CarryOut" value may eventually become the "CarryIn" of the next adder.

Mulitplexer

Α0	Τ	A1	Τ	In0	Τ	In1	Τ	In2	Τ	In3	Τ	Out Expected Output
0	Ĺ	0	Ť	1	Ť	0	Ť	0	Ť	0	Ť	1 In0
0	Т	1	Т	0	Т	1	Т	0	Т	0	Т	1 In1
1	Τ	0	Т	0	Т	0	Т	1	Т	0	Т	1 In2
1	Ī	1	Ī	0	Ī	0	Т	0	Т	1	Ī	1 In3



A multiplexer uses 2 Inverters, 4 AND gates, and 1 OR gate. The purpose of a multiplexer is to use the "a" and "b" inputs in order to select one (or zero) of the 4-bit input options.

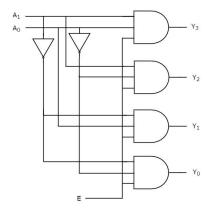


In the wave diagram, we can see at any given point, the output is true because at least one input, A through D (in0-in3), is true at any moment, funneling into our final output.

Decoder

En	Α0	A1	00	01	02	03	-	Expected Output
0	0	0	0	0	0	0	Ť	All false
0	1	0	0	0	0	0	Ť	All false
0	0	1	0	0	0	0	Ĺ	All false
0	1	1	0	0	0	0	Ĺ	All false
1	0	0	1	0	0	0	Ĺ	00 Only
1	1	0	0	1	0	0	Ĺ	O1 Only
1	0	1	0	0	1	0	İ	02 Only
1	1	1	0	0	0	1	Ĺ	03 Only

The decoder is a logic device that will convert binary codes (in this case, 2-bit) into 2^n possible values, or, the opposite of an encoder. Here, 2 input values, and an enabler switching the device "on" or "off" will create possible output results.



As you can see on the wave graph below, although there are changes in inputs like address0 early on, the outputs remain constant until the enable switch is activated. Once this happens at 4000 sec, the outputs begin to react to changes. At any given moment in the graph, only 1 output is true.

