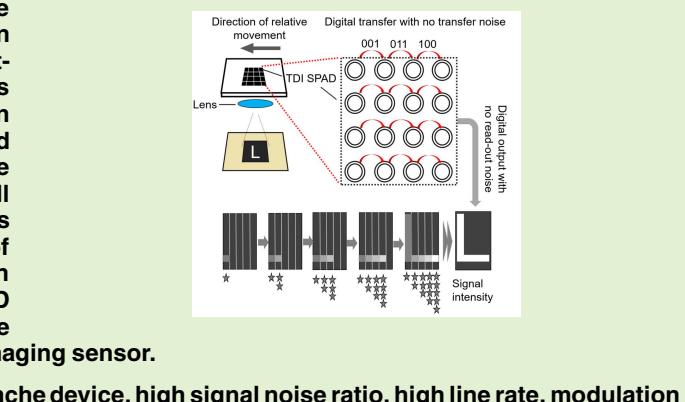


Time-Delay-Integration Imaging Implemented With Single-Photon-Avalanche-Diode Linear Array

Xiangshun Kong, Cheng Mao^{ID}, Xuemei Hu^{ID}, Member, IEEE, and Feng Yan

Abstract—In this paper, we propose a novel kind of time delay integration (TDI) image sensor based on single photon avalanche diode (SPAD), i.e. TDI-SPAD. Compared with existing TDI imaging devices, the proposed TDI-SPAD sensor is characterized by low noise, high sensitivity, high modulation transfer function (MTF) and transfer efficiency. The proposed architecture design of multi-stages TDI-SPAD sensor and the digital transfer circuits are discussed in detail, and the full function of TDI-imaging is demonstrated with experiments based upon two SPAD sensors. First, the imaging function of TDI-SPAD is verified through imaging of scanning scene with a 128 × 128 SPAD array. Then, we fabricate a 256 × 2 TDI-SPAD sensor, build a TDI-imaging camera system, and demonstrate the feasibility and SNR improvement of the proposed TDI-imaging sensor.

Index Terms—Time delay integration, single photon avalanche device, high signal noise ratio, high line rate, modulation transfer function.



I. INTRODUCTION

TIME delay integration (TDI) is an ingenious imaging method to obtain high signal to noise ratio (SNR) images in high speed line-scan mode imaging systems. With TDI imaging, the equivalent integration time is prolonged with the number of stages, and the signal to noise ratio (SNR) can be improved accordingly. In general, TDI technique is widely applied to improve SNR significantly in low light level and high speed imaging applications [1], [2], such as satellite remote sensing imaging, airborne push broom imaging and industrial monitoring, etc. For example, in the satellite remote sensing imaging, the integration time of the sensor is relatively short due to the fast motion of the satellite. The single-stage linear array imaging sensor cannot obtain images with enough

SNR, so it is necessary to improve the SNR with the help of TDI technology.

TDI imaging is firstly implemented upon CCD sensors [3] due to the fact that the working principle of charge transfer in CCD could be directly utilized to realize signal transfer and accumulation. In TDI-CCD sensors, charges of the former stage are transferred to the next stage for further integration. However, this analog shift mode cannot guarantee the integrity of the signal in the process of transfer, so that the SNR and modulation transfer function (MTF) will be reduced.

Some other kind of TDI imaging sensors are proposed, i.e. TDI CMOS image sensors (TDI-CIS) [4]. Most of the TDI-CIS are designed for digital signal accumulation, which is different from the traditional analog signal transfer and accumulation mode of TDI-CCDs. The key advantage of digital signal accumulation is that the noise introduced by the charge transferring could be avoided since the signal is accumulated in digital mode. However, the signal must be converted to digital signal with analog to digital (ADC) process first before being accumulated, which requires more time to process the signal and introduces additional read out noise.

Recently, single photon avalanche diode (SPAD) is emerging and gains wide interest due to its capability in detecting single-photon [6]. With SPAD, light intensity could be detected in digital mode, with no ADC process required and

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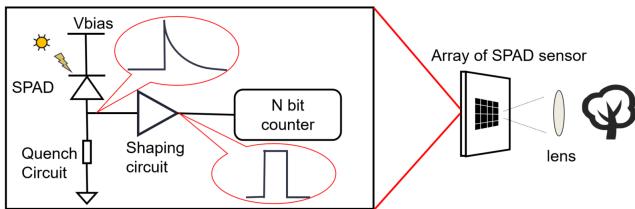


Fig. 1. Working mechanism and circuit structure of SPAD for imaging.

thus no read out noise introduced. Due to these characteristics, SPAD is promising for implementing the next generation of TDI techniques. In [12], an imaging sensor based upon SPAD is proposed to accumulate signals of different columns with the single photon counting mode of SPAD. However, multiple columns of the SPAD sensor are connected to the same counter and there is no transfer structure between stages. So pixels of different columns cannot detect signals simultaneously, thus the proposed sensor is not capable of realizing time delay integration imaging.

In this paper, we propose a TDI imaging technique based upon SPAD. To our knowledge, we are the first to realize the full function of TDI-imaging based upon SPAD [7]. Specifically, the implementation details of the proposed TDI-SPAD sensor is provided, including both the design of the digital TDI transfer structure, and the multi-stage TDI-SPAD sensor design. Then, we thoroughly analyse the performance characteristic and advantages of the proposed TDI-SPAD, through comparing with the existing TDI technologies. Furthermore, we demonstrate the proposed TDI-SPAD design through experiments with two designed TDI-SPAD sensors. In all, we propose a novel TDI-SPAD architecture, and demonstrate the effectiveness and advantage of it through both theoretical analysis and physical experiments.

II. TDI-SPAD DESIGN

A. Working Mechanism of SPAD Device as Imaging Device

Fig. 1 shows the architecture of single SPAD sensor, consisting of a reverse diode, quenching circuits, shaping circuits and N-bit counters. The diode is reverse biased at a voltage that exceeds the breakdown voltage of the p-n junction. When photons incident on the active area of the diode, an avalanche will be triggered, and the quenching circuit is applied to lowering the biased voltage to quench the avalanche. After the avalanche and quenching, the current impulse is generated and transferred to a shaped pulse. The counter can detect the rising edge of the shaped pulse and count the number of photons arrived during the exposure time. Since the number of photons are recorded in a digital way and no readout circuits are required, compared with the traditional CCD and CIS devices, SPAD has the characteristics of zero readout noise and high dynamic range [9], [10].

As shown in Fig. 2, here we show a 4-bit asynchronous counter. The 4-bit counter is composed of 4 D flip-flop (DFF), which is the most common and simple counter structure in digital circuit.

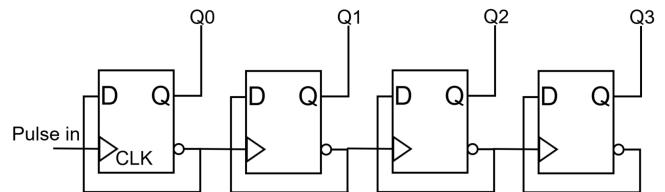


Fig. 2. Schematic of 4-bit ripple counter.

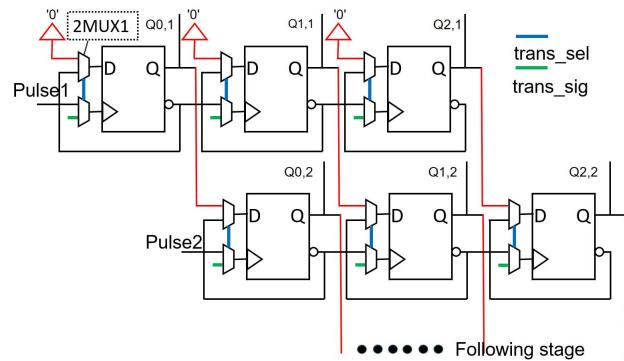


Fig. 3. Schematic of ripple counter designed for TDI.

However this kind of counter structure can only realize single-stage photon counting, and can not transfer the count value to the the counter of next stage. So based on this structure, we design a novel transfer counter circuit used for TDI imaging, which will be introduced as followed part B.

B. Design of Digital TDI Transfer Structure

Due to the imaging mode of photon counting, the digital signal can be easily transferred to the next stage of counter for integration. The digital transfer mode structure is designed based on common ripple counter, as shown in Fig. 3. For simplicity, here we show two adjacent TDI stages, each with a 3-bit counter. As shown, two 2-1 multiplexer (MUX) modules are connected to the D and CLK inputs of each D flip-flop (DFF) respectively. With the MUX module, the proposed circuit could work in both counting mode and transferring mode. In the counting mode, the circuit works in the same way as the ripple counter as shown in Fig. 2. When each photon-induced rising edge of a shaped pulse is input to the counter, the count value of the counter is increased by one. In the transferring mode, the DFF sequence works like shift registers. The signal of the former TDI stage will be transferred to the counter of the next TDI stage when the rising edge of the transfer signal arrives. Note that since the first stage counter has no data to transfer from, it is reset to zero.

The timing diagram of the signal transfer is shown in Fig. 4, when the tran_sel signal is set to logic low, the circuit works in the counting mode, which can detect the rising edge of the pulse of each stage and realize the counting function. When the signal is set to logic high, the circuit works in the transfer mode. Upon the arrival of rising edge of the trans_sig signal, the data of former stage will be transferred to the next stage synchronously. Due to the rising edge triggered mode of the shift register, the count value of all registers will be

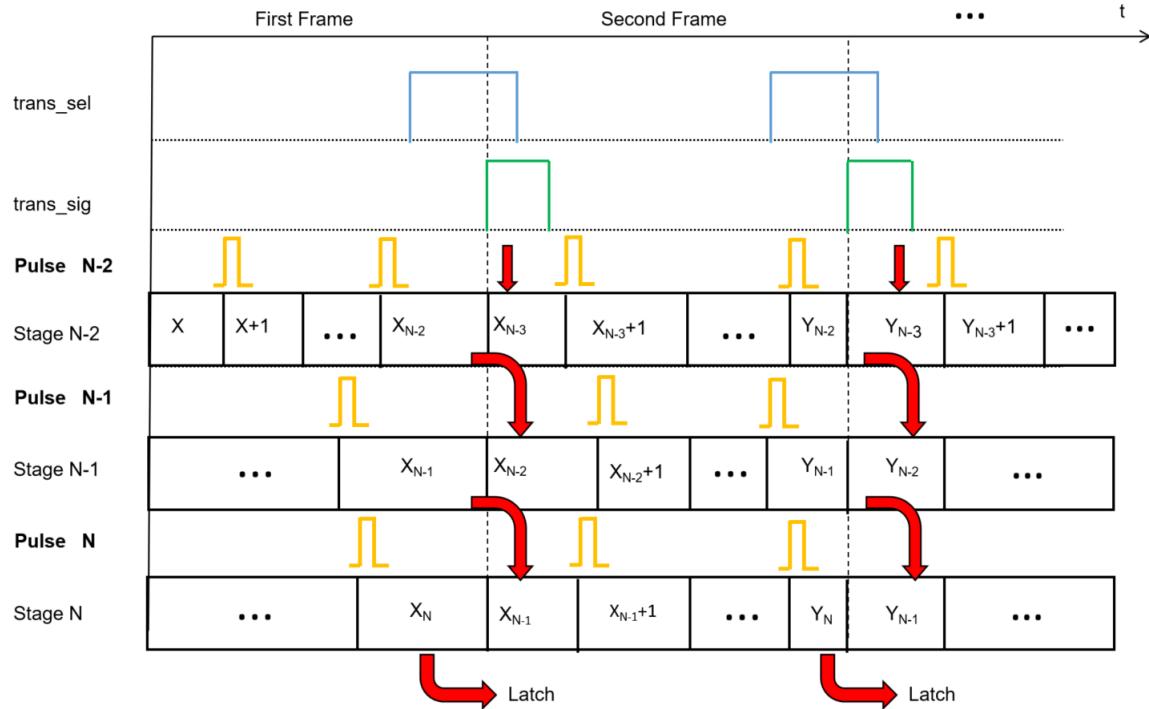


Fig. 4. The timing diagram of transfer process.

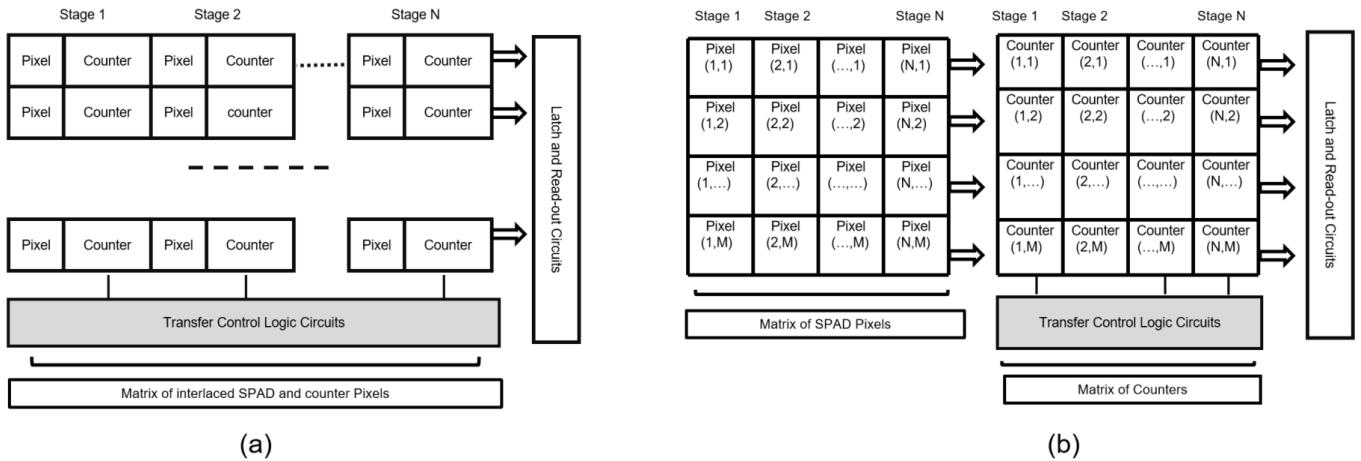


Fig. 5. Block diagram and circuit structure of SPAD for imaging. (a) is the first kind of implementation method diagram, which arranges pixels and counter circuits alternately. (b) is the second kind of implementation method diagram, which places pixels and registers separately to form two arrays.

synchronously transferred to the next level in one clock cycle. The count value of the last stage counter will be transferred to the latch, and the addressing circuit will read it out circularly and the reading process of one frame TDI image is completed.

On the basis of common ripple counter, we have carried out innovative design and proposed a counter architecture with transfer function. This counter circuit can realize the combination of count and transfer function to achieve the TDI requirements.

C. Multi-Stage TDI-SPAD Design

Based on the structure of transfer counter circuits proposed above, the transferring of digital signal between adjacent stage pixel can be realized, and multi-stage TDI SPAD array can be designed.

Depending on the arrangement of pixel and counter, the layout of the sensor can be different, as shown in Fig. 5 (a) and Fig. 5 (b). In the existing 2D planar CMOS process, there are two TDI-SPAD implementation methods of circuits layout. The first way is to arrange pixels and counter circuits alternately, as shown in Fig. 5 (a). The other way is to place pixels and registers separately to form two arrays, and the circuit structure is shown in the Fig. 5 (b). The first schematic of TDI-SPAD implementation is simple and easy to fabricate. However, the area occupied by the counter will largely decrease the fill factor and reduce the MTF caused by optical lens distortion. So in our implementation, we adopt the second type of sensor layout.

The second kind of TDI-SPAD layout is similar to the traditional CCD and CIS arrangement, as shown in Fig. 5 (b).

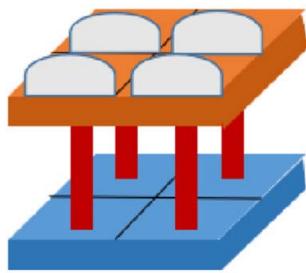


Fig. 6. 3D stacking technology applied in TDI-SPAD.

The pixels and the counter are arranged in two array separately and the signals between them are transmitted by metal interconnects, so that the fill factor will not be influenced by the counter array.

These two kinds of TDI-SPAD have their own advantages in different application scenarios. The first structure is simple in design, but it will lose the spatial resolution; the second one is not conducive to large-scale stages integration in 2D CMOS process, but the design is compact and the spatial resolution is relatively high during same integration time.

With the increase of TDI stages, the connection between pixels and counters will become more difficult in second kind layout. As far as we know, 3D stacking technology has been successfully applied in the design of SPAD detector array [11], and has gradually become the mainstream of research in breaking layout limit in SPAD array design. So when more TDI stages applied, 3D stacking technology will be helpful to solve this problem. As shown in Fig. 6, the detector array and logic circuit are designed in two layers, and connect them by Through silicon Via (TSV) to solve the problem of connection difficulty when the stages is too much. This method is one of our research directions, but it is not emphasized in this paper. The detailed design of the sensor architecture will be discussed in Sec. III.

III. CHARACTERISTIC OF TDI-SPAD

In this section, we will give a thorough discussion of the characteristics of TDI-SPAD by comparing with the existing TDI-technologies implemented in CCD and CMOS.

A. Transfer Mechanism & Line Rate

In TDI applications, line rate is a very important parameter, which means the times of signal transfer in a unit time when TDI sensor working. It determines the exposure time of each TDI stage and the time required to scan a scene. Generally speaking, the higher the speed of push scan imaging, the higher the line rate required and for the same push scan speed, the higher the line rate is, the higher the imaging resolution will be. Among different TDI imaging techniques, signals are transferred by different mechanism, thus the line rate bottleneck is different. Here we will discuss the line rate and transfer noise in different TDI imaging methods and compare it with the proposed TDI-SPAD imaging technique.

In TDI-CCD sensors, charges are transferred among different stages to realize time delay integration imaging, shown

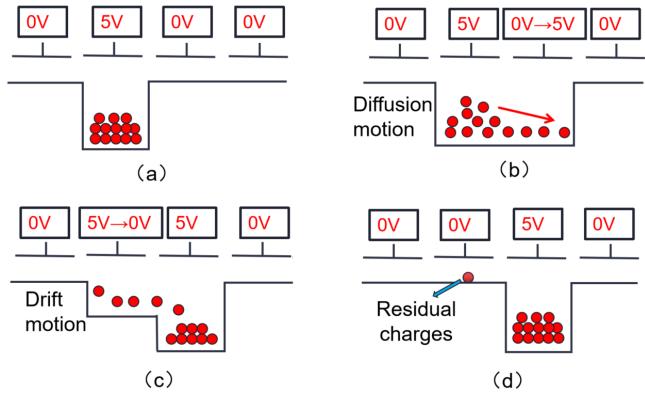


Fig. 7. Transfer process of CCD device. (a) First phase in transfer process. (b) Second phase in transfer process. (c) Third phase in transfer process. (d) The transfer process accomplish and residual charges generated.

as Fig. 7. Through changing semiconductor surface potential well voltage under the electrode, charges can be either stored or transferred. The charges motion mode in CCD contains drift motion and diffusion motion. Because drift motion is much faster than the diffusion motion in semiconductor and the relaxation time of transfer process is determined by diffusion motion, the transfer frequency of TDI-CCD are mainly limited by the carrier diffusion rate. In diffusion and drift motion process, since the charge at the electrodes decreases exponentially with time, so charges will not completely be transferred to the next stage and part of charges will be lost.

For example, for a three-phase TDI-CCD, at room temperature, with signal loss rate at 10^{-4} , the transfer time between two stages is at least 30ns [16]. Therefore, for general TDI-CCD, the highest transfer frequency can be more than 10 MHz, and it is independent with the stages' number of image sensors. Besides, limited by the ADC process at the last stage of TDI, the working line rate of TDI-CCD is generally lower than 200kHz, e.g. the maximum line rate of a commercial TDI-CCD of Hamamatsu is 50kHz [19].

TDI-CIS has attracted much attention in recent years, and there are mainly two methods to realize it. The first way to transfer the charges between the well capacitance of CMOS, imitating the charges transfer method of CCD [15]. However, since analog transfer TDI-CIS is not mature enough, it has not become the mainstream design method. The other method is based on the digital transfer of CIS area array coupled with on-chip adder [4], [13], as shown in Fig. 8. This structure usually shares a column of ADC, and the output signal of ADC is shifted and added by peripheral adder and register array to realize the function of digital transfer. The TDI line rate of this implementation method is comparably low, especially when the stages is large. For example, TDI-CIS in [15] of digital transfer mode have maximum line rate of 40 kHz with the stage number of 12, while TDI-CIS in [13] have maximum line rate up to 3.8 kHz when the stage number is 128. The more times column ADC is multiplexed, the longer it takes to complete a frame exposure, so the lower line rate is.

Different from TDI-CCD and TDI-CIS, the process of TDI-SPAD signal transfer is implemented with digital shift register, as discussed in Fig. 3, requiring only a

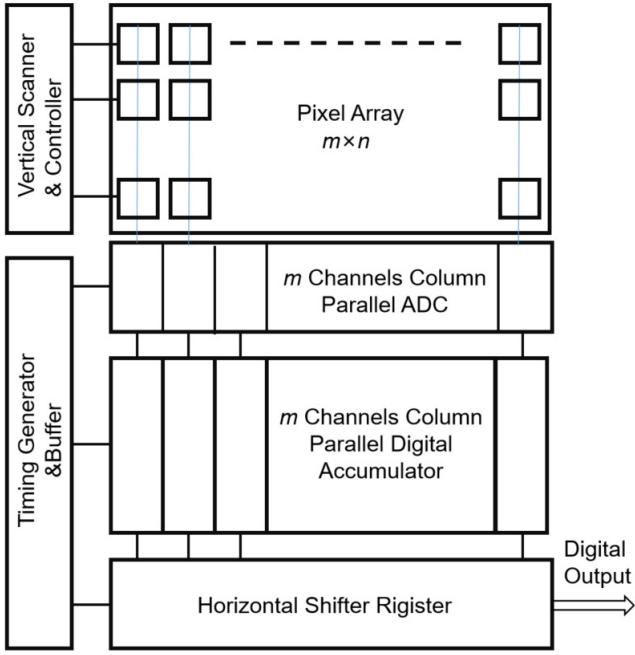


Fig. 8. Block diagram of TDI CMOS image sensor.

few nanoseconds. Since there is no ADC process in TDI-SPAD imaging system and its signal transfer process is all digital, neither the transfer time nor ADC time is the bottleneck of TDI-SPAD's line rate. The line rate of TDI-SPAD is bottlenecked by the working clock and the dead time of SPAD sensor, which can reach up to 50 MHz in theory. Thus in terms of line rate, TDI-SPAD is promising in the field of ultra-high speed scanning imaging. However, in general TDI-SPAD imaging process, enough data reading time are required, so that the maximum line rate can only reach around 1 MHz. Note that, by using higher speed data read-out or buffer method, the line rate of 50 MHz or even higher can be achieved.

B. Noise and Modulation Transfer Function

In a TDI image system of N stages, the enhancement of SNR could be expressed as Eq. 1,

$$\text{SNR} = 20 \log \frac{\sqrt{N} \cdot Q_{\text{photon}}}{\sqrt{Q_{\text{photon}} + \sigma_{\text{noise}}^2}}, \quad (1)$$

where Q_{photon} denotes the average signal of each stage, $\sqrt{Q_{\text{photon}}}$ denotes photon shot noise and σ_{noise} denotes the other noise. For different TDI-imaging techniques, there are different sources of σ_{noise} .

In TDI-CCD, σ_{noise} is mainly composed of fixed pattern noise, dark current noise, transfer noise, reset noise, etc. It can be represented as,

$$\sigma_{\text{noise}}^2 = N \cdot \sigma_{\text{dark}}^2 + N \cdot \sigma_{\text{fpn}}^2 + \sigma_{\text{cte}}^2 + \sigma_{\text{read}}^2 + \sigma_{\text{reset}}^2 \quad (2)$$

where σ_{dark} is dark current noise of CCD image sensor, σ_{fpn} is fixed pattern noise due to the difference of light sensitivity between pixels, σ_{cte} is charge transfer efficiency (CTE) noise due to the photon charges residue during transferring process,

σ_{read} is mainly composed of KTC noise and ADC quantization noise [20]. The charge transfer efficiency noise is

$$\sigma_{\text{cte}}^2 = 2Q_{\text{trans}}(1 - \eta)N \quad (3)$$

where Q_{trans} is the number of electrons transferred, η is the charge transfer efficiency. The CTE noise is positively correlated with stage number N , so that the more stages, the larger the CTE noise will be introduced.

As for TDI-CIS, σ_{noise} is composed of fixed pattern noise, dark current noise and read-out noise, etc. It can be represented as

$$\sigma_{\text{noise}}^2 = N \cdot \sigma_{\text{dark}}^2 + N \cdot \sigma_{\text{read}}^2 + N \cdot \sigma_{\text{fpn}}^2 \quad (4)$$

where σ_{dark} is dark current noise of CIS sensor, σ_{read} is mainly composed of KTC noise and ADC quantization noise, and σ_{fpn} is fixed pattern noise [21]. N times read out noise in the process of N stage signal accumulation is introduced in TDI-CIS.

In TDI-SPAD, σ_{noise} consists of dark noise and fixed pattern noise,

$$\sigma_{\text{noise}}^2 = N \cdot \sigma_{\text{dark}}^2 + N \cdot \sigma_{\text{fpn}}^2 \quad (5)$$

where σ_{dark} is the dark count noise in SPAD, which is similar to dark current noise of CCD caused by thermal excitation. Besides, the inhomogeneity between pixels will introduce the FPN noise, which can be eliminated by flat field correction [10]. The verification of FPN correction method will be introduced in the next section. Compared with the other TDI imaging sensors, other types of noise such as read-out noise, charge transfer noise and reset noise are not contained in the noise of TDI-SPAD, attributing to the digital counting mode of SPAD imaging. The main noise source of SPAD is dark noise, and the main factors that influence the dark noise level are doping concentration, processing node, and device structure of SPAD device. Through applying advanced technology, the dark noise level could be reduced to less than 1cps [22], which is close to the noise level of CCD or CIS sensors.

Further, we analyze the influence of transfer noise on modulation transfer function (MTF). There are two main reasons for the decreasing of MTF in TDI imaging mode, i.e. optical distortion and incomplete charge transfer of imaging sensor. Without loss of generality, only the latter one is discussed. The noise introduced by charge transfer can be represented as [23]–[25],

$$\text{MTF} = \exp(-2N(1 - \eta)) \quad (6)$$

where η denotes the transfer efficiency of TDI sensor, and N denotes the stages number of TDI-sensor.

We plot the MTF of TDI-CCD, TDI-CIS and TDI-SPAD in Fig. 9 and compare the influence of charge transfer efficiency and stage number upon MTF. As shown, for TDI-CCD, MTF decreases with the increase of stage number and the decreasing speed is higher with a lower charge transfer efficiency. Since that there is no analog charge transfer process in TDI-SPAD and TDI-CIS, all the signal captured by each stage is transferred to next stages completely via digital transfer process.

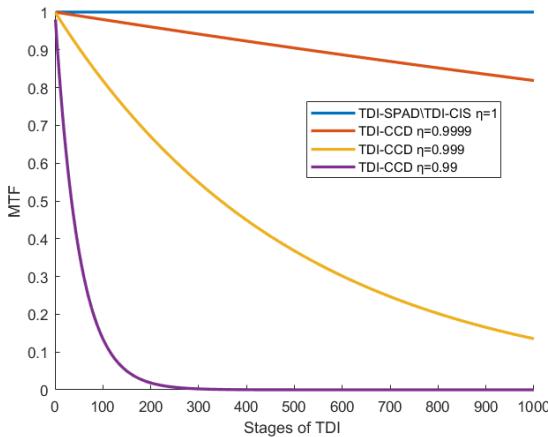


Fig. 9. Modulation transfer function of different TDI-techniques.

C. Light Response Characteristic

The definition of light saturation in the imaging mode of SPAD photon counting is different from that of CCD and CIS. For CCD and CIS sensors, when the light intensity is saturated, it means that the photocarriers completely occupy the potential well, which indicates that even under very low illumination, after a long time of integration, the sensor will get saturated [16]. For SPAD devices, saturation happen only when the illuminance (i.e. incident photon rate) is high, which is not related with the amount of charge accumulated in exposure time [10]. When the photon rate is too high and the output pulse interval approaches the dead time of SPAD, the SPAD become saturated. The comparison of light saturation principle between SPAD and CIS/CCD is shown in the Fig. 10.

Taking the passive quenching circuit model as an example, the light response of SPAD can be described by the Eq. 7 [27],

$$N_{\text{count}} = \frac{q\phi T}{1 + q\phi\tau_d} \quad (7)$$

where N_{count} denotes photon count value of SPAD device excited by photon incidence, ϕ denotes incident photon rate, T denotes exposure time, q denotes quantum efficiency of SPAD device, and τ denotes the dead time of SPAD. When ϕ is relatively low, the response curve is approximately linear, and when ϕ is high, the response curve begins to bend, shown as Fig. 10. Since TDI imaging method are mostly applied under low illuminance [4], [19], each stage of TDI-SPAD could work in the linear light response state. Furthermore, due to the fact that the accumulation is implemented in digital mode, at any stage under low light, the SPAD is working in linear response state, so that the nonlinear errors is ignorable in TDI-SPAD.

For TDI-CCD devices, the situation is different: the front stages devices can be kept linear, but as the number of stages increases, the equivalent integration time becomes longer, the well capacitance approaches full, and the response curve begins to bend, causing non-ignorable nonlinear errors, especially when the stage number is large.

Although TDI-CIS is a charge accumulation device, the accumulated charge will be emptied after each digital transfer, so the well charges would not be saturated with the increase of the integral times either.

In low light illuminance, TDI-SPAD devices can keep working at linear light response stage and the bit width of the counter of each stage is the only restriction of the maximum photon count of SPAD, i.e. the dynamic range is determined by the bit width of the counter. In TDI imaging mode, the equivalent integration time of the front stage is relatively shorter than the equivalent integration time of the successive stage. Therefore, instead of adopting uniform bit width of counter, it is efficient to adopt non-uniform count bit-width, i.e., the maximum bit width of the counter changes with the stage number. Assuming that the maximum number of photon counting in the integration time is K , the number of bits of the first stage counter n_1 must meet the condition $2^{n_1} \geq K$. Since the second stage will inherit the photon counting data of the first stage, the maximum number of photons counting in the second stage is $2K$. Therefore, the corresponding full count value of the i th stage register is iK , and the counter bit width n of the i th stage should satisfy the following equation $2^{n_i} \geq iK$, i.e. $n_i \geq \log_2(i \cdot K)$.

As shown in Table I, we conclude the main characteristics of three different TDI devices. It can be seen that TDI-SPAD device has outstanding advantage in the main noise source, transfer efficiency, line rate and so on compared with the other two kind of TDI devices, which is quite promising to be applied in the TDI technique. For applications that require high line rate and low transfer noise, TDI-SPAD is a more promising choice for many applications, such as satellite remote sensing, airborne push broom imaging and industrial monitoring, etc., compared with TDI-CCD/CMOS. Specifically, due to its high line-rate, it is more promising to adopt TDI-SPAD in satellite remote sensing and airborne push broom imaging to obtain images with much higher ground resolution. At the same time, due to the advantage of lower transfer noise and no readout noise, TDI-SPAD can be designed with more stages to obtain sufficient SNR. In the field of industrial monitoring, the faster the scanning speed of the monitoring, the less sufficient light to guarantee enough SNR in monitoring. TDI-imaging based upon the proposed TDI-SPAD with more stages is essential in higher SNR improvement without introducing additional readout noise or transfer noise compared with TDI-CCD/CMOS.

IV. CHIP DEMONSTRATION & EXPERIMENTAL RESULTS

Two group of experiments are carried out to verify the feasibility of TDI-SPAD. The first group of experiments is based on 128×128 SPAD array, and the TDI process is simulated by off chip accumulation to verify the working mechanism of multi-stage TDI-SPAD. The other group of experiments is based on 256×2 TDI-SPAD chip with transfer counter to verify the feasibility of the transfer counter circuit, the effect of multi-stage accumulation on imaging quality, and the feasibility of flat field correction in TDI-SPAD mode.

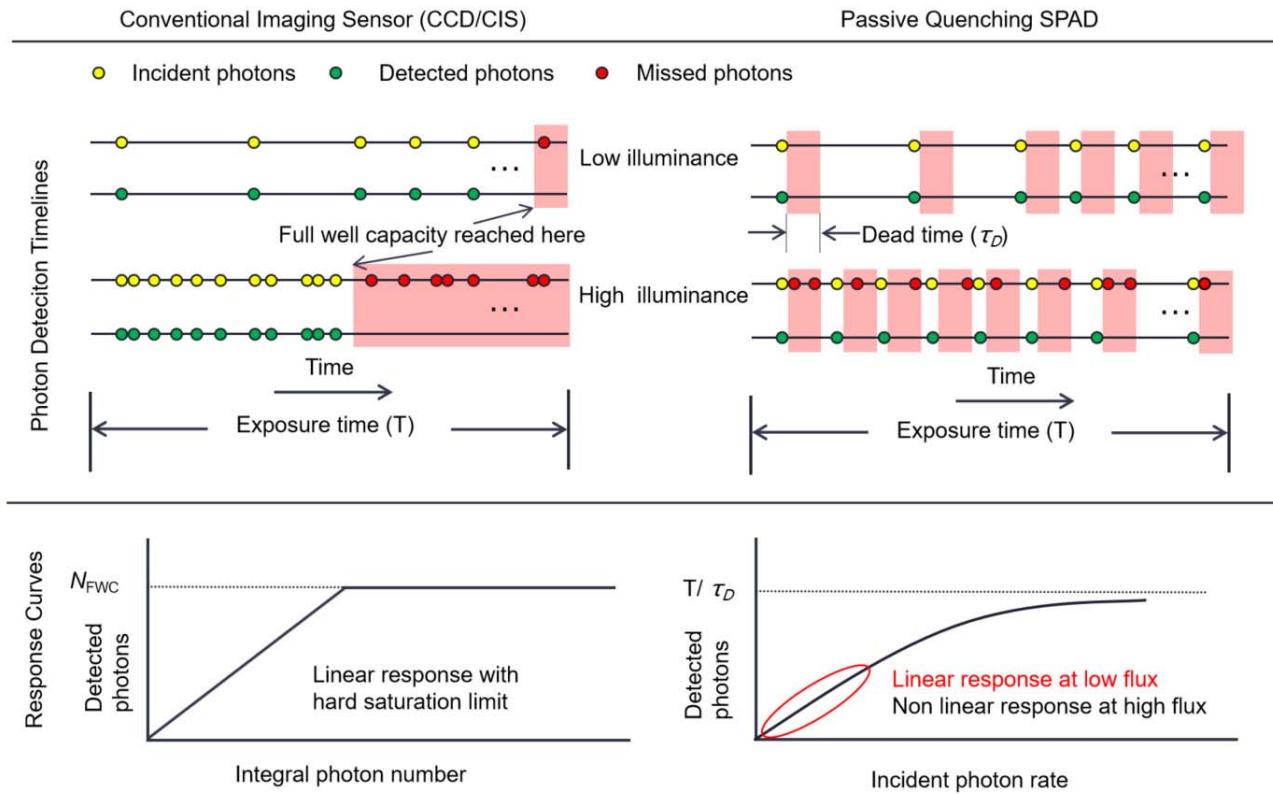


Fig. 10. Light response of SPAD device compared with CCD/CIS light response.

TABLE I
COMPARISON BETWEEN TDI-CCD, TDI-CIS, AND TDI-SPAD

	TDI-CCD	TDI-CIS (Digital)	TDI-SPAD
Mode of transfer	Analog transfer mode	Digital transfer mode	Digital transfer mode
Process	Special	Standard CMOS	Standard CMOS
Design complexity	Low	High	Low
Cost	Costly	Inexpensive	Inexpensive
Stage number bottleneck	MTF reduction with stage increasing	Line-rate reducing with stage increasing	Chip size
Main noise	Transfer noise	Read-out noise	Dark Noise
Transfer efficiency	$\leq 99.99\%$	100%	100%
Line rate	High/100 kHz level	Low & Decreases with increase of stages	Very High/ 1 MHz level

A. Realization of 128×128 TDI-SPAD Imaging

As shown in Fig. 11, we first verify the feasibility of TDI-SPAD function based upon a 128×128 SPAD array chip. The design diagram of the SPAD chip is illustrated in Fig. 12 and the specific parameters of the chip are listed in Table. II. As shown, each column of SPAD sensor shares one 15 bit counter, and the counter is multiplexed through addressing circuits. This kind of chip architecture is similar to [12], which can not realize the function of data transfer between pixels, but all original data of each stage can be read out, and the TDI-imaging function can be verified by off-chip data accumulation.

Specifically, as illustrated in Fig. 13, we build a camera system based upon the 128×128 SPAD sensor and simulate the scanning through moving the scene. As shown in Fig. 13, through calibration of the imaging scene, we could get the distance between the lateral positions that corresponding to different columns of pixels. After each frame of image acqui-

sition is completed, we move the scene with the corresponding distance by a high-precision translation platform to simulate the TDI-imaging with the moving scene. Note that we implemented this experiment to initially demonstrate the principle of TDI-imaging with our TDI-SPAD camera and we haven't yet introduced the automatic synchronization, we will leave this engineering work as one of our future work. The SPAD camera requires 2.5 ms to take one image and 130 frames of images of the scene are taken in total. We then stack the 130 images with each image shifted in the direction of scanning and obtain an image of 128×258 . Demonstration of working mode of TDI-SPAD simulated by off chip accumulation is shown as Fig.14.

A part of the region with similar illumination scene is selected for analysis. As shown in Fig. 15, the picture selected in the red box is the part for data analysis. The photon counting values in the flat field area are plotted in order, shown as Fig. 15. The experimental results are

TABLE II
PERFORMANCE SUMMARY OF 128×128 SPAD ARRAY CHIP

Technology	$0.18 \mu\text{m}$ 1P6M CMOS
Chip size	$2.2 \text{ mm} \times 2.8 \text{ mm}$
Array size	$128 (\text{H}) \times 128 (\text{V})$
Pixel size	$15 \mu\text{m}$
Counter width	15 bit
Dark counts rate	200 cps
Dead time	20 ns (Active quench mode)
PDE	15.7% @490 nm
Power supply	1.8 V (Digital) / 3.3 V (Analog) /12 V (SPAD cathode voltage)

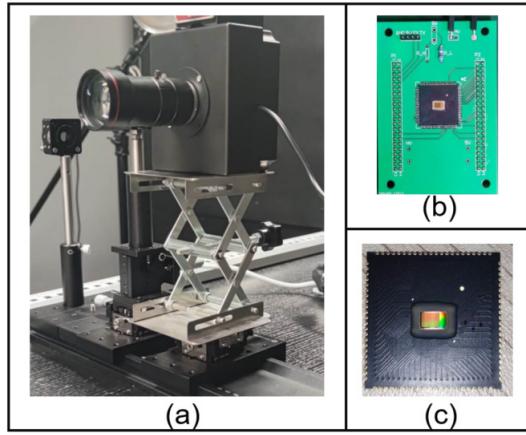


Fig. 11. (a) 128×128 SPAD camera (b) SPAD chip on PCB (c) SPAD chip overview.

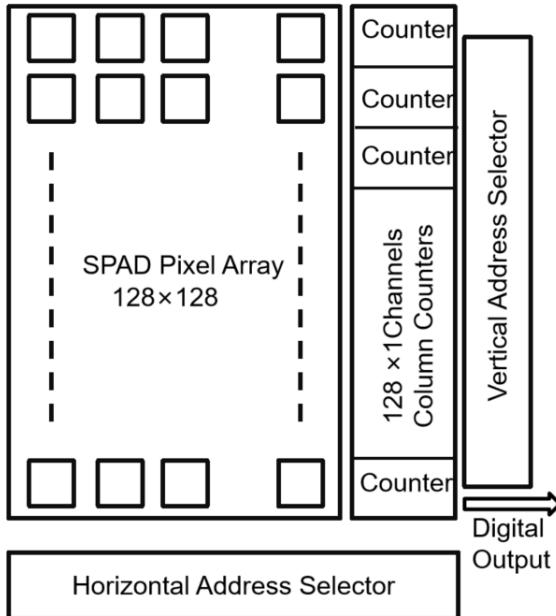


Fig. 12. Block diagram of 128×128 SPAD chip.

consistent with the expected results, and the grey level of this area increases linearly with the increase of TDI stages.

Then, we calculate the SNR in this region to analyze the enhancement of SNR in TDI-SPAD mode. The SNR can be

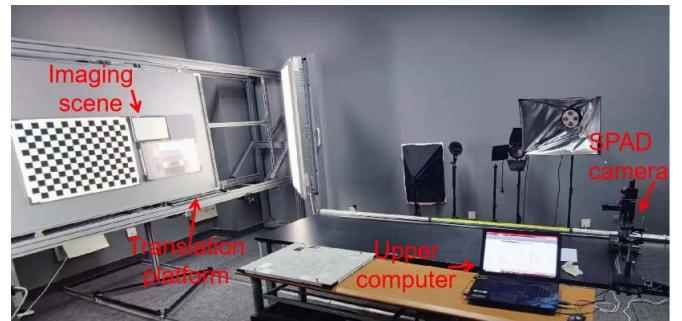


Fig. 13. Demonstration of imaging scene.

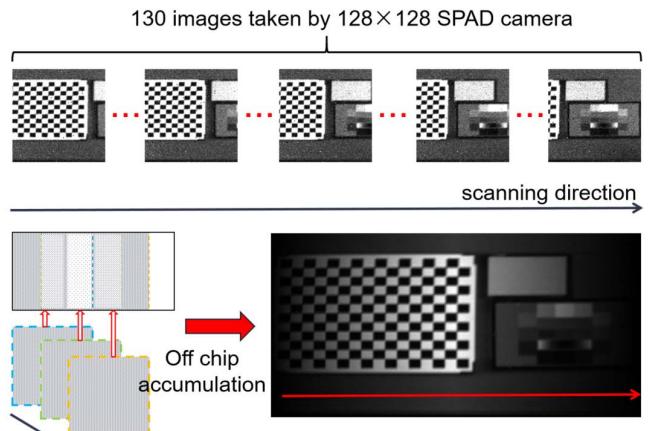


Fig. 14. Demonstration of working mode of TDI-SPAD simulated by off chip accumulation.

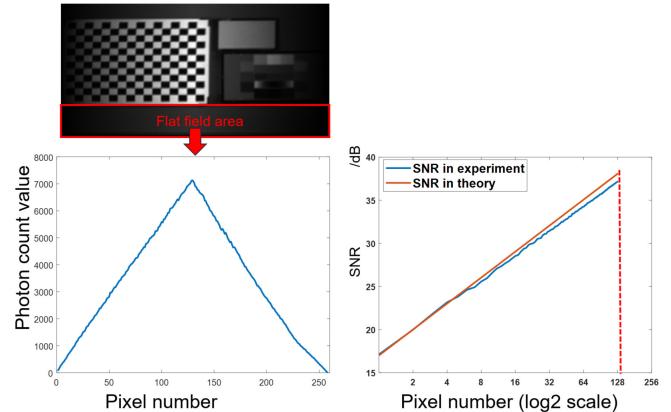


Fig. 15. Photon counting number and SNR enhancement in flat-field region.

calculated with the flat field area data, by

$$\text{SNR}(n) = 20 \cdot \log \frac{Q_{\text{photon}}(n)}{\sqrt{Q_{\text{photon}}(n) + \sigma_{\text{noise}}^2(n)}}, \quad (8)$$

where n denotes the pixel number, $Q_{\text{photon}}(n)$ denotes average photon count value of the n th column pixel, and $\sigma_{\text{noise}}^2(n)$ is the average dark count value of n th column pixel. Note that without loss of generality, we assume that the dark count of

TABLE III
PERFORMANCE SUMMARY OF 2×256 SPAD ARRAY

Technology	0.18 μm 1P6M CMOS
Chip size	4.4 mm \times 1.8 mm
Array size	256 (H) \times 2 (V)
Pixel size	15 μm
Counter width	15 bit
Dark counts rate	200 cps
Dead time	20 ns (Active quench mode)
SNR improvement	3.17 dB (Average)
PDE	15.7% @490 nm
Power supply	1.8V (Digital) / 3.3 V (Analog) / 12V (SPAD cathode voltage)
Power consumption	5 mW @12 V SPAD cathode voltage

the sensor is the same with the same exposure time (2.5ms in our experiments). We first capture an image with no light to get the dark count noise level. Then we capture a scene image with the same exposure time and the captured photon count could be represented as,

$$Q_{\text{out}}(n) = Q_{\text{photon}}(n) + \sigma_{\text{noise}}^2(n). \quad (9)$$

So the SNR can be calculated with:

$$\text{SNR}(n) = 20 \cdot \log \frac{Q_{\text{out}}(n) - \sigma_{\text{noise}}^2(n)}{\sqrt{Q_{\text{out}}(n)}}. \quad (10)$$

With Eq. 9 and Eq. 10, the SNR-stage number of the first 128 column are calculated, and the theoretical SNR-stage number curve is obtained according to the SNR value of the first column and the expected SNR improvement, as shown in Fig. 15. In theory, each time the TDI stage is doubled, the SNR enhancement is supposed to be improved by $\sqrt{2}$ (3dB in logarithm). For example, for stage number N at 4 and 8, SNR is increased by 6dB and 9dB respectively. In the above figure, the blue curve is calculated from the experimental data, and the red curve is the theoretical SNR. The SNR of both curves starts at 17dB, and after 128 time delay integrals, the SNR is theoretically increased by about 21 dB, i.e. the SNR is 38 dB at 128 th stage. The experimental SNR improvement is similar to the theoretical one, i.e. the SNR is 37.1 dB at stage 128 th stage. This results show that the improvement of SNR of TDI-SPAD device is consistent with expectation, and verifying the working mechanism of TDI-SPAD.

B. 256×2 TDI-SPAD Chip With Transfer Circuits

With the TDI function verified upon the 128×128 SPAD, we then design a 256×2 TDI-SPAD chip with transfer circuits to realize TDI-SPAD imaging. The performance summary of the TDI-SPAD chip is shown in Table. III. Specifically, we adopt the $0.18 \mu\text{m}$ 1P6M CMOS technology, the SPAD pixel size is $15 \mu\text{m}$. The array size is 256×2 and the bit-depth of the counter is 15 bit for each stage. Note that here we simply use the same bit width for the two stage, while in the design of more stage TDI-SPAD, the change of counters bit width should be considered for efficiency. Generally, the dark-count noise is in the range of several hundreds counts per second. The calibrated dark count of the proposed TDI-SPAD is 200 cps at room temperature, i.e. 300K. With integration time around several milliseconds, the dark-count will be less than 10, and the imaging count can be 100 thousands at most. So the

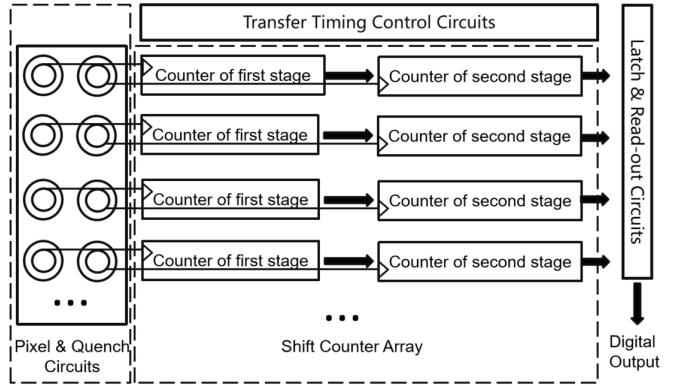


Fig. 16. The layout of the proposed TDI-SPAD chip.

influence of dark noise is relatively small. The dead-time of the sensor is about 20 ns. With two stages of TDI imaging, the experimental SNR improvement is 3.17 dB compared with the same SPAD array with no TDI imaging mode, the details is provided in the following discussion.

The structure of the chip is shown in Fig. 16, which is composed of two stages of SPAD pixel array, counter circuits with transfer function, and the read out circuits.

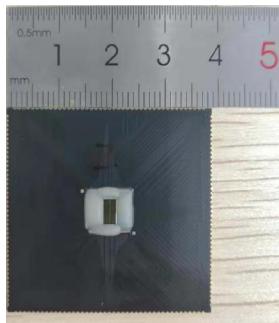
The packaged TDI-SPAD chip is shown in Fig. 17(a). We build a camera system with the chip and a lens of 12 mm focal length. The TDI-SPAD camera is placed on a high-precision rotating platform, and scanning is realized through rotating. Besides, we adopt an FPGA system to collect the data output from the chip and upload it to the upper computer through USB2.0, the experimental setup and peripheral circuits are shown in Fig. 17(b). The internal structure of the chip and the pixel layout is shown in Fig. 17(c). Two columns of pixels are placed side by side, and the transfer circuit is placed on the other side.

C. Flat-Field Correction Applied in TDI-SPAD

Through scanning of the TDI-SPAD camera, we obtained a picture of the scene as shown in the Fig. 18(a). As shown, there are horizontal strips due to pixel inconsistency. Generally, for a single pixel, the captured pixel value is linearly related to the intensity of the incident light. However, due to inconsistency among pixels, i.e. the fixed pattern noise, the response of different pixels on the sensor to the incident light is different, i.e. the starting points and the slope of pixel response function are different. To reduce the fixed pattern noise, we apply flat-field correction method to calibrate the slope (i.e., signal gain) and offset (i.e., signal offset) of the light response of each pixel.

The most commonly used flat-field correction method is the two-point correction method [28], [29]. First, dark field images with no incident light are captured to obtain the offset of each pixel. Then, bright field image of a uniform grey-level object under uniform lighting conditions are captured to calibrate the slope of different pixel. The flat-field correction is implemented for each pixel and the specific calculation formula is

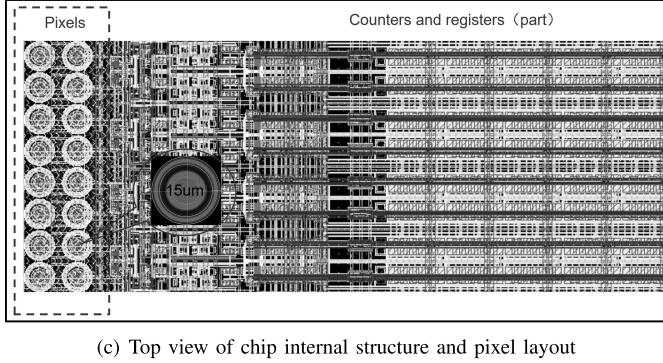
$$N_{\text{ffc}} = \frac{N_{\text{out}} - N_{\text{dark}}}{N_{\text{flat}} - N_{\text{dark}}} \cdot k \quad (11)$$



(a) Top view of packaged chip



(b) TDI-SPAD imaging system



(c) Top view of chip internal structure and pixel layout

Fig. 17. The chip and the imaging system of TDI-SPAD.

where N_{ffc} denotes the value after flat-field correction, N_{out} denotes the original data of scene imaged by SPAD, N_{dark} denotes the dark field image, N_{flat} denotes the bright field image, and k is the normalization constant.

For TDI-SPAD imaging devices, the fixed pattern noise mainly appears as a striped pattern, as shown in Fig. 18(a). After flat field correction, the effect of fixed pattern noise can be completely eliminated. The method of flat-field correction is proved effective in single-stage linear array, and here we give a simple derivation to prove the effectiveness of the flat-field correction upon multi-stage TDI-SPAD. The multi-stage light response of TDI-SPAD device $N(P)$ is the accumulation result of the array count value of each stage $F_i(P)$ when the light intensity is P ,

$$N(P) = \sum_{i=1}^N F_i(P), \quad (12)$$

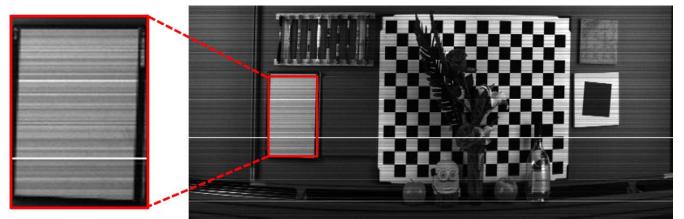
Since the light response curve of SPAD devices under low light conditions is approximately linear, which is can be written as,

$$F_i(P) = A_i \cdot P + B_i, \quad (13)$$

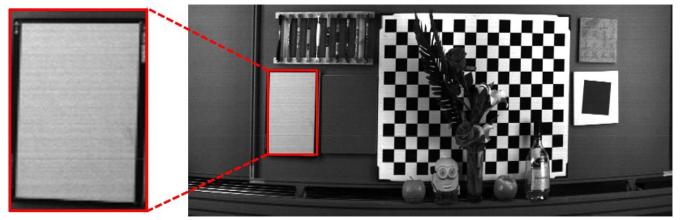
The response curve obtained by adding these linear curves is still linear, so the two-point method can be also used for the flat-field correction for multistage TDI.

$$N(P) = \sum_{i=1}^N A_i \cdot P + B_i = A_{\text{sum}} \cdot P + B_{\text{sum}}, \quad (14)$$

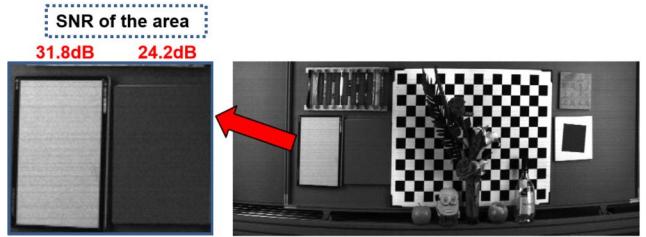
Fig. 18(b) shows the flat field corrected imaging results of the two-stage TDI-SPAD image. From the enlarged image, it can see that the flat field correction almost eliminates the stripes caused by pixel inconsistency, and the FPN noise can also be ignored.



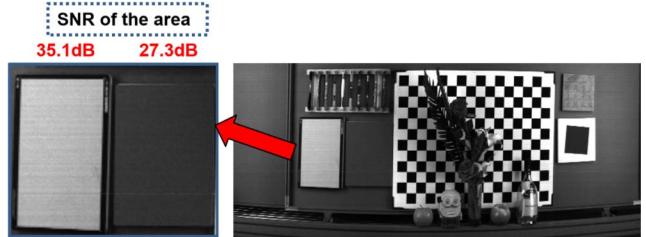
(a) Image before flat-field correction



(b) Image after flat-field correction

Fig. 18. Flat field correction of the single stage TDI-imaging.

(a) Imaging results of single stage SPAD linear array



(b) Imaging results of two stages TDI transfer mode SPAD linear array

Fig. 19. SNR improvement of two-stage TDI.

Flat field correction is very important in the application of imaging sensor. We have verified its feasibility through theory and experiment, which clears the obstacles for the application of TDI-SPAD in the case of more stages.

D. Experiment of TDI-SPAD on SNR Improvement

In order to verify the performance of the transfer circuit and the improvement SNR in TDI imaging mode, the same scene is imaged twice. First, TDI transfer mode is not used for imaging, and the integration time is 10 ms. For the second time, TDI transferring mode is used, and the equivalent integration time is 20 ms. The SNR can be calculated with the uniform grey value part of the images. When the stages N is 2, the SNR enhancement is supposed to be $\sqrt{2}$ (3 dB in logarithm).

It can be observed from Fig. 19 that the image of two stages TDI-SPAD has less noise and better image uniformity. In order to more intuitively represent the improvement of SNR in TDI applications through data, two cardboards with

different uniform reflectances were placed in the imaging scene. We calculate the SNR with Eq. 8, and the SNR values have been marked in the figure. The imaging of TDI mode has improved the SNR of the two card boards by 3.22 dB and 3.13 dB, respectively, which is approximately consistent with the theoretically result of 3 dB.

With these experiments, TDI-imaging based upon SPAD is fully demonstrated. From the conception and design of transfer counter to the final function verification, a circuit which can realize TDI function through digital transfer is realized for the first time by us. Our method could provide the circuit foundation for more advanced TDI-SPAD devices in future.

V. CONCLUSION

In conclusion, a novel TDI imaging sensor based upon SPAD are proposed in this paper. The full design of the TDI-SPAD sensor is proposed including the transfer circuit and the sensor architecture. Two TDI-SPAD imaging system are built to demonstrate the functionality of TDI-imaging. The proposed TDI-SPAD architecture is characterized by low noise, high transfer efficiency, which is promising to become the next generation of TDI image sensors.

Moreover, due to the imaging mode of photon counting, all the data obtained are digital, and the data between pixels can carry out real-time correlation operation to achieve data compression, pattern recognition, spatiotemporal filtering and other operations. In paper [30], a digital CMOS image sensor that combines detection, ADC, and signal processing electronics into a single massively parallel architecture has been developed and applied to several interesting applications. Significant size, weight, power, and imaging performance benefits have been realized for TDI, stabilization, a signal processing modes of operation. Based on this idea, we will also carry out the digital correlation operation between SPAD pixels, so as to reduce the amount of data read out, improve the data processing ability, and increase the further SNR improvement in our future work.

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