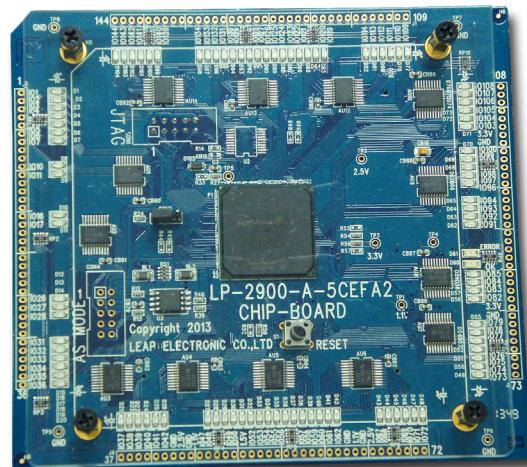

LP-2900 CPLD Digital Logic Circuit Design Experiment Board With Altera Cyclone VE Board



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LEAP ELECTRONIC CO., LTD.
overseas1@leap.com.tw

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II.	Update and install Quartus II	6
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IV.	Create a programming file	24
V.	Pin arrangement of LP-2900	26

I. Introduction to LP-2900

LP-2900 is a lab platform that created by Leap Electronic, which provides changeable FPGA chips in different brand and model. The menu focuses on how LP-2900 goes with Altera Cyclone VE chip. The 5CEFA2F23C8 FPGA offers 25000 available logic gates, and I/O modules with status indicator are designed in the chip board to monitor I/O status.

LP-2900 offers complete experimental environment with complementary testing tools, which uses 10MHz system frequency. The input interface includes logic input, original press point with light, dip switch, impulse press button generator and 3×4 array keyboard. The output interface includes Red-Yellow-Green LED, 6 digits 7-segment display with common cathode, buzzer, electronic dices, LCD display, and 8×8 dot matrix LED display. Moreover, A/D and D/A experimental interface and 8051 single chip are also provided for experimental use. Referring to FPGA program download, the sof file can be downloaded to FPGA using USB ports.

It supports USB interface, which can be connected to PC to design FPGA with ALTERA's Quartus II software. After simulation and compilation, FPGA can be transferred to LP-2900 Cyclone VE chip directly, and be verified with LP-2900

Overview of LP-2900 CPLD Logic Design Experimental Platform

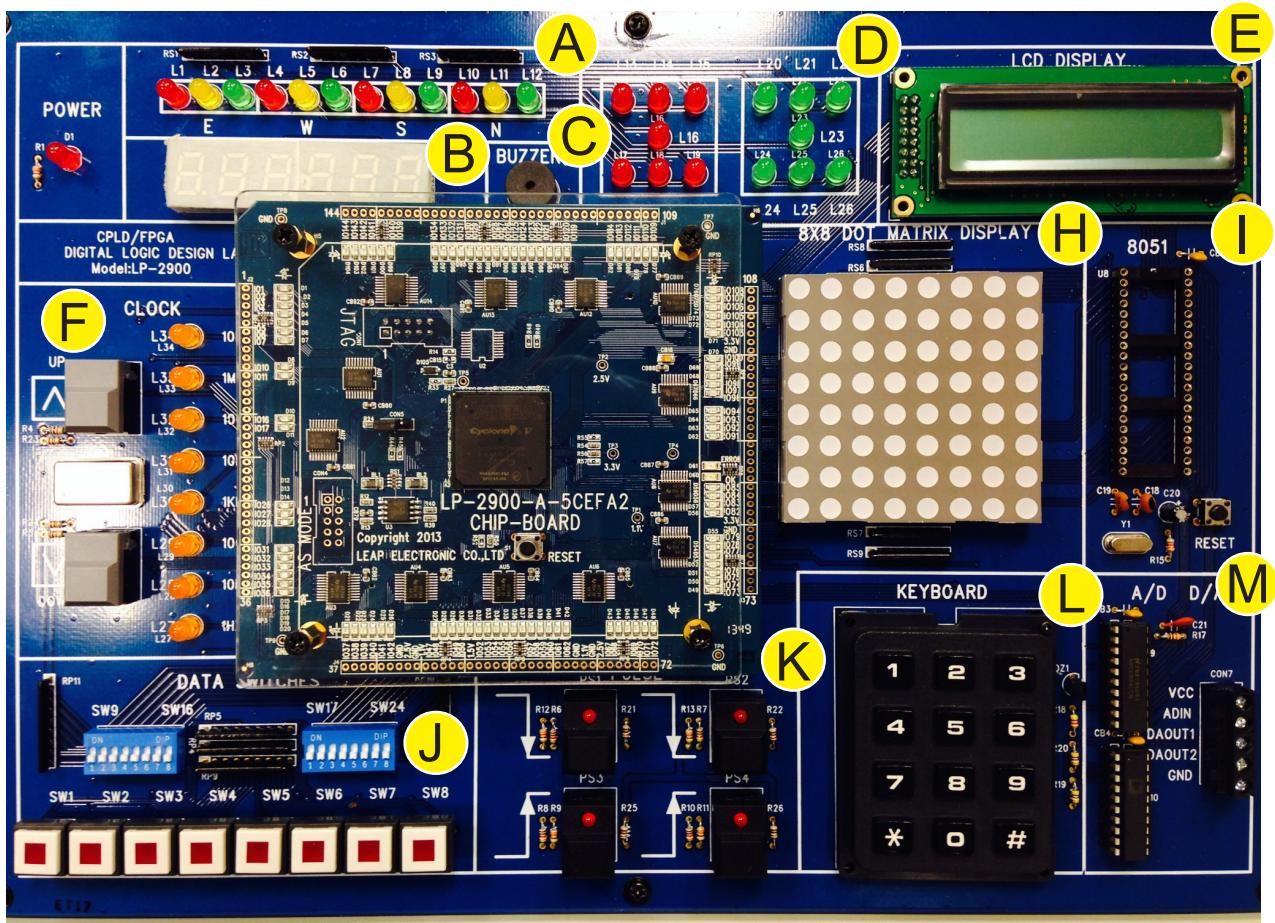


Figure1.1 LP-2900 Logic Design Lab Platform

- A: 4 sets of red, yellow, and green LED
- B: 6 common cathode 7-segment display
- C: one buzzer
- D: two electronic dices
- E: one LCD display
- F: one clock circuit
- G: one 8×8 dot matrix display
- H: 8051 module
- I: A/D & D/A circuit modules
- J: 3 sets of 8-bit data switches
- K: 4 pulse switches
- L: one 4×3 keyboard
- M: A/D & D/A circuit modules

II. Update and install Quartus II

- Go to Altera's official website at www.altera.com
 Point to Support and click on Downloads on the Altera homepage.
 (Note: Download location may vary according to website adjustment.)



- Select Quartus II Web Edition→Download

The screenshot shows the Altera Download Center page. On the left sidebar, there are links for Design Software, Embedded Software, Archives, Licensing, Programming Software, and Drivers. The main content area features a 'Download Center' header and a section titled 'Get the complete suite of Altera design tools'. It highlights 'Quartus II Version 13.1'. Below this, there are three download options:

- Quartus II Subscription Edition**: Paid license required. Includes a 30-day trial. A 'Download' button is shown.
- Quartus II Web Edition**: FREE, no license required. A free version for CPLD or medium-density FPGAs. An IP available for purchase. A 'Download' button is highlighted with a red circle.
- Quartus II Arria 10 Edition Subscription Edition license required**: Includes only Arria 10 devices. Free 30-day trial. A 'Download' button is shown.

On the right side, there is a 'Related Links' sidebar with sections for What's New, Compare Quartus II Web and Subscription Edition, Compare ModelSim-Altera and ModelSim-Altera Starter Edition, and University Software.

● Select Combined Files→Download

Quartus II Web Edition

Home > Support > Downloads > Quartus II Web Edition

Release date: November, 2013

Quartus II Web Edition v13.1

Select a previous version of Quartus II: 13.1

Operating System: Windows Linux

Select the operating system on which you will run the Quartus II software.

Download Method: Akamai DLM3 Download Manager Direct Download

Select whether you will use the download manager (Windows only) or directly download the files. The download manager allows you to pause the download and can help you recover from interrupted downloads.

The Quartus II software version 13.1 supports the following device families: all Cyclone III, Cyclone IV, MAX II, and MAX V devices; select Arria II and Cyclone V devices.

- Use the Software Selector on the Download Center (finds all software versions)
- Refer to the Device Support List (lists last supported software version)

Combined Files Individual Files DVD Files Additional Software Updates

Download and install instructions:

- Download the software .tar file.
- Extract the files into the same temporary directory.
- Run the setup.bat file.

[Read Altera Software v13.1 Installation FAQ](#)

[Quick Start Guide](#)

Quartus II Web Edition Software (Device support included) [Quartus-web-13.1.0.162-windows.tar](#) Size: 4.4 GB MD5: E8511F9028269296EA42A56FE24E1C0

UPDATE

- For first-time users, enter the email address and click on Create Account. After being redirected to Account Registration page, enter user information (* indicates required fields).
- Create an **User Name** and a **Password**, and click on **Create Account**.

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User Name Forget Your User Name or Password?

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- Create your account.

- Download the Quartus II Web Edition, after your account has been created.

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You can use this account to register for classes, download software, file a service request and much more.

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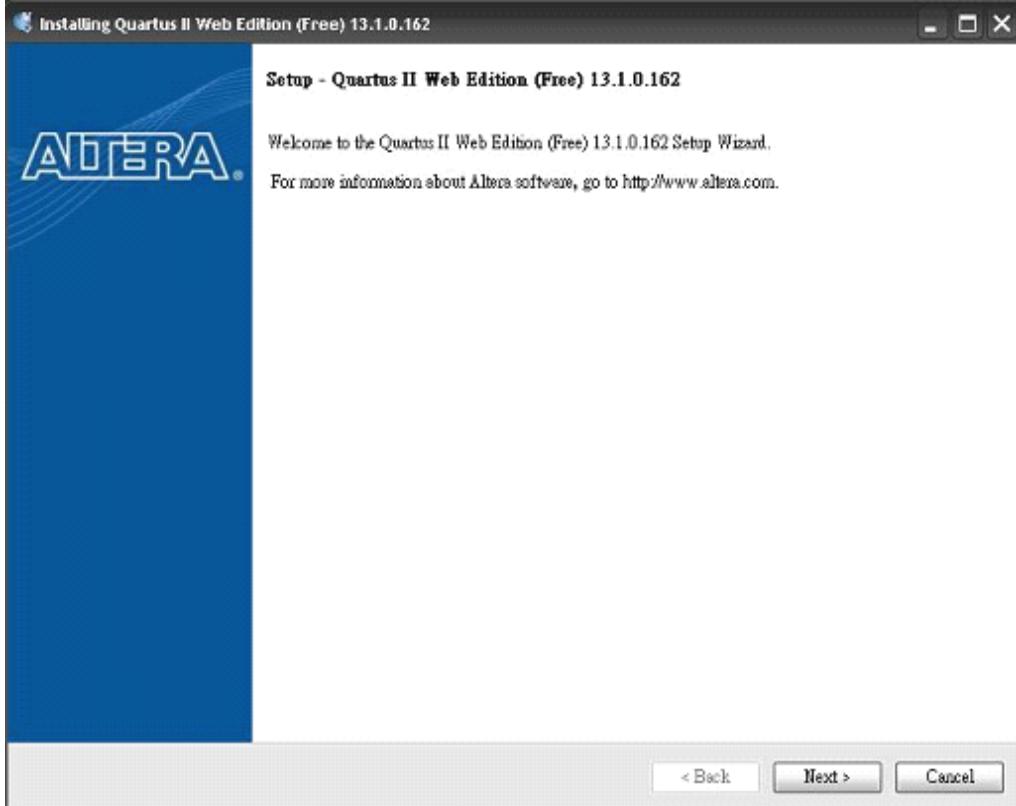
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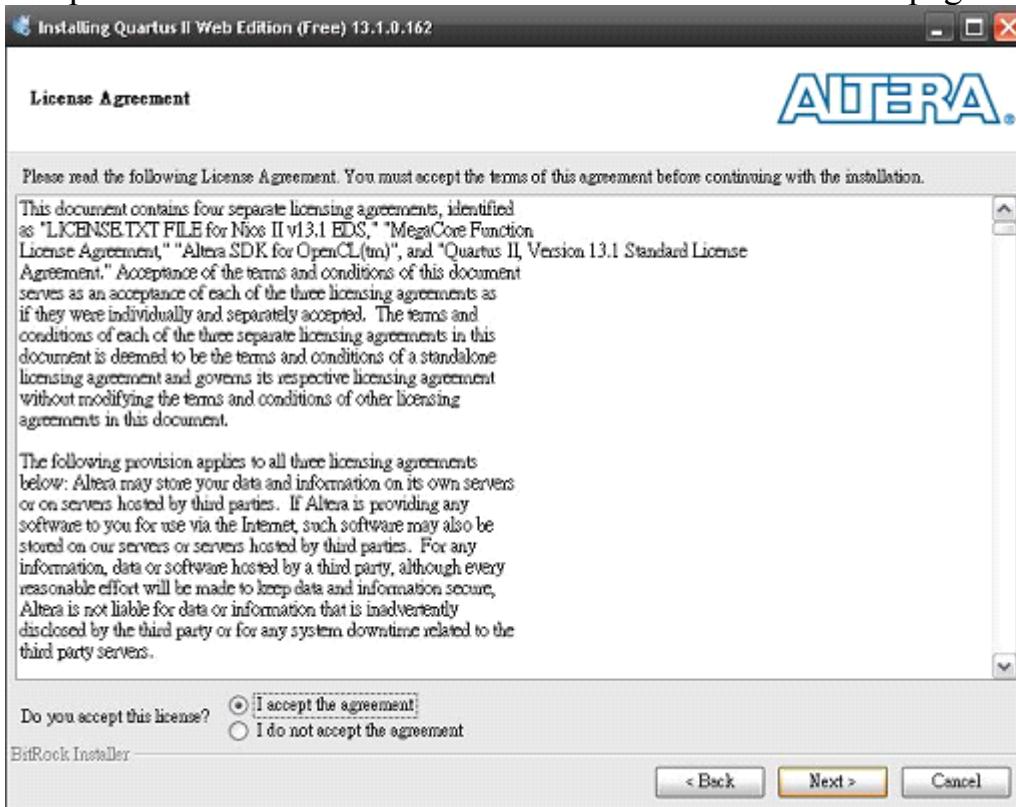
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Install Quartus II software

- Run Setup. bat and set up the Quartus II.



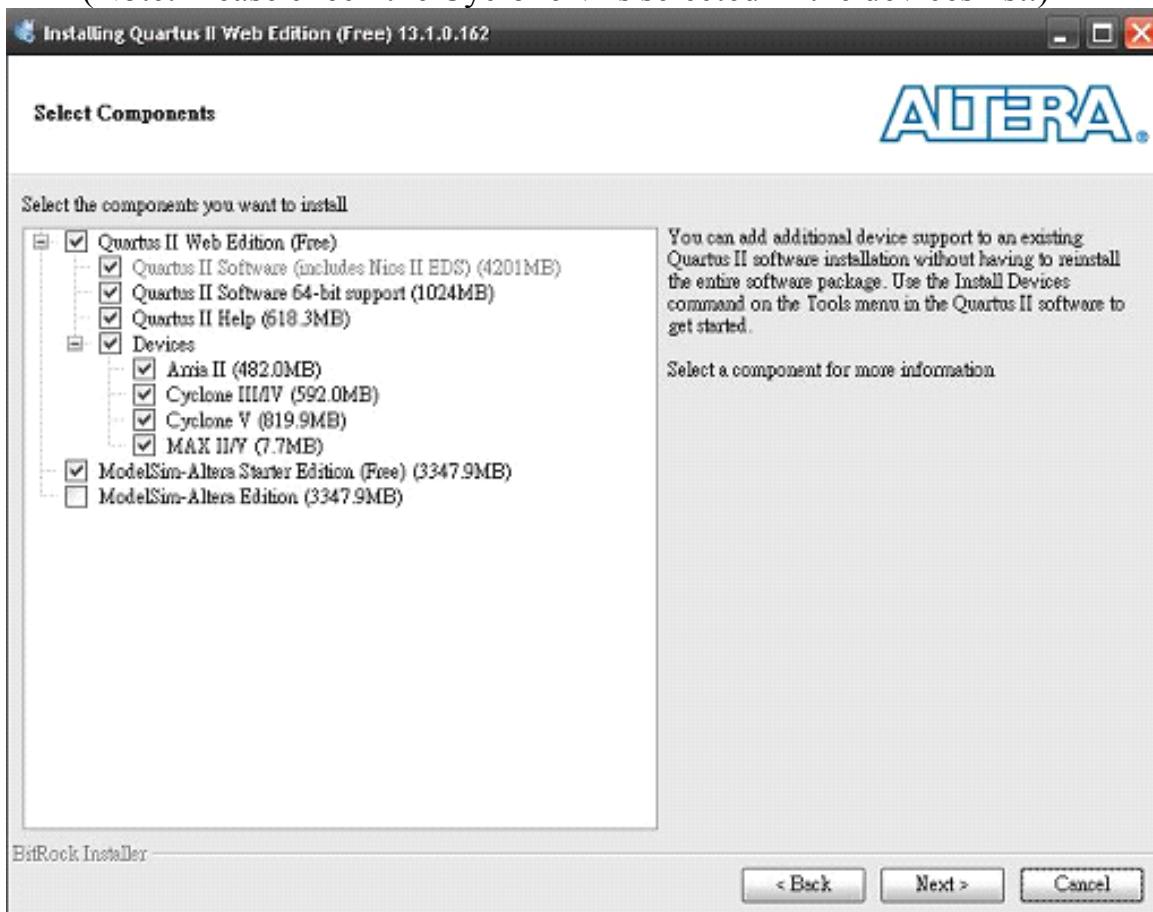
- Please read the following License Agreement. If you agree with the agreement please click "Yes" then select choose "Next" to the next page.



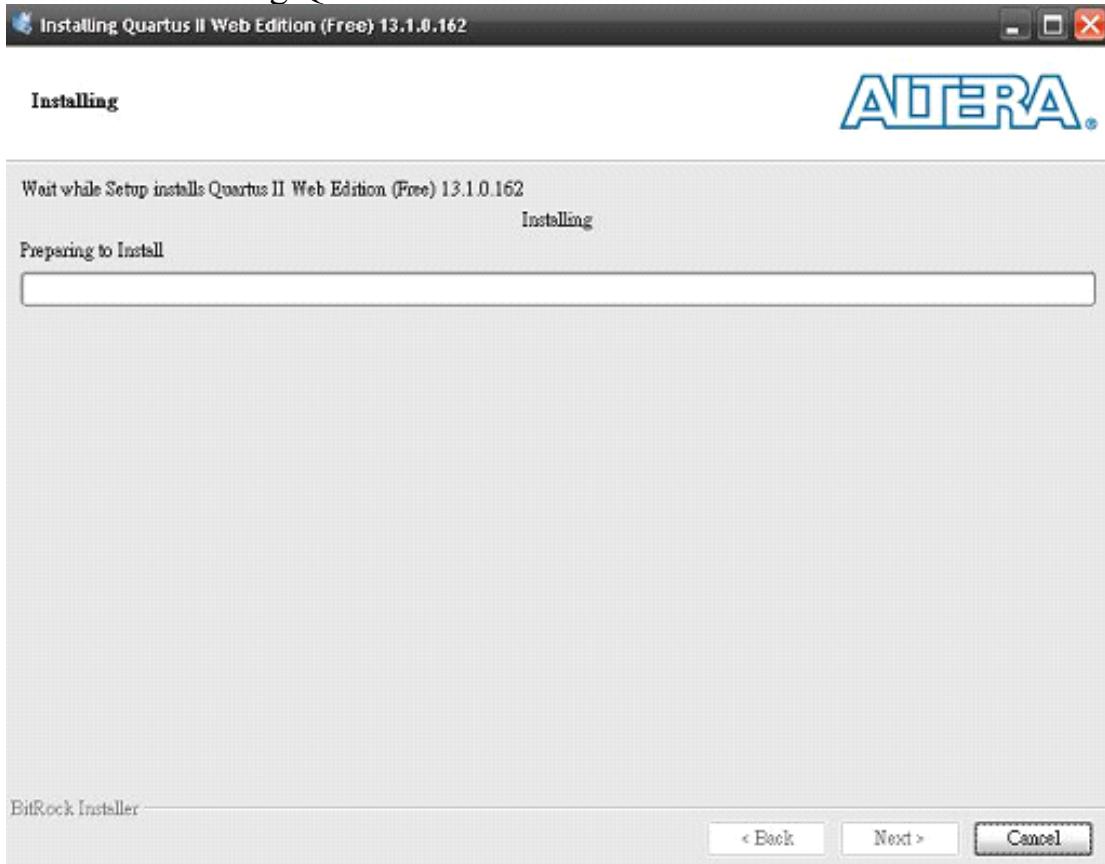
- Please specify the directory where Quartus II will be installed.
(Default C:\altera\13.1)



- Shown in the photo below is to select components, which is a default photo.
(Note: Please check the Cyclone V is selected in the devices list.)



- Start installing Quartus II web edition.



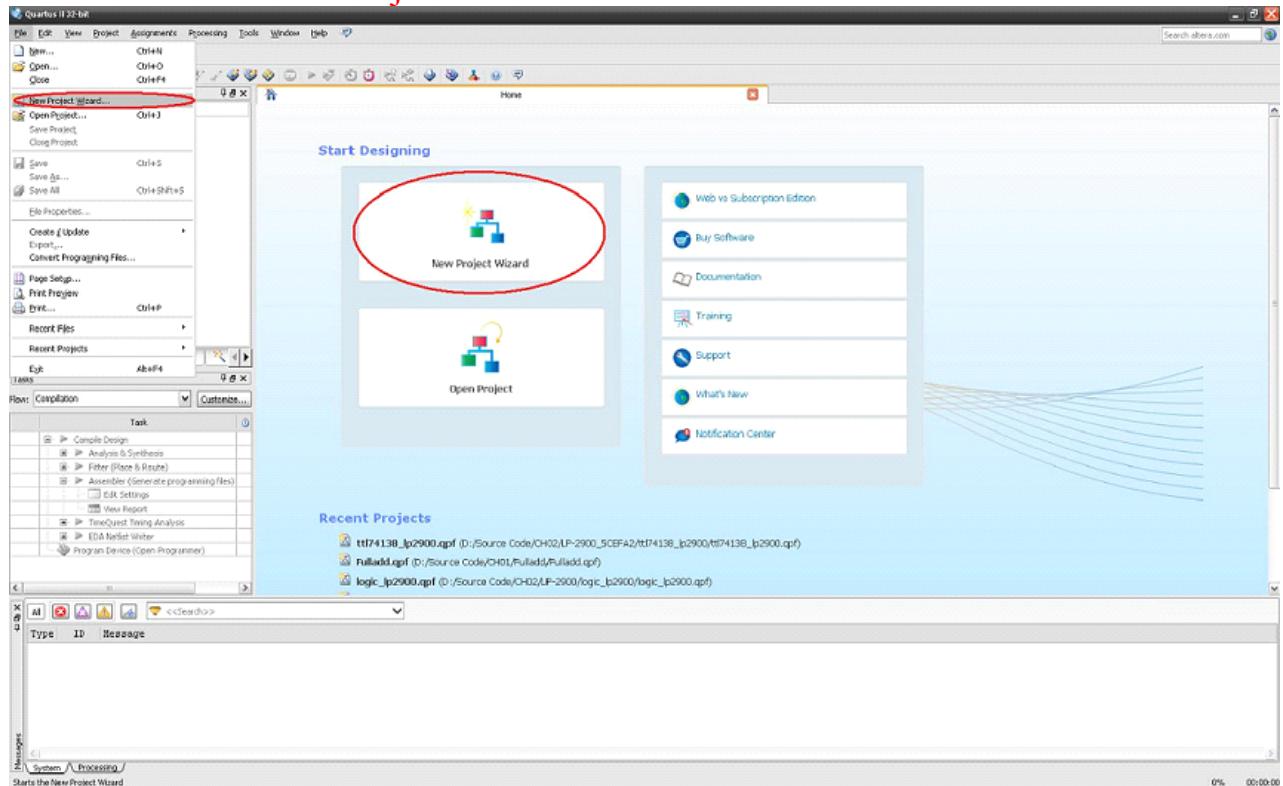
- Complete the installation.

III. Start a new project

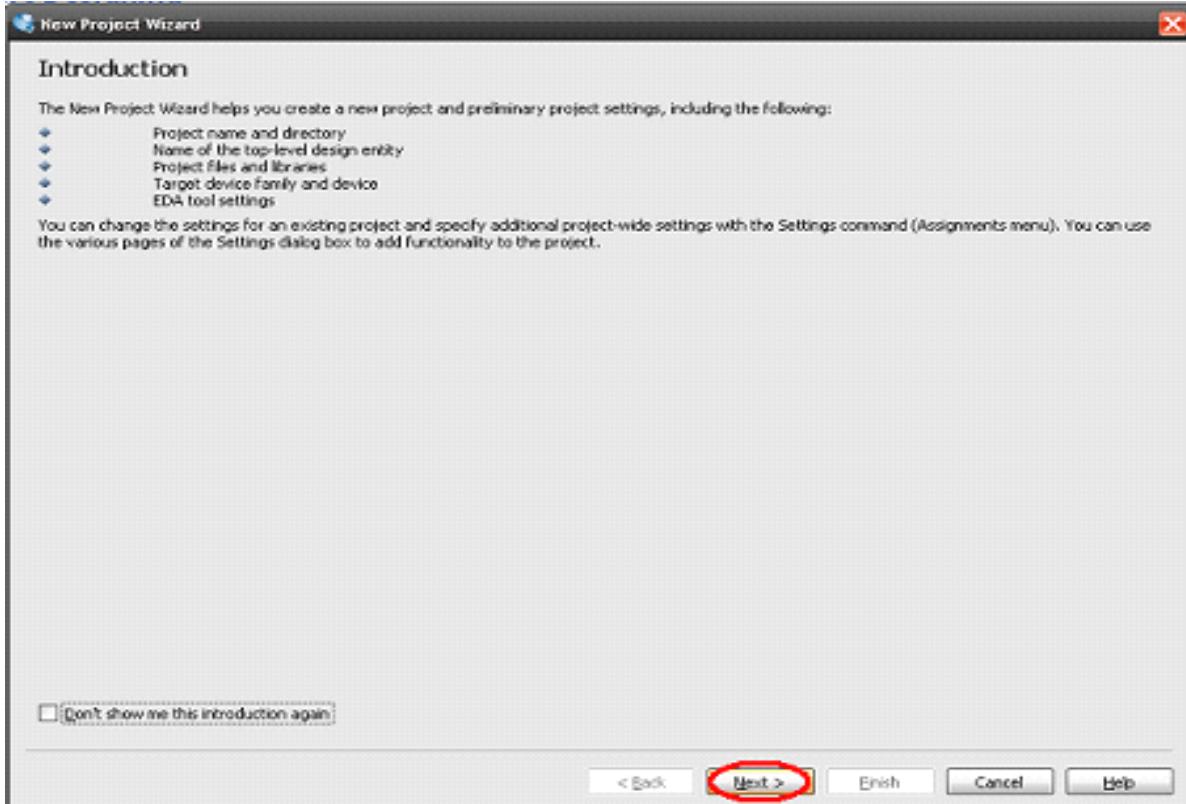
- Select a program → Altera → Quartus II (32 bit or 64 bit)



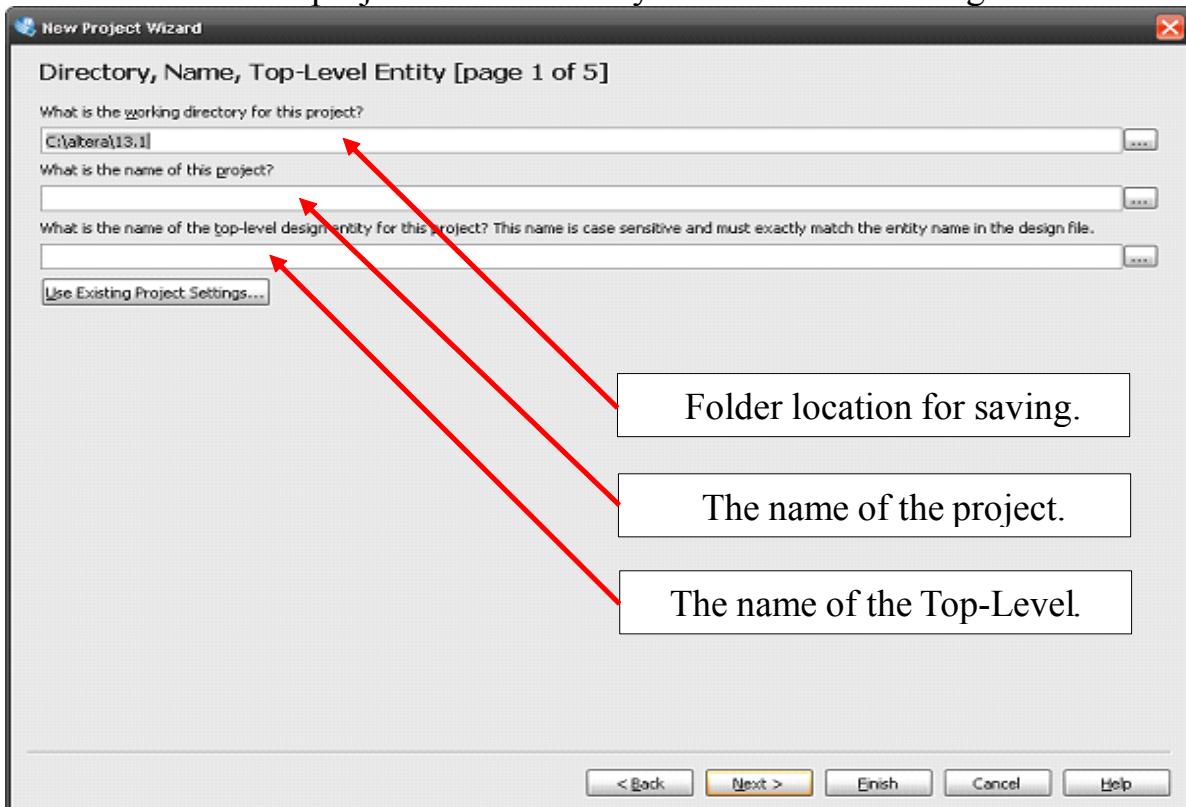
- Select File → New Project Wizard



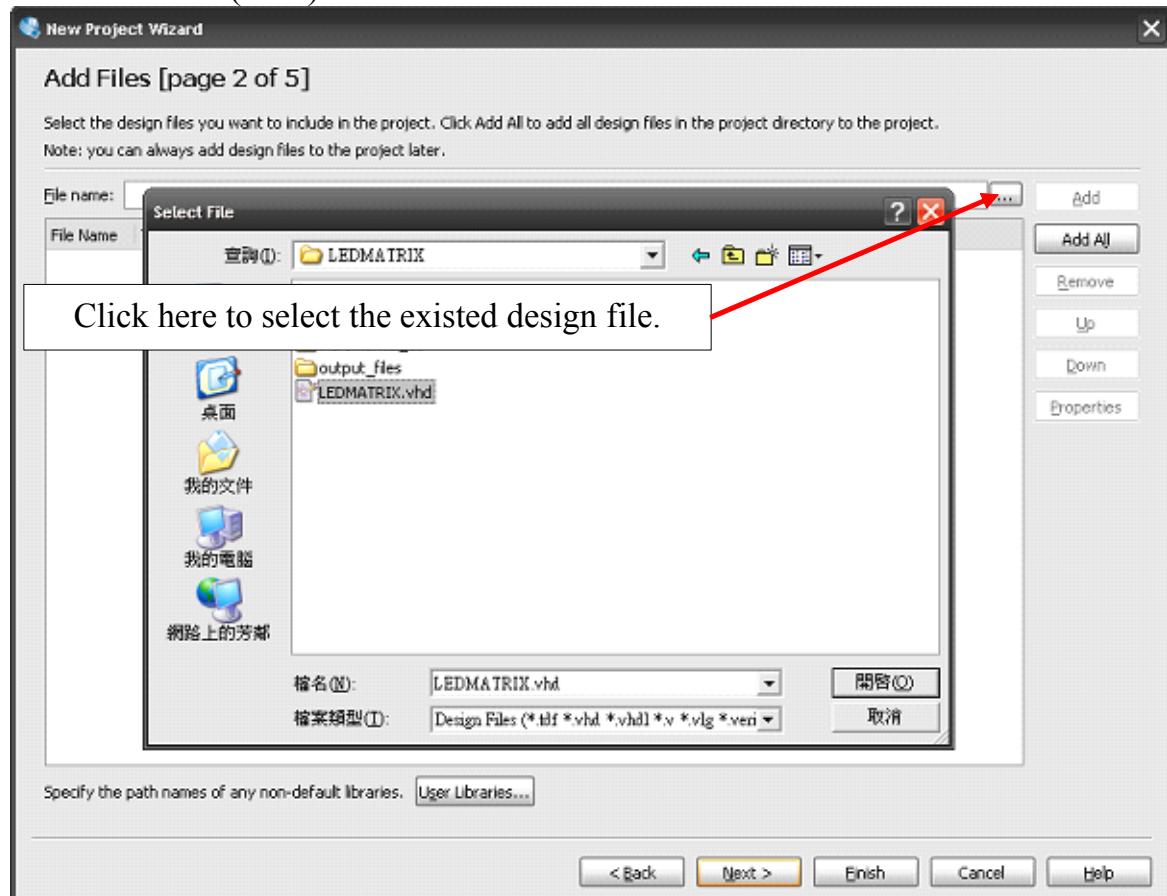
- Click “Next”.



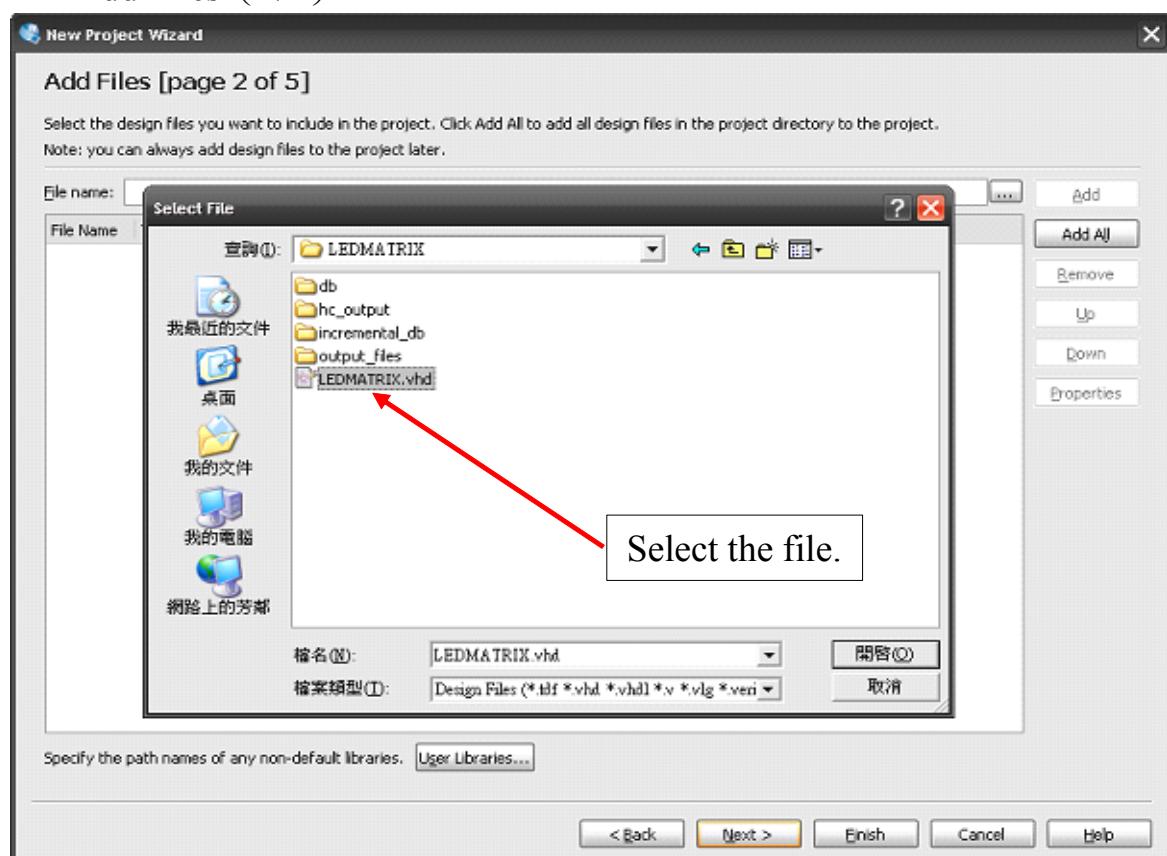
- Create project name, working directory and Top-Level design entity name.
(Note: case sensitive and must exactly match the entity name in the design file and do not save the project under directory that contains non-English characters.)



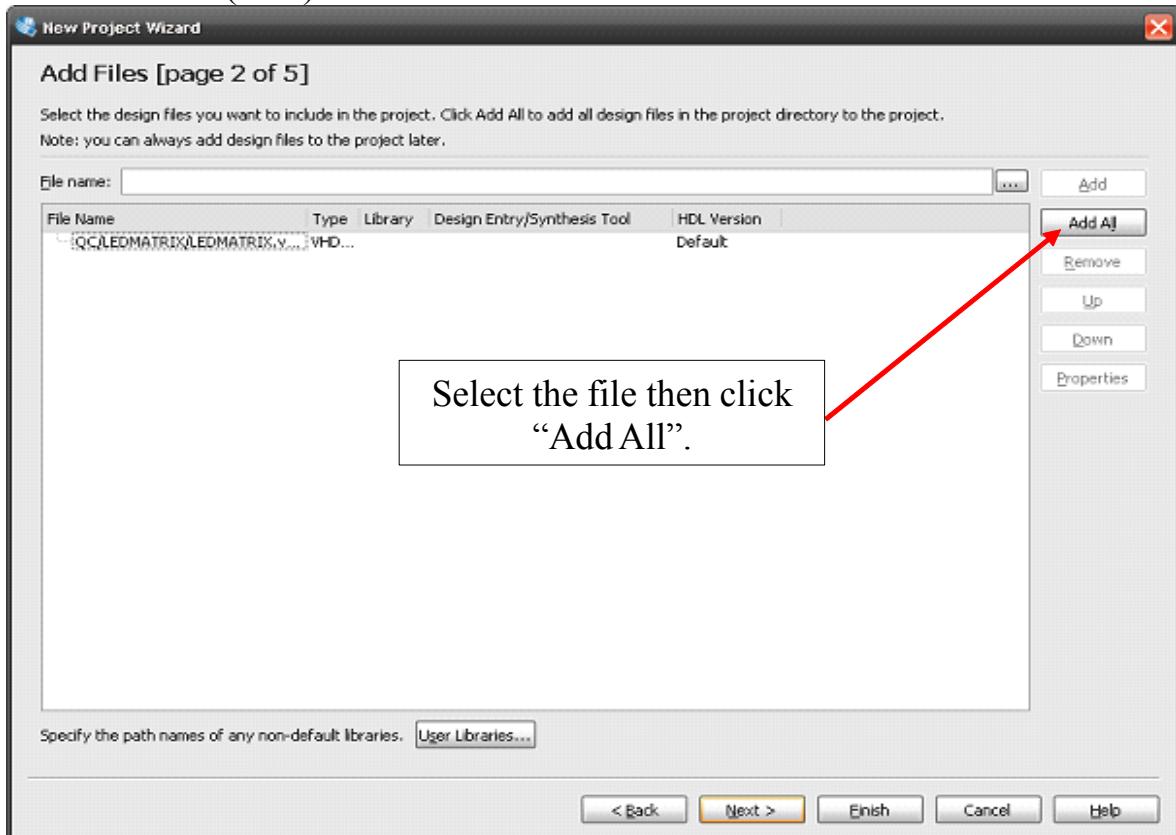
● Add Files (1/4)



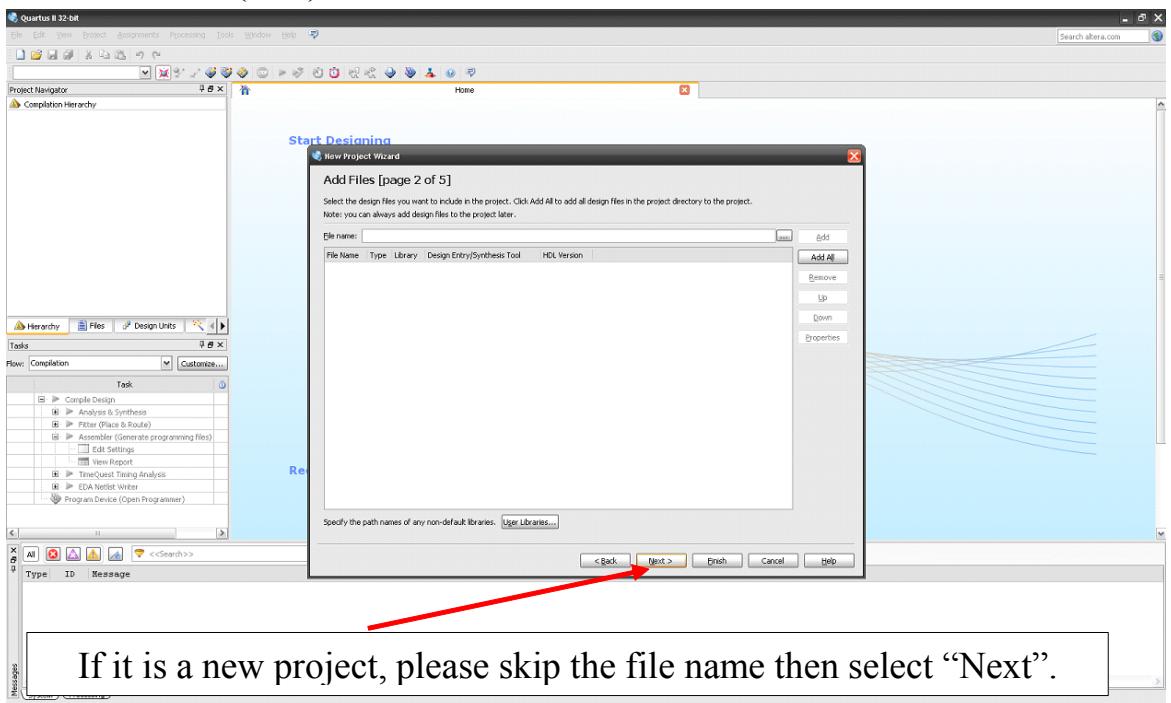
● Add Files (2/4)



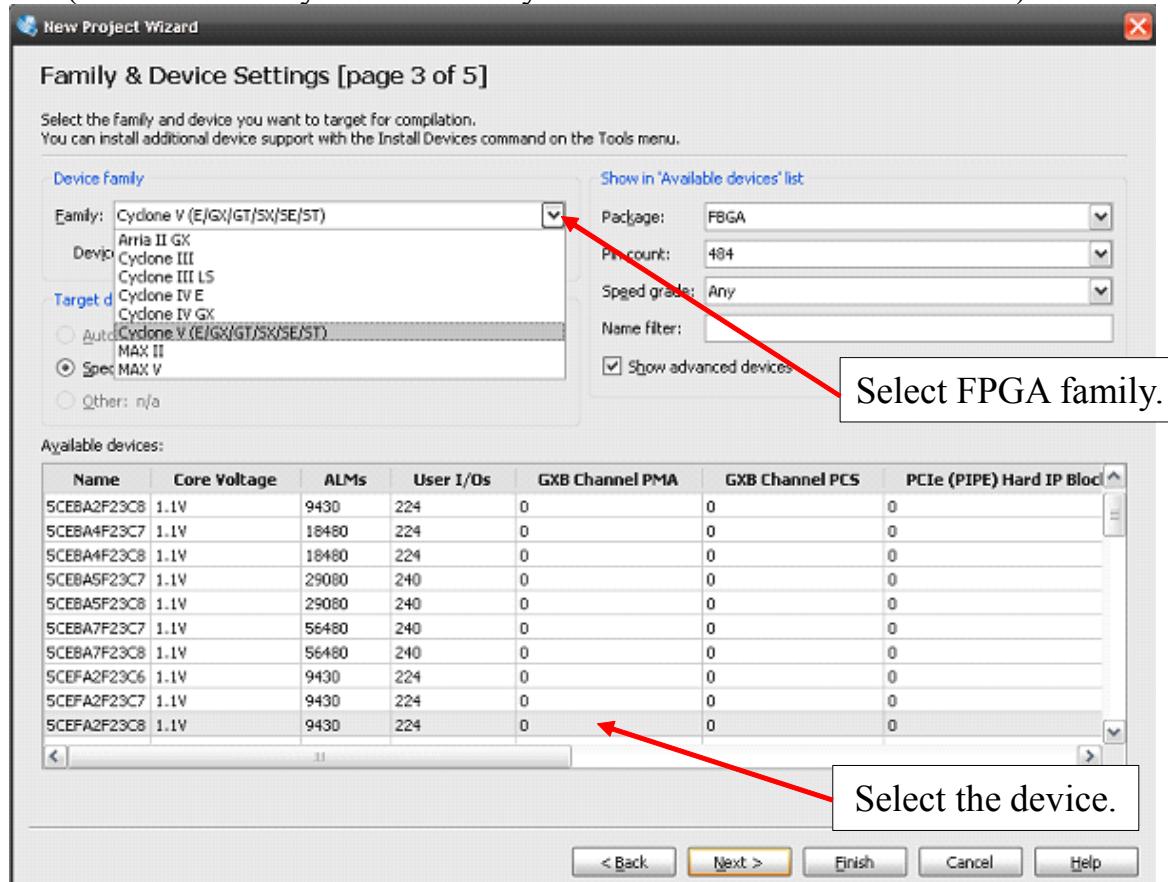
● Add Files (3/4)



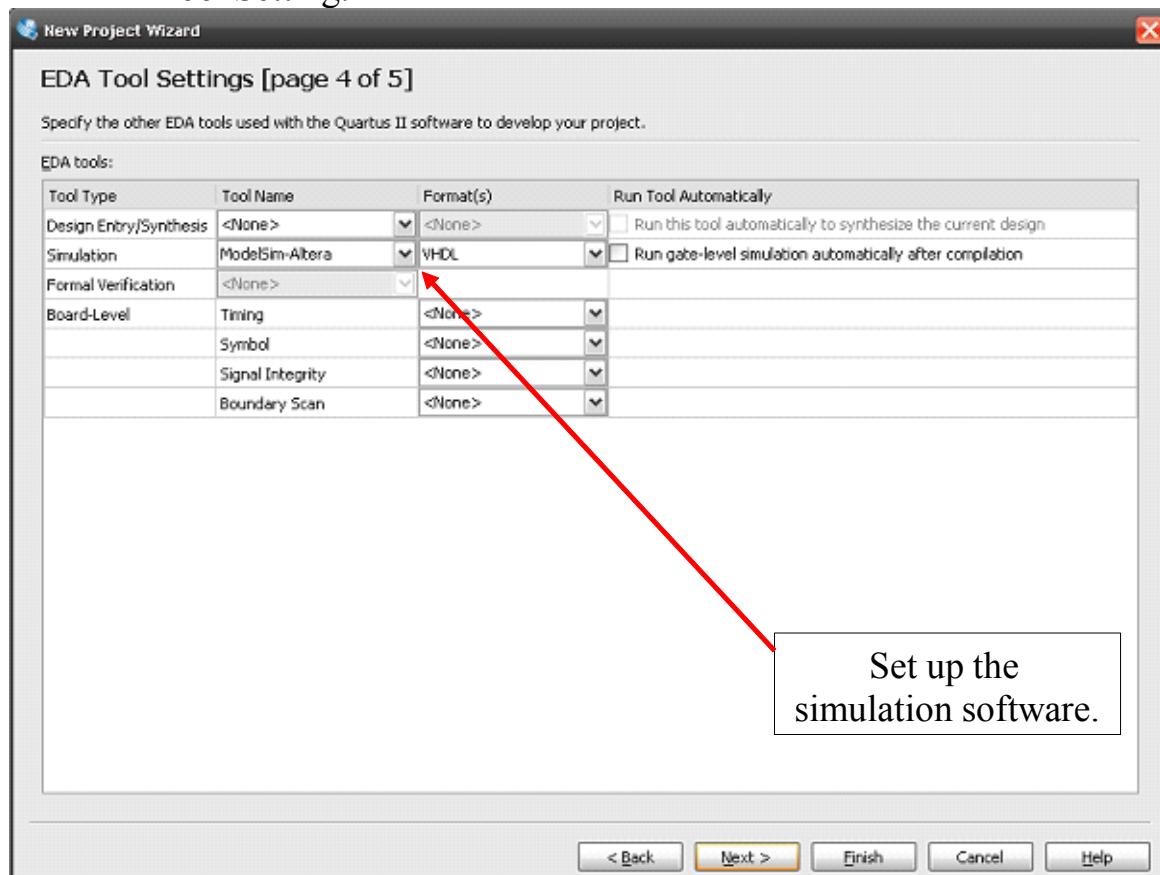
● Add Files (4/4)



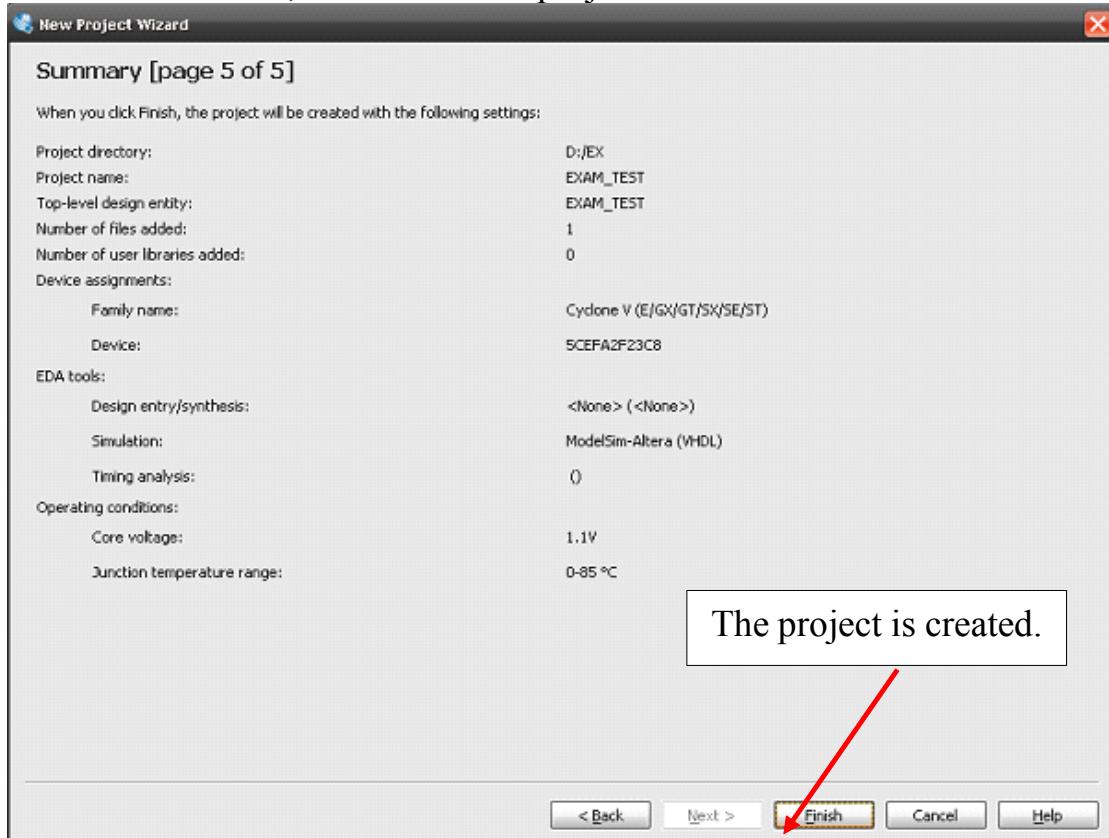
- Now is the time to choose an FPGA device.
(Please select Cyclone V family and the 5CEFA2F23C8 device.)



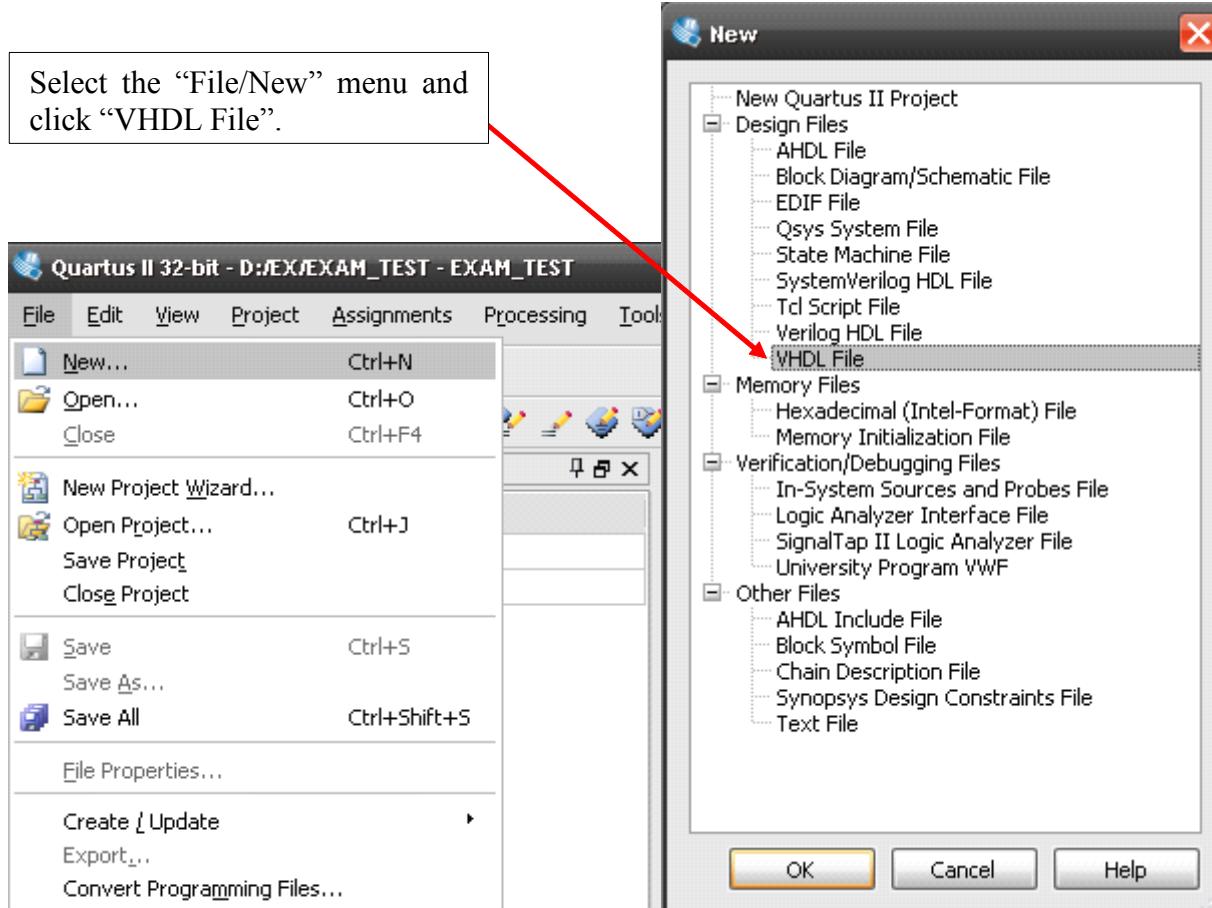
- EDA Tool Setting.



- Click “Finish”, to create a new project.



- Create a new VHDL File.



● Type the following text in editor display.

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity LEDMATRIX is
port ( LED1_14 : out std_logic_vector(13 downto 0);
       CLK      : in std_logic;
       RG_EN   : out STD_LOGIC;
       BAR_EN  : out STD_LOGIC;
       DOT     : out STD_LOGIC;
       DE1_2   : out std_logic_vector(2 downto 0);
       SEV1_7  : out std_logic_vector(6 downto 0);
       sw1_8   : in std_logic_vector(7 downto 0);
       sw1_16  : in std_logic_vector(7 downto 0);
       sw17_24 : in std_logic_vector(7 downto 0);
       sw1_COM : out std_logic_vector(7 downto 0);
       sw9RED : out std_logic_vector(7 downto 0);
       sw17GEN : out std_logic_vector(7 downto 0)
      );
end LEDMATRIX;

architecture a of LEDMATRIX is
signal CNT:std_logic_vector(29 downto 0);
begin
  DE1_2 <= CNT(17 downto 15);
  DOT <= CNT(23);
  RG_EN <= '1';
  BAR_EN <= '1';
  U1: PROCESS(CLK)
    BEGIN
      IF CLK'event AND CLK ='1' THEN
        CNT <= CNT+1;
      END IF;
    END PROCESS U1;
end architecture;

```

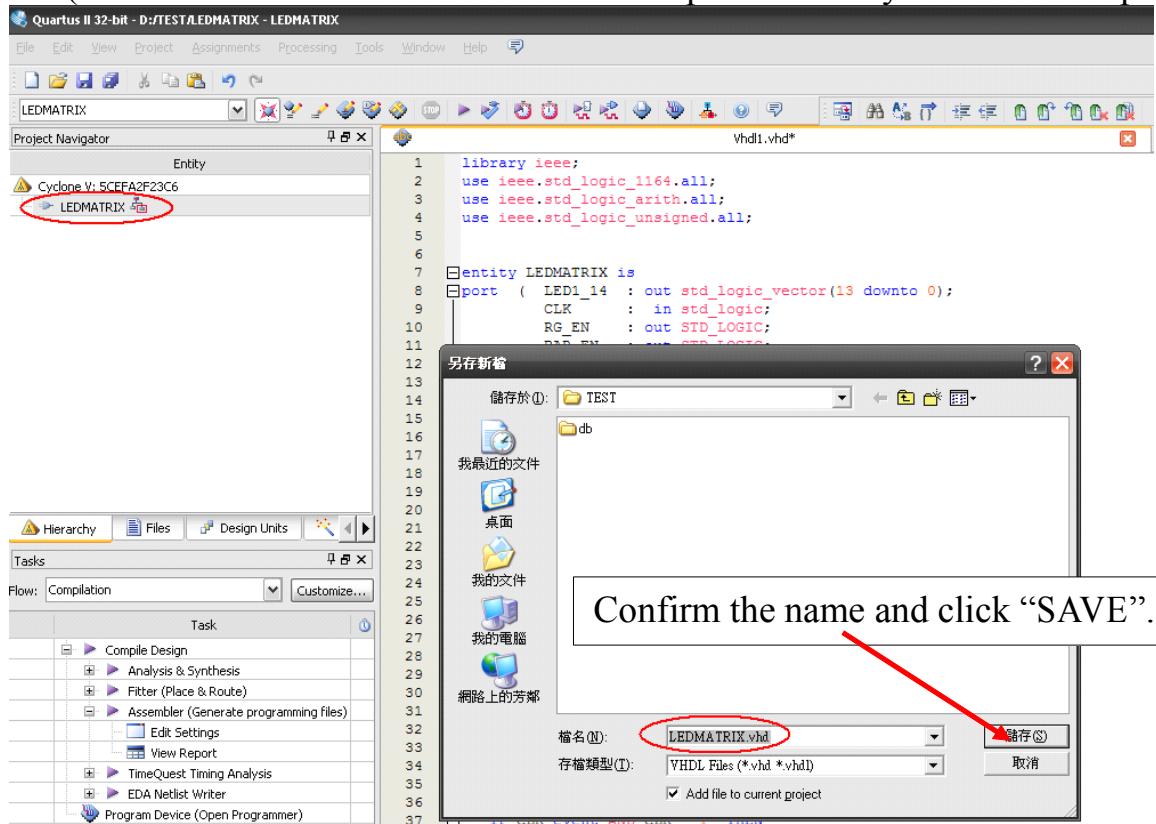
Editor Display.

● Save the edited file.

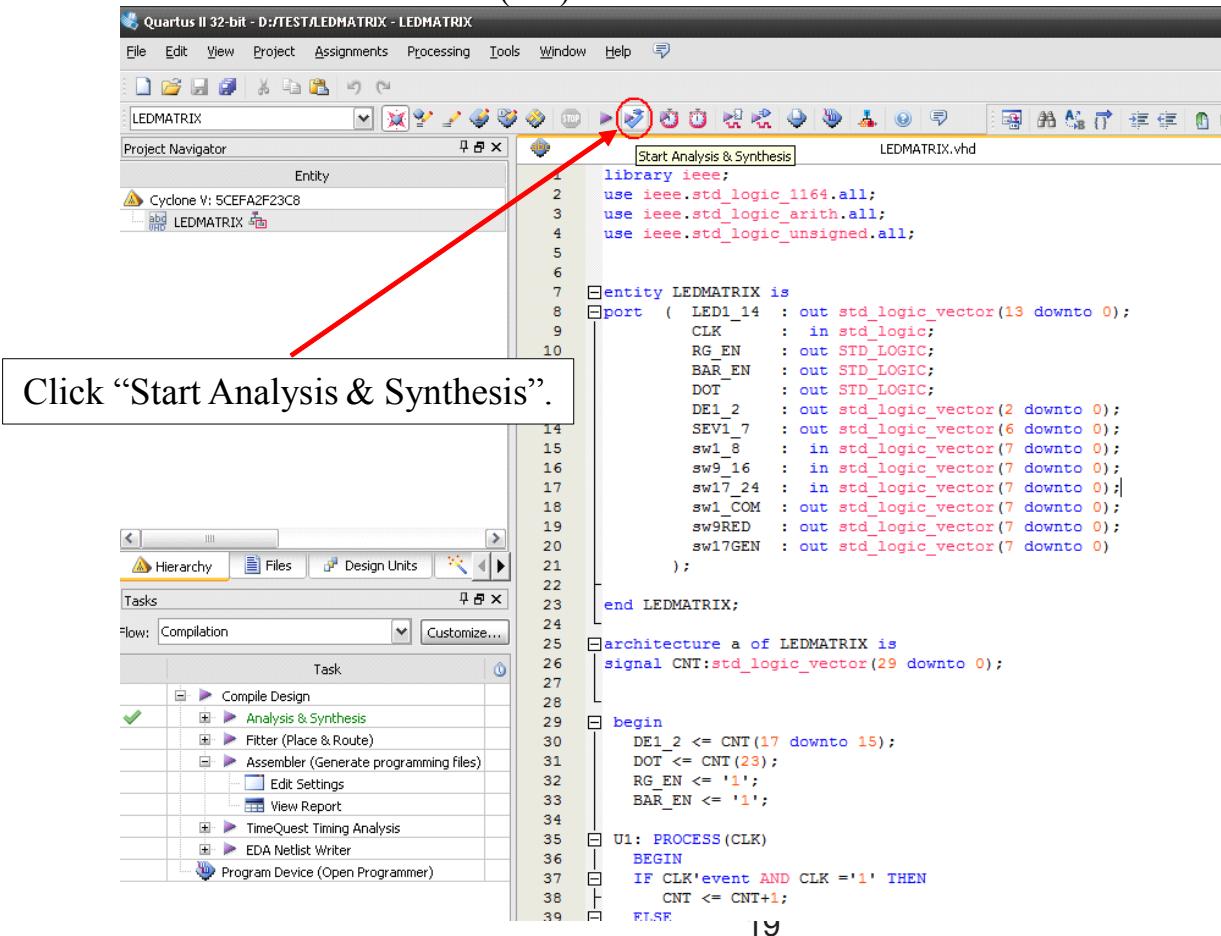
Save the edited file.

● Save the file name.

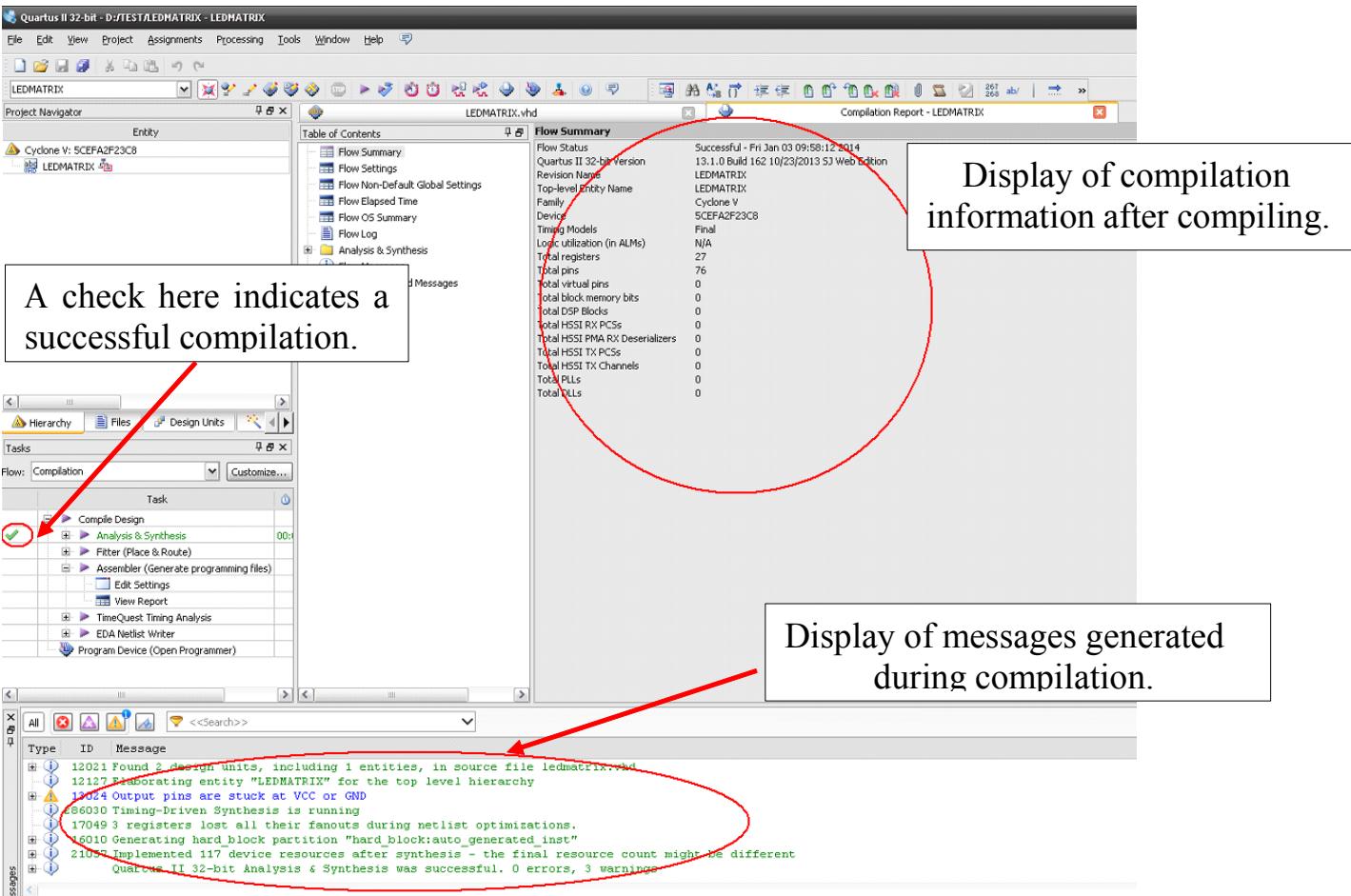
(Note: file name should be the same as Top-Level Entity Name for this project.)



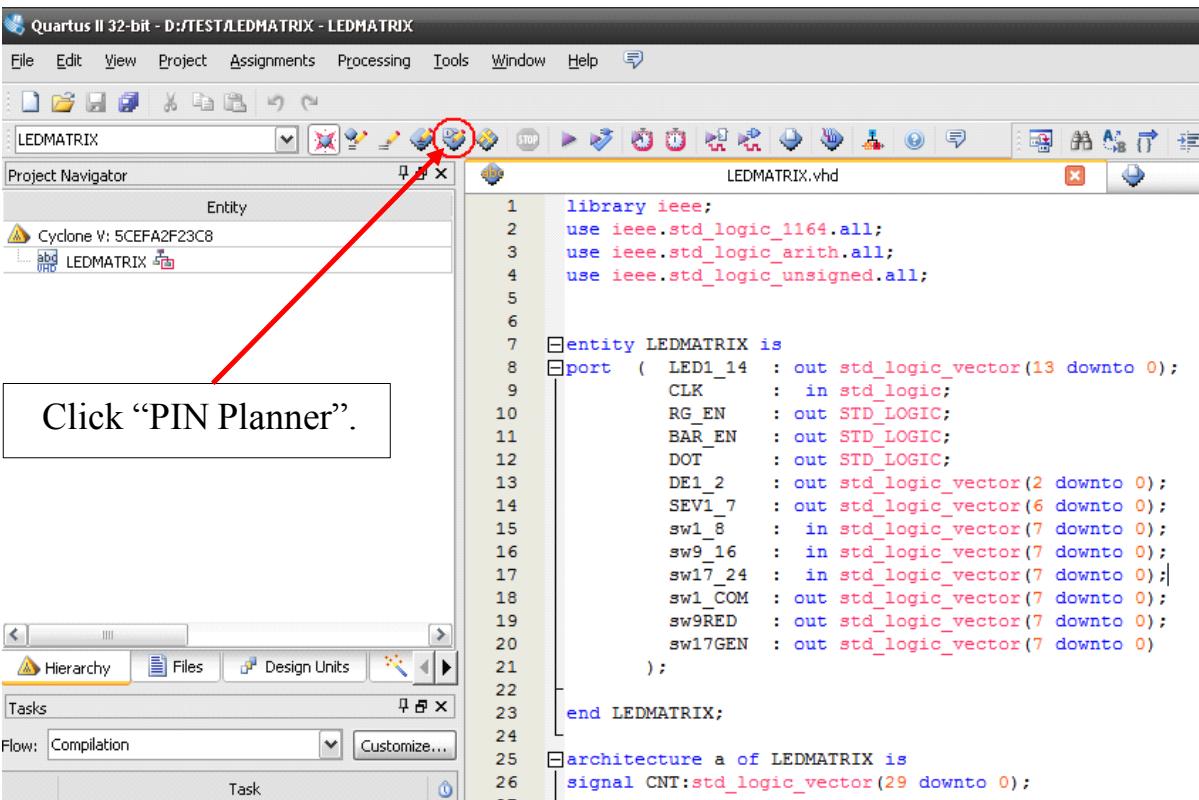
● PIN ASSIGNMENT (1/7)



● PIN ASSIGNMENT (2/7)

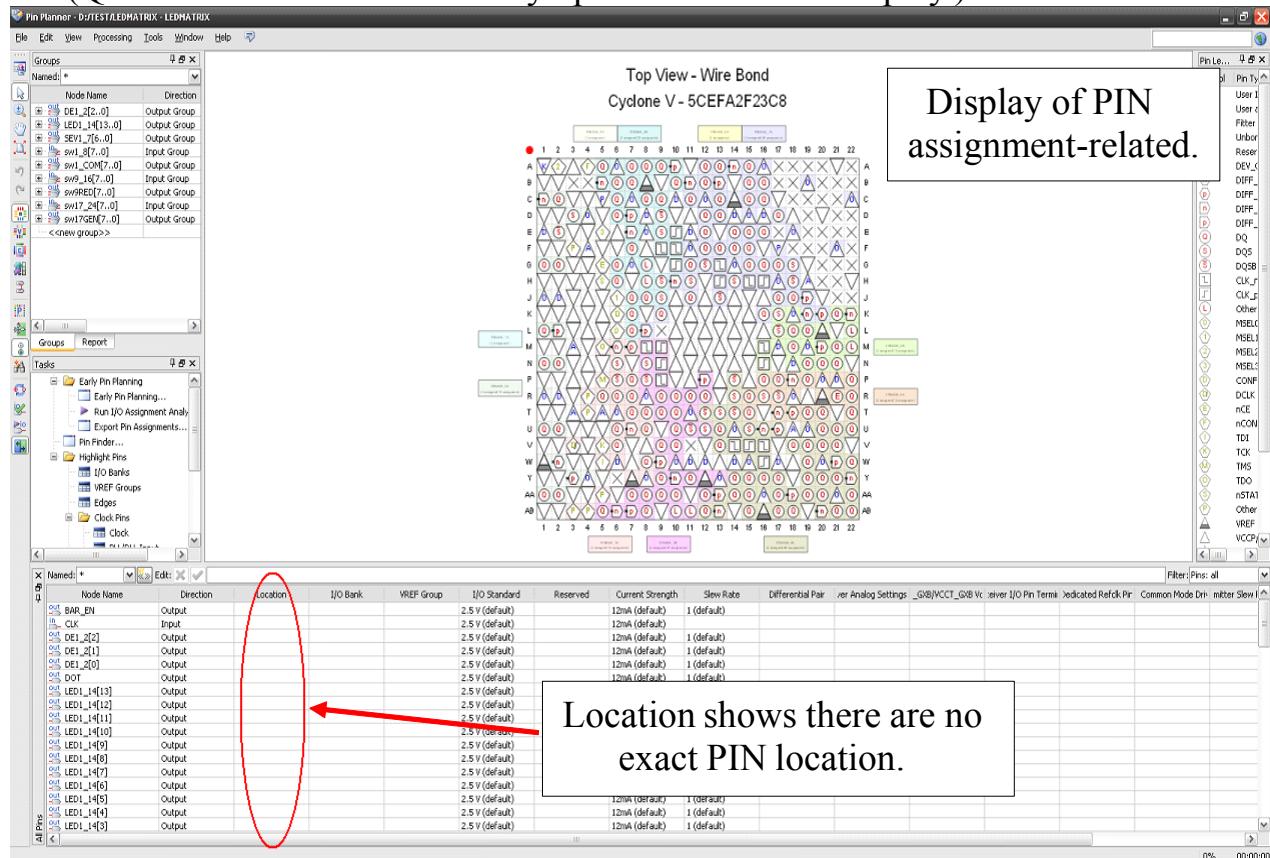


● PIN ASSIGNMENT (3/7)



● PIN ASSIGNMENT (4/7)

(Quartus II would automatically open a Pin Planner display.)



● PIN ASSIGNMENT (5/7)

(Set up PIN assignment by entering location or choosing location from drop-down list.)

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate
out BAR_EN	Output				2.5 V (default)		12mA (default)	1 (default)
in CLK	Input				2.5 V (default)		12mA (default)	
out DE1_2[2]	Output				2.5 V (default)		12mA (default)	1 (default)
out DE1_2[1]	Output				2.5 V (default)		12mA (default)	1 (default)
out DE1_2[0]	Output				2.5 V (default)		12mA (default)	1 (default)
out DOT	Output				2.5 V (default)		12mA (default)	1 (default)
out LED1_14[12]	Output				2.5 V (default)		12mA (default)	1 (default)

● PIN ASSIGNMENT (6/7)

Table showing Pin Assignment (6/7) with a red oval highlighting the last four rows:

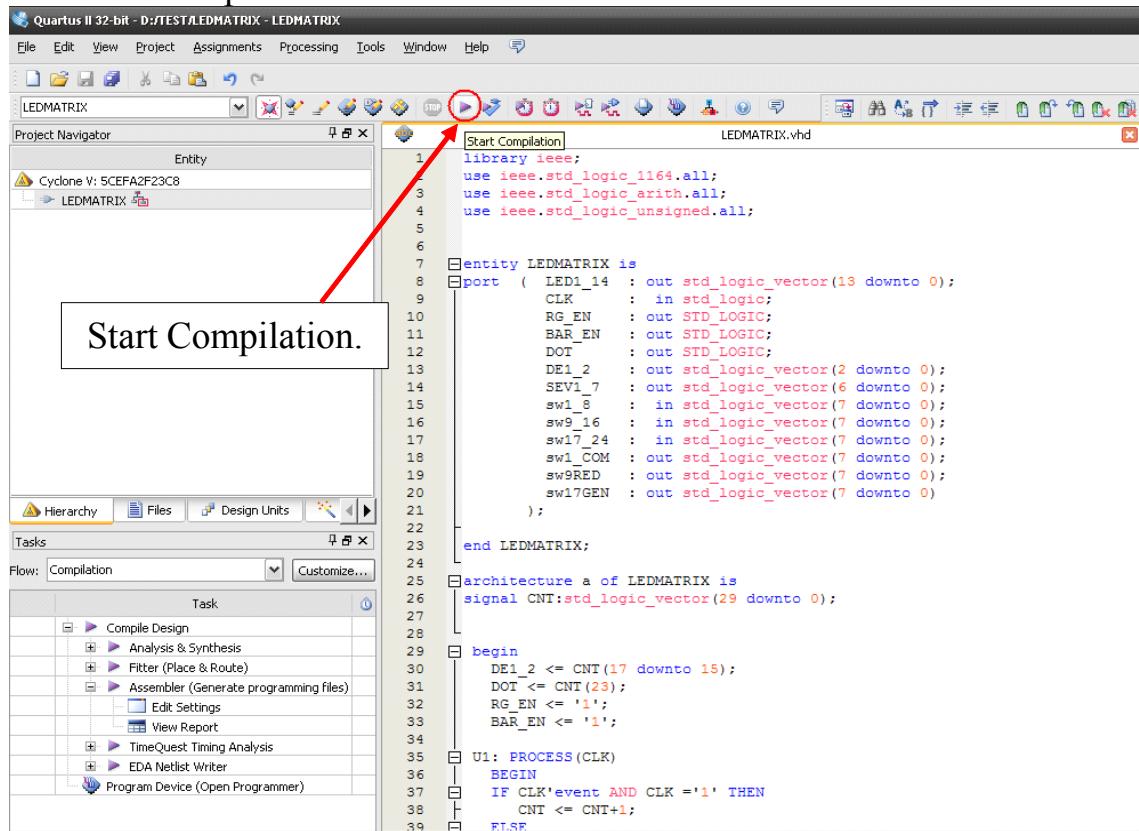
Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Dif
out BAR_EN	Output	PIN_A13	IOBANK_7A	Column I/O	DIFFIO_TX_T14n, DIFFOUT_T14n, DQ2T				
in CLK	Input	PIN_A14	IOBANK_7A	Column I/O	DIFFIO_TX_T8n, DIFFOUT_T8n				
out DE1_2[2]	Output	PIN_A15	IOBANK_7A	Column I/O	DIFFIO_TX_T8p, DIFFOUT_T8p, DQ1T				
out DE1_2[1]	Output	PIN_AA1	IOBANK_2A	Row I/O	DIFFIO_TX_L16n, DIFFOUT_L16n, DQ1L				
out DE1_2[0]	Output	PIN_AA2	IOBANK_2A	Row I/O	DIFFIO_TX_L16p, DIFFOUT_L16p, DQ1L				
out DOT	Output	PIN_AA7	IOBANK_3B	Column I/O	DIFFIO_TX_B12n, DIFFOUT_B12n, DQ2B				
out LED1_14[13]	Output	PIN_AA8	IOBANK_3B	Column I/O	DIFFIO_TX_B13n, DIFFOUT_B13n, DQ2B				
out LED1_14[12]	Output	PIN_AA9	IOBANK_3B	Column I/O	DIFFIO_TX_B16p, DIFFOUT_B16p, DQ2B				
out LED1_14[11]	Output	PIN_AA10	IOBANK_3B	Column I/O	DIFFIO_TX_B16n, DIFFOUT_B16n, DQ2B				
out LED1_14[10]	Output	PIN_AA12	IOBANK_3B	Column I/O	DIFFIO_TX_B24n, DIFFOUT_B24p, DQ3B				
							12mA / Default	1 / Default	

● PIN ASSIGNMENT (7/7) (PIN ASSIGNMENT is done.)

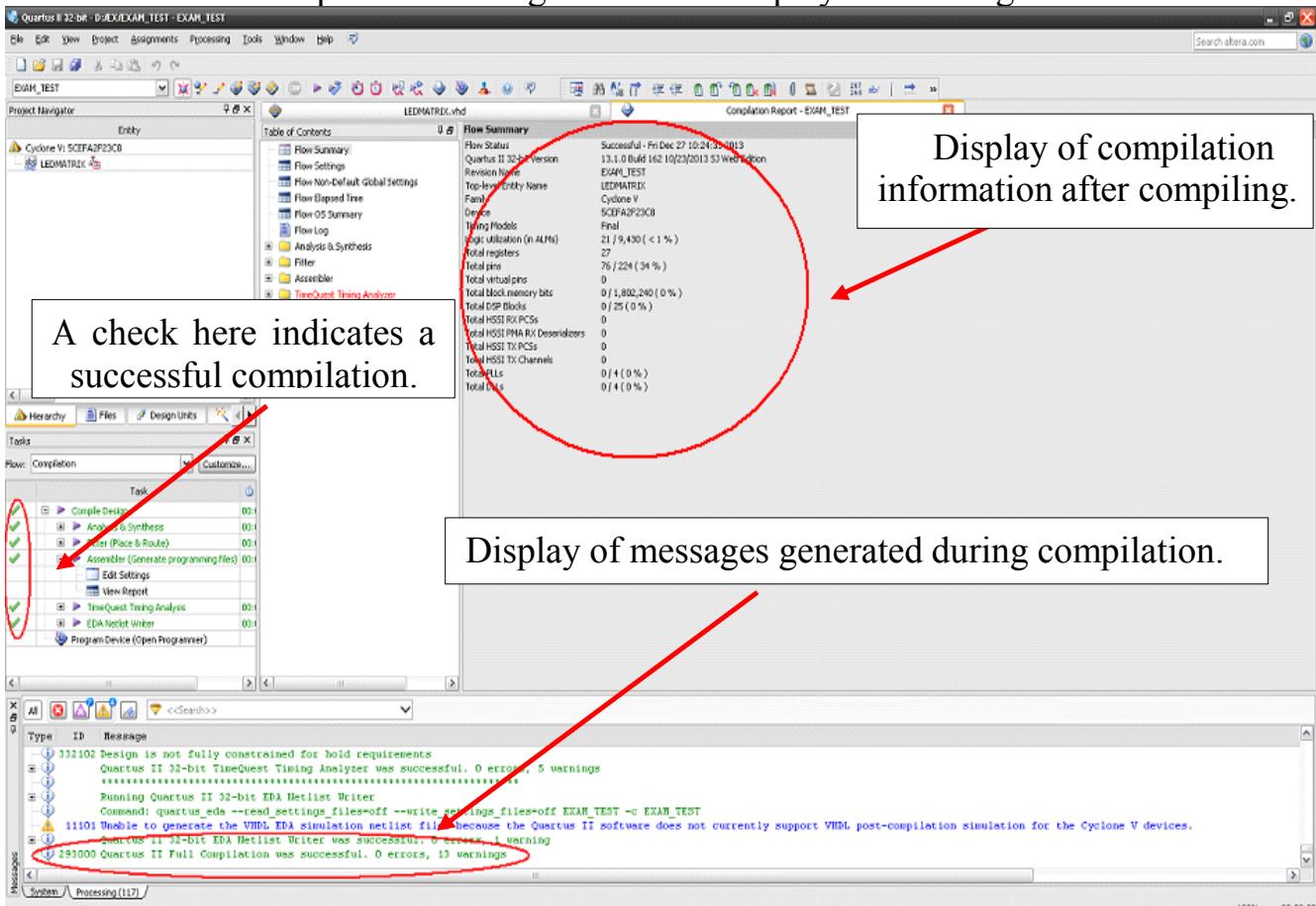
Table showing Pin Assignment (7/7) with a red oval highlighting the last four rows:

Node Name	Direction	Location	I/O Bank	VREF Group
out BAR_EN	Output	PIN_N21	5B	B5B_NO
in CLK	Input	PIN_W16	4A	B4A_NO
out DE1_2[2]	Output	PIN_AB10	3B	B3B_NO
out DE1_2[1]	Output	PIN_AB11	3B	B3B_NO
out DE1_2[0]	Output	PIN_AA12	3B	B3B_NO
out DOT	Output	PIN_AA8	3B	B3B_NO
out LED1_14[13]	Output	PIN_U1	2A	B2A_NO
out LED1_14[12]	Output	PIN_W2	2A	B2A_NO
out LED1_14[11]	Output	PIN_AA1	2A	B2A_NO
out LED1_14[10]	Output	PIN_AA2	2A	B2A_NO
out LED1_14[0]	Output	DTM_N1	2A	B2A_NO

● Start Compilation.



● Successful compilation messages would be displayed as the figure shown below.



IV. Create a programming file

- Click on “Programmer”.

```

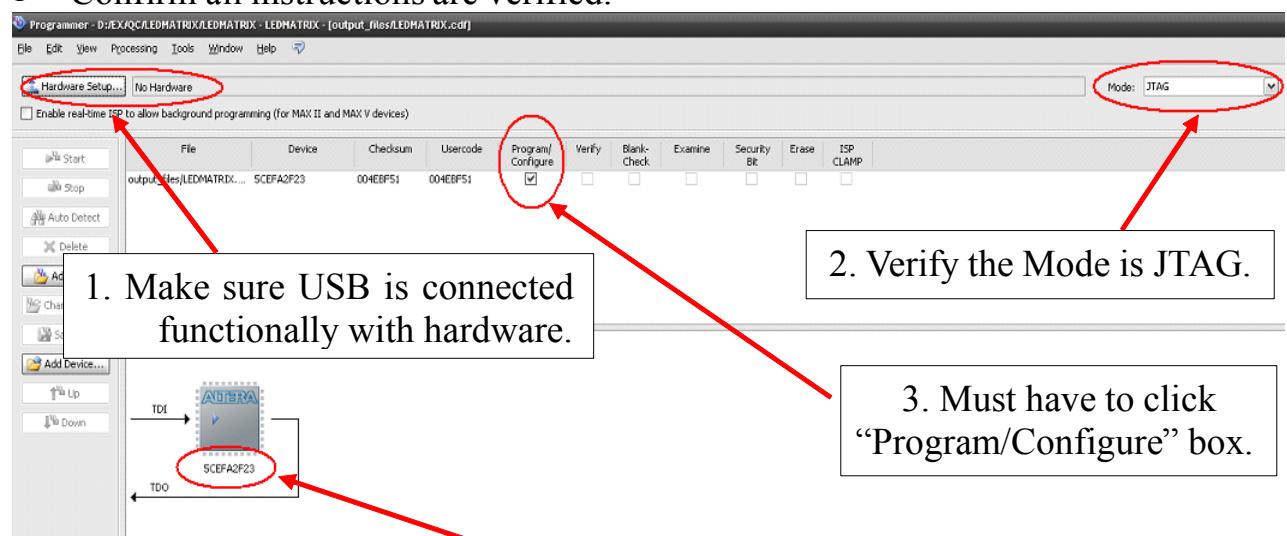
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity LEDMATRIX is
port ( LED1_14 : out std_logic_vector(13 downto 0);
       CLK      : in std_logic;
       RG_EN   : out STD_LOGIC;
       BAR_EN  : out STD_LOGIC;
       DOT     : out STD_LOGIC;
       DE1_2   : out std_logic_vector(2 downto 0);
       SEV1_7  : out std_logic_vector(6 downto 0);
       sw1_8   : in std_logic_vector(7 downto 0);
       sw9_16  : in std_logic_vector(7 downto 0);
       sw17_24 : in std_logic_vector(7 downto 0);
       sw1.COM : out std_logic_vector(7 downto 0);
       sw9RED : out std_logic_vector(7 downto 0);
       sw17GEN : out std_logic_vector(7 downto 0)
      );
end LEDMATRIX;

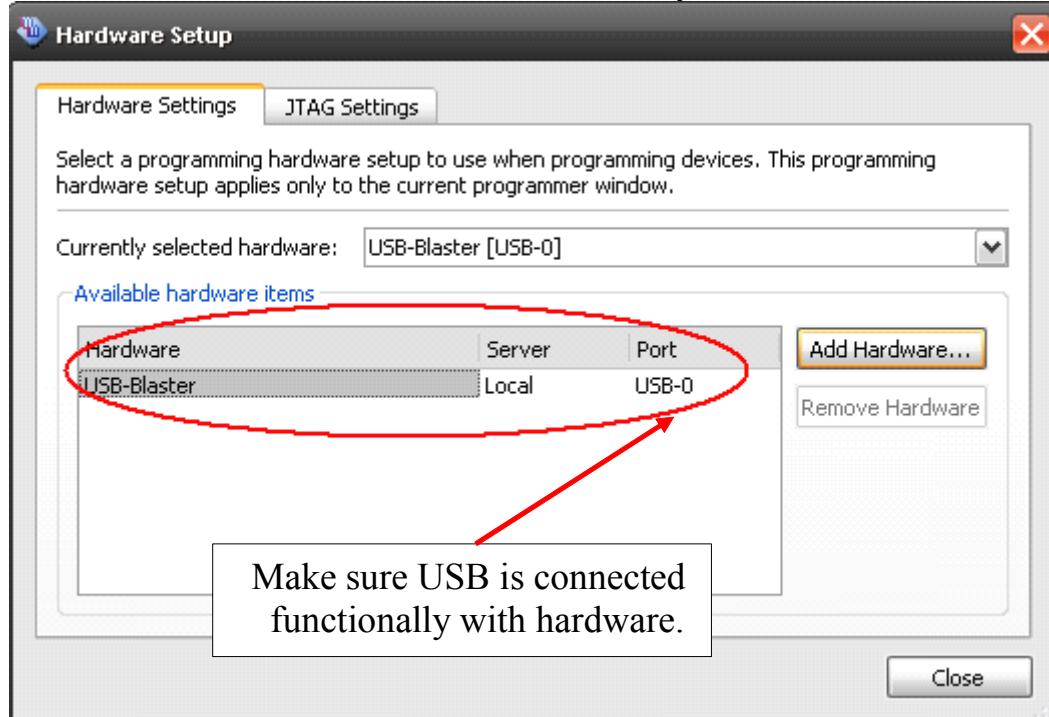
architecture a of LEDMATRIX is
signal CNT:std_logic_vector(29 downto 0);
begin
  DE1_2 <= CNT(17 downto 15);
  DOT <= CNT(23);
  RG_EN <= '1';
  BAR_EN <= '1';
  U1: PROCESS (CLK)
    BEGIN
      IF CLK'event AND CLK = '1' THEN
        sw1_8 <= CNT(29 downto 22);
        sw9_16 <= CNT(29 downto 22);
        sw17_24 <= CNT(29 downto 22);
        sw1.COM <= CNT(29 downto 22);
        sw9RED <= CNT(29 downto 22);
        sw17GEN <= CNT(29 downto 22);
      END IF;
    END PROCESS U1;
end architecture a;

```

- Confirm all instructions are verified.



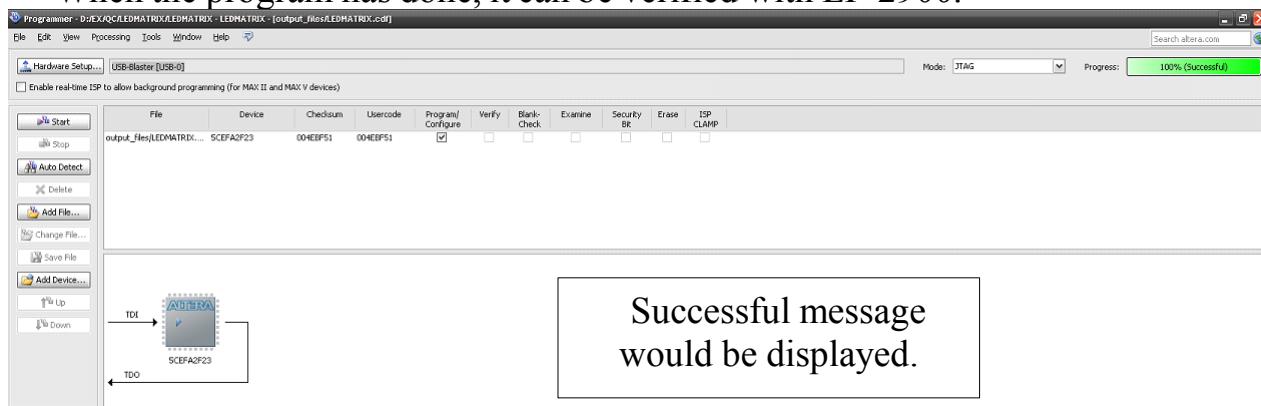
- Make sure USB is connected functionally with hardware.



- To program the IC chip.



- When the program has done, it can be verified with LP-2900.



V. Pin arrangement of LP-2900

Red-Yellow-GreenLED



Code	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	LED_COM
Device	Red LED	Yellow LED	Green LED	Red LED	Yellow LED	Green LED	Red LED	Yellow LED	Green LED	Red LED	Yellow LED	Green LED	LED 1~12
Pin	E1	D3	C2	C1	L2	L1	G2	G1	U2	N1	AA2	AA1	N20

- L1 to L12 are LED anode inputs for each LED, driven by HI.
- L1 to L8 are connected with P2.0 to P2.7 of 8051.
- LED_COM is the common cathode of all LED, driven by HI.
- LED_COM is connected to P1.6 of 8051.

7-Segment Display with Common Cathode



DE3	DE2	DE1	000	001	010	011	100	101
C1	C2	C3	C4	C5	C6			

Code	A	B	C	D	E	F	G	DP
Device	7 Segment Display							
Pin	AB7	AA7	AB6	AB5	AA9	Y9	AB8	AA8

Code	DE1	DE2	DE3
Device	74138		
Pin	AA12	AB11	AB10

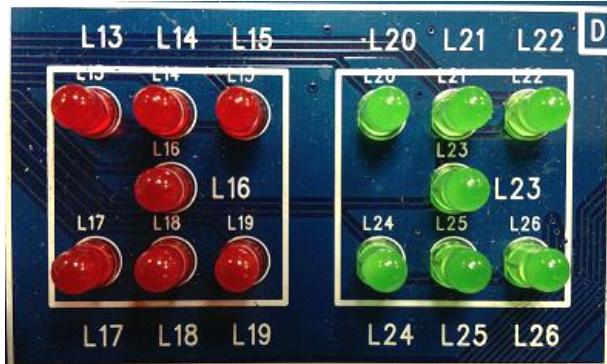
- A to DP are 7- segment display anode inputs, driven by HI.
- DE1, DE2 and DE3 are connected to 74138 which outputs Y0 to Y5 as C1 to C6.
- C1 to C6 are the common cathodes of 6 7-segment display.

Buzzer



Code	BUZZER
Device	BUZZER
Pin	AB15

Electronic Dices



Code	L13	L14	L15	L16	L17	L18	L19
Device	Red Dice						
Pin	E2	D3	C2	C1	L2	L1	G2

Code	L20	L21	L22	L23	L24	L25	L26
Device	Green Dice						
Pin	G1	U2	N1	AA2	AA1	W2	U1

Code	Dice_COM
Device	Common cathode of L13 to L26
Pin	N21

- L13 to L26 are anode inputs for each LED, driven by HI.
- L21 to L26 are connected with P1.0 to P1.5 of 8051.
- Dice_COM is the common cathode of L13 to L26, driven by HI.
- Dice_COM is connected with P1.7 of 8051.

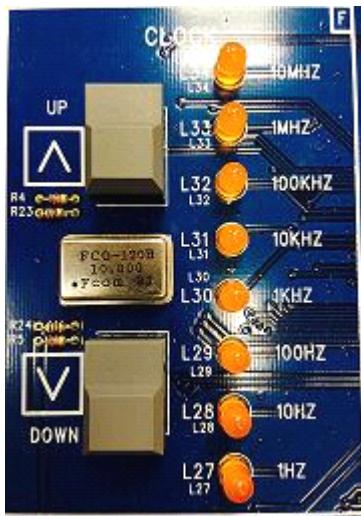
LCD Display



Code	EN	RS	RW	D0	D1	D2	D3	D4	D5	D6	D7
Device	LCD										
Pin	B1 5	B1 6	C1 5	K2 0	K1 9	J19	D1 7	L19	L22	K2 1	K2 2

- D0 to D7 are connected with P0.0 to P0.7 of 8051, and DB0 to DB7 of A/D & D/A.
- RS is connected to P3.6, and CA of A/D & D/A.
- RW is connected to P3.7, and /WR of A/D & D/A.

Clock Circuit



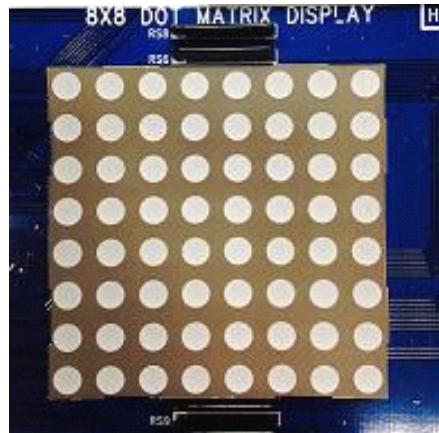
Code	L27	L28	L29	L30	L31	L32	L33	L34
Device	Yellow LED							
Pin	AB7	AA7	AB6	AB5	AA9	Y9	AB8	AA8

Code	DE1	DE2	DE3
Device	74138		
Pin	AA12	AB11	AB10

Code	OSC	UP	DOWN
Device	OSC	Button	Button
Pin	W16	R22	P22

- L27 to L34 are LED anode inputs for each LED, driven by HI.
- DE1, DE2 and DE3 are connected to 74138 which output Y6 as common cathode of L27 to L34. At this time, please set 011 on DE1, DE2 and DE3.
- OSC is the system tick of LP-2900, which provide 10 MHz.
- The UP and Down are impulse press buttons. The logic state is 0 when it is pressed, otherwise the logic state is 1.

8x8 Dot Matrix LED Display



CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8
CG1 CG2 CG3 CG4 CG5 CG6 CG7 CG8

Common Anodes

Code	Row1	Row2	Row3	Row4	Row5	Row6	Row7	Row8
Device	8 X 8 Dot Matrix							
Pin	T22	R21	C6	B6	B5	A5	B7	A7

- Row1 to Row8 driven by HI.

Red Cathodes

Code	CR1	CR2	CR3	CR4	CR5	CR6	CR7	CR8
Device	8 X 8 Dot Matrix							
Pin	D7	D6	A9	C9	A8	C8	C11	B11

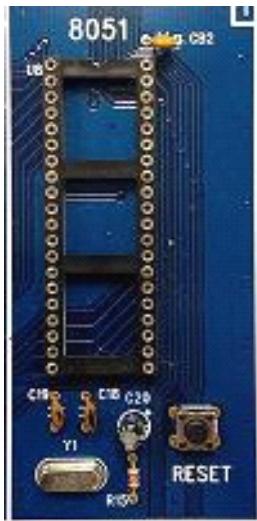
- CR1 to CR8 driven by HI.

Green Cathodes

Code	CG1	CG2	CG3	CG4	CG5	CG6	CG7	CG8
Device	8 X 8 Dot Matrix							
Pin	A10	B10	A13	A12	B12	D12	A15	A14

- CR1 to CR8 driven by HI.

8051 Single Chip



Code	P0.0	P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	P0.7
Device	8051							
Pin	K20	K19	J19	D17	L19	L22	K21	K22

- P0.0 to P0.7 are connected with D0 to D7 of LCD, also connected with DB0 to DB7 on A/D and D/A.

Code	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
Device	8051							
Pin	U2	N1	AA2	AA1	W2	U1	N20	N21

- P1.0 to P1.7 are connected with L21 to L26 and LED_COM and Dice_COM.

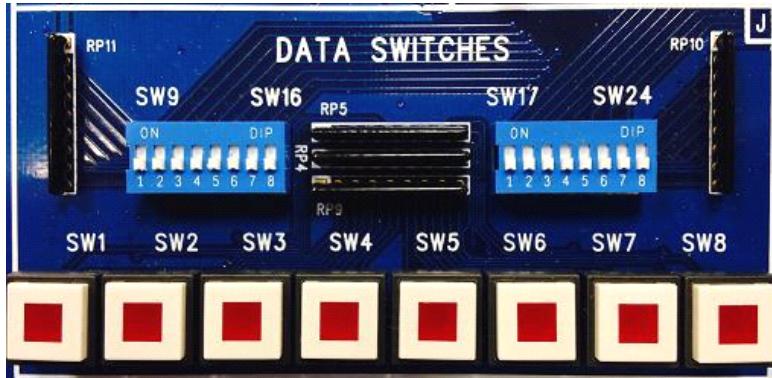
Code	P2.0	P2.1	P2.2	P2.3	P2.4	P2.5	P2.6	P2.7
Device	8051							
Pin	E2	D3	C2	C1	L2	L1	G2	G1

- P2.0 to P2.7 are connected with L1 to L8.

Code	P3.0	P3.1	P3.2	P3.3	P3.4	P3.5	P3.6	P3.7
Device	8051							
Pin	AB13	M22	D7	D6	A9	C9	B16	C15

- P3.2 to P3.5 are connected to 8x8 Dot Matrix.
- P3.6 to P3.7 are connected to RS and RW on LCD.

Data Switches



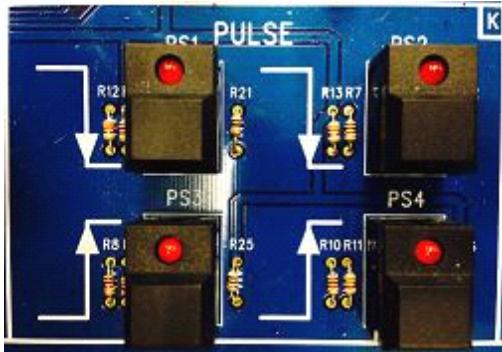
Code	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Device	Push Button							
Pin	AA15	AA14	AB18	AA18	AB17	AA17	AB20	AA20

Code	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Device	Dip Switch							
Pin	AA19	Y19	AB22	AA22	AB21	Y21	W22	W21

Code	SW17	SW18	SW19	SW20	SW21	SW22	SW23	SW24
Device	Dip Switch							
Pin	W19	Y22	U21	V21	V20	V19	U22	T20

- P3.2 to P3.5 are connected to 8x8 Dot Matrix.
- P3.6 to P3.7 are connected to RS and RW on LCD.

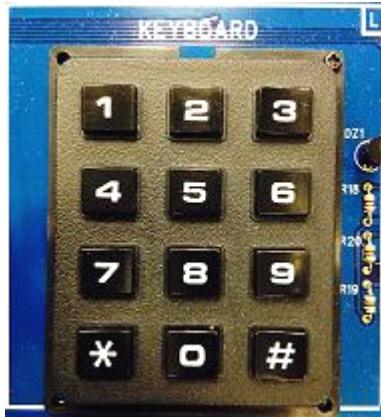
Pulse



Code	PS1	PS2	PS3	PS4
Device	Push Button With LED			
Pin	C13	B13	C16	N2

- SW1 to SW8 are pulse buttons. The logic state is 1 when it is pressed, otherwise the logic state is 0.
- SW9 to SW24 are dip switch. The logic state is 1 when it is ON, otherwise the logic state is 0.

Keyboard



Code	DE1	DE2	DE3	RK1	RK2	RK3
Device	Keyboard					
Pin	AA12	AB11	AB10	AA13	AB12	Y16

- DE1, DE2 and DE3 are connected to 74138 which outputs, Y0 to Y3 are connected to the keyboard.

A/D、D/A



A/D→ADC0804

Code	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
Device	ADC0804							
Pin	K20	K19	J19	D17	L19	L22	K21	K22

- DB0 to DB7 are connected with D0 to D7 on LCD, also connected with P0.0 to P0.7 on 8051.

Code	/CS	/RD	DE1	DE2	DE3	AD_INTR
Device	ADC0804					
Pin	AB10	C15	AA12	AB11	AB10	M21

- AD_WR connect to the output Y6 of 74138.
 - DE1, DE2 and DE3 are connected to 74138 as inputs.
 - /RD is connected to RW on LCD

D/A→AD7528

Code	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
Device	ADC0804							
Pin	K20	K19	J19	D17	L19	L22	K21	K22

- DB0 to DB7 are connected with D0 to D7 on LCD.

Code	/CS	/WR	/DACA
Device	AD7528		
Pin	AA10	C15	B16

- /WR connect RW on LCD.
 - /DACA connected RS on LCD.



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