BoF SBI extension stuff

LPC 2022

Andes/Renesas:

- They don't have DMA coherent peripherals
- They used some SBI extensions to configure non-coherency
- Sent RFC patchset that almost certainly needs to become alternatives if acceptable
- Touches a bunch of arch code as is, some could (and should) be moved to drivers/soc
- https://lore.kernel.org/linux-riscv/20220906102154.32526-1-prabhakar.mahadev-lad.rj@bp.renesas.com/

Microchip:

- Use an extention for our AMP inter-hart communication as an isolation mechanism
- Allows e51 to handle all writes to the IP
- "No" arch code impact - just in a mailbox and a remoteproc driver (like qcom)
- https://github.com/linux4microchip/linux/blob/linux-5.15-mchp/drivers/mailbox/mailbox-miv-ihc.c

Arch policy doc:
https://www.kernel.org/doc/html/latest/riscv/patch-acceptance.html "To avoid the maintenance complexity and potential performance impact of adding kernel code for implementor-specific RISC-V extensions, we'll only to accept patches for extensions that have been officially frozen or ratified by the RISC-V Foundation."