7-Segment SPI Slave Display

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Display Behaviour

The display has 10 8-bit registers to control which digits appear on the screen. Register 0 acts as a bitmask to control which digits of the 7-Segment display are enabled. Registers 1 through 8 contain the value to display in the corresponding location, with index 1 appearing at the right hand side of the board and index 8 on the far left. Register 9 will control the radix point. These registers can be written to via SPI and at startup all will contain zero.
Each bit in Register 0 and 9 are active high. Writing all zeros to these registers will disable all digits or radices respectively. Registers 1 through 8 expect an 8 bit unsigned integer of which only the lower 4 bits will be used. The value will be automatically decoded into the appropriate segments.

SPI Behaviour

The display can be controlled over SPI with the signals `spi_sclk_i`, `spi_ss_i` and `spi_mosi_i`, `spi_miso_o` all of which are idle high. The data is clocked on the positive edge of `spi_sclk_i`. The maximum transfer frequency is not yet established but the display is clocked at 5 MHz so the recommended maximum SPI clock is 25 MHz.
Each transaction is 16 bits long, which is transferred in two 8 bit sections. The upper byte is sent first and each byte is MSB first. The 16 bit long message is broken up as follows: The only command that is currently valid is the write command of `0001`. The

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
command				address				display value							

address is the 4 bit unsigned integer representation of the register number.