

**Computer Science Fundamentals:**  
Intro to Algorithms, Systems, & Data Structures

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October 2024

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## Preface

Big thanks to **Christine Papadakis-Kanaris**  
for teaching Intro. to Computer Science II,

**Dora Erdos** and **Adam Smith**

for teaching BU CS330: Introduction to Analysis of Algorithms

With contributions from:

**S. Raskhodnikova, E. Demaine, C. Leiserson, A. Smith, and K. Wayne,**  
at Boston University

*Please note:* These are my personal notes, and while I strive for accuracy, there may be errors. I encourage you to refer to the original slides for precise information. Comments and suggestions for improvement are always welcome.

## Prerequisites

## Circuits and Logic

### 1.1 Representing Information

#### 1.1.1 Electricity & Information: Volts, Amps, & Watts

Figuring out how to represent information is tricky: Nature encodes information in DNA, though it may be hard to store because of decay (This is an active area of research). Punching holes in cards was a common method of storing information, but it's difficult to manipulate [7]. Ideally:

- **Inexpensive:** We want to reproduce at scale with low costs.
- **Stable:** Reliably store information for long periods.
- **Mutable:** The ability to manipulate information easily.

##### Definition 1.1: Electricity & Information

Electricity is a flow of electrons, which can be used to represent information. We can use the presence or absence of an electric current to represent binary values:

- **1** for presence of current;
- **0** for absence of current.

This is the basis of digital electronics and computing.

This is great for our applications, as electricity is relatively inexpensive given the scale of production.

##### Theorem 1.1: Noise & Error Accumulation

We ought to keep in mind that electricity is not perfect. Though we design systems to measure information, slight inaccuracies or environmental factors may introduce noise, which over time corrupts information.

It's important that we understand the difference between analog and digital systems:

### Definition 1.2: Analog vs. Digital Circuits

A **circuit** is a closed path through which electricity flows, allowing us to manipulate and measure electrical signals.

An **analog** system is one that uses continuous signals to represent information, while a **digital** system uses discrete values (e.g., binary) to represent information.

### Example 1.1: Real World Analog vs. Digital

Vinyl records are analog, as the grooves on the record represent sound waves continuously. In contrast, a digital system would be a CD or MP3 file, where sound is represented as discrete samples of the original sound wave. ■

Our main focus will be on digital systems, representing the strength of electricity as binary values. First we will briefly understand the terminology used in electrical systems:

### Definition 1.3: Voltage, Amps, & Watts

Definition wise we have the following terms in electrical systems:

- **Voltage (Volts):** The potential difference between two points in an electrical circuit, measured in volts (V).
- **Amperage (Amps):** The flow of electric **current**, measured in amperes (A/I).
- **Resistance (Ohms):** The opposition to the flow of electric current, are ohms ( $\Omega/R$ ).
- **Power (Watts):** The rate at which electrical energy is transferred, are watts (W).

We calculate all such as follows:

- **Voltage:**  $V = I \cdot R$  (Voltage = Current  $\times$  Resistance).
- **Current:**  $I = P/V$  (Current = Power / Voltage).
- **Resistance:**  $R = V/I$  (Resistance = Voltage / Current).
- **Power:**  $P = V \cdot I$  (Power = Voltage  $\times$  Current).

These ratios between Voltage, Current, and Resistance are part of **Ohm's Law**.

Let's understand this with a common analogy to water flow:

### Example 1.2: Water & Electric Flow Analogy

Imagine a water pipe system:

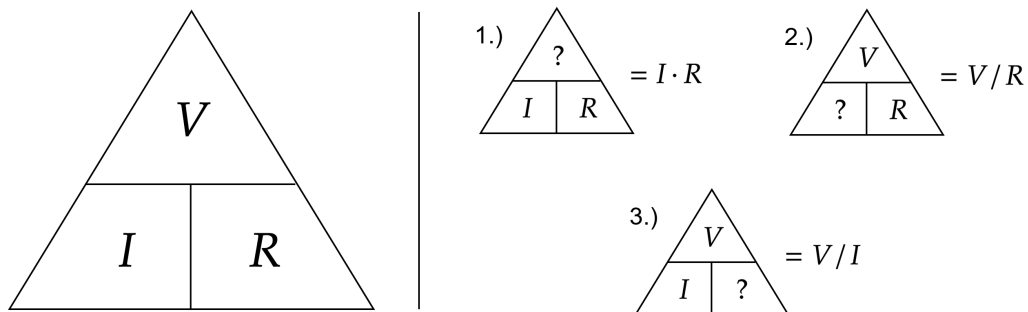
- **Voltage** is the water pressure in the pipes, the force pushing water through the system.
- **Current** is the amount of water flowing through the pipes at any given time.
- **Resistance** is the size of the pipes, which affects how easily water can flow.
- **Power** is the total amount of water that flowed through the system over time.



The relationship between Voltage, Current, and Resistance has a handy visualization:

### Definition 1.4: Ohm's Triangle

Ohm's Triangle is a visual representation of the relationship between Voltage, Current, and Resistance. If any two values are known, the third can be calculated using the triangle:



Here, Voltage ( $V$ ) is at the top, with Current ( $I$ ) and Resistance ( $R$ ) at the bottom corners:

1. **Voltage** is unknown:  $V = I \cdot R$ .
2. **Current** is unknown:  $I = V / R$ .
3. **Resistance** is unknown:  $R = V / I$

A common mnemonic to remember is "Viral" for VIR (Voltage, Current, Resistance).

Now for completeness sake, we distinguish the following:

**Definition 1.5: Energy vs. Power**

**Energy** is the capacity to do work, measured in joules (J). **Power** is the rate at which work/energy is done or used, measured in watts (W). This is given by the formulation:

$$P = E/t$$

where  $P$  is power,  $E$  is energy, and  $t$  is time.

**Example 1.3: Energy-Power Water Analogy**

Continuing with the water analogy:

- **Energy** is the total amount of water stored in a tank.
- **Power** is how fast water flows out of the tank per second.

If we have a large tank (more energy), and water flows out slowly, we have high energy but low power. Conversely, if we open the tap wide (high power), we use up the water quickly. ■

We will wrap up such with a final analogy that uses numbers:

**Example 1.4: Mathematical Water Analogy**

- **Water Gun:** Imagine a water gun with very high pressure granted by the resistance of its small nozzle, so only a little water comes out.
  - Pressure (Voltage) = 10 V
  - Water Flow (Current) = 1 A
  - Power = 10 V  $\times$  1 A = 10 W
- **Large Hose:** Now, consider a large fire hose with lower pressure but a much wider opening with less resistance, allowing a lot of water to flow.
  - Pressure (Voltage) = 2 V
  - Water Flow (Current) = 5 A
  - Power = 2 V  $\times$  5 A = 10 W

Both systems consumed the same amount of power (10 W), despite supporting different voltages, currents, and possibly energy supplies. **Question:** What is the resistance of each system? ■



### 1.1.2 Combinational Devices

We now focus on the conduits of representing information digitally:

#### Definition 1.6: Digital Current Encoding Threshold

Given a line of voltage  $V$ , which we measure,  $V_{TH}$  serves as a threshold:

$$0\text{-bit} < V_{TH} < 1\text{-bit}$$

In practice, we have noise  $\epsilon$  in our measurements, making it hard to discern  $V_{TH} + \epsilon$  from  $V_{TH} - \epsilon$ . To mitigate this, we pad the threshold from both sides called the **forbidden zone**:

$$0\text{-bit} \leq V_L < \text{"Forbidden Zone"} < V_H \leq 1\text{-bit}$$

Where  $V_L$  (low-level) and  $V_H$  (high-level) are the region markers for valid voltage distinction.

#### Definition 1.7: Combinational Device

A **combinational device** is follows four specifications (spec.) called the, **static discipline**:

- **Input:** A set of input signals (i.e., measuring voltage levels).
- **Output:** A set of output signals (i.e., outputting voltage levels).
- **Functional Spec:** A mapping of all possible input combinations to an output value.
- **Timing Spec:** Detailing an upper bound  $t_{PD}$  (**Propagation Delay**), which is the minimum amount of time needed for the output to stabilize on a new value after an input change.

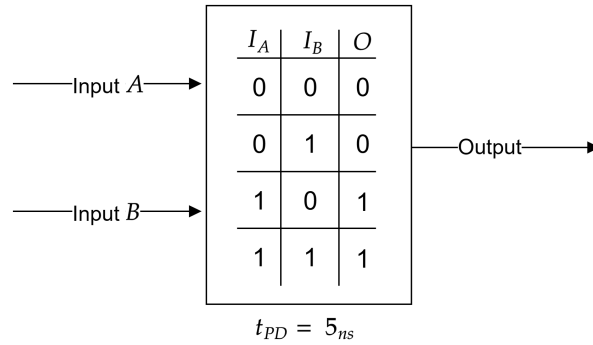


Figure 1.1: A combinational device with inputs  $A$  and  $B$ , and a truth table detailing mappings towards the output. The  $t_{PD} = 5_{ns}$  (nanoseconds).

**Definition 1.8: Combinational Digital Systems**

A combinational device may also be made up of multiple other combinational devices. It must follow that:

- Each device is indeed a combinational device.
- Every input is connected to a single output.
- Each parent input will at most visit the same child input once (i.e., no cycles).

The  $t_{PD}$  of the system is the sum of sub-devices  $t_{PD}$ 's along a path such that it is the maximum such  $t_{PD}$  path in the system.

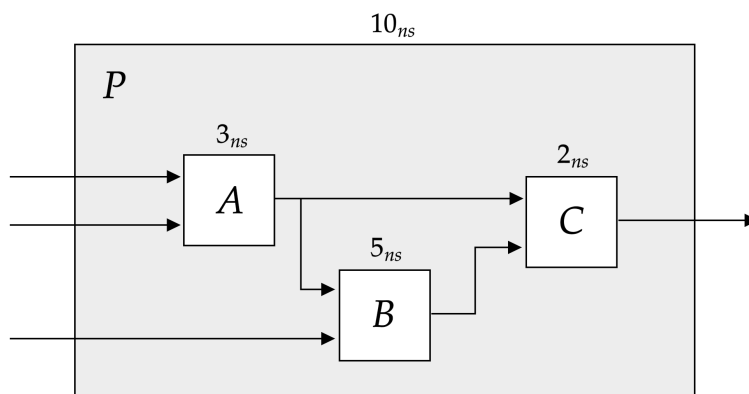


Figure 1.2: A combinational digital system, with a parent device  $P$  and children devices  $A$ ,  $B$  and  $C$ . We abstract away the mappings focusing on the components and their connections. We see that there are no cycles and all sub components are also combinational devices; Hence, the parent system is a combinational device. The  $t_{PD}$  of the system is  $10_{ns}$ , as the longest path takes  $A \rightarrow B \rightarrow C = 3_{ns} + 5_{ns} + 2_{ns} = 10_{ns}$ , the effective bottleneck of the system.

Though this introduces a new problem:

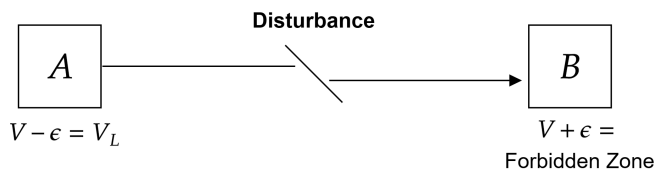
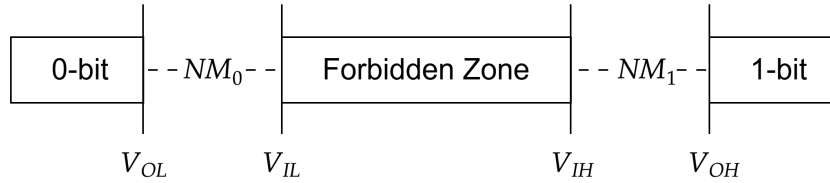


Figure 1.3: Combinational devices  $A$  and  $B$  communicate; However,  $A$ 's output ( $V$ ) is dangerously close to  $V_L$ , over the wire there is a disturbance, causing the input of  $B$  to enter the forbidden zone.

We offer a simple fix to this problem, by loosening up the thresholds during certain phases:

#### Definition 1.9: Noise Margins

To mitigate noise from outputs of a combinational device, we decrease the *forbidden zone* (FZ) for the receiving device. The overlap between the output's FZ and the input's FZ is called the **noise margin**. Concretely, we define the following:



Where,  $V_{OL}$  and  $V_{OH}$  are the output bounds, while  $V_{IL}$  and  $V_{IH}$  are the new input bounds. Then  $NM_0$  is the noise margin for the 0-bit, and  $NM_1$  is the noise margin for the 1-bit. The smallest of the two is called the **noise immunity** of the device (i.e., the worst case that must be supported).

Now when building our systems or combinational devices we must standardize how a particular device behaves on inputs and outputs to account for the worst case noise.

#### Definition 1.10: Voltage Transfer Characteristics (VTC)

The **Voltage Transfer Characteristics** (VTC) is a graphical representation which shows how a device's inputs affect its outputs after stabilization. The horizontal axis measures the input voltage, while the vertical axis measures the output voltage.

- **Horizontal Axis ( $V_{in}$ ):** Contains  $V_{IL}$  and  $V_{IH}$ :

$$V_{in} \leq V_{IL} \text{ (0-bit)} \quad \text{and} \quad V_{in} \geq V_{IH} \text{ (1-bit)}$$

Otherwise, the input is in the forbidden zone.

- **Vertical Axis ( $V_{out}$ ):** Contains  $V_{OL}$  and  $V_{OH}$ :

$$V_{OL} < \text{Invalid Outputs} < V_{OH} \quad \text{such that} \quad V_{in} < V_{OL}, V_{in} > V_{OH}$$

I.e., if the input is already in the forbidden zone, the output is irrelevant.

It's given that the device must perform properly such that a  $V_{in} > V_{IH}$  will always yield a  $V_{out} > V_{OH}$ , and a  $V_{in} < V_{IL}$  will always yield a  $V_{out} < V_{OL}$ . Each device has its own VTC, plotting the input-output relationship. The resulting curve is the **VTC** of the device.

Diagram next page.

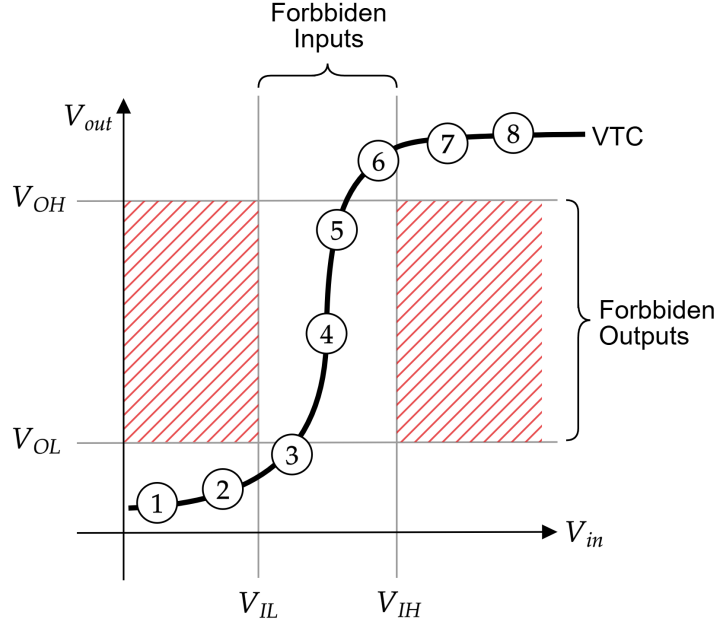


Figure 1.4: A Voltage Transfer Characteristics (VTC) diagram, showing the input-output relationship of a device. The horizontal axis represents the input voltage, while the vertical axis represents the output voltage. The invalid output regions are shaded in red. The VTC is the bold line that crosses each point. Possible points: (1-2) received a low input and output reading, (3-6) undefined, and (7-8) high input and output reading. E.g., an inverter device (inverts logic) would be a vertical flip of the above VTC curve.

Notice how in Figure (1.4) the center white region is taller than it is wide:

#### Theorem 1.2: Properties of VTC – Gain & Nonlinearity

Since more leeway is allowed for input voltages, the following suffices  $V_{OH} - V_{OL} > V_{IH} - V_{IL}$ . We can compactly write this as:

- **Width of the transition (x-axis):**  $\Delta V_{in} = V_{IH} - V_{IL}$ .
- **Height of the swing (y-axis):**  $\Delta V_{out} = V_{OH} - V_{OL}$ .

Since  $\Delta V_{out} > \Delta V_{in}$ , the **gain** (average slope) satisfies:  $(\text{avg.}) \text{ gain} = \frac{\Delta V_{out}}{\Delta V_{in}} > 1$ .

Because of this ratio ( $\text{gain} > 1$ ) small deviations (wiggles) in the input are amplified (exaggerated) in the output, which **regenerates** the signal (i.e., the output is a reinforced version of the input). The slope of the VTC must be **nonlinear** to ensure flat stable regions around 0 and 1 bits, and steep transitions between the forbidden zones (as seen in Figure 1.4).

### 1.1.3 Building Transistors: The Chemistry of Silicon

To even begin to manage currents and voltages, we will need a way to control the flow of electricity:

#### Definition 1.11: Transistor

A **transistor** is a small electronic semiconductor device. A **semiconductor** (e.g., silicon) is a material with electrical conductivity between that of a **conductor** (great electricity conductor) and an **insulator** (inhibits electric flow). Transistors fall into two broad families:

- **Bipolar Junction Transistor (BJT)**: a current-controlled device with three terminals (pins),
  - **Emitter (E)**: current flows *out*.
  - **Base (B)**: controls operation.
  - **Collector (C)**: current flows *in*.
- **Field-Effect Transistor (FET)**: a voltage-controlled device with three terminals,
  - **Source (S)**: current flows *in*.
  - **Gate (G)**: controls operation.
  - **Drain (D)**: current flows *out*.

Low-power transistors are molded in an epoxy (resin) package. Higher-power transistors often use a metal tab or “can” that you bolt to a **heat sink** (a metal object that dissipates heat).

Pin order and package style vary by model; check the **part number** and manufacturer’s **datasheet** for exact details [1, 6].

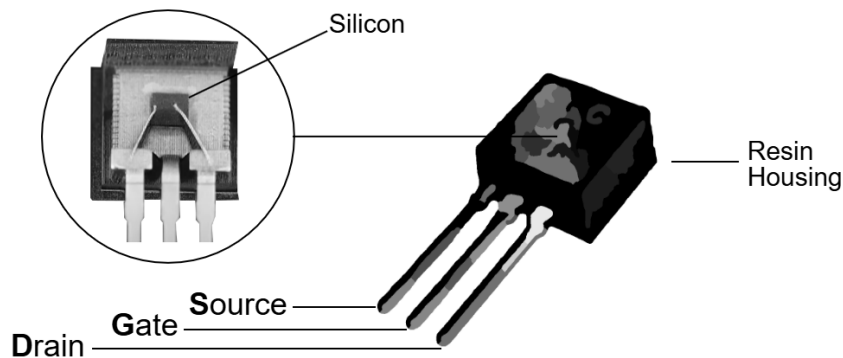


Figure 1.5: Cross-section of a discrete transistor: a silicon die (center) is bonded to three metal leads, all encased in an epoxy package. A metal tab (not shown) may be added for heatsinking.

**Theorem 1.3: FETs over BJTs**

A BJT needs continuous base current, which wastes energy. A MOSFET only requires its gate to be charged or discharged (i.e., voltage applied or removed), which is more efficient.

Now we briefly step into chemistry for completeness sake to understand differing silicon charges:

**Definition 1.12: Anatomy of an Atom**

An **atom** is the smallest unit of matter that retains the properties of an element. It consists of three main subatomic particles:

- **Protons:** Positively charged particles found in the nucleus.
- **Neutrons:** Neutral particles also found in the nucleus (same size as protons).
- **Electrons:** About the same charge as proton, but negative, and about 1800x smaller and lighter than a proton.

Protons and neutrons are tightly packed together in a space called the **nucleus**, gaining the name **nucleons**; Electrons orbit the nucleus at discrete distances called **shells** or **energy levels**. The number of protons in the nucleus defines the element (i.e., specifications). E.g., 79 protons will always be gold.

Opposite charges attract, causing an **orbital space**, in which subatomic particles never collide (i.e., alike orbiting planets). Neutrons act as a buffer between protons (e.g., Silver is stable with 60 or 62 neutrons, but unstable with 61). Atoms with different number of neutrons are called **isotopes**, latin for “same place”. Electrons may jump between shells and atoms. If there is a greater number of electrons to protons, the atom is **negatively charged** (anions), otherwise it is **positively charged** (cations) [2].

**Definition 1.13: Periodic Table**

The **Periodic Table of Elements** organizes all known elements by the number of protons in their nuclei. This is called an **atomic number** (e.g., gold’s atomic number is 79). Elements are abbreviated from their latin translations (e.g., gold is **aurum**, AU, which means “shining dawn”). There are 118 elements, with 80 being stable and the rest being unstable isotopes. Anything past 82 protons (lead) is unstable, undergoing radioactive decay.

**Tip:** The periodic table is complete, hence movies that claim “we discovered a new element!” truly deserve science-fiction as their defining genre.

We'll stop with the chemistry dive after these next two critical definitions

**Definition 1.14: Shell Capacities & Valence Electrons**

The first shell of any atom can hold up to 2 electrons, and the second 8. From 1-20 periodic elements, the third and fourth shells can hold 8 and 2 respectively. A *full* shell is considered **stable**, otherwise it is **unstable**. This arrangement of electrons within the shells is called the **electron configuration** (EC) of the atom. An EC is written as a n-tuple, starting with the inner-most shell (e.g., 2, 8, 8, 2 for calcium).

The outer most shell is called the **valence shell**. An atom's **valency** (the number of electrons in the valence shell) determines whether a chemical reaction will occur. If an atom is stable (i.e., full valence shell), it will not react with other atoms. Unstable atoms *strive* to become stable by either gaining, losing, or sharing electrons with other atoms [5].

**Definition 1.15: Chemical Bonds – Molecules & Compounds**

The act of atoms joining together (e.g., sharing electrons, which is called a **covalent bond**), forms a **molecule**. Concretely, a molecule is a merger of two or more elements. We use subscripts to denote the number of atoms in a molecule (e.g.,  $\text{H}_2\text{O}$  is water, with two hydrogen atoms and one oxygen atom). **Compounds** are a subset class of molecules that consists only of two more more **different** elements (e.g.,  $\text{H}_2\text{O}$  is a compound, but  $\text{O}_2$  is not, as it only has one element, oxygen) [8].

Now to what we've been waiting for:

**Definition 1.16: Doping – N-type & P-type Silicon**

Silicon has 14 atoms, with an EC of (2, 8, 4); Hence silicon is unstable. If we view silicon (Si) as a 3D lattice (a string of Si atoms in 3D grid), each Si atom will share its four valence electrons with its neighbors to become stable (covalent bonding). This creates a **silicon crystal**.

Adding another element to the silicon lattice is called **doping**. We are interested in two types of doping [6]:

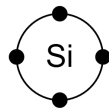
- **N-type:** When adding an element like phosphorus (P), EC of (2, 8, 5), is added to the silicon lattice, one electron goes unused after the covalent bonding. This free electron creates a **negative charge carrier** (hence N-type).
- **P-type:** Conversely, adding boron (B), EC of (2, 8, 3), creates a **positive charge carrier** (hence P-type). This is because boron won't have enough to share with its neighbors, causing **holes** (absence of electrons), overall lowering the density of electrons.

Let's visualize what we've learned so far:



Figure 1.6: An image of a silicon crystal [4].

1.)



2.)

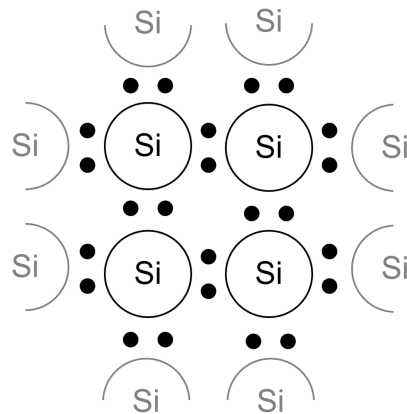


Figure 1.7: (1) Shows a single silicon atom (Si) and its valence electrons (4 black dots). (2) Shows a flattened silicon lattice where neighboring Si atoms share their electrons to become stable. This creates an electron configuration of (2, 8, 8) for surrounded Si atoms.



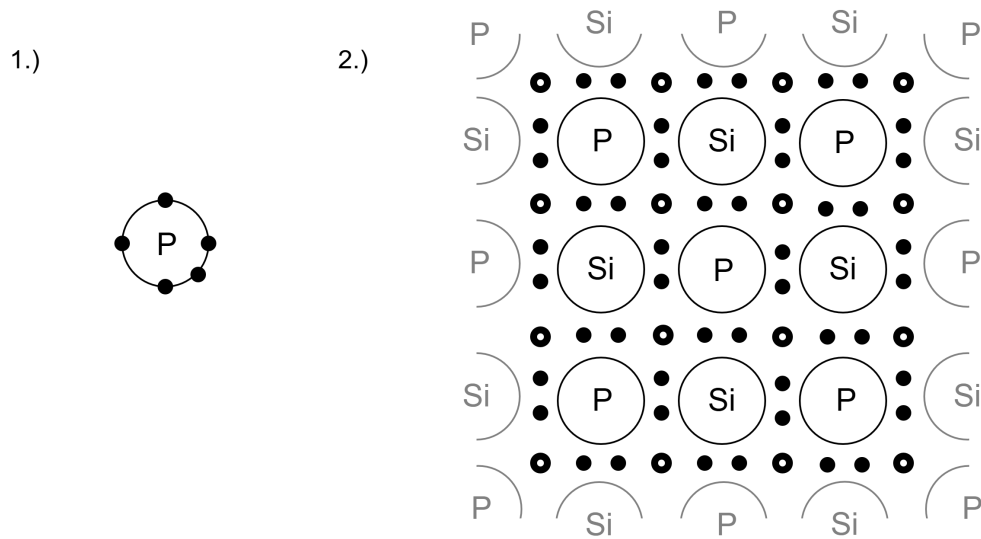


Figure 1.8: (1) Shows a single phosphorus atom (P) and its valence electrons (5 black dots). (2) A silicon lattice where phosphorus is doped, creating free electrons (thick dots with holes).

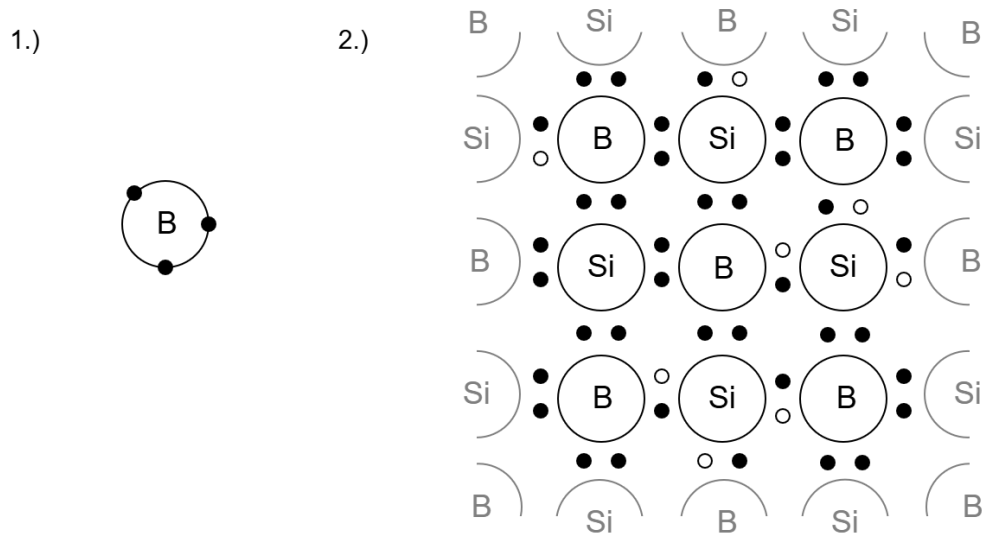


Figure 1.9: (1) Shows a single boron atom (B) and its valence electrons (3 black dots). (2) Shows a flattened silicon lattice where boron is doped, creating holes (halo dots).

**Definition 1.17: N-type & P-type Junctions**

When a N-type and P-type material are placed next to each other creates a **PN-junction**. At this junction, we get a **depletion region**, where N-type electrons and P-type holes cross; This leaves a slightly positive region on the N-type side and a slightly negative region on the P-type side. This manifests an electric field, creating a barrier, preventing further flow across the junction [6].

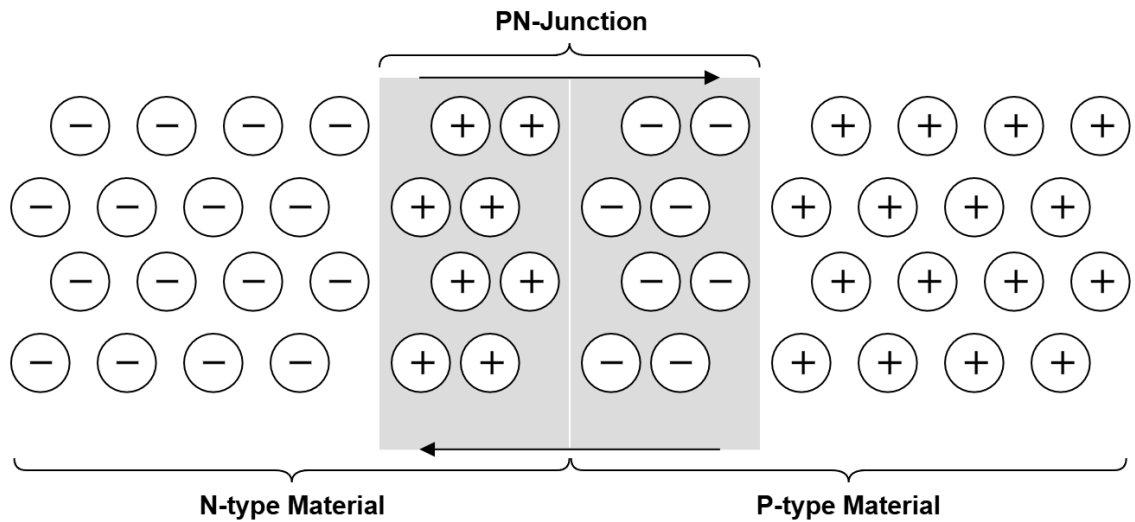


Figure 1.10: A PN-junction, where the depletion region is shown in gray.

**Definition 1.18: MOSFET – High-Level Overview**

A **MOSFET** (Metal-Oxide-Semiconductor Field-Effect Transistor) is a type of FET that uses its gate to control the flow of current. It consists of two default starting states:

- **Enhancement:** Normally **off** (i.e., no current flows), until such voltage is applied:
  - **N-Channel Enhancement:** A positive voltage.
  - **P-Channel Enhancement:** A negative voltage.
- **Depletion:** Normally **on** (i.e., current flows), until such voltage is applied:
  - **N-Channel Depletion:** A negative voltage.
  - **P-Channel Depletion:** A positive voltage.

**Definition 1.19: MOSFET – Anatomy of N-Channel**

A MOSFET **N-Channel Enhancement** is constructed as follows:

- **Substrate:** A base-layer of P-type material from which all parts will build upon.
- **Source & Drain:** Two motes are dug at either ends of the substrate and filled with N-type material; One for our **source** and the other for our **drain**. Two metal contacts are placed on these motes (our terminals); A body of metal is connected to the bottom of the substrate (**base/body terminal**), which connects to the source terminal.
- **Gate:** A metal contact pad is placed between the motes on top of the  $\text{SiO}_2$  layer, forming the **gate terminal**. A layer of silicon dioxide ( $\text{SiO}_2$ ) is sandwiched between the gate and the substrate. Since  $\text{SiO}_2$  is a superb insulator, it prevents the gate terminal from touching/interacting with the substrate.
- **Channeling:**  $\text{SiO}_2$  is a **dielectric** material, meaning that when a charge is applied to one side, the opposite charge builds on the other side, creating an electric field. When a positive charge is applied, it attracts negative electrons from the other side, creating a **channel** (i.e., bridge) between the two motes (source to drain), allowing current.

The **M**etal from gates, the **O**xide from the  $\text{SiO}_2$  layer, the **S**emiconductor from the substrate and motes, and the **FET** from the field-effect, gives us the name **MOSFET**.

For **N-Channel Depletion**, A *thin* N-type substrate-channel is already present, bridging the two motes (source and drain) together. Once a negative charge is applied to the gate, positive holes are attracted, weakening the channel; This effectively stops the flow of current.

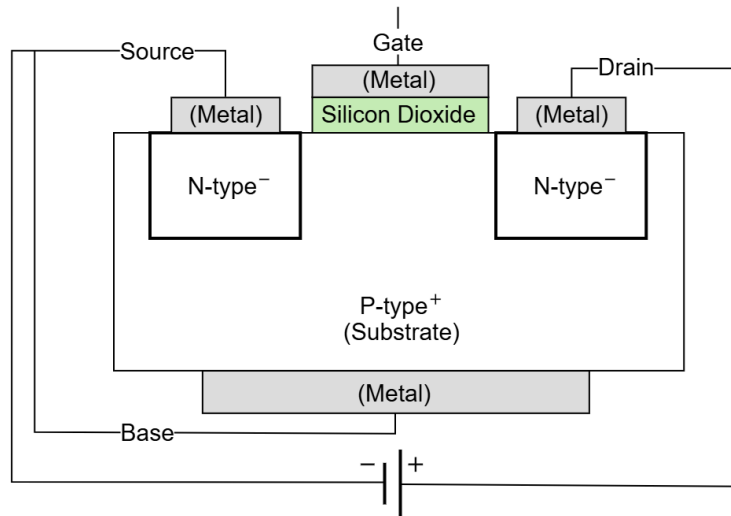


Figure 1.11: N-Channel Enhancement (off). Negative battery side to source, positive to drain.

**Theorem 1.4: Flow of Electrons**

Recall that a body of electrons that are negatively charged (low potential), have a surplus of electrons. A positive charge (high potential) reflects a deficit of electrons. Therefore, when given the chance (alike water), electrons will flow to fill the void.

**Tip:** An empty stomach has a high potential for food, while a full stomach has a low potential, as there's not much more room left to stuff food into.

**Definition 1.20: MOSFET – N-Channel Battery Configuration**

One battery is used to power the MOSFET, and another to control the gate. The source connects to the negative, and the drain to the positive side of the battery.

The gate is connected to a second battery, which can be either positive or negative, depending on the MOSFET type. The **other** end of this battery is connected to the source terminal.

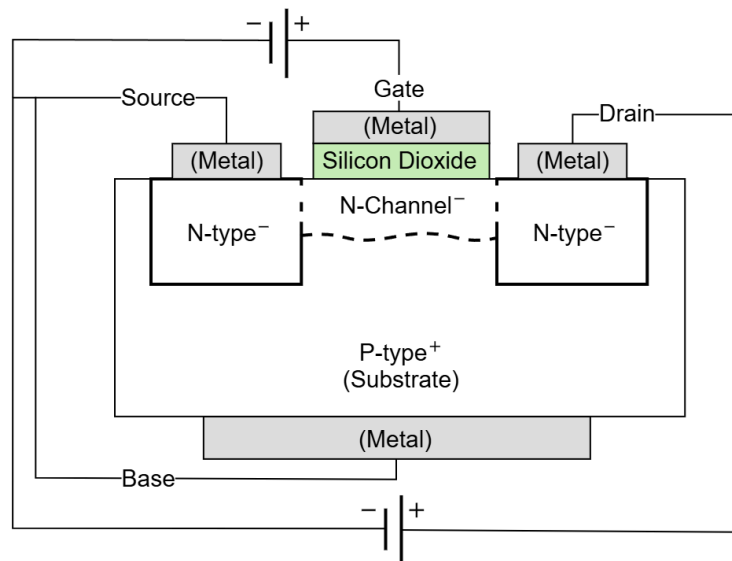


Figure 1.12: N-Channel Enhancement (on). Negative battery side to gate, positive to source. Positive charge given to the gate attracts negative electrons on the other side of the  $\text{SiO}_2$  layer, creating a channel between the source and drain.

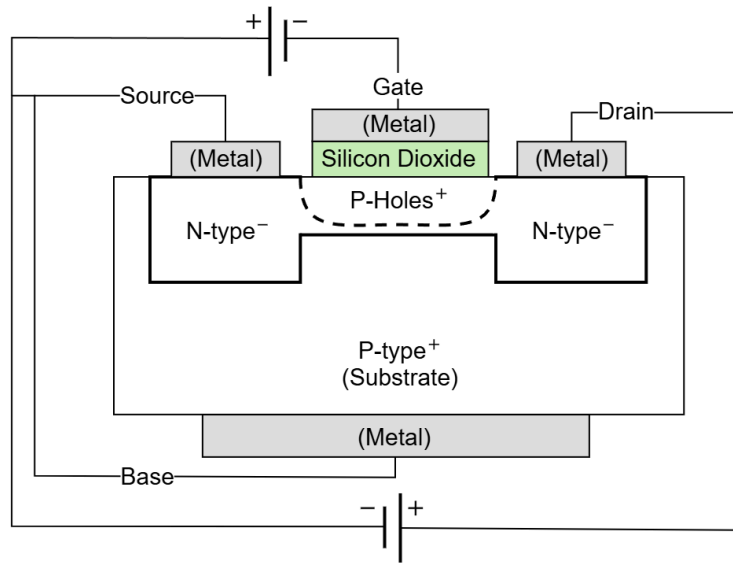


Figure 1.13: N-Channel Depletion (on). Negative charge to gate, creates holes into the channel.

#### Definition 1.21: MOSFET – Anatomy of P-Channel

The P-Channel variation follows the same logic as the N-Channel Definition (1.19); Instead, we swap N-type for P-type materials, and vice versa. Then apply negative for Enhancement and positive for Depletion on the gate to open or close the channel respectively (1.18). **In particular**, source now connects to a high potential and drain to a low potential.

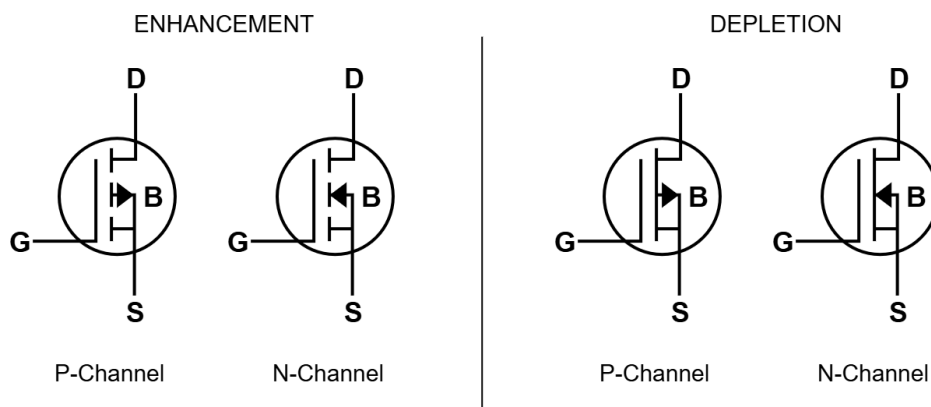


Figure 1.14: MOSFET symbols, **G** (gate), **S** (source), **D** (drain), and **B** (body) terminals.

### 1.1.4 Logic Gates & Functional Completeness

This section will cover how we take MOSFETs and use them to build logic gates.

#### Definition 1.22: Gate-Source Voltage $V_{GS}$

Recall Definition (1.20), the gate battery's opposite end is connected to the source terminal. This serves as a zero-volt reference for the gate terminal. The difference in potential between the gate and source terminals is called the **gate-source voltage** ( $V_{GS}$ ):

$$V_{GS} = V_G - V_S,$$

Once  $V_{GS}$  exceeds the threshold voltage  $V_{TN}$  (for N-channel) or is below the threshold voltage  $V_{TP}$  (for P-channel), the MOSFET turns on, allowing current to flow from source to drain.

**Tip:** Notice that source takes from gate, i.e., for N-channel, the gate must overcome the source's negative charge. Hence we must exceed a threshold voltage to turn on the MOSFET. For P-channel, the same logic applies, but in reverse, as the components are implemented in a complementary manner.

#### Definition 1.23: Pull-Up & Pull-Down Switches

Let  $V_{DD}$  be the positive supply ("logical 1") and ground (0 V) be "logical 0." A CMOS logic gate uses:

- **Pull-Down Switch** (Off: 0, On: 1): N-channel enhancement. If  $V_{GS} > V_{TN}$ , source connects to drain, producing a logical 1.
- **Pull-Up Switch** (Off: 1, On: 0): P-channel enhancement. If  $V_{GS} < V_{TP}$ , source connects to  $V_{DD}$ , producing a logical 1.

**Tip:** Think of pull-down as "pulling down to the ground" to allow electrons to escape.

Additionally, the "DD" in  $V_{DD}$  does not stand for anything; it was made not to be confused with  $V_D$ , the voltage at the drain terminal. Though, unimaginative, it is simply convention.

**Definition 1.24: CMOS Logic Gate**

A **CMOS logic gate** is a circuit that uses **Complementary MOSFETs** to perform logical operations. It consists of:

- **Pull-Down Network (PDN)**: N-channel MOSFETs (NFET) connected to ground.
- **Pull-Up Network (PUN)**: P-channel MOSFETs (PFET) connected to  $V_{DD}$ .

The output is high when the PUN is active and the PDN is inactive, and vice versa.

Pull-up	Pull-down	Digital
on	off	"1"
off	on	"0"
on	on	undefined
off	off	disconn.

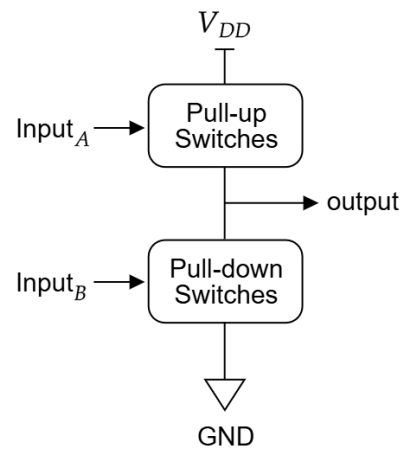
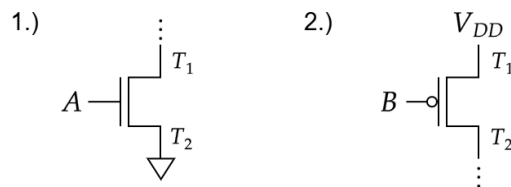


Figure 1.15: Simple CMOS logic gate, where **GND** stands for ground,  $V_{DD}$  for positive supply. **Note:** That even if the circuit is disconnected, the output may still “remember” its last state for some time until the charge dissipates.

**Definition 1.25: Simplified NFET & PFET Symbols**

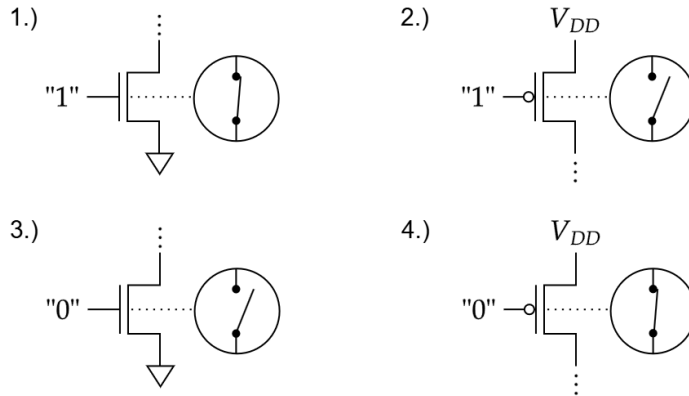
Below are input gates  $A$  and  $B$ , with two other terminals  $T_1$  and  $T_2$ , simplifying Figure(1.15):



(1) NFET,  $T_1$  output, and  $T_2$  ground; (2) PFET,  $T_1$  is  $V_{DD}$  (typically 1V), and  $T_2$  output [3].

**Definition 1.26: Open & Closed Circuits – NFET & PFET Logic**

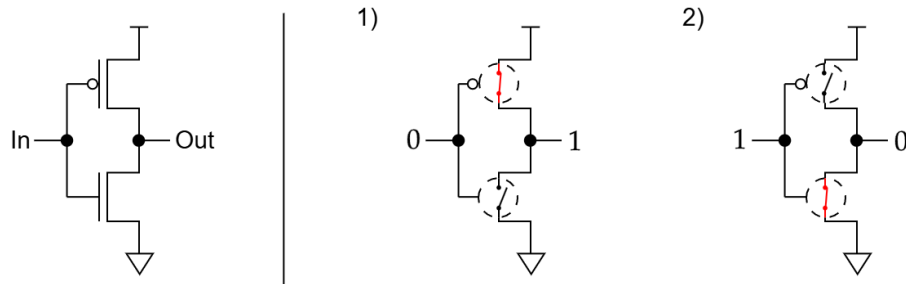
A **closed circuit** is a complete path for current to flow, while an **open circuit** is an incomplete path:



- (1) An NFET is closed when given a digital 1 (high voltage), while (2) a PFET, is open;  
 (3) NFET, open when given 0 (low voltage), while (4) a PFET is closed.

**Definition 1.27: MOSFET Logic Gate – Not**

Below shows a logic gate, NOT, using MOSFETs (NFET and PFET):



Both the NFET and PFET share the same input. The top line represents  $V_{DD}$  (positive supply), while the bottom line is ground (triangle). (1) input low, NFET is open, PFET is closed, output is high from  $V_{DD}$ ; (2) input high, NFET is closed, PFET is open, output is low from ground. **Important:** A black dot connecting two or more lines represents a connection.



**Definition 1.28: Functional Completeness**

it can be used to express all possible Boolean functions. For example, the set of operators {AND, OR, NOT} is functionally complete. However, we can do better. The NAND gate (and NOR gate) by itself is functionally complete.

**Example 1.5: Functionally Complete Sets of Operators**

1. {NAND} alone

$$\begin{aligned}\neg A &= A \text{ NAND } A, \\ A \wedge B &= \neg(A \text{ NAND } B) = (A \text{ NAND } B) \text{ NAND } (A \text{ NAND } B), \\ A \vee B &= (A \text{ NAND } A) \text{ NAND } (B \text{ NAND } B).\end{aligned}$$

2. {NOR} alone

$$\begin{aligned}\neg A &= A \text{ NOR } A, \\ A \vee B &= \neg(A \text{ NOR } B) = (A \text{ NOR } B) \text{ NOR } (A \text{ NOR } B), \\ A \wedge B &= (A \text{ NOR } A) \text{ NOR } (B \text{ NOR } B).\end{aligned}$$

3. { $\wedge, \neg$ } alone

$$\begin{aligned}\neg A &= \neg A, \\ A \wedge B &= A \wedge B, \\ A \vee B &= \neg(\neg A \wedge \neg B).\end{aligned}$$

4. { $\vee, \neg$ } alone

$$\begin{aligned}\neg A &= \neg A, \\ A \vee B &= A \vee B, \\ A \wedge B &= \neg(\neg A \vee \neg B).\end{aligned}$$

5. { $\rightarrow, \neg$ } alone

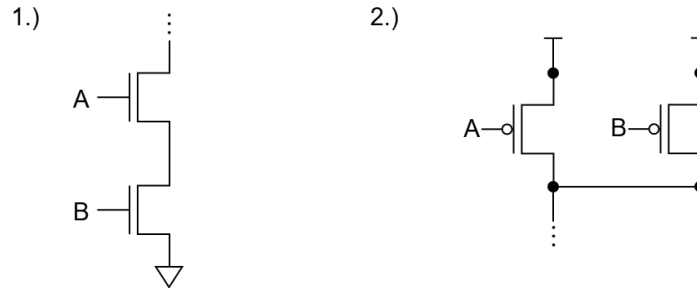
$$\begin{aligned}\neg A &= \neg A, \\ A \vee B &= \neg A \rightarrow B, \\ A \wedge B &= \neg(A \rightarrow \neg B).\end{aligned}$$

Recall,  $A \rightarrow B$  is logically equivalent to  $\neg A \vee B$ . ■

Let's brainstorm possibilities for an AND and NAND, and elaborate on Definition (1.24):

**Theorem 1.5: Balancing Series & Parallel Connections**

It's important in a CMOS circuit that the PUN and PDN are in fact complements of each other. Below illustrates two types of connections:



(1) Shows a NFET **series** connection (i.e., sequentially connected). Theoretically in isolation, this represents an AND gate ( $A \cdot B$ ), meaning both  $A$  and  $B$  must be high to close the circuit.

(2) Shows a PFET in **parallel** connection (i.e., side-by-side connected). As per complementarity, this represents the NAND gate ( $\overline{A + B} = \overline{A} \cdot \overline{B}$ ), by De Morgan's Law; Either  $A$  or  $B$  must be low to close the circuit.

Hence to **balance**, between the PUN and PDN, we must ensure that:

- each NFET series requires a PFET parallel.
- each PFET series requires a NFET parallel.

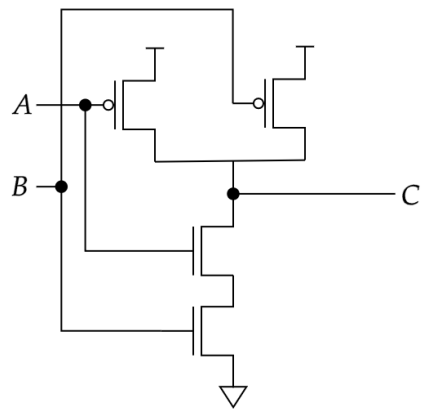
This keeps our networks complementary, ensuring that when one is closed, the other is open.

**Tip:** Think about how to create this before moving to the next page. understand that the placement of the output determines the logic of the circuit. Since PUNs default to high, think about how that might affect the output.

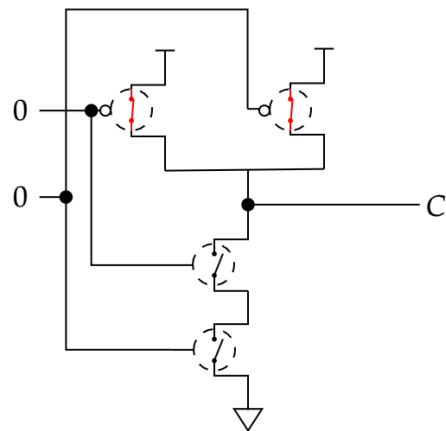
In CMOS, there must be both a PUN and PDN, think about how to balance the (2), from the above Theorem (1.5), to create a NAND gate.

**Theorem 1.6: CMOS Logic Gate – NAND**

Combining both networks in Theorem (1.5) yields a NAND gate in the following configuration:



$A$	$B$	$C$
0	0	1
0	1	1
1	0	1
1	1	0



$A$	$B$	$C$
<b>0</b>	<b>0</b>	<b>1</b>
0	1	1
1	0	1
1	1	0

Figure 1.16: Both inputs are (0,0), PUN closed, PDN open, hence the output is high (1).

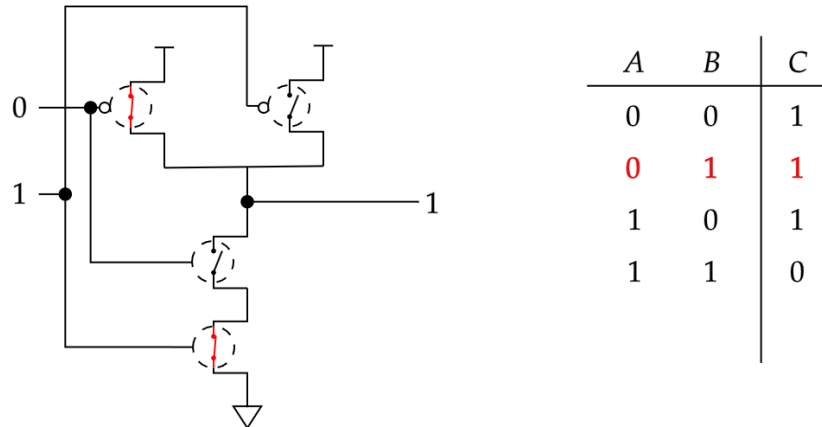


Figure 1.17: Both inputs are (0,1), PUN half-closed reaching the output, PDN half-closed, but can't reach the output; Hence the output is high (1).

## Bibliography

- [1] What is a transistor? YouTube video, <https://youtu.be/AwXp6jVaTV4?si=s4-UwlgglmiCBPso>, 2022.
- [2] CrashCourse. The nucleus: Crash course chemistry #1. YouTube video, [https://youtu.be/FSyAehMdpYI?si=h5ngW3IvcCTi0oL\\_](https://youtu.be/FSyAehMdpYI?si=h5ngW3IvcCTi0oL_), 2013. Published February 12, 2013.
- [3] EngMicroLectures. Building logic gates from MOSFET transistors. <https://youtu.be/1rZyGL1K5QI?si=ODgxP84kuHqVq6Bi>, ?? 2013. [Online; accessed 2025-07-13].
- [4] Getty Images. Getty Images Stock Photo 700832601. [https://www.thoughtco.com/thmb/TTC7l9oab0l\\_A2\\_xRPrYeoHSvXc=/2092x1433/filters:no\\_upscale\(\):max\\_bytes\(150000\):strip\\_icc\(\)/GettyImages-700832601-5bb602c0c9e77c002609fe08.jpg](https://www.thoughtco.com/thmb/TTC7l9oab0l_A2_xRPrYeoHSvXc=/2092x1433/filters:no_upscale():max_bytes(150000):strip_icc()/GettyImages-700832601-5bb602c0c9e77c002609fe08.jpg). Thumbnail image hosted on ThoughtCo via Getty Images. Accessed: 2025-07-07.
- [5] Infinity Learn. Concept of valency - introduction | atoms and molecules. YouTube video, August 2018. Accessed: 6 July 2025.
- [6] The Engineering Mindset. Mosfet explained - how mosfet works. YouTube video, [https://youtu.be/AwRJsze\\_9m4?si=whrgmMmzrychH2c](https://youtu.be/AwRJsze_9m4?si=whrgmMmzrychH2c), 2024.

- [7] Chris Terman. 6.004 computation structures, 2017. Undergraduate course, Spring 2017.
- [8] Wayne Breslyn (Dr. B.). Molecule vs compound: Examples and practice. YouTube video, 2013. Accessed: 6 July 2025.