

Figure 2 - Technology Schematic

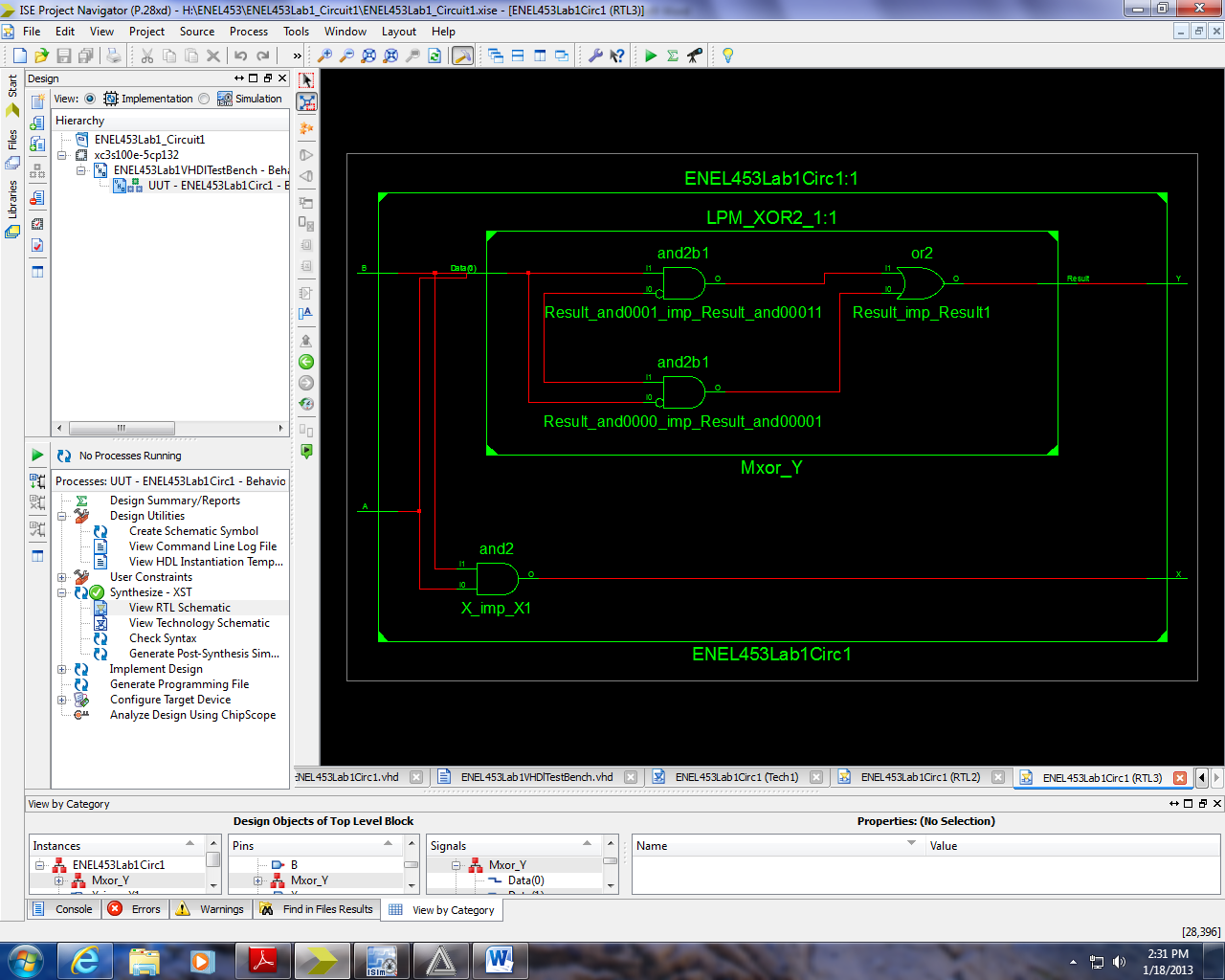


Figure 1 - RTL Schematic

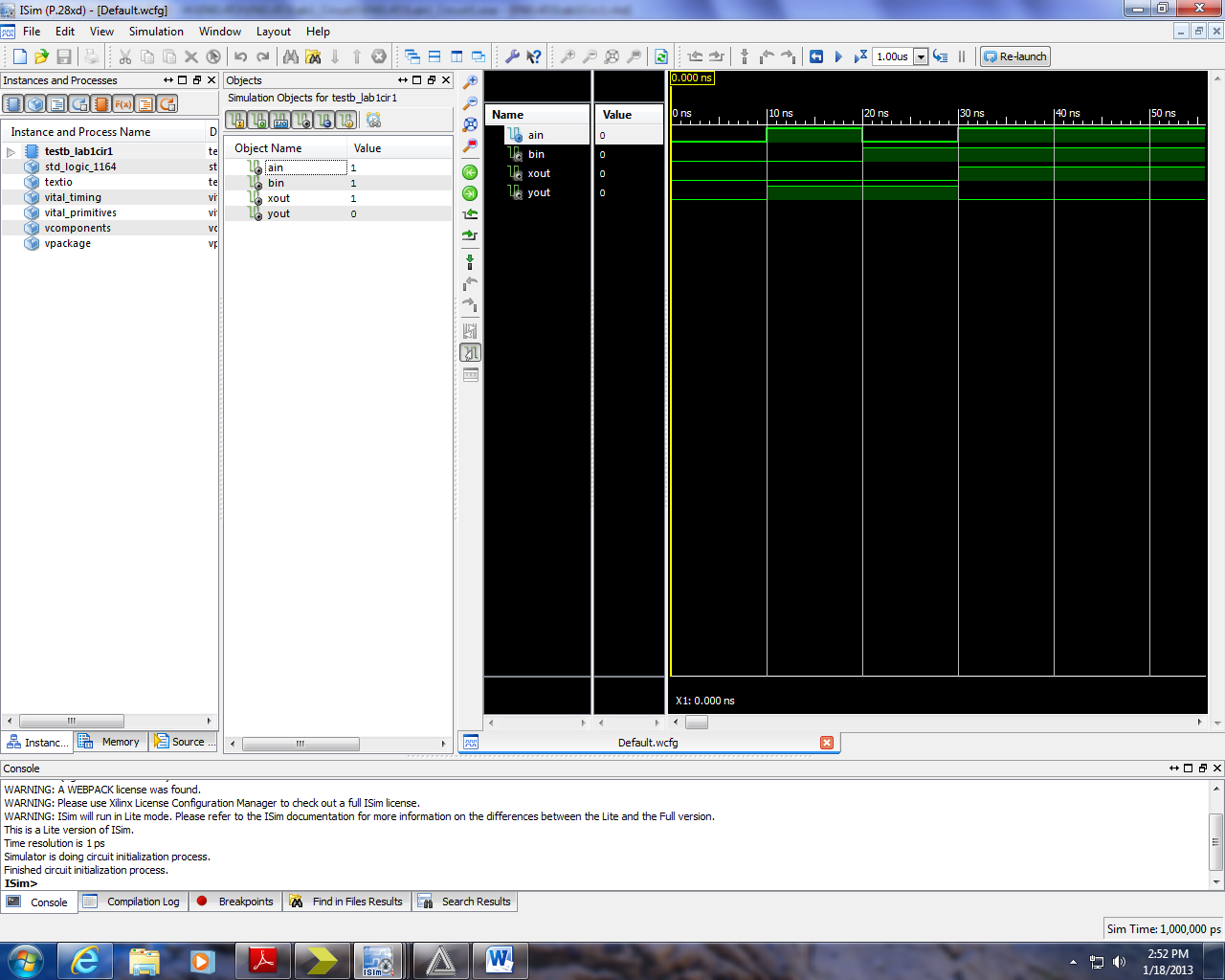


Figure 3 - Waveforms for Structure

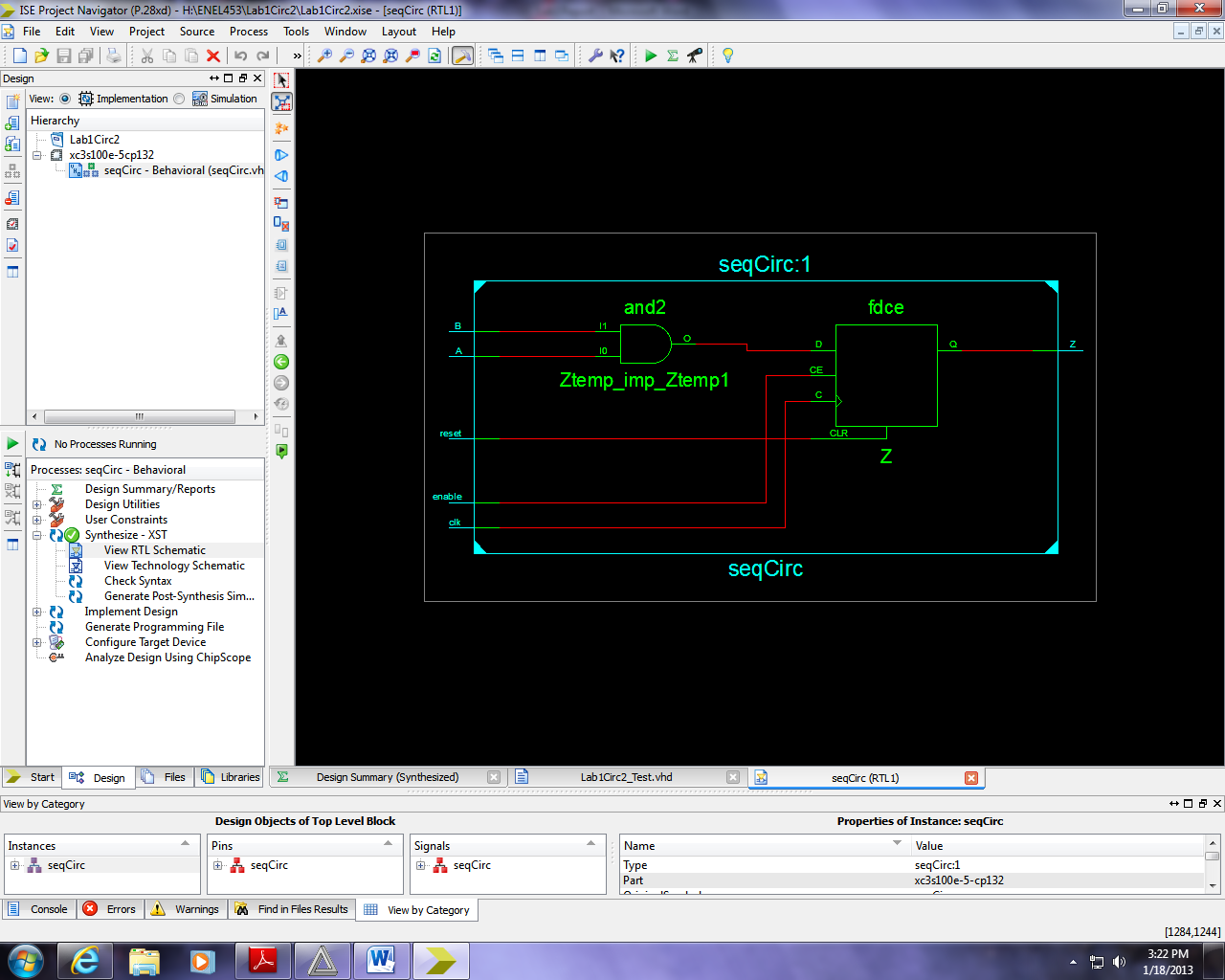


Figure - Sequential Circuit RTL Schematic

For the broken circuit, the reason that it shows an error when simulated with a value of:

*A <= ‘1’*

is due to the fact that the first line in the architecture is a concurrent statement setting the value of Y, whereas the process (sequential) is in contradiction to the concurrent statement resulting in an unknown value for the simulator.

Concurrent: *Y <= A and B; -- equals ‘0’ (1 and 0 = 0)*

Sequential: *Y <=A; -- equals ‘1’ (as A=’1’)*

When attempting to synthesize the circuit, an error stating that “multiple drivers” were present for the output signal, Y. This would appear to reinforce the above explanation as a correct diagnosis of the problem. (ie. Concurrent and Sequential Circuits are mixed together)