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| University of Calgary |
| ENEL 453 |
| **Laboratory #2: Building a Digital Clock for Generic Counters** |
| **Lab: B06** |
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| **2/5/2012** |

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| We declare that this laboratory report is entirely our own work and includes no material which has been copied from any other source excepting that material which is clearly identified as the work of others. |

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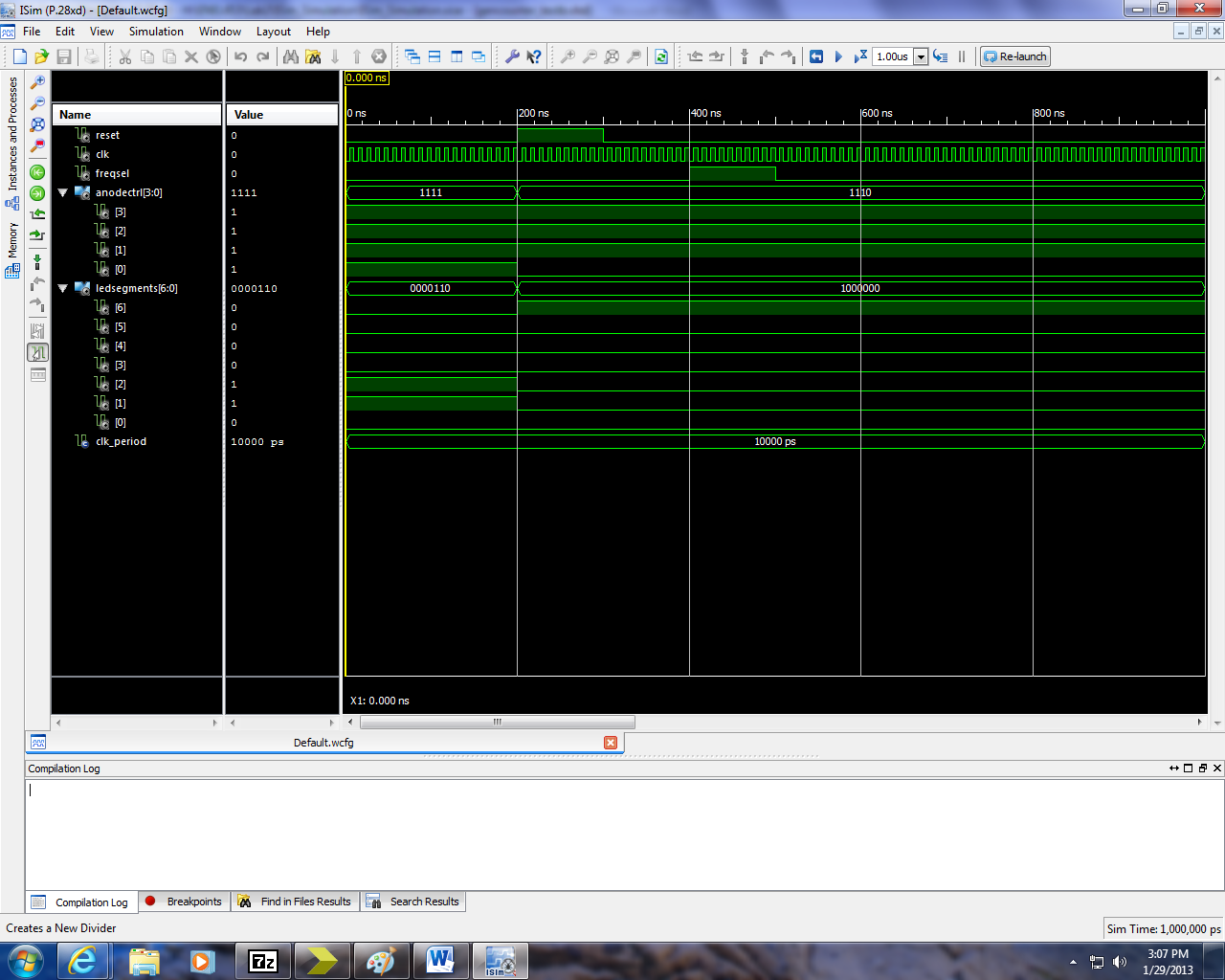
**Prelab: VHDL Code and Testbench Suites**

All VHDL code files and testbench Files are included in the folder associated with this report.

**Lab: Simulation Results**

**3.1**

After simulating the behavioural description of the code and running the circuit the following waveform was observed.



As can be seen, all values appear to be running, but as it is a clock circuit, and this simulation only runs on the scale of ns, it was a bit too impractical to run the simulator long enough to elicit a functional response for the LCD screen signals.

**3.2**

**a)** The reason that the signal q\_int was used instead of the original q port is because the original q signal was just a std\_logic\_vector, and is not capable of doing plain arithmetic so by creating and casting a new signal as unsigned it can perform the calculations required. The reason only two flip-flops were generated was due to the fact that the vector was only in need of 2 bits.

**b)** **Warning Messages:**

*WARNING:Xst:753 - "//engfs.eng.ad.ucalgary.ca/home/kderbyma/ENEL453/Lab2/Clockdivider.vhd" line 47: Unconnected output port 'q' of component 'gencounter'.*

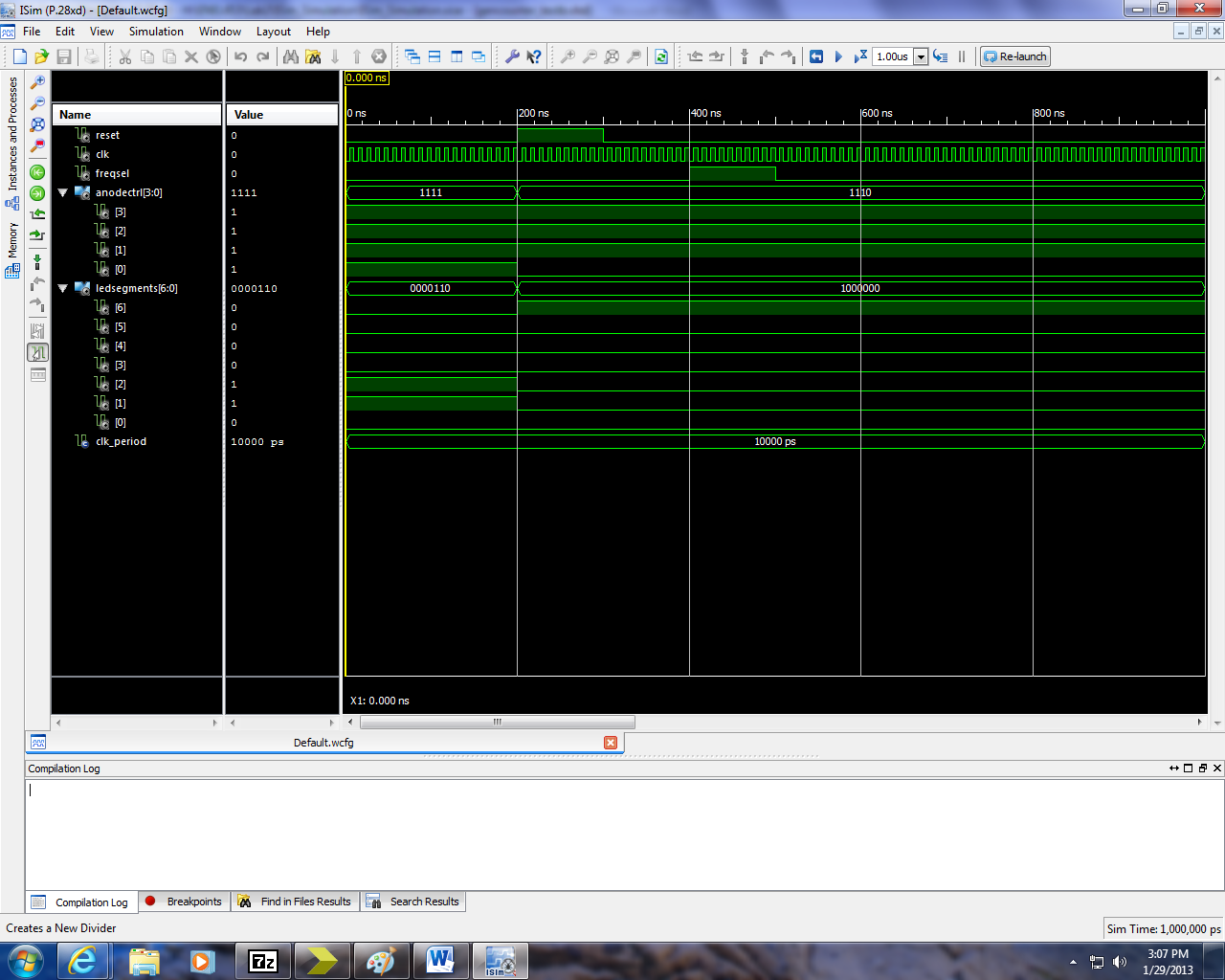
*WARNING:Xst:753 - "//engfs.eng.ad.ucalgary.ca/home/kderbyma/ENEL453/Lab2/Clockdivider.vhd" line 53: Unconnected output port 'q' of component 'gencounter'.*

*WARNING:Xst:753 - "//engfs.eng.ad.ucalgary.ca/home/kderbyma/ENEL453/Lab2/Clockdivider.vhd" line 53: Unconnected output port 'q' of component 'gencounter'.*

The warning messages are just stating that that one of the ports on a component being used is not connected to anything. It is not serious but a useful message in case of debugging.

**c) - f)** All simulated circuits diagrams are located in the screenshots folder associated with this report. Only the diagrams requested in the lab report have been added to this document.

**g)** After running the simulation on the post-translate model, the following waveforms were observed:



**h)** After compiling and programming our FPGA, our circuit worked as was expected and the counter and clock functionality were observed and demonstrated.

**Part 4: Additional Questions**

1. In VHDL, an entity is a declarative piece of code which outlines the interface for what is effectively a circuit or sub-circuit. It describes the pins (ie. Inputs and output signals) for the circuit and any additional generic parameters. Along with an entity is its corresponding architecture description which outlines its operation.

A component is a way of implementing other circuits/subcircuits into your design. It is effectively a way to import other entities and use them in your code, and it is similar to other OOP (Object-Oriented Programming) concepts.

An instance is similar to a clone of a component. It is a component whose only differentiable feature is usually its label. It is just a way of making copies and being capable of maintaining them individually when more than one of the same component may be needed at once.

1. Generic parameters are just means of passing values and information into an entity. Sort of like a constant in other programming languages. It may be used to perform arithmetic calculations or to describe system parameters such as which frequency to act on.
2. The reason that arithmetic operations aren’t defined for the *std\_logic\_vector* type is because in order to perform calculations the value within the vector must have some context. It must be casted so that the FPGA can know which type of arithmetic to perform (ie, sign or unsigned). Prior to being casted, the vector is merely seen as a blank container which could contain very different results depending on which type of data it carries.

The reason that the code has a logical error is due to the numbers being signed integers. This results in a potential overflow problem due to a potential carry-over into the sign-bit. If it was unsigned, it would not have any logical problems associated with it, rather just potentially have regular overflow, but that would still be available via the carry-bit.

1. Division is not something which can be implemented into a circuit on the fly, rather it would either need to have values pre-tabulated or be implemented specifically for each circuit as it is not a simple digital operation.
2. Based on the report and the simple fact that an FPGA is ultimately constrained in size it would appear that size would be in terms of LUT’s, Logic Gates, MUX’s etc. Since the FPGA is prebuilt it has a limited number of components built in, so all in all the complexity of the logic involved requires more physical space consequently.
3. In order to change the circuit so as to add the capability of displaying hours all you would have to do is to adjust the min60sec60 code and have it also count for hours and then have all the signals go into a MUX which can either choose to output MM:SS or HH:MM based on the position of an addition switch.
4. You could adjust the entity by adding a generic parameter “clkFreq” and then having the code instead implement the first divisor (“*div25:* *gencounter*”) by having it pass on the clkFreq value for which to originally divide the clock by.
5. The reason they are multiplexed in because it allows for simple control and flexibility. Each display panel also requires its own signal vector in order to properly display so by multiplexing the signals you can ensure they get loaded at same time and thus display correctly, also you can choose which order and which panels to use the display with. The reason that the panel was set to a frequency of 1kHz is to ensure that the panels are updated much more frequently than is truly necessary. Since the clock only responds are 1Hz and 10Hz having it cycle through them all with a much higher frequency means no noticeable discontinuities with the timing. Since the segment is MUX’d it would appear that each panel would get refreshed 250 times a second.