

Prof.(Dr.) Kunal Kishore Korgaonkar
Lead Researcher - ‘Confluences of Computing’ Lab
Asst. Professor - CSIS Department, BITS Pilani, Goa Campus, India
Postdoc (Technion, Israel), PhD (UC San Diego, US), MS (IIT Madras, India)

Webpages: <https://www.bits-pilani.ac.in/goa/kunal-kishore-korgaonkar/>, <http://cseweb.ucsd.edu/~kkorgaon>;

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Area of Interest

A big focus of the ‘Confluence lab’ is on exploring and unearthing novel computing paradigms that connect end-application and end-user needs with the capabilities of emerging computing technologies, architectures, and systems. The lab especially focuses on the impact of technology on health, education, safety and other key socio-economic developmental aspects of society.

Our research work therefore spans diverse topics in computer science and systems engineering and related fields, spanning topics such as: scalable software and hardware architectures, systems of machine learning and data science, secure and trustworthy systems, data-centric systems, dependable and sustainable systems, democratization of computing, and socio-technological development.

The overarching goal of confluence lab is in “building” computer systems, algorithms, and solutions, at all scales, such that they are exceedingly intelligent, trustworthy, efficient and usable.

Education

- **University of California San Diego (UCSD)**, California, USA 2012 - 2018
Doctor of Philosophy (PhD), Computer Science and Engineering (Defence: May 2019)
[\[CGPA: 9.33/10\]](#)
Thesis title: Building Scalable Architectures using Emerging Memory Technologies
Advisor: Prof. Steven Swanson
[Mentors: Jishen Zhao, Dean Tullsen, Leo Porter, George Porter, Geoff Volker]
- **Indian Institute of Technology Madras (IITM)**, Chennai, India 2008 - 2010
Masters of Science (MS), Computer Science and Engineering
[\[CGPA: 9.6/10\]](#)
Thesis title: Reconstructing Transactional Memory for Workload Optimized Systems
Advisor: Prof. V. Kamakoti
[Mentors: Shankar Balachandran, Madhu Mutyam]
- **Goa Engineering College (GEC)**, Goa, India 2001 - 2005
Bachelor of Engineering (BE), Computer Science and Engineering

Academic Achievements and Fellowships

- **OPERA Award - For Research and Teaching** - CSIS, BITS Pilani, Goa Campus, India (2022-2027)
- **Lady Davis Postdoctoral Fellowship in Israel** - EE/CS, Technion, Israel (2020 - 2021)
- **Semiconductor Research Cooperation Fellowship in US** - CSE, UCSD, USA (2012-2019)
- **Technion Visiting Scholar & Postdoctoral Fellowship** - EE/CS, Technion, Israel (2018 - 2020)
- **UC San Diego PhD Fellowship** - CSE, UCSD, USA (2012-2019)
- **IITM-Intel Joint MS Fellowship Award** - Intel’s University Research Program (2008-2010)
- **Admits and Fellowships to IISC/IITK/IITM - For their MS in CS Programs**
- **In top 250 Computer Science Aptitude Test (GATE exam)** - Country-wide Merit List
- **In top 20 in Physics, Chemistry and Math Tests** - State-wide Merit List
- **In top 100 in School Board** - State-wide Merit List

Research and Engineering Positions

- **Assistant Professor, BITS Pilani [Goa Campus, India] [Regular, Full-time]** 2022 onwards
Computer Science and Information Systems Department
Lead Researcher of “Confluences of Computing” Lab
Working on all aspects of ‘Computer System Design and Implementation’
[Collaborators: Vinayak Naik, Arnab Paul, Snehanishu Saha, Ramprasad Joshi]
- **Postdoctoral Research Fellow, Technion [Haifa, Israel] [Regular, Full-time]** 2018 - 2021
EE/CS Department, Israel
Architectural and algorithmic implications of fusing compute and memory.
[Collaborators: S. Kvatinsky, M. Silberstein, A. Mendelson, I. Keider, H. Attiya]
- **Researcher & Architect, Intel**
Intel Labs [Bangalore, India] [Internship] (07-12) 2016
Micro-architecture and Memory Hierarchy Research Team
Revisiting on-chip caching in wake of new memory technologies.
[Mentors: Sreenivas Subramoney, Jayesh Gaur, Ishwar Bhati, Tanay Karnik]
Intel Products [Oregon, US] [Internship] (07-09) 2014
Intel Binary Translation Team
Workload characterization and optimization for heterogeneous platforms.
[Mentors: Karthik Sankaranarayanan, Suresh Srinivas]
- **Researcher, AMD Research [Austin, US] [Internship]** (07-09) 2015
Exascale High-Performance Computing Team
Heterogeneous system memory coherence and new memory interfaces.
[Mentors: Brad Beckmann, Sooraj Puthoor, David Roberts]
- **Researcher, IBM Research Labs [Bangalore, India] [Regular, Full-time]** 2010 - 2012
Network Processing Team
Architectural exploration and performance analysis of on-chip accelerators.
[Collaborators: Shivkumar Kalyanaraman, Ravi Kokku, Malolan Chetlur]
- **Systems Programmer, DG2L Technologies [Pune, India] [Regular, Full-time]** 2006 - 2008
A deep-tech start-up (Got acquired!)
Embedded Products Division
Developing OS/IO abstraction libraries for embedded system-on-chip.
- **Systems Engineer, National Stock Exchange [Mumbai, India] [Regular, Full-time]** 2005 - 2006
Data Center Scaling and Management Team
Ensuring performance and scalability of online trading software and hardware.

Publications

- Evaluating Infrastructure as Code: Key Metrics and Performance Benchmarks;
Aditya Gupta, Paras Mittal, **Kunal Korgaonkar**;
HotInfra Workshop, Symposium on Operating Systems Principles (SOSP) 2024;
- **Kunal Korgaonkar** and many authors;
Validation of a point-of-care Artificial Intelligence (AI)-based screening tool for oral cancer, India
BMC Public Health 2024 (under submission)
- Videet Acharya, Nakul Bhachawat, **Kunal Korgaonkar**;
Expand-Map-Reduce: A Elementary Framework for Understanding Quantum Algorithms;
HiPCW, IEEE 31st International Conf. on High Perf. Computing, Data and Analytics Workshop, 2024
<https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10898624>
- Ria Khatoniar, Vishu Vyas, Videet Acharya, Amit Saxena, **Kunal Korgaonkar**;
Quantum Convolutional Neural Network for Medical Image Classification: A Hybrid Model;
TQCEBT, IEEE International Conf. on Trends in Quantum Computing & Emerging Business Tech. 2024
<https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=10545121>
- Towards Mutable Smart Contracts in a Blockchain;
Aishwarya Parab, Pranay Nandan Varshney, Nirmal Govindaraj, **Kunal Korgaonkar**, Arnab Paul;
HiPC 2023 Student Research Symposium (HiPC SRS 2023)

- S Sai Vineet, Natasha Meena Joseph, **Kunal Korgaonkar**, Arnab K. Paul;
A Data-Centric Approach for Analyzing Large-Scale Deep Learning Applications;
ICDCN, International Conference on Distributed Computing and Networking, 2023
[\[Top Systems and Networking Event\]](#)
<https://dl.acm.org/doi/abs/10.1145/3571306.3571414>
- Natasha Meena Joseph, S Sai Vineet, **Kunal Korgaonkar**, Arnab K. Paul;
Characteristics of Deep Learning Workloads in Industry, Academic Institutions and National Laboratories;
ICDCN, International Conference on Distributed Computing and Networking, 2023
[\[Top Systems and Networking Event\]](#)
<https://dl.acm.org/doi/abs/10.1145/3571306.3571428>
- R. Ronen, A. Eliahu, N. Peled, O. Leitersdorf, **K. Korgaonkar**, A. Chattopadhyay, B. Perach, S. Kvatinsky;
The Bitlet Model: A Parameterized Analytical Model to Compare PIM and CPU Systems;
JETC ACM Journal on Emerging Technologies in Computing Systems 2021
[\[Top Journal\]](#)
<https://dl.acm.org/doi/full/10.1145/3465371>
- **K. Korgaonkar**, R. Ronen, A. Chattopadhyay, S. Kvatinsky;
A Deluge of Processing-in-Memory Frameworks and How Analytical Modeling Could Help!;
NVMW (Non-Volatile Memories Workshop) 2020
<http://cseweb.ucsd.edu/~kkorgaon/papers/nvmw-2020-deluge-Of-PIM.pdf>
- **K. Korgaonkar**, R. Ronen, A. Chattopadhyay, S. Kvatinsky;
The Bitlet Model: Defining a Litmus Test for the Bitwise Processing-in-Memory Paradigm;
CATC (Compilers Architecture and Tools Conference) 2019
<https://software.intel.com/sites/default/files/managed/3b/a6/session3-talk3.pdf>
- **K. Korgaonkar**, J. Izraelevitz, J. Zhao, S. Swanson;
Vorpai: Vector Clock-Inspired Ordering For Large Persistent Memory Systems;
PODC (Principles of Distributed Computing Conference) 2019
[\[Top Conference\]](#) [\[Acceptance rate: 29%\]](#)
<https://dl.acm.org/doi/abs/10.1145/3293611.3331598>
- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, S. Swanson, I. A. Young, H. Wang;
To Cache Or To Bypass? A Fine Balance For Emerging Mem. Tech. Era;
NVMW (Non-Volatile Memories Workshop) 2019
<http://cseweb.ucsd.edu/~kkorgaon/papers/nvmw-2019-high-density-caches.pdf>
- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, S. Swanson, I. A. Young, H. Wang;
Density Tradeoffs of NVM as a Replacement for SRAM LLCs;
ISCA (International Symposium on Computer Architecture Conference) 2018
[\[Top Conference\]](#) [\[Top Journal \(SIGARCH\)\]](#) [\[Acceptance rate: 17%\]](#)
<https://ieeexplore.ieee.org/document/8416837>
- **K. Korgaonkar**, Shelby Thomas;
Granular Computing: Blending Terabit Network with Terabyte Main Memories;
ARM Research (ARM Industry-Academia Research Forum) 2018
<http://cseweb.ucsd.edu/~kkorgaon/papers/arm-research-2018-granular-computing.pdf>
- S. Patil, Y. Kim, **K. Korgaonkar**, I. Awwal, T. Rosing;
Characterization of User's Behavior Variations for Design of Replayable Mobile Workloads;
MobiCase (Mobile Computing, Applications, and Services Conference) 2015
[\[Top Conference\]](#) [\[Acceptance rate: 37%\]](#)
https://link.springer.com/chapter/10.1007/978-3-319-29003-4_4

- **K. Korgaonkar**, K. Sankaranarayanan, S. Srinivas;
CPU or GPU Bound?: In-Depth Case-Studies of Mobile Gaming Workloads;
Intel Technical Report (Intel Internal Report) 2014
[\[Industry Impact\]](#)
- A. Gautham, **K. Korgaonkar**, Patanjali S., S. Balachandran and V. Kamakoti;
Implications of Shared-Data Synchronization Techniques on Multi-Core Energy Efficiency;
HotPower (Workshop on Power-Aware Computing and Systems) 2012
[\[Top Usenix Event\]](#) [\[Acceptance rate: 25%\]](#)
<https://www.usenix.org/conference/hotpower12/workshop-program/presentation/gautham>
- **K. Korgaonkar**, Kashyap G. and V. Kamakoti;
Size-proportional signature sharing for transactional memory systems;
FASPP (Workshop on Future Architecture Support for Parallel Programming) 2012
<http://cseweb.ucsd.edu/~kkorgaon/papers/faspp-2012-sizeprop-signature-for-tm.pdf>
- **K. Korgaonkar**, P. Jain, D. Tomar, K. Garimella and V. Kamakoti;
Reconstructing hardware transactional memory for workload optimized systems;
APPT (Advanced Parallel Processing Technologies Symposium) 2011
https://link.springer.com/chapter/10.1007/978-3-642-24151-2_1
- **K. Korgaonkar** and V. Kamakoti;
Thread synchronization: from mutual exclusion to transactional memory;
IETE Review (The Institution of Electronics and Telecommunications Engineer Review) 2011
<https://www.tandfonline.com/doi/abs/10.4103/0256-4602.83551>
- **K. Korgaonkar**, G. Kurian, M. Gautam and V. Kamakoti;
HTM Design Spaces: Complete Decoupling from Caches;
OSR Operating Systems Review (Position Paper) 2009
<https://dl.acm.org/doi/10.1145/1531793.1531809>

Patents

- **Kunal Korgaonkar**, Ashwin Prabhakaran, Marlon Vaz;
A Mechanism for producing tilting and rotational motion in robotic arm;
[Indian patent - 202411096073]
- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, H. Wang, I. A Young;
Reducing write congestion in non-volatile memory based last level caches
[US Patent App. 15/475,197]
- I. Bhati, H. Liu, J. Gaur, **K. Korgaonkar**, S. Manipatruni, S. Subramoney, T. Karnik, H. Wang, I. Young;
Write congestion aware bypass for non-volatile memory
[US Patent 10,331,582]
- A. Ambati, **K. Korgaonkar**, M. Madhavan, R. Polavarapu; Smart Communications for Power Consumption Information
[US Patent App. 13/213,254]
- V. Arya, M. Chetlur, P. Dutta, S. Kalyanaraman, **K. Korgaonkar**, R. Polavarapu; Optimizing streaming a group of videos
[US Patent 9,037,742, US Patent 9,060,205]
- M Chetlur, U Devi, S Kalyanaraman, R Kokku, **K Korgaonkar**; Incremental preparation of videos for delivery
[US Patent 9,152,220]

Funding and Grants

- Government of India, PoC for Point of care Screening Tool for Oral Cance, AICOE Grant 2023 onwards

■ ABCEL-BITS Cyber Security Grant	2025 onwards
■ BITS Pilani, Cross-Disiplinary Research Funding Grant	2023 onwards
■ Government of Goa, DTE Grant	2024 onwards
■ DST, BioCyTiH Funding Grant, under National BIO-CPS grant	2021 onwards
■ BITS Pilani, OPERA Award Grant	2021 onwards
■ Toshiba Emerging Memories Grant	2016 - 2019
■ Technion Cyber Security Center Grant	2018 - 2021
■ GenPro RISC-V Based Processing-In-Memory Emulation Israel Center Grant	2020 - 2021
■ Hyundia Capabilities Architectures for Predictable Performance Grant	2020 - 2021

Teaching Positions

■ Course Instructor for System Security (BITS-Goa Jan 2024)	
■ Course Instructor for Quantum Architecture and Programming (BITS-Goa Jan 2023)	
■ Course Instructor for Systems for ML/DS (BITS-Goa Jan 2023)	
■ Course Instructor for Principles of Programming Languages (BITS-Goa Aug 2022)	
■ Course Instructor for Quantum Architecture and Programming (BITS-Goa Jan 2022)	
■ Course Lab Instructor for Compiler Construction (BITS-Goa Jan 2022)	
■ Teaching Assistant for Computer Architecture Theory and Lab (UCSD CSE141/141L)	5 qtrs
■ Teaching Assistant for Embedded Systems (UCSD CSE 237A and WES 237B)	2 qtrs
■ Teaching Assistant for Computer Architecture and Verification (IITM CSE in 2009, 2010)	2 sems

Student Advising

- Videet Acharya, PhD (Ongoing) (Bits-Goa)
- Sabari Sreekumar, PhD (Ongoing) (Bits-Goa and ISRO, Bangalore)
- Rakesh Paul, PhD (Ongoing) (Bits-Goa)
- Sankar Menon, PhD (Ongoing) (Bits-Goa)
- Melissa Rodrigues, PhD (Ongoing) (Bits-Goa and Goa University)(Advising along with: Kavita Asnani)
- Aishwarya Parab, PhD (Ongoing) (Bits-Goa), (Advising along with: Arnab Paul)
- Gal Assa, PhD (Ongoing) (Technion) (Advising along with: Idit Keidar)
- Ashok Gautham, MS (Completed) (IITM) (Advising along with: Shankar Balachandran, V. Kamakoti)
- Nishil Talati, MS (Completed) (Technion) (Advising along with: Shahar Kvatinsky)
- And numerous undergraduate students from BITS-Goa, UCSD, IITM and Technion

Academic Service

- HiPC 2025 - Program Committee Member

- Nullcon 2025 - Co-Organizer
- ATS 2024 - Session Program Chair
- Indocrypt 2023 - Organizing Co-chair
- Nullcon 2023 - Co-Organizer and Reviewer
- Springer VLSI-SOC 20 - Book Editor
- IEEE VLSI-SOC 20 - Publication Chair
- ASPLOS 20, DAC 20, ISCAS 19, ICECS 19, DATE 18, DATE 15 - Reviewer