Dr. Kunal K. Korgaonkar

Assistant Professor (Tenure-Track)
Computer Science and Information Systems Department
BITS Pilani, Goa Campus, India

Postdoc (Technion, Israel), PhD (UC San Diego, US), MS (IIT Madras, India)

Webpages: https://www.bits-pilani.ac.in/goa/kunalk/profile, http://cseweb.ucsd.edu/~kkorgaon;
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Google Scholar: http://bit.ly/Kunal-GS **Linkedin**: http://bit.ly/Kunal-LN

Area of Interest

My overarching interest is in building computer systems that are exceedingly intelligent, trustworthy, usable and efficient, right from atomic all the way to planetary scale. My research work spans diverse topics in computer science and engineering, spanning topics such as computer architectures, hardware & software architectures, data-centric systems, dependable & sustainable systems, democratization of computing, and socio-technological development.

Education

- **University of California San Diego (UCSD)**, California, USA 2012 - 2018
  Doctor of Philosophy (PhD), Computer Science and Engineering (Defence: May 2019)
  [CGPA: 9.33/10]
  Thesis title: Building Scalable Architectures using Emerging Memory Technologies
  Advisor: Prof. Steven Swanson
  [Mentors: Jishen Zhao, Dean Tullsen, Tajana Rosing, Leo Porter, George Porter, Geoff Volker]
- **Indian Institute of Technology Madras (IITM)**, Chennai, India 2008 - 2010
  Masters of Science (MS), Computer Science and Engineering
  [CGPA: 9.6/10]
  Thesis title: Reconstructing Transactional Memory for Workload Optimized Systems
  Advisor: Prof. V. Kamakoti
  [Mentors: Shankar Balachandran, Madhu Mutyam]
- **Goa Engineering College (GEC)**, Goa, India 2001 - 2005
  Bachelor of Engineering (BE), Computer Science and Engineering

Academic Achievements and Fellowships

- **OPERA Award - For Research and Teaching** - BITS Pilani, Goa Campus, India (2022-2027)
- **Lady Davis Postdoctoral Fellowship in Israel** - EE/CS, Technion, Israel (2020 - 2021)
- **Semiconductor Research Coorporation Fellowship in US** - CSE, UCSD, USA (2012-2019)
- **Technion Visiting Scholar & Postdoctoral Fellowship** - EE/CS, Technion, Israel (2018 - 2020)
- **UC San Diego PhD Fellowship** - CSE, UCSD, USA (2012-2019)
- **IITM-Intel Joint MS Fellowship Award** - Intel's University Research Program (2008-2010)
- **Admits and Fellowships to IISC/IITK/IITM - For Master in CS Programs**
- **In top 250 Computer Science Aptitude Test (GATE exam)** - Country-wide Merit List
- **In top 20 in Physics, Chemistry and Math Tests** - State-wide Merit List
- **In top 100 in School Board** - State-wide Merit List

Employment History

- **Assistant Professor, BITS Pilani, Goa Campus** 2022 onwards
  [Full-time] [Goa, India]
  Tenure Track Position, Research and Teaching Role,
  Computer Science and Information Systems Department
  Research Topics: Computer Architecture, Data-centric and Dependable Systems, Programming Methodologies, 21st Century Education, etc.
  [Collaborators: Vinayak Naik, Biju Raveendran, Snehanshu Saha, Ramprasad Joshi, Arnab Paul, Swati Agarwal]

- **Postdoctoral Research Fellow, Technion** 2018 - 2021
  [Full-time] [Haifa, Israel]
  Plus, Visiting Scholar and Lady David Postdoctoral Fellowship
  EE/CS Department, Israel
  Architectural and algorithmic implications of fusing compute and memory.
  [Collaborators: S. Kvatinsky, M. Silberstein, A. Mendelson, I. Keider, H. Attiya]

- **Researcher and Computer Architect, Intel Labs** (07-12) 2016
  [Internship] [Bangalore, India]
  Micro-architecture and Memory Hierarchy Research Team
  Revisiting on-chip caching in wake of new memory technologies.
  [Mentors: Sreenivas Subramoney, Jayesh Gaur, Ishwar Bhati, Tanay Karnik]

- **Researcher, AMD Research** (07-09) 2015
  [Internship] [Austin, US]
  Exascale High-Performance Computing Team
  Heterogeneous system memory coherence and new memory interfaces.
  [Mentors: Brad Beckmann, Sooraj Puthoor, David Roberts]

- **Researcher and Computer Architect, Intel Products** (07-09) 2014
  [Internship] [Oregon, US]
  Intel Binary Translation Team
  Workload characterization and optimization for heterogeneous platforms.
  [Mentors: Karthik Sankaranarayanan, Suresh Srinivas]

- **Researcher and Software Engineer, IBM Research Labs** 2010 - 2012
  [Full-time] [Bangalore, India]
  Network Processing Team
  Architectural exploration and performance analysis of on-chip accelerators.
  [Collaborators: Shivkumar Kalyanaraman, Ravi Kokku, Malolan Chetlur]

- **Systems Programmer, DG2L Technologies** 2006 - 2008
  [Full-time] [Pune, India]
  A deep-tech start-up (Got acquired!)
  Embedded Products Division
  Developing OS/IO abstraction libraries for embedded system-on-chip.

- **Systems Engineer, National Stock Exchange** 2005 - 2006
  [Full-time] [Mumbai, India]
  Data Center Scaling and Management Team
  Ensuring performance and scalability of online trading software and hardware.

Publications

- R. Ronen, A Eliahu, N. Peled, O. Leitersdorf, **K. Korgaonkar**, A. Chattopadhyay, B. Perach, S. Kvatinsky;
  The Bitlet Model: A Parameterized Analytical Model to Compare PIM and CPU Systems;
  JETC ACM Journal on Emerging Technologies in Computing Systems 2021
  [Top Journal]
  `https://dl.acm.org/doi/full/10.1145/3465371`

- **K. Korgaonkar**, R. Ronen, A. Chattopadhyay, S. Kvatinsky;
  A Deluge of Processing-in-Memory Frameworks and How Analytical Modeling Could Help!;
  NVMW (Non-Volatile Memories Workshop) 2020
  `http://cseweb.ucsd.edu/~kkorgaon/papers/nvmw-2020-deluge-Of-PIM.pdf`

- **K. Korgaonkar**, R. Ronen, A. Chattopadhyay, S. Kvatinsky;
  The Bitlet Model: Defining a Litmus Test for the Bitwise Processing-in-Memory Paradigm;
  CATC (Compilers Architecture and Tools Conference) 2019
  https://software.intel.com/sites/default/files/managed/3b/a6/session3-talk3.pdf

- **K. Korgaonkar**, J. Izraelevitz, J. Zhao, S. Swanson;
  Vorpal: Vector Clock-Inspired Ordering For Large Persistent Memory Systems;
  PODC (Principles of Distributed Computing Conference) 2019
  [Top Conference] [Acceptance rate: 29%]
  https://dl.acm.org/doi/abs/10.1145/3293611.3331598

- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, S. Swanson, I. A. Young, H. Wang;
  To Cache Or To Bypass? A Fine Balance For Emerging Mem. Tech. Era;
  NVMW (Non-Volatile Memories Workshop) 2019
  http://cseweb.ucsd.edu/~kkorgaon/papers/nvmw-2019-high-density-caches.pdf

- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, S. Swanson, I. A. Young, H. Wang;
  Density Tradeoffs of NVM as a Replacement for SRAM LLCs;
  ISCA (International Symposium on Computer Architecture Conference) 2018
  [Top Conference] [Top Journal (SIGARCH)] [Acceptance rate: 17%]
  https://ieeexplore.ieee.org/document/8416837

- **K. Korgaonkar**, Shelby Thomas;
  Granular Computing: Blending Terabit Network with Terabyte Main Memories;
  ARM Research (ARM Industry-Academia Research Forum) 2018
  http://cseweb.ucsd.edu/~kkorgaon/papers/arm-research-2018-granular-computing.pdf

- S. Patil, Y. Kim, **K. Korgaonkar**, I. Awwal, T. Rosing;
  Characterization of User's Behavior Variations for Design of Replayable Mobile Workloads;
  MobiCase (Mobile Computing, Applications, and Services Conference) 2015
  [Top Conference] [Acceptance rate: 37%]
  https://link.springer.com/chapter/10.1007/978-3-319-29003-4_4

- **K. Korgaonkar**, K. Sankaranarayanan, S. Srinivas;
  CPU or GPU Bound?: In-Depth Case-Studies of Mobile Gaming Workloads;
  Intel Technical Report (Intel Internal Report) 2014
  [Industry Impact]

- A. Gautham, **K. Korgaonkar**, Patanjali S., S. Balachandran and V. Kamakoti;
  Implications of Shared-Data Synchronization Techniques on Multi-Core Energy Efficiency;
  HotPower (Workshop on Power-Aware Computing and Systems) 2012
  [Top Usenix Event] [Acceptance rate: 25%]
  https://www.usenix.org/conference/hotpower12/workshop-program/presentation/gautham

- **K. Korgaonkar**, Kashyap G. and V. Kamakoti;
  Size-proportional signature sharing for transactional memory systems;
  FASPP (Workshop on Future Architecture Support for Parallel Programming) 2012
  http://cseweb.ucsd.edu/~kkorgaon/papers/faspp-2012-sizeprop-signature-for-tm.pdf

- **K. Korgaonkar**, P. Jain, D. Tomar, K. Garimella and V. Kamakoti;
  Reconstructing hardware transactional memory for workload optimized systems;
  APPT (Advanced Parallel Processing Technologies Symposium) 2011
  https://link.springer.com/chapter/10.1007/978-3-642-24151-2_1

- **K. Korgaonkar** and V. Kamakoti;
  Thread synchronization: from mutual exclusion to transactional memory;
  IETE Review (The Institution of Electronics and Telecommunications Engineer Review) 2011
  https://www.tandfonline.com/doi/abs/10.4103/0256-4602.83551

- **K. Korgaonkar**, G. Kurian, M. Gautam and V. Kamakoti;
  HTM Design Spaces: Complete Decoupling from Caches;
  OSR Operating Systems Review (Position Paper) 2009
  https://dl.acm.org/doi/10.1145/1531793.1531809

Patents

- **K. Korgaonkar**, I. Bhati, H. Liu, J. Gaur, S. Manipatruni, S. Subramoney, T. Karnik, H. Wang, I. A Young; Reducing write congestion in non-volatile memory based last level caches
  [US Patent App. 15/475,197]

- I. Bhati, H. Liu, J. Gaur, **K. Korgaonkar**, S. Manipatruni, S. Subramoney, T. Karnik, H. Wang, I. Young; Write congestion aware bypass for non-volatile memory
  [US Patent 10,331,582]

- A. Ambati, **K. Korgaonkar**, M. Madhavan, R. Polavarapu; Smart Communications for Power Consumption Information
  [US Patent App. 13/213,254]

- V. Arya, M. Chetlur, P. Dutta, S. Kalyanaraman, **K. Korgaonkar**, R. Polavarapu; Optimizing streaming a group of videos
  [US Patent 9,037,742, US Patent 9,060,205]

- M Chetlur, U Devi, S Kalyanaraman, R Kokku, **K Korgaonkar**; Incremental preparation of videos for delivery
  [US Patent 9,152,220]

Teaching Roles and Courses Delivered

- Course Instructor for Quantum Architecture and Programming (BITS-Goa, Jan 2022) — 1 sem
- Course Lab Instructor for Compiler Construction (BITS-Goa, Jan 2022) — 1 sem
- Teaching Assistant for Computer Architecture Theory and Lab (UCSD CSE141/141L) — 5 qtrs
- Teaching Assistant for Embedded Systems (UCSD CSE 237A and WES 237B) — 2 qtrs
- Teaching Assistant for Computer Architecture and Verification (IITM CSE in 2009, 2010) — 2 sems

Student Advising

- MS (IIT), Ashok Gautham (Advisor: Shankar Balachandran, V. Kamakoti)
- MS (Technion), Nishil Talati (Advisor: Shahar Kvatinsky)
- PhD (Technion), Gal Assa (Advisor: Idit Keidar)
- And numerous undergraduate students from IITM, UCSD, Technion and BITS-Goa

Academic Service

- Book Editor for Springer VLSI-SOC in 2020
- Publication Chair for VLSI-SOC in 2020
- Reviewer for ASPLOS, DAC in 2020
- Reviewer for ISCAS, ICECS in 2019
- Reviewer for DATE in 2018
- Reviewer for DATE in 2015

References

- Prof. V. Kamakoti
  Director of Institute &
  Full Professor, Computer Science and Engineering Department
  IIT Madras, Chennai, India
  kama@cse.iitm.ac.in

- Prof. Steven Swanson
  Director of NVSL &
  Full Professor, Computer Science and Engineering Department
  UC San Diego, California, USA
  swanson@cs.ucsd.edu