



Revision History

Rev 5.0.1 – Remove PG8 control of U4; swap pins of Bat1 footprint
Rev 5.0.2 – Add physical connection to unused pins of U5
Rev 5.0.4 – Add connection from AXP209 (pin 48) to P1–8 (IRQ to NEO)
Rev 5.0.5 – Add C16 (noise filter for IRQ)
Rev 5.0.6 – Add time delay from AXP209 to FET Switch; add test points
Rev 5.0.7 – Add R12 pull down on PG11 to set pedigree
Rev 5.0.8 – Mounting holes went missing in 5.0.7, added back in 5.0.8
Rev 5.0.9 – Change P4 to TH mount, SMD electrical; changes layout only

Orders

5.0.0 – Boards ordered from PCBWay –
11/03/18
5.0.2 – Boards ordered from PCBWay –
12/06/18
5.0.4 – Order boards from PCBWay
for 100 unit build

TO DETERMINE BOARD PEDIGREE (from cli.py):

– Is PA6 HIGH?
Y => HAT connected; L => no HAT
– Is AXP209 present (via i2c)?
Y => Q3Y2018 or later;
Is PA1 HIGH (with NEO soft pull low on PA1)?
Y => Q3Y2018, N => Q4Y2018
N => (test for display)
Is OLED present (via i2c)?
Y => Q4Y2019; N => Q1Y2018

Sheet: /Notes/
File: HAT_ver_5.1-p3.sch

Title: ConnectBox HAT

Size: USLetter Date: 2019-10-19
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