Radiation Hardness Performance of 2 Gbit LPDDR SDRAM Fabricated on Epitaxial Wafer for Space Applications

Mi Young Park, Jang–Soo Chae, Chol Lee, Jungsu Lee, Im Hyu Shin, and Sinae Ji

***Abstract*-- Radiation hardness performance of 2 Gbit low-power double data rate synchronous dynamic random access memories (LPDDR SDRAMs) fabricated on a 4 μm epitaxial layer (38 nm CMOS technology) are presented.**

I. Introduction

The Satellite Technology Research Center (SaTReC) at the Korea Advanced Institute of Science and Technology (KAIST) is developing high density low-power double data rate synchronous dynamic random access memory (LPDDR SDRAM) modules with 3-dimensional bare die stacks of several LPDDR SDRAM chips for space applications.

The space products have radiation hardness requirements for the total ionizing dose (TID) effect and single event effects (SEEs). Because the TID effect and SEEs data never been reported, the survey for radiation-immune LPDDR SDRAM candidates and an analysis of the radiation characteristics of those candidates must be preceded.

The SaTReC chose 2 Gbit LPDDR SDRAMs fabricated on a 4 μm epitaxial layer from SK Hynix as a unit chips for space qualified high density LPDDR SDRAM modules and analyzed for their radiation hardness characteristics. This paper shows heavy-ion-induced SEEs with a primary emphasis on single event latch-up (SEL), single event functional interrupt (SEFI), single event upset (SEU), and burst error and presents γ-ray induced TID data for 2 Gbit LPDDR SDRAMs fabricated on a 4 μm epitaxial layer from SK Hynix.

II. Device under Test (DUT) Preparation

Table 1 and Fig. 1 show the details of the DUT [2]. The DUTs were prepared without epoxy mold compound as shown in Fig. 1 such that the heavy-ion can penetrate deep enough into the active region of the DUT with sufficient LET to capture all mechanisms that can lead to SEEs [3].

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TABLE I
DETAILS OF DUT

	Description
Part number	H5MS2G62
Manufacturer	SK Hynix
Type	LPDDR SDRAM
Technology	38nm CMOS
Density	2 Gbit (4 banks × 32 Mbit × 16 I/O)
Power supply	V_{DD}=V_{DDQ}=1.70~1.95 V
Interface	LVCMOS 1.8V

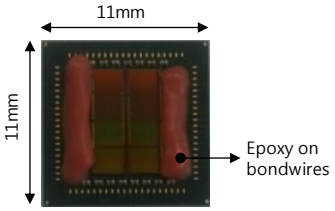

Fig. 1. DUT preparation

TABLE 2
TAMU ION COCKTAIL

Ion	Energy (Mev/u)	Range (μm)	Incidence angle (deg.)	Effective LET (MeVcm²/mg)
N	15	391.6	0	1.3
Ne	15	279.4	0	2.7
Ar	15	192.1	0	8.3
Cu	15	135.5	0	19.6
Ag	15	119.3	0	42.2
Pr	15	117.5	0	58.3
	15	105.6	26	64.9
Ho	15	119.5	0	69.1
Ta	15	118.6	0	77.3
Au	15	118.1	0	85.4

TABLE 3
IRRADIATION CONDITION FOR TID TEST

Sample #	TID (krad(Si))	Dose rate (krad(Si)/h)	Test mode
1	172	28.7	Operated
2	198	33.0	Unbiased

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III. Test Facility

A. Heavy-ion-induced SEE Test Facility

The heavy-ion-induced SEE test was conducted at the Radiation Effects Facility at the Cyclotron Institute in Texas A&M University [4]. The properties of the heavy ion beams used in our experiments are shown in Table 2.

B. γ-Ray Induced TID Test Facility

The Co-60 gamma source for low level gamma irradiation of the Korea Atomic Energy Research Institute (KAERI) was used for the TID test. The irradiation conditions for the TID test are shown in Table 3.

IV. Test Description

A. Heavy-ion-induced SEE Test

To detect SEFI, SEU, and burst error cross section versus heavy ion energy, and to characterize the SEL threshold heavy ion energy, both functional testing and current monitoring were performed. Also, examination of memory error maps, reinitialization of the DUT, and recycling the power supply were carefully performed to distinguish SEL from SEU, SEFI, burst error, and so forth.

The functional tests were performed at a clock frequency of 133 MHz with normal bias setting (V_{DD} = V_{DDQ} = 1.8 V). The entire memory device was tested using a checkerboard pattern (a logical series of ones and zeros), and dynamic tests were performed. The test flow was as follows [5]:

1) Write DUT with a checkerboard pattern.
2) Read back and verify DUT repeatedly.
3) Begin irradiation.
4) Correct the error before continuing reading if the data stored in the DUT are determined to be changed.
5) Terminate the test when the desired number of events is recorded or maximum fluence has been attained.

In our experiments, the SEL threshold current was set to a value ten percent higher than the static bias supply [3].

DUTs were exposed to heavy ions through the front side and irradiations took place at room temperature, unless otherwise stated.

B. γ-Ray Induced TID Tests

In the TID test, we monitored only current variances and whether the DUTs functioned normally. No additional parametric measurements were made [5]. Two samples were used with different test configurations. During irradiation, sample #1 was operated by a test board, the same as the SEE test, while another sample (sample #2) was located separately and unbiased.

The same test board and test procedures were used for the TID test for Sample #1 as those for the SEE test.

V. Data Analysis

A. Heavy-ion-induced SEE Performance

In this paper, SEE data were classified into [5- 6]:

- SEUs - cause a change of state in a memory cell. This type of event causes no permanent damage and the device can be reprogrammed for correct function after such an event has occurred.
- Burst errors - cause upsets at many address locations, which could be as large as 1000, with one ion strike. They can be written over with the original pattern (or other patterns). This type of event causes no permanent damage and the device can be reprogrammed for correct function after such an event has occurred.
- SEFIs - cause burst errors requiring initialization of the DUT. These are similar to burst errors. However, the device can no longer be reprogrammed for correct function. They require reinitializing and reprogramming the DUT (without power recycling) for recovery.
- SELs - cause to flow a high current of above SEL threshold current level, which can possibly lead even to the destruction of a DUT. SELs are not recovered by stopping the beam and reinitializing the DUT. They require power recycling for recovery.

Figs. 2-4 show our heavy-ion-induced SEL, SEFI, and SEU cross section data for the 2 Gbit LPDDR SDRAMs from SK Hynix. In these figures, we plotted the SEE cross section data with two sigma error bars to represent statistical uncertainty due to the finite number of events observed. If the number of observed events in our experiments was larger than 50, two sigma error bar was plotted by Poisson statics [5]. If not, two sigma error bar was plotted Swift's correction factors instead of Poisson statistics. This gives the statistical limits with 95% confidence (essentially two sigma) [7]. SEL tests were performed at room temperature and elevated temperature (70°C). Fig. 2 shows the SEL cross section data with two sigma error bars.

At room temperature test, SEL was observed at LET=77.3 MeVcm^2/mg for the first time as shown in Fig. 2(a). The upper limit for the cross section at next highest LET (69.1MeVcm^2/mg) tested is 7.4×10^{-8} cm^2/device because no SELs were observed up to maximum fluence level (5×10^7 ions/cm^2). The low SEL cross section at 77.3 MeVcm^2/mg and low upper limit for cross section at next highest LET (69.1 MeVcm^2/mg) suggest that the SEL threshold level at room temperature is probably closer to LET=77.3 MeVcm^2/mg rather than the lower limit of the range.

At elevated temperature test SEL was observed at LET=64.9 MeVcm^2/mg for the first time as shown in Fig. 2(b). Similarly, the upper limit for the cross section at next highest LET tested (58.3 MeVcm^2/mg) is also 7.4×10^{-8} cm^2/device because no SELs were observed up to the same maximum fluence level (5×10^7 ions/cm^2). The low SEL cross

section at 64.9 MeVcm^2 /mg and low upper limit for cross section at next highest LET (58.3 MeVcm^2/mg) suggest that the SEL threshold level at 70^{o}C is probably closer to LET=64.9 MeVcm^2/mg rather than the lower limit of the range. The additional characteristics of SEL cross section curve at elevated temperature is that the SEL threshold level is near the SEL saturation level.

Fig 3 shows SEFI cross section data. Only two LET levels (19.6 and 58.3 MeVcm^2/mg) showed SEFI events and SEFI cross section curve appears to saturate over this range. All SEFI events showed many errors in a single row or column of memory map. Our DUT showed substantially less SEFI errors than 90-100nm Samsung 1Gb DDR SDRAMs [5].

Only one run with LET=58.3 MeVcm^2/mg showed a burst errors with 1.33x10^{-16}cm^2/bit cross section.

Fig. 4 shows the heavy-ion-induced SEU cross section curves with two sigma error bars for our DUT and Samsung 1 Gbit DDR SDRAM [5]. As shown in Fig. 4, our DUT SEU cross section value was a minimum 10 times lower than that for the Samsung DDR SDRAMs tested with 10 MeV/amu beam energy similar to our beam energy. The difference between NASA and Aerospace Corporations's results for similar device was explained in [5].

B. γ-Ray Induced TID Degradation

For CMOS devices, TID tolerance has been increasing with device scaling [8]. In our experiments, TID data concerned only DUT current variances, supply current variances, and whether the DUTs functioned normally as dose accumulated.

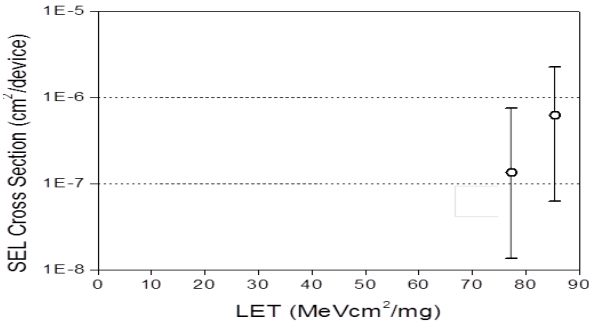
The biased and functioned DUT (sample #1) worked with no errors, no remarkable current consumption, and no apparent degradation to 172 krad(Si). For the unbiased DUT (sample #2), the DUT and test board supply current after 198 krad(Si) were similar to those of the functioned DUT (sample #1).

VI. Conclusion

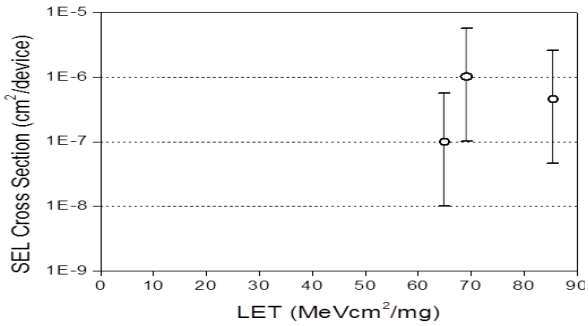
Our experiments present the first heavy-ion-induced SEE test results for LPDDR SDRAMs fabricated on epitaxial wafer. In space systems which have strict limitations on power consumption and radiation hardness, it is important to use radiation-hardened low power consuming ICs. This paper presented the heavy-ion-induced SEE and gamma-ray induced TID data for the SK Hynix 2 Gbit LPDDR SDRAMS fabricated on an epitaxial layer. Those data show that our DUTs could be effective candidates for space flight applications.

VII. Acknowledgment

This research was supported by the 'NEXTSat-1' program funded by the Korean Ministry of Science, ICT, and Future Planning (Grant No. 2012M1A3A4A01040017). The authors are especially thankful SK Hynix for providing the LPDDR SDRAMs used for this experiment.



(a)at room temperature



(b) at elevated temperature

Fig. 2. Heavy-ion induced SEL cross section

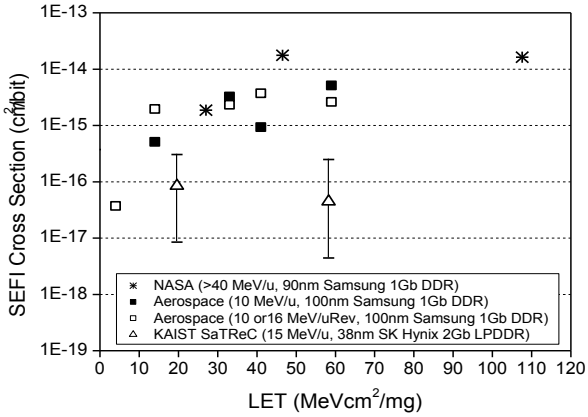


Fig. 3. Heavy-ion induced SEFI cross section

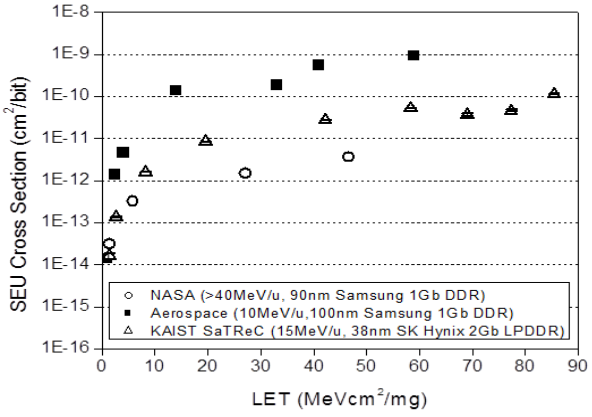


Fig. 4. Heavy-ion induced SEU cross section

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