# A High Performance Rad Hard 2-3 GHz Integer N CMOS Phase Lock Loop

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## *Abstract*

We report here on the performance of a 2-3GHz Phase Lock Loop (PLL) designed specifically for commercial space applications requiring low power dissipation, very good phase noise, good temperature stability, excellent SEE tolerance, and little degradation over a 100kRad(Si) total dose exposure. The device is built in a 0.5μm fully depleted ultra thin silicon on sapphire technology (UTSi). Product level radiation data is presented showing performance as a function of total dose. Following gamma exposures to 100kRad(Si), the device shows an integrated phase noise of less than 0.8 degree for 2.18 GHz. operation for frequency step sizes of 1 MHz. This is a performance level exceeding all known integrated PLL's currently in the commercial marketplace.

## I. Introduction

Poor Single Event Upset (SEU) and Single Event Latchup (SEL) immunity are of major concern in high speed RF Phase Lock Loops (PLL's) incorporated in many of today's commercial satellites. As a result, greater demands are placed at the system level to compensate for this. These include reloading programming every clock cycle, parallel interfaces, and redundancy which result in increased size, weight, complexity and power. We present in this paper a 2-3GHz integer N PLL which is inherently SEL immune, has an SEU rate estimated at less than $10^{-8}$ errors/bit-day (orders of magnitude better than currently available) as well as excellent phase noise performance up 100kRad(Si) total dose. This part is currently being manufactured on Peregrine Semiconductor's 0.5μm Ultra Thin Silicon on Sapphire UTSi® process and was designed specifically for commercial space applications. Allowances were made during the design phase to accommodate for the effects of radiation on the device thresholds and leakage. The product is manufactured using a commercial process flow with no modifications for hardening.

## II. Device Fabrication

Much of the process and device description was presented last year at this conference [1]. Using the single solid phase epitaxy (SSPE) re-growth technique [2][3], a high-quality silicon-on-sapphire (SOS) film is formed. This process yields a low defect-density silicon film with a final thickness of 100nm and electron and hole mobilities similar to those found in bulk silicon [4]. The resulting SOS wafers are processed with standard CMOS processing equipment. The process described here uses LOCOS for transistor isolation, 100Å gate oxide, 0.5μm minimum drawn poly gates with W polycide, LDD drain engineering using oxide spacers, SOG planarization, and three levels of AlCuSi metal.

## III. Results and Discussion

### *A. Device Level Radiation Test Results*

We reported last year in this conference considerable radiation performance data on 0.8μm N channel and P channel transistors [1]. Among the principal findings was the complete absence of back channel leakage in the N channel device. We observe the same behavior for 0.5μm drawn transistors (Leff=0.35μm). The mechanism for the absence of back channel leakage in fully depleted SOS has been previously discussed at this conference [5]. In that paper lower E-Fields at the Si/Sapphire interface were used to explain less radiation-induced charge for fully depleted vs. partially depleted devices. Device simulations performed by Peregrine are consistent with this model.

Figures 1 thru 4 show subthreshold characteristics on sample N and P Channel devices after a total dose of 100 kRad(Si) when biased in both the on and off condition at 3.0V. Testing was performed using the Aracor 4100 Semiconductor 50keV X-ray Irradiation system [6]. Testing performed across several wafer lots shows the capabilities of this technology to be less than 1nA of post radiation leakage per transistor at a total dose of 100 kRad(Si). Figures 1 & 3 show no sign of back channel leakage in the N-Channel transistor after irradiation. The small changes seen in the N-Channel subthreshold slope are more characteristic of a small edge leakage component.

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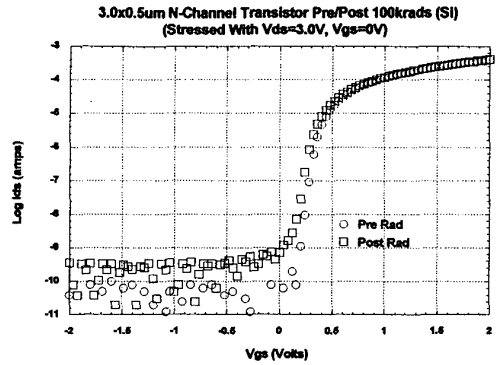


Figure 1: N-Ch I/V Pre/Post Radiation - Off Condition

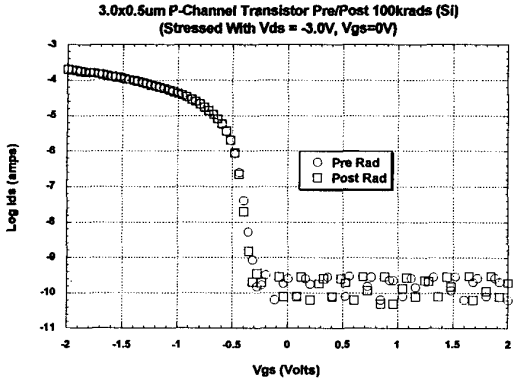


Figure 2: P-Ch I/V Pre/Post Radiation - Off Condition

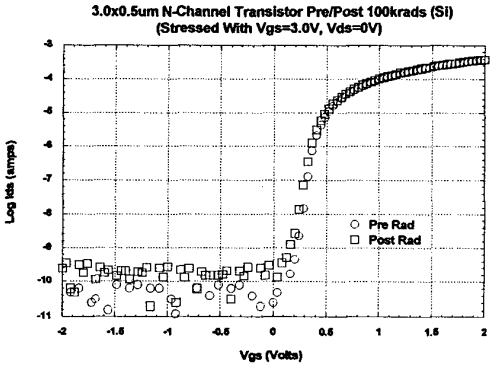


Figure 3: N-Ch I/V Pre/Post Radiation - On Condition

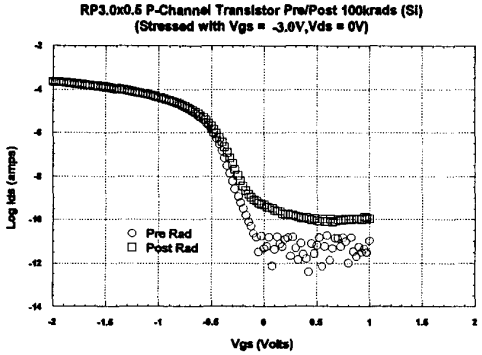


Figure 4: P-Ch I/V Pre/Post Radiation - On Condition

Figure 4 shows that the post radiation P-Channel subthreshold leakage is actually worse than the N-Channel. This was also observed on the P-Channel in our 0.8um process and reported at this conference last year [1]. Peregrine has subsequently identified the cause of the P-Channel leakage and is currently qualifying a modification to the process, which will significantly reduce it. The improvement seen in the P-Channel leakage as a result of these process modifications can be seen in Figure 5.

Figures 1-4 show that threshold voltage shifts seen due to ionizing radiation in this technology are very small. On average, only a 30-40mV shift in threshold voltage is seen after 100kRad(Si) under worse case bias conditions. The small shifts in threshold are a result of the high quality thin gate oxide (100 Å) used in this technology.

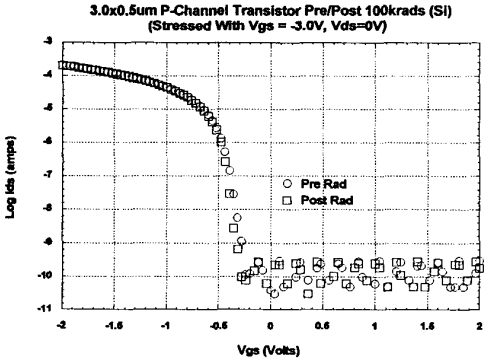


Figure 5: P-Ch I/V Pre/Post Radiation after Process Modifications

## *B. Product Description*

An industry standard integer N Phase Lock Loop incorporating a 10/11 prescalar and internal charge pump (Figure 6) has been built using the process described above. The PLL was fabricated without the process improvements identified to reduce P-Channel post radiation leakage. The part (PE9601) was packaged in a

44-lead ceramic CQFP package for ATE and Cobalt-60 total dose testing.

Based on extensive total dose testing on Peregrine's commercial PLL product line, several design modifications were incorporated to our radiation hard PLL to ensure performance and stability in an ionizing radiation environment. Most of the modifications were aimed at keeping critical bias networks or timing paths stable over radiation. Changes were also made to the charge pump design to minimize mismatch and leakage over total dose.

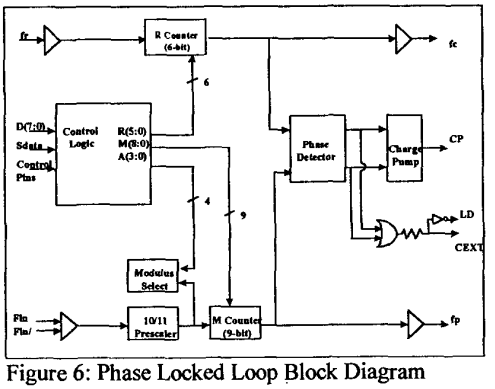


Figure 6: Phase Locked Loop Block Diagram

## *C. Product Performance Summary*

Figure 7 shows the PLL operational Idd at 2GHz. over voltage and temperature. The worst case current value is less than 28mA (3V operation) compared to 120-200mA for 5V Bi-CMOS devices currently on the market. On average, this translates to an order of magnitude reduction in power which is significant considering the number of PLL's incorporated into today's commercial satellite designs. Figure 8 shows the source vs. sink current percent mismatch of the charge pump over voltage and temperature. Several design techniques were used to minimize charge pump mismatch across temperature and ionizing radiation. Minimizing mismatch is a key element to the excellent spurious performance of the PLL.

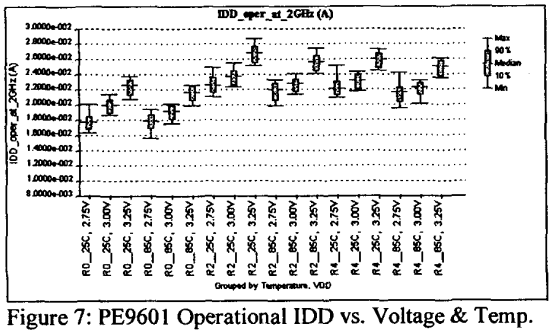


Figure 7: PE9601 Operational IDD vs. Voltage & Temp.

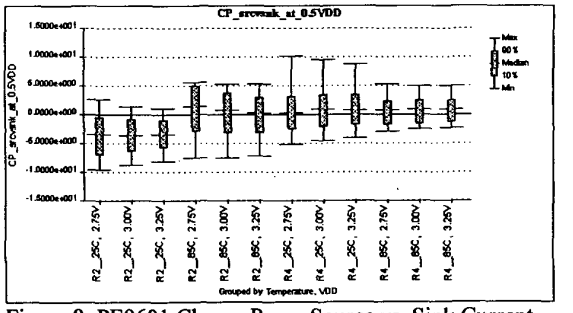


Figure 8: PE9601 Charge Pump Source vs. Sink Current

Figures 9-11 show phase noise versus offset frequency from the carrier for 824MHz., 2.18GHz. and 3.0GHz. respectively measured at 25° C using a 1MHz. Step size and a 10Mhz. reference frequency. These figures clearly show the excellent phase noise performance of this part even out to 3GHz. operation.

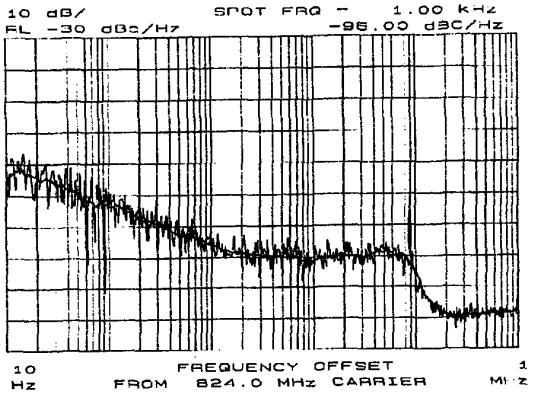


Figure 9: PE9601 Phase Noise vs. Offset – 824MHz.

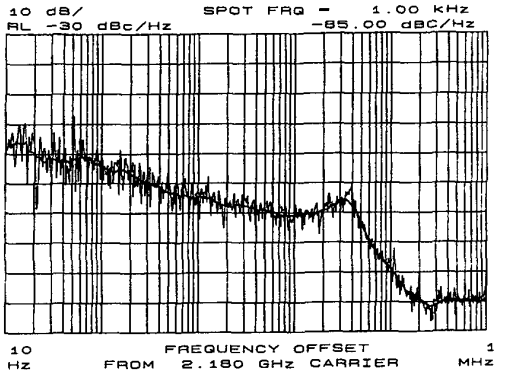


Figure 10: PE9601 Phase Noise vs. Offset – 2.18GHz.

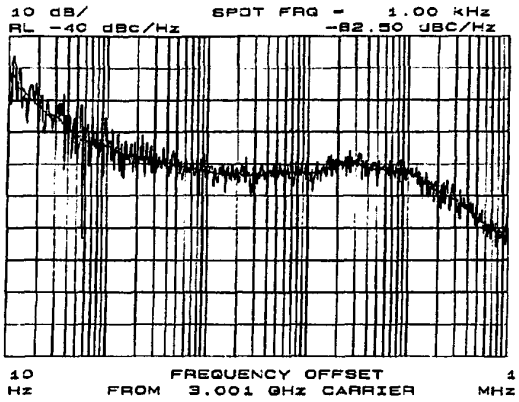


Figure 11: PE9601 Phase Noise vs. Offset – 3.0GHz

Spurious performance for the PE9601 is shown in figure 12. The spurs shown are for 2.18GHz. operation using a 1MHz. step size, a 10 MHz. reference and measured at 85° C. The -61dB spurious performance at temperature compares favorably to current radiation hardened PLL parts currently on the market.

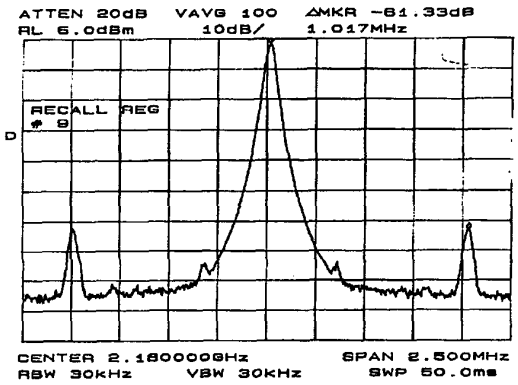


Figure 12: PE9601 Spurious Performance

### *D. Product Level Total Dose Response*

Total dose testing of the PLL was performed using the test setup shown in Figure 13. A Shepherd 150-C Co-60 point source [7] was used to irradiate the part, which was operating at 3.0V in a locked loop condition at room temperature.

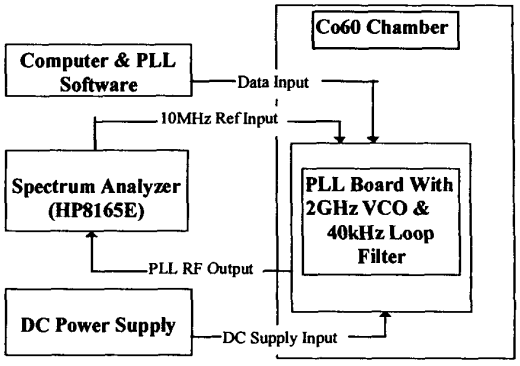


Figure 13: PLL Cobalt-60 Test Setup

Parts were irradiated out to 100kRad(Si) total dose at 200rads/minute. During irradiation the RF output was monitored using an HP8165E spectrum analyzer to ensure the part remained locked. ATE testing as well as phase noise and spurious performance was measured both before and after irradiation. Table 1 shows phase noise performance was virtually unchanged after 100kRad(Si) total dose. The stability of the parts phase noise performance with total dose is attributed to the design techniques used to minimize the parts sensitivity to ionizing radiation as well as the small threshold shifts seen in this technology with total dose. The spurious performance in Table 1 shows 2-3 dB degradation after 100kRad(Si) total dose. The 2-3 dB change was correlated to leakage in the charge pump as a result of the post radiation P-Channel leakage described above. It is believed that the spurious performance can be improved even further on this part by implementing the process improvements identified to reduce post radiation P-Channel leakage.

Table 1
Pre/Post Radiation PLL Performance

| Serial Number | Total Dose (Krads) | Temp. Deg C | Phase Noise (dBc/Hz) 1kHz Offset | 10kHz Offset | Int Noise (Deg) (10Hz-1MHz) | Spurs (dB) |
|---|---|---|---|---|---|---|
| 14 | 0 | 25 | -87.0 | -93.2 | 0.63 | -62 |
| 14 | 0 | 65 | -85.7 | -91.3 | 0.75 | -62 |
| 14 | 0 | 85 | -85.3 | -92.0 | 0.75 | -63 |
| 14 | 100 | 25 | -88.2 | -92.3 | 0.60 | -60 |
| 14 | 100 | 65 | -85.0 | -91.2 | 0.77 | -60 |
| 14 | 100 | 85 | -85.7 | -92.5 | 0.73 | -60 |

### *E. Single Event Upset Test Results*

At last years conference, we presented SEU test data on the 0.8um UTSi technology [1]. Single event upset testing was performed on a 100k gate digital shift register at Vdd=2.5V using a LBL 88-inch cyclotron [8]. An SEU rate of 1.1E-9 errors/bit-day was calculated for a 0.4x4.09x0.1μm cross sectional area (Figure 14). SEU testing on a 3.0V PLL built in the 0.8um UTSi technology is reported in another workshop paper presented at this conference (W-9). SEU testing on the 2-3GHz. PLL design has not yet been performed, but simulations predict

a very slight degradation in the SEU rate based on the more aggressive design rules used.

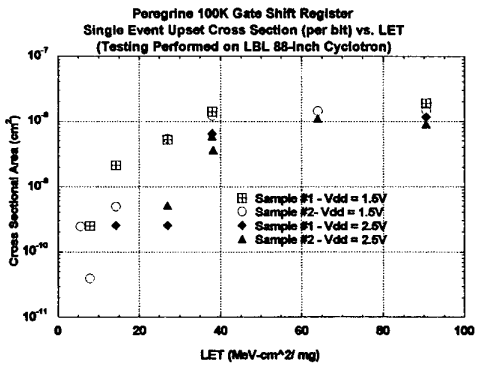


Figure 14: SEU data on 100k Gate Shift Register

## IV. CONCLUSIONS

We have shown a very high performance 2-3GHz Phase Lock Loop which shows near immunity to the total dose radiation levels associated with many of today's commercial satellite applications. Due to the very thin silicon layer, the SEU performance is also expected to be excellent. The device is built in a commercial process and demonstrates the feasibility of multi GHz. RF functions in CMOS for space applications.

## ACKNOWLEDGEMENTS

Boeing Radiation Effects Laboratory for the SEU data presented in Figure 5.

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