Characterization of Various SEE Hardened Power Management ICs

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Abstract -- Single event effects test results are reported for several power management devices that have been specifically SEE-hardened by design. Single event transient, as well as single event latchup data is presented and discussed.

I. INTRODUCTION

IN an effort to provide more efficient and reliable space-based systems, designers are becoming more concerned with single event effects (SEE) that heavy ions have on spacecraft electronics. These effects can lead to system-level failures including disruption and permanent device damage. Nowhere is this more evident than in the area of power control, where reliable performance is highly critical to mission success [1], [2].

Until recently, there have not been any power control devices available that were specifically SEE hardened. The unique features of Intersil's radiation hardened silicon gate (RSG) process, in combination with the use of innovative circuit design techniques, have been successfully applied in the development of several SEE hardened power control devices, called the Star*Power™ family.

This paper discusses specific hardening techniques and presents testing results validating successful implementation of SEE mitigation methods in the design of various hardened power management ICs.

II. DESIGNING FOR SEE HARDNESS

A. SEE Hardened Process Requirements

Developing SEE hardened devices requires a well-modeled, hardened process and the use of specialized design techniques. The process must be hardened during development, taking into account options for isolation technology, doping profiles and concentration, and oxide thickness. Layout ground rules must support the hardened device structures.

B. Rad Hard Silicon Gate (RSG) Process Features

Intersil's radiation hardened silicon gate (RSG) process is a high voltage, dielectrically isolated (DI) BiCMOS process that is inherently latchup immune and is total dose hardened to 300krad(Si). The process device portfolio includes 35V complementary bipolar, 35V NMOS/PMOS, 120V NDMOS and 150V extended drain PMOS devices. The process characteristics have been described in detail in previous

papers [3], [4]. Additionally, the use of vertical device architectures for both PNP and NPN bipolar transistors enables the design of devices that demonstrate only a slight sensitivity to enhanced low dose rate (ELDRS) effects [4].

III. TEST OBJECTIVES AND FACILITY CAPABILITY

The objective was to validate the single event latchup (SEL) and single event transient (SET) performance of several Star*Power™ ICs that were specifically designed for SEE and total dose hardness. Separate SEE test reports are available from Intersil [5], which provide considerably more information than is detailed in this report.

Testing was performed at Texas A&M during two sessions, over several days, in August 2000. A wide variety of species and energies are available at the facility, and the beam angle can be varied to simulate higher linear energy transfer (LET) values. The devices were packaged in open packages and all testing was performed outside of the vacuum on device specific fixtures. Gold (Au), krypton (Kr) and argon (Ar) ions were chosen for these sessions. The actual LET values vary slightly from device to device due to the difference in spacing between the beam and the surface of the tested devices.

IV. SEE TEST RESULTS FOR HARDENED POWER MANAGEMENT DEVICES

A. IS-2100ARH Half- Bridge Driver

The IS-2100ARH is a high frequency, 150V power MOSFET driver IC that is an SEE hardened equivalent of the industry standard 2110 and HIP2500 half-bridge drivers. The low side and high side output drivers are independently controlled and are matched for precise timing control. The high side driver is capable of switching 150V. A novel level shifting architecture yields the low-power benefits of pulsed operation with the safety of DC operation. The device was designed for an SEU LET hardness level of 80MeV/mg/cm². This was achieved through the use of redundancy/voting logic and/or increasing device sizes at critical circuit nodes.

The objective of the testing was to validate the elimination of SEE-caused low-to-high (LH) output transitions in the IS-2100ARH. Having both power FETs ON causes destructive "shoot-through" in half-bridge DC-DC converter applications. High-to-low (HL) output glitches will only momentarily cause both FETs to be OFF, which will not lead to an overstress. The parts were tested with the supply voltage

at both 12V and 20V, while switching 150V at 1KHz with a 50% duty cycle. All testing was performed using Au at 90.9MeV/mg/cm² to a fluence of 1x10⁷p/cm².

The IS-2100ARH did not exhibit any latchup or destructive effects. As shown in Fig. 1, some harmless HL transients were observed. However, no potentially destructive (at the system level) LH transients were encountered at this high LET, validating the SEE hardness of this part.

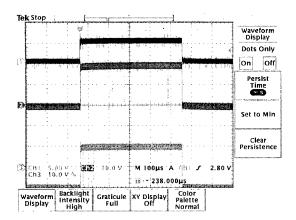


Fig. 1. IS-2100ARH High-to-Low transients with 90MeV/mg/cm² Au ions at 25°C ambient. Trace 1 is the control input to both drivers; trace 2 is the high side output (riding on 150V); trace 3 is the low side output. Note absence of Low-to-High transients.

B. HS-4080ARH Full-Bridge FET Driver

The HS-4080ARH is a high frequency, medium voltage, full-bridge power MOSFET driver. It is well suited for use in DC-DC converters and motor drivers where both direction and speed control are required. The part is constructed in the RSG DI process and was designed for a total dose hardness level of 300krad(Si).

Because of the nature of its use as a full-bridge driver, the transitions of interest would be the outputs inadvertently changing from a low to a high during exposure. This condition will cause both N-Channel MOSFETs on the same side of the full-bridge configuration to conduct at once, risking burnout.

During testing the parts were toggled at 1KHz and 20KHz with a 50% duty cycle. All SEL testing was performed using 90.9MeV/mg/cm² Au ions at 60 degrees, for an effective LET of 181.8MeV/mg/cm², to a fluence of 1x10⁷p/cm². Several devices were exposed at temperatures of both 25C and 125C. SEE testing of the HS-4080ARH did not produce any latchup or other destructive effects, and there was little or no difference in the pre- and post-irradiation supply currents. However, as noted in Table 1, transients were observed at these higher LET values.

Transient testing was then performed using Kr at an angle of 60 degrees for an effective LET of 70MeV/mg/cm². No potentially destructive (at the system level) LH transients were observed. However, some non-fatal HL transients were seen in the static mode. (In an actual application, a HL transient would have no effect on system operation.)

TABLE I HS-4080ARH SEL TEST RESULTS

	CUR	RENT	CONDITIONS AND COMMENTS		
UNIT		POST	$V_{CC} = 20V; V_{BOOT} = 80V$		
	(mA)	(mA)	Temp = 27° C & 125° C; Ion = GOLD		
			Fluence = 1×10^7 ; Flux = 6.5×10^4		
'			Angle = $\underline{60 \text{ degrees}}$; LET _{eff} = $\underline{181.8}$		
			Total Accumulated Dose = 1.4x10 ⁴ rad(Si)		
13	12.5	12.5	20 KHz - No Latchup or Burnout - BHO goes High		
			While BLO is High		
13	13.4	13.1	Temp = 125°C - 20 KHz - BHO goes High While		
			BLO is High - No Latchup or Burnout		
14	12.6	12.6	1 KHz - No Latchup or Burnout - BHO goes High		
			While BLO is High		
15	13.1	13.1	1 KHz - No Latchup or Burnout		

Based on these results a conservative transient cross-section and minimum LET can be estimated. At a fluence of 1×10^6 particles/cm², and assuming 100 transients per output (approximate number seen with Au), the saturated cross-section would be 1×10^{-4} cm². Because only a couple of transients were seen in the static mode, and no transients were seen in the dynamic mode when using Kr at 60 degrees, the minimum LET number can be established at 70MeV/mg/cm^2 .

C. IS-1845ASRH Current Mode PWM

Pulse width modulation (PWM) controllers are commonly used in various switching mode power supplies. These devices offer special features to optimize performance, while minimizing the need for external circuitry. The devices generally have an error amplifier, an oscillator circuit, an output circuit and an internal reference circuit. In addition to these functions, the IS-1845ASRH also contains a current limit comparator and an under voltage lockout (UVLO) circuit. The current limit comparator is used to limit the duty cycle, if an overcurrent condition arises. The UVLO circuit is used to bring the PWM into regulation after it has reached a designated threshold value.

The IS-1845ASRH utilizes the RSG DI process and is hardened to a total ionizing dose level of 300krad(Si). The device was designed for a high level of SET tolerance, using device sizing and redundancy techniques. During testing the parts were operated in a free-running mode at 300KHz with a 20% duty cycle. They were irradiated using Au at 89.1MeV/mg/cm² and Kr at 35.0MeV/mg/cm², both to a fluence of 1x10⁶p/cm². No destructive single-event effects or latchup were observed using Au at the maximum LET of 89.1MeV/mg/cm².

Although upsets were observed at the higher LET value (LET= 89.1MeV/mg/cm²) using Au as an ion source, there were no indications of upset using Kr ions at an LET of 35MeV/mg/cm². These upsets resulted in duty cycle changes and perturbations in oscillator frequency. The calculated capture cross section was 5x10⁻⁶cm². None of these upsets lasted longer than a clock cycle before recovery and hence, would not cause system-level effects. This is similar to what occurred during testing of the industry standard versions of these part types at substantially lower LET values.

D. IS-1715ARH Complementary FET Driver

The IS-1715ARH is an SEE hardened, high speed, complementary output, power MOSFET driver designed for use in synchronous rectification applications. It has a single TTL compatible input that controls the complementary outputs and can run at frequencies up to 1MHz. The device is constructed in the Intersil RSG DI process, is hardened to 300krad(Si), and had a design goal of 80MeV/mg/cm² for SEE tolerance.

All testing was performed using Au at 90.9MeV/mg/cm² to a fluence of 1x10⁷p/cm². SEL testing was done at an angle of 60 degrees, which equates to an effective LET of 181MeV/mg/cm². As expected, SEE testing did not produce any latchup or destructive effects.

The IS-1715ARH was designed so that ion strikes would not produce any low-to-high (LH) glitches on the outputs. Having both power FETs ON causes destructive "shoot-through" in DC-DC converter applications. High-to-low (HL) output glitches will only momentarily cause both FETs to be OFF, which will not lead to an overstress.

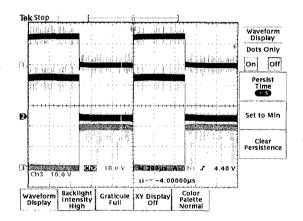


Fig. 2. IS-1715ARH SET response during dynamic exposure to Au ions; V_{CC} =20V. Note lack of low-to-high transients.

During SET testing, no potentially destructive (at the system level) LH transients were encountered. The bottom two traces on the scope photo in Fig. 2 show the lack of LH transients on the complementary outputs. Using a very conservative estimate of 100 HL transients (more than were seen) at a fluence of 1x10⁶ p/cm², the saturated cross-section would be 1x10⁻⁴cm². Because no LH transients were recorded using Au ions, the minimum LET number can be established at 90MeV/mg/cm², validating the SET hardness of this part.

E. IS-705RH Power-up Microprocessor Reset Circuit

The IS-705RH is a power supervisory circuit that monitors the supply voltage and battery functions in microprocessor systems. The device provides a reset output pulse during power-up and power-down conditions, a precision 4.65V voltage monitor, a watchdog timer for processor interfacing, a

1.25V threshold detector to monitor other voltages, and a manual reset input.

Intersil's UHF-2 non-hardened, JI process is used to implement the part, which had to be SEL hardened by design to a goal of 80MeV/mg/cm² and total dose hardened to 100krad(Si) by design. Hardening techniques included the use of special edgeless N-channel devices and guard rings to control N-channel leakage after total dose irradiation, and specific device sizing rules and logic redundancy to harden the part to SEE.

During testing the part was toggled with 1KHz on various inputs, and irradiated using Au at 89.1MeV/mg/cm² and Kr at 35.0MeV/mg/cm², both to a fluence of 1x10⁷p/cm². Unlike the other Star*Power devices, the IS-705RH is built in a junction-isolated process, in which latchup is at least a theoretical possibility. Other Intersil Star*Power devices use various dielectrically isolated (DI) processes, in which latchup is not possible.

Accordingly, the first testing sequence looked at destructive effects. No burnout or latchup was observed using Au ions (LET = 87.0MeV/mg/cm²) at 60 degree incidence from perpendicular (representing an effective LET of 174.0MeV/mg/cm², as compared to testing at normal incidence).

The second testing sequence was conducted to evaluate the transient response of the device. The LET design goal for transient immunity was 40MeV/mg/cm², so upsets were expected when testing initially with Au at the higher LET of 87.0MeV/mg/cm². Upsets were indeed measured; the data is presented below.

TABLE II IS-705RH TRANSIENTS WITH AU IONS

Ion Angle	Temp	Serial #	Fluence	Reset	Error
from	°C		/cm²	HLH	cross section
normal				transients	cm ²
60°	25	5	1x10 ⁷	125	1.25x10 ⁻⁵
		_ 6	1.07x10 ⁷	116	1.08x10 ⁻⁵
Total flue	ence, tra	nsients	$2.07x10^7$	241 1.16x10 ⁻⁵	
	125	4	1.01x10 ⁷	131	1.30x10 ⁻⁵
		_ 5	1x10 ⁷	150	1.5x10 ⁻⁵
		_ 6	1.04x10 ⁷	161	1.55x10 ⁻⁵
Total flue	Total fluence, transients		3.05×10^7	442	1.45x10 ⁻⁵
0 °	125	6	1.4x10 ⁷	236	1.69x10 ⁻⁵

SET testing of the IS-705RH was then performed using Kr ions at an LET of 38MeV/mg/cm². The initial test set Vcc at 4.5V and master reset (MR) at Vcc; under these conditions, RESET should be low (as Vcc is below the nominal Vcc reset threshold of 4.65V). Using a fluence of 1x10⁶/cm², no upsets or transients were observed during this test. This validated that during a low Vcc condition there would be no false

signals sent from RESET indicating that Vcc is within tolerances.

The second test set Vcc at 4.75V and MR at Vcc; hence RESET should be high (as Vcc is above the nominal Vcc reset threshold of 4.65V). Two runs of fluence $1x10^6/\text{cm}^2$ each were run and a total of 24 (10+14) HL transients were observed for a transient cross section of $1.2x10^{-5}\text{cm}^2$. Vcc was then raised to 5V, a more typical application, and the upsets were reduced to 4 (cross section $4x10^{-6}\text{cm}^2$). Vcc was then raised to 5.5V and no upsets were observed.

Testing was next performed with different LET values to characterize cross section vs. LET. Kr ions were again used with their energy increased to obtain an LET of 26.8MeV/mg/cm². The RESET cross section appeared to increase to 2.4x10⁻⁵ (71 upsets at a fluence of 3x10⁶/cm² with Vcc=4.75V). Again, there were no LH transients when Vcc=4.5V. Testing with Ar with an LET=17.5MeV/mg/cm² yielded a cross section of 6x10⁻⁶ (30 upsets at a fluence of 5x10⁶/cm²) for the HL upsets. While no upsets would have been the preferred result for these tests, the RESET HL transient cross section is so low that unnecessary resets of the uP would be extremely rare. With these LET and cross-section values, unnecessary resets would be hundreds to thousands of years apart.

When RESET was driven low by setting MR = 0V (Vcc was returned to 5V) there were no upsets with Kr or Ar with LET values ranging from 27 to 38MeV/mg/cm². Observing no upsets was not a surprising result, as the SET would have to last longer than the 200ms Reset timer period to get a false transition to a "1" level. So, the manual reset function is SEU "immune".

RESET summary: The part has no RESET LH transients when Vcc is less than 4.75V or is held low by MR input being held low. This means the system will not have any false RESET signal telling it that Vcc is within tolerance when it isn't, or that it can operate while the MR is being applied. When Vcc>4.75V and MR = "1" there are HL upsets that would cause the system to go through an unnecessary reset cycle. Again, since the error cross-section is so small, this would be an unlikely occurrence.

The key objectives of burnout or latchup hardness to an LET in excess of 87.0MeV/mg/cm² and no RESET LH transients to an LET of 38MeV/mg/cm² have been demonstrated. Other functions have demonstrated cross sections so small as to not occur for hundreds to thousands of years. These characteristics must be evaluated by the system designer for use in the particular environment of interest, based on the usage of available features. Further details are included in the IS-705RH SEE Test Report available from Intersil.

F. IS-1009RH 2.5V Reference

The IS-1009RH is a monolithic precision voltage reference fabricated using Intersil's dielectrically isolated EBHF process. The process features complementary bipolar devices and laser-trimmable NiCr thin-film resistors, making it well suited for reference applications. The device is single event latchup (SEL) immune by construction and is hardened to a total dose level of 300krad(Si).

Functionally, the device is a 2.5V shunt regulator designed to provide a stable 2.5V reference over a wide current range, over temperature and after irradiation. It operates at a lower minimum current than standard 1009 types and features a 0.2% tolerance achieved by on-chip laser trimming.

In order to validate the design and construction, and to determine any SEE-related application restrictions, the device was irradiated using Au at 87.0MeV/mg/cm² to a fluence of 1x10⁶p/cm² for both SEL/SEB and SET tests. The IS-1009RH was found to be free of destructive latchup and burnout effects. However, the part was found to display SET effects at this LET, with the magnitude of the SET pulses dependent on the external filter parameters. The use of such filtering is a common SET mitigation technique for voltage references, usually consisting of an RC filter tied to the device output.

A series of runs were made for several combinations of output filter components using 87.0MeV/mg/cm^2 Au ions. The initial run was made with no external filtering of the output. The reference voltage was significantly perturbed from its steady-state value. Counts of 363 to 445 pulses were recorded at the test fluence of $1 \times 10^6 \, \text{p/cm}^2$ for an approximate cross section of $4 \times 10^{-4} \text{cm}^2$. As can be seen in Fig. 3, most of the transients observed were narrow pulses, but a significant number were full-scale deflections stretched out by saturation effects in the device.

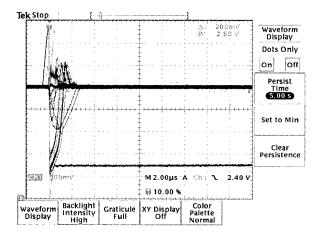


Fig. 3. IS-1009RH SET response during exposure to Au ions; with no external filter components.

Several runs were then made to investigate the response of the device with various filter combinations, the results of which are shown in Table III.

TABLE III
IS-1009RH RESPONSE TO FILTER COMBINATIONS

		1	2	3	4	5
Filter R	None	1Kohm	1K	10K	None	None
Filter C	None	0.01uF	0.1uF	0.01uF	10uF	100uF
Error	2V	1.5V	SET-	SET-	500mV	-500mV
			Free	Free		1
Pulse	45usec	60usec	SET-	SET-	<10nsec	<10nsec
Width			Free	Free	ł	}

The error term improves with the first external filter network, but the recovery time is stretched out to 60usec. Further improvement is provided by the second filter combination; here, the error voltage nearly disappears, as it does in the third filter combination (Fig. 4). Finally, the results for capacitive-only filtering are shown, in which we see a moderate error term of 500mV and very quick recovery.

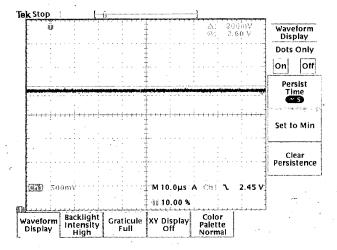


Fig. 4. IS-1009RH SET response with Au ions, 10Kohm and 0.01uF filter. Acquire started after beam shutter open, no visible transients.

The IS-1009RH voltage reference was tested with Au ions at an LET of 87MeV/mg/cm² and was found to be free of destructive latchup and burnout effects. The part was found to display single event transient (SET) effects at this LET, with the magnitude of the SET pulse dependent on the external filter parameters. These SET effects introduce an applications dependence. In most cases the reference will be used to drive a buffer amplifier, which enables the use of significant resistance in the output RC filter, thereby reducing any transients to a few millivolts.

G. IS-139ASRH SEE Hardened Quad Comparator

The Intersil IS-139ASRH is a functional equivalent to industry standard 139 type quad voltage comparators. These standard types have been widely used in space systems and have been the subject of frequent radiation testing in both the total dose and energetic heavy ion environments. The standard types have also shown vulnerability to low dose rate effects (ELDRS) and will propagate single-event pulse (SEP) phenomena into the circuitry they are driving, necessitating redundancy, filtering or error correction techniques to avoid system upset.

The IS-139ASRH, manufactured on the RSG DI process, is total dose hardened to 300krad(Si) and SEE hardened by design to an LET of 80MeV/mg/cm². This is achieved through the use of redundant comparator architecture, on-chip filtering and appropriate device sizing [6].

During SEL testing the inverting inputs were tied to 1V and the non-inverting inputs were toggled between zero and 2V at 1KHz with a 50% duty cycle. SEL testing was performed

using Au at 83.9MeV/mg/cm² at 60 degrees, for an effective LET of 168MeV/mg/cm², to a fluence of 1x10⁷p/cm². As expected, the IS-139ASRH quad comparator showed no destructive effects or latchup.

The first SET test session was performed with 1V of input overdrive into the device, using Au ions at an LET of 83.9MeV/mg/cm². Under these test conditions, no output transients were recorded. However, the device is designed to have the correct output state when the inputs are only 5mV apart (the specified input offset voltage). Under these input test conditions, the device is vulnerable to noise induced into the test fixturing by an ion strike on input or output transistors.

In order to enable accurate measurements with very low input overdrive levels, SET testing was next performed using specially designed, low-noise fixturing. Upsets at the comparator output were observed with 5mV of input overdrive. The input overdrive was then increased to determine the threshold for SET-free operation. At an input overdrive value of 5.8mV, all output transients ceased. This confirmed that no output transients would occur once sufficient overdrive is applied.

Testing was performed to determine the minimum input overdrive voltage required to eliminate output transients for a wide range of source resistances and capacitances.

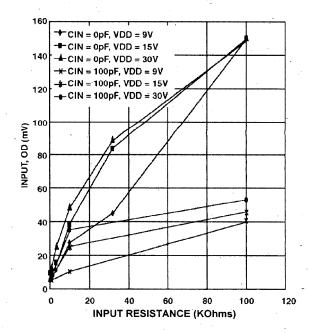


Fig. 5. The minimum input overdrive for SET-free operation as a function of input resistance, input capacitance and supply voltage using Kr ions at 38.0MeV/mg/cm². (Top set of curves, 0pF; bottom set of curves, 100pF.)

Fig. 5 shows a plot of minimum input overdrive required for SET-free operation of the IS-139ASRH as a function of source resistance and input capacitance, using Kr ions at 38.0MeV/mg/cm². The source resistance is in series with each comparator input and the capacitance is a shunt capacitance from each comparator input to ground. Fig. 6 shows an

equivalent set of curves for Au ions at an LET of 84.0MeV/mg/cm². Both figures also show the effects of supply voltage on the minimum overdrive requirements. The Kr data shows some supply dependence, while the Au data shows none.

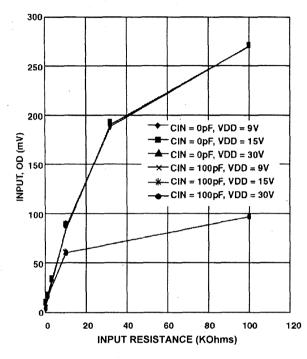


Fig. 6. The minimum input overdrive for SET-free operation as a function of input resistance, input capacitance and supply voltage using Au ions at 83.9MeV/mg/cm². (Top curve, 0pF; bottom curve, 100pF.)

V. SUMMARY

A family of SEE and total dose hardened power control ICs, called Star*Power™, has been developed and SEE test results have been reported. The devices exhibit greatly improved SEE hardness capabilities over previously available options. Spacecraft power circuit designers now have SEE hardened, QML Class V devices available that allow mission requirements to be met, while providing significantly improved power system performance and reliability.

TABLE IV SINGLE EVENT EFFECTS TEST SUMMARY

Device	Function	SEL (1)	SET (I)
IS-139ASRH	Quad Comparator	>84	>84 (2)
IS-705RH	uP Reset Circuit	>87	>38
IS-1009RH	2.5V Reference	>87	>87 (3)
IS-1715ARH	Comp. FET Driver	>90	>90
IS-1845ASRH	PWM	>89	>35 (4)
IS-2100ARH	Half-Bridge Driver	>90	>90
HS-4080ARH	Full-Bridge Driver	>90	>70

- (1) SEL and SET-Free measurements in MeV/mg/cm²
- (2) Requires minimum overdrive dependent on source impedance.
- (3) IS-1009RH SET >87 requires filtering
- (4) IS-1845ASRH SET >89 with cross section = 5e⁻⁴

VI. REFERENCES

- [1] K. LaBel, "Single Event Effect Criticality Analysis", 1996 radhome.gsfc.nasa.gov/radhome/papers/seeai.htm
- [2] K. LaBel and M. Gates; "Single Event Effect Mitigation from a System Perspective", IEEE Transactions on Nuclear Science Special Edition, 1996
- [3] N. W. vanVonno, et al. "Applying a High Voltage BiCMOS Process to Hardened Power Management Functions", RADECS Workshop Summary, Sept, 2000, pp 124-128.
- [4] J. F. Krieg, et al, "Enhanced Low Dose Rate Sensitivity (ELDRS) in a Voltage Comparator Which Only Utilizes Complementary Vertical NPN and PNP Transistors", IEEE Trans. on Nuclear Science, 46(6), Dec, '99, pp. 1616 to 1619
- [5] Device SEE Test Reports, Intersil Corporation, Nov, 2000; www.intersil.com
- [6] N. W. vanVonno and B. R. Doyle, "Design Considerations and Verification Testing of an SEE-Hardened Quad Comparator", unpublished.