A Compendium of Single Event Transient Data

M. W. Savage *Member IEEE*, T. Turflinger *Member IEEE*, J. W. Howard, Jr. *Senior Member IEEE*, S. Buchner *Member IEEE*

Abstract—**We present a compendium on observed Single Event Transients on analog and digital circuits. Both the data and the test methods used are presented.**

I. Introduction and Background

As heavy ions penetrate the sensitive structures in microelectronics, the generated charge can produce a spurious voltage on a node of the device. The voltage deviation or pulse is known as a Single Event Transient (SET). In Fig. 1 three SETs on a Harris HS139RH (which is a total dose radiation hardened version of the HS139) are shown. In each case the ion LET and input biases are the same but different internal nodes were struck, causing large differences in response. This variation in circuit response illustrates the difficulties in quantifying SETs. Since the early 1980's, SETs have been observed in many devices and microcircuits. In early literature, SETs in analog circuits [1] were often termed analog Single Event Upsets (SEUs), whereas in digital circuits a transient that causes the data output to be latched into an incorrect state has been consistently referred to as a digital SEU [2]. In Microprocessors, the obtainable data often incorporates both SETs and SEUs together as SEUs [24]-[42]. While traditionally the upset of a storage element by these transients was the major concern, as technology evolves, the SET's have become a direct problem in many circuits. While SETs have also been observed in optical devices, such as optocouplers [20], they are not covered herein. This document will focus exclusively on SET in silicon microcircuits and the methods used to capture and count their occurrence.

II. Testing Methods

Test methods differ significantly from experimenter to experimenter and from test to test. However, experimental methods used follow several measuring techniques. Some of these techniques will be described in brief. The abbreviations used in table 3 are described in tables 1 and 2.

A. Sampling Scope:

One common technique is to use a high speed storage scope [9], as shown in Fig. 2. In this method, an oscilloscope measures the output of the device under test (DUT). As the

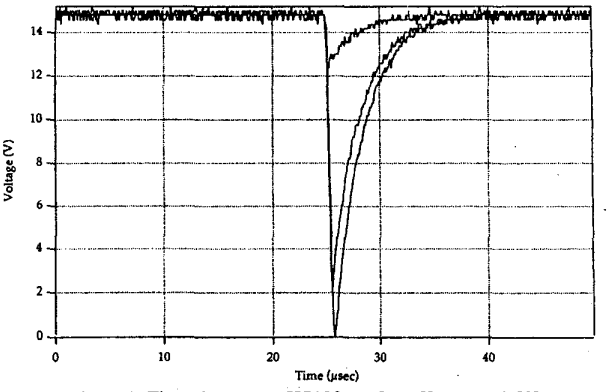

Figure 1. Three SETs on a HS139RH from Koga et. al. [8]

DUT is several feet away from the oscilloscope, some method is needed to compensate for attenuation of the transient signal. In the example of Fig. 2, a high-impedance high-bandwidth active FET probe is used. Another approach is to feed the output through a resistance network, which is fed to the sampling scope. The advantage of this measurement technique is that the transient signal can be fully characterized via the recording of pulse height, pulse width, and polarity. In addition, modern digitizing oscilloscopes have sophisticated trigger circuitry that allows trigger pulses to be counted for the cross-section, so that all required data is collected by a single instrument. For this reason, this approach is becoming the most common test technique. The attenuation of pulse signals and oscilloscope bandwidth limitations are disadvantages of this technique.

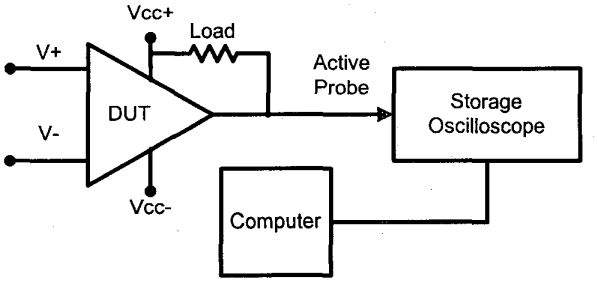

Figure 2. A Typical Analog SET Experiment using a Storage Oscilloscope.

B. Level Discriminator:

In this experimental method, the output was measured by a series of voltage discriminators [3]. As the transient signal of some preset amplitude or greater encounters the voltage discriminators, the pulse amplitude is converted into a trigger pulse. The trigger pulses are then sent to a counter. Alternatively, the voltage discriminators can be set to record the time between the rising and falling time of the pulse, giving the pulse width. The output of the discriminators is

Work sponsored by Defense Threat Reduction Agency (DTRA) and NASA Electronic Parts and Packaging (NEPP) Program.

Mark W. Savage and Tom Turflinger, are with NAVSEA Surface Warfare Center Division, Crane, IN 47522 USA (telephone: 812-854-6927, e-mail: savage_m @atd.crane.navy.mil).

Jim Howard is with NASA GSFC/J&T, Greenbelt, MD, 20771 USA (telephone: 301-286-1023, e-mail: jim.howard@gsfc.nasa.gov).

Steve Buchner is with NRL/SFA, Washington DC, 20375 USA (telephone: 202-767-5460, e-mail: buchner@ccf.nrl.navy.mil).

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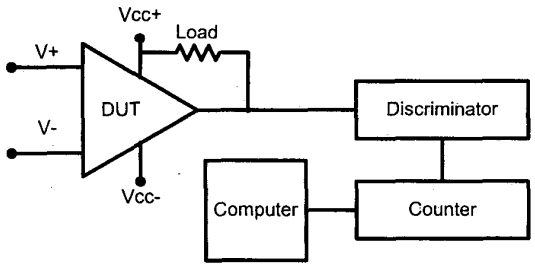

Figure 3. A Typical Analog SET Experiment Using a Level Discriminator.

the input into a counter, as shown in Fig. 3. The ability to perform on chip measurements without attenuation of the output signal are some of the advantages of this technique, however the original signal is lost in this method, limiting post test analysis.

C. Current Measurements:

In this experimental method, the supply current was measured for increases or decreases in the leakage current [7]. Here the transient signal is measured as a current fluctuation. In this method, the DUT can be simultaneously monitored for both the transient signal as well as latchup. However, as in the previous method, the original signal is lost.

D. Transient Interruption of Output Signal:

In experiments such as Jobe's [18] investigation of high-speed digital phase-locked loops or Reed's study of Emitter Coupled Logic (ECL) Devices [2], the measurement of SETs is complicated either by test conditions or by the DUT itself. Under those conditions, the output of the DUT is compared to the expected outcome. An example from Reed's investigation is shown in Fig. 4. In this example, the data sequence generator passes a 2^7-1 pseudo-random number

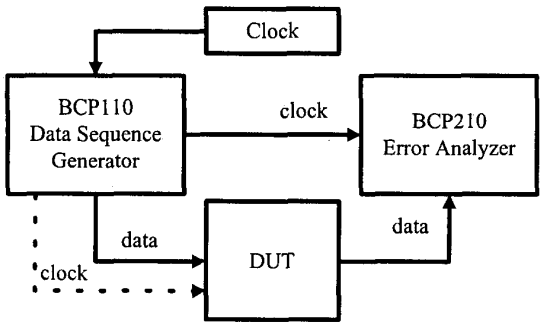

Figure 4. Block Diagram of R.A. Reeds ECL setup [2]

Table 1: Test Methods Used.

Abbr.	Test Method
SS	Sampling Scope
CM	Current Measurements
TO	Transient interruption of Output signal
LD	Level Discriminator

(PRN) bit sequence to the DUT, and then subsequently to the error analyzer. The clock signal is sent to both the DUT (if it is a clocked circuit) and the error analyzer. The error analyzer uses a self-synchronizing PRN error detection scheme. If the data is found to be incorrect during the sampling window, a SET is counted. In this method, the original signal is not characterized, however, this is the only method applicable in some experimental conditions.

III. Accelerator Facilities

Experiments were preformed at a wide variety of accelerator facilities such as Tandem Van de Graaff accelerators to superconducting cyclotrons. The facilities that were used, along with their abbreviations, are given in Table 2.

Table 2: Accelerator Facilities

Facility	Abbr.
Brookhaven National Laboratories	BNL
Institut de Physique Nucleaire; Orsay France.	IPN
Cyclotron for High Energy Heavy Ions; Caen, France.	GANIL
Tandem Van de Graaff, University of Washington	UW
Texas A&M University- Cyclotron Institute	TAM
Michigan State University	MSU
Tandem Accelerator Super-Conducting Cyclotron, Chalk River Laboratory, Canada	CRL
Lawrence Berkeley Laboratory	LBL

IV. Data Organization

The scope of this paper is to summarize and collect previously published Single Event Transient Data in analog and digital devices from numerous authors. This compendium covers the period between 1980 to 2000. Photonic devices, which are substantially featured in the literature, will not be covered here.

Unfortunately, in most circuits, parameters such as peak pulse height and maximum pulse width are application specific and usually dependant on bias and load. Therefore only the reported threshold LET and saturation cross-section, and not pulse heights and widths are summarized. If the test method includes waveform capture, refer to the cited work for waveform details. The collected SET data is given in Table 3.

Table 3: SET Results.

Device	Mfg.	Function	Test Mth.	Test Fac.	σ_{sat}	LET_{Thres}	Notes	Rf
Converters								
AHE2815	Advanced Analog	DC-DC Converter	-	BNL	-	20-26	Tested both at inputs of 28V (350 mA), 34V (272mA)	9
AHF2812	AA	DC-DC converter	SS	BNL	-	<37	Output load effects whether a SET occurs	-6

Device	Mfg.	Function	Test Mth.	Test Fac.	σ_{sat}	LET_{Thres}	Notes	Ref
ASA2805S	AA	DC-DC converter	SS	BNL	-	<10	Output load effects whether a SET occurs	6
ATW2805	AA	DC-DC converter	SS	BNL	-	<37	Output load effects whether a SET occurs	6
AD536	Analog	RMS-DC converter	SS	BNL	$5x10^{-3}$	<1.4	+/-8 Volt Bias	1
7804	AA	DC-DC converter	SS	BNL	-	>37	No SETs observed, maximum LET used was 37	6
DAC8222	Analog	12-bit DAC	SS	BNL	$1x10^{-3}$	40 hi: 10 lo	+8 Volt Bias	1
MCH2805S	MDI	DC-DC Converter	-	BNL	-	>100	No SEE observed	12
MFL2805S	Interpoint	DC-DC Converter	-	BNL	-	>72	Tested with nominal inputs = 28V (125mA) output of 5 V, no SEE effects observed with LET_{MAX}=72	9
MFL2812S	Interpoint	DC-DC Converter	-	BNL	$5x10^{-6}$	50	Tested with nominal inputs = 28V (180mA) output of 12 V	9
MFL2815D	Interpoint	DC-DC Converter	-	BNL	-	45-59.7	Tested both with nominal inputs = 28V (410mA), and 34V (360mA) with dual output of 15 V	9
MFL2815S	Interpoint	DC-DC Converter	-	BNL	-	>72	Tested both with nominal inputs = 28V (240mA), and 34V (230mA) with an output of 15 V, no SEE effects observed with LET_{MAX}=72	9
MTR2805SF	Interpoint	DC-DC converter	SS	BNL	-	>82	21, 28, 35 Volt Bias at both low and high load conditions, No upsets observed at LETs used	1
MX7847TQ	Maxim	12-bit DAC		BNL	-	~10		6
Amplifiers								
A250	Amptek	Charge Sensitive Amp	CM	BNL	-	>90	SETs are application specific	7
AD524	Analog Devices	Amplifier	TO	BNL	$1x10^{-3}$	11.5	Input +5V peak to peak sine wave, with an operating current of 3.6mA	9
AD8001	ADI	OP Amp	LD	BNL	-	>82	σ dependant on discrimination levels	21-22
CLC449	National	OP Amp	CM	BNL	-	>60	+/-5 and +/-5.5 Volt V_s, 2 Volts V_{pp}, SET results are application specific.	7
EL2243	ELN	OP Amp	TO	BNL	$1x10^{-3}$	5	LET_{SEL}>110	4
HS3530RH	Harris	OP Amp	SS	LBL	$2x10^{-3}$	~3	σ_{sat} is dependent on input, LET_{th} is independent on input voltage.	11
LM108	National	OP Amp	SS	LBL	$\sim 8x10^{-3}$	<3	ΔV_{in} does not change cross-section and LET_{th}	10
LM108	Motorola	OP Amp	SS	IPN	$2x10^{-3}$ >.5V $8x10^{-3}$ >.2V	2	σ dependant on discrimination levels, gain did not effect results	13
LM108A	LTN	OP Amp	-	TAM	$6x10^{-4}$	<<7	Amplitude and width of transient pulse dependant on Vin	5
LM108AH	PMI	OP Amp	TO	BNL	$5x10^{-4}$	24	V_{CC}=±8V with an operating current = 0.7mA. LET_{SEL}~60	9
LM124	National	OP Amp	SS	PNI	$1x10^{-4}$	<1.7	Transient defined as DV =.10 Volts	16
OP05	PMI	OP Amp	SS	LBL	$7x10^{-4}$	<1	σ_{sat} is independent on input, LET_{th} is very dependant on input voltage.	11
OP07AJ	PMI	OP Amp	TO	BNL	-	11.5-13	Input +5V peak to peak sine wave, with an operating current of 1mA	9
OP-15	PMI	OP Amp	SS	LBL	$2x10^{-3}$	~2	σ_{sat} is independent on input, LET_{th} is very dependant on input voltage.	11
OP400	PMI	OP Amp	SS	BNL	-	~20	Transient defined as ΔV =.25 Volts	6
OP-42	Analog	OP Amp	SS	LBL	$\sim 2x10^{-3}$	<3	ΔV_{in} does not change cross-section and LET_{th}	10
PA07	APEX	High Power OP Amp	CM	BNL	-	>37	SETs are application specific.	7
RH1056	LTN	OP Amp	-	TAM	$1x10^{-3}$	2	0.5 Volts & Other Inputs, A reverse input polarity reverses output transient	5
RH1056	LTN	OP Amp	-	BNL	$1x10^{-3}$	1.45	Amplitude and width of transient pulse dependant on Vin	5
RH108A	LTN	OP Amp	-	TAM	$6x10^{-4}$	<<7	Very similar to LM108A	5

Device	Mfg.	Function	Test Mth.	Test Fac.	σ_{sat}	LET_{Thres}	Notes	Rf
LM218H	National	OP Amp	-	Cf-252			This fast op amp has a greater σ than MOT LM108	13
Comparators/Voltage Reference								
AD9696	Analog	Comparator	SS	LBL	~$1x10^{-5}$	<3	ΔV_{in} does not change cross-section and LET_{th}	10
HS139	Harris	Comparator	SS	BNL	-	>37	Only slightly sensitive on Bias	7
HS139RH	Harris	Comparator	SS	LBL/BNL	~10^{-4} to $1x10^{-3}$	10	Does not have a strong consistent dependence on input bias.	8
ICL7662MTV-4	Maxim	Voltage Converter	-	BNL	-	>80		12
LM111	National	Comparator	SS	BNL	$8 x10^{-6}$	-	Transients were effected by values of ΔV_{in} > 1Volt	14
LM111	National	Comparator	SS	LBL	$1x10^{-3}$ 15V $1x10^{-4}$ 10V $9x10^{-5}$ 5V	<3	ΔV_{in} changes cross-section and LET_{th} σ and LET_{th} @ ΔV=.05V	10
LM111	National	Comparator	SS	TAM	$2.8x10^{-4}$	<<7	LET=44 MeV/(mg/cm^2) Δv_{in}=25mV	15/5
LM111	National	Comparator	SS	TAM	$8.5x10^{-5}$	<<7	LET=7.3MeV/(mg/cm^2) Δv_{in}=25mV	15/5
LM111	Motorola	Comparator	SS	IPN	$2x10^{-4}$	2	σ dependant on discrimination levels V_{CC} = ± 5V	13
LM111H	National	Comparator	SS	LBL	$1x10^{-4}$	>10	ΔV=.05V, V_{cc}=±15V, transients predominately negative going pulses.	11
LM119	National	Comparator	SS	LBL	~$1x10^{-4}$	<3	ΔV_{in} does not change cross-section and LET_{th} V_{CC} = ± 15V	10
LM139	National	Comparator	TO	BNL	-	<10	Multiple transient sizes LET_{SEL}>37	6
LM139	National	Comparator	SS	BNL	$2x10^{-4}$ high $1x10^{-4}$ Low	20	LET_{th}, σ_{sat}, and output transient characteristics are a dependant on input bias. +/-7 Volt V_{cc}	7
LM139	National	Comparator	SS	LBL	~$5x10^{-3}$	<3	V_{cc} =13 V, 10V and 5V ΔV_{in} changes cross-section and LET_{th}	8
LM139	National	Comparator	SS	TAM	$5.9x10^{-4}$	-	LET=44 MeV/(mg/cm^2) Δv_{in}=25mV V_{cc} =±15 V	15
LM139	PMI	Comparator	SS	TAM	$7x10^{-4}$	-	LET=44 MeV/(mg/cm^2) Δv_{in}=25mV V_{cc} =±15 V	15
LM139	PMI	Comparator	SS	TAM	$1x10^{-4}$	-	LET=7.3MeV/(mg/cm^2) Δv_{in}=25mV V_{cc} =±15 V	15
LM139	PMI	Comparator	SS	BNL	-	<<1.45	V_{cc}=±15 Volts, high output voltage.	15
LM139	PMI	Comparator	SS	BNL	-	<1.45	V_{cc}=±15 Volts, low output voltage.	15
LM139	National	Comparator	-	BNL	$2x10^{-5}$, @LET=100	50	No SEL for LET>110 at $1x10^6$ ions/cm^2	21
LM140	National	Comparator	SS	TAM	$1.5x10^{-4}$	-	LET=7.3MeV/(mg/cm^2) Δv_{in}=25mV	15
LM140	National	Comparator	SS	BNL	-	2	Vcc=25 Volts	15
LP365	National	Comparator	SS	BNL	$1x10^{-3}$	<3	ΔV_{in} changes cross-section and LET_{th}	14
PM139	Analog	Comparator	SS	BNL	$2x10^{-4}$	<10	ΔV_{in} changes cross-section and LET_{th}	14
REF-02	Analog	Voltage Reference	SS	LBL	~$8x10^{-4}$	<3	Changes in ΔV_{in} was not measured	10
Transceivers								
AX3411	AFX	Transceiver	TO	BNL	$3x10^{-4}$, @LET=80	<11.5	Supply=15V	4
AX3453	AFX	Transceiver	TO	BNL	$5x10^{-5}$, @LET=80	<11.5	Supply=5V	4
CT1487D	MED	Transceiver	TO	BNL	$5x10^{-5}$	11.5	Supply=15V, SEL LET_{TH}>80	4
CT2521	MED	Transceiver	TO	BNL	$4.5x10^{-4}$	<26.5	Supply=5V	4/21
63125	DDC	Transceiver	TO	BNL	$3x10^{-4}$	14	Supply=15V	4/21
FC1553921	STC	Transceiver	-	BNL	$2x10^{-3}$	<11.5	Supply=5V, SEL LET_{TH}>80	4

Device	Mfg.	Function	Test Mth.	Test Fac.	σ_{sat}	LET_{Thres}	Notes	Rf
M63147	UTM/MIR	Transceiver	-	BNL	$1x10^{-4}$	<11.5	Supply=5V, SEL LET_{TH}>80	4
NH1500	National	Transceiver	-	BNL	$6x10^{-6}$	<11.5	Supply=15V, SEL LET_{TH}>80	4
NH1529	National	Transceiver	-	BNL	$1.5x10^{-5}$	<11.5	Supply=5V, SEL LET_{TH}>80	4
UT63M124-BPC	UTM	Transceiver	-	-	-	11		5
UT63M125	UTM	Transceiver	-	BNL	$3x10^{-4}$, @LET=80	<11.5	Supply=15V	4
UTMC63M125	UTM	Transceiver	-	BNL	-	11		21
74FTC163245PV	IDT	Transceiver	-	BNL	None at LET < latchup threshold		Supply=5V, SEL LET_{TH}<22.5	21
Other								
100307	National	XOR	TO	CRL/BNL	-	-	σ and LET_{th} dependant with Data Frequency	2
100324	National	TTL to ECL Translator	TO	CRL/BNL	-	-	σ and LET_{th} dependant with Data Frequency	2
100325	National	ECL to TTL Translator	TO	CRL/BNL	-	-	σ and LET_{th} dependant with Data Frequency	2
100331	National	D Flip Flop	TO	CRL/BNL	-	-	σ and LET_{th} dependant with Data Frequency	2
932665	National	8k X 8 PROM	LD	LBL	-	-	Pulse width versus upset per bit day.	3
26C31	National	Line Driver	-	UW?	-	-	No SEE observed LET_{MAX}>80	4
26C32	National	Line Receiver	-	UW?	-	-	No SEE observed LET_{MAX} >80	4
26LS31	National	Quad Diff. Line Driver	LD	LBL	-	15	Pulse width versus upset per bit day.	3
26LS32	National	Quad Diff. Line Receiver	LD	LBL	-	<15	Pulse width versus upset per bit day.	3
54HCS244	Marconi	Octal line Driver/Receivr	LD	LBL	-	<40	Pulse width versus upset per bit day.	3
54LS05	National	Hex Inverter	LD	LBL	-	74	Pulse width versus upset per bit day.	3
54LS14	Signetics	Hex Inverter	LD	LBL	-	74	Pulse width versus upset per bit day.	3
88C20	National	Diff. Line Receiver	-	BNL	$1x10^{-5}$	11		4
88C30	National	Diff. Line Driver	-	BNL	-	>120		4
AD565A	Analog Devices	DAC	TO	BNL	-	>80	Tested both with nominal inputs = ±12V (+5mA/-20mA), no SEE effects observed with LET_{MAX}=80	9
AD783SQ	Analog	Sample and Hold	SS	BNL	$1x10^{-4}$	7	Pulse widths typically <2μs, Pulse heights between 0.4-1 Volts and as some as large as 2-3 Volts	7
AM29LV800	AMD	Flash Memory	CM	MSU	$2x10^{-6}$	<5	SETs were high current transients, possibly upset producing events	1
DAC08AQ	Analog Devices	DAC	TO	BNL	$1.9x10^{-2}$	3.5	Tested with a nominal I_{CC}=6mA	9
HI-509	Analog Mux	Analog Mux/demux	SS	BNL	-	>60	+/-9 and +/-15 Volt Bias No upsets observed at LETs used	1
HS26C31	Harris	Diff. Line Driver	-	BNL	-	>80	No SEE LET>80	4
HS26C32	Harris	Diff. Line Receiver	-	BNL	-	>80	No SEE LET>80	4
HS5212	Analog Devices	DAC	TO	BNL	$1x10^{-3}$	2	SEL Measurements (LET_{Th}>80 σ_{Sat}~$1x10^{-7}$ cm^2)	9
M3G2805D	Magnitude-3	DC-DC converter	SS	BNL	-	>82	35 and 21 Volt Bias at 0.5 Amp and 3.0 Amp Loads, No SETs observed	1
MC68000	Motorola	Microprocessor	TO	Neutrons	$7x10^{-13}$	-	Only 1 transient recorded, with a fluence of 1.38×10^{12} $1/cm^2$	17
MSA0670	HP	MMIC Amplifier	-	BNL	-	>85	7.93 and 8.03 Volts power supply, V_{in} = 0.5 Volts at 150MHz	7
Q3216	Qualcom	PLL Frequency Synthesizers	TO	LBL	$1x10^{-3}$	>1	Phase cross-sections in serial mode at both 1.0 and 1.5 GHz	18

Device	Mfg.	Function	Test Mth.	Test Fac.	σ_{sat}	LET_{Thres}	Notes	Rf
Q3216	Qualcom	PLL Frequency Synthesizers	TO	LBL	$3x10^{-4}$	>1	Frequency cross-sections in serial mode at both 1.0 and 1.5 GHz	18
Q3216	Qualcom	PLL Frequency Synthesizers	TO	LBL	$1x10^{-3}$	>1	Phase cross-sections in parallel mode at both 1.0 and 1.5 GHz	18
Q3236	Qualcom	PLL Frequency Synthesizers	TO	LBL	$1x10^{-3}$	>1	Phase cross-sections in serial mode at both 1.0 and 1.5 GHz	18
Q3236	Qualcom	PLL Frequency Synthesizers	TO	LBL	$3x10^{-4}$	>1	Frequency cross-sections in serial mode at both 1.0 and 1.5 GHz	18
Q3236	Qualcom	PLL Frequency Synthesizers	TO	LBL	$1x10^{-3}$	>1	Phase cross-sections in parallel mode at both 1.0 and 1.5 GHz	18
QS3384DM	QSI	Bus Switch	-	BNL	-	-	1 MHz checkerboard input. No SEU's seen SEL LET_{Th}=15-18	12
SG1549	Silicon General	Current Sense Latch	SS	LBL	$\sim 5x10^{-4}$	<3	ΔV_{in} changes cross-section and LET_{th}	10
TC4428	TCS	MOSFET Driver	-	TAM	-	-	SEL Measurements (LET_{Th}=24 $\sigma_{Sat}\sim 1x10^{-8}$ cm^2)	5
TSC4429	TEL	MOSFET Driver	-	BNL	-	>120	SEL LET_{TH}>120	4
UC1802	UTR	PWM	-	LBL	$5x10^{-4}$	1		19
UC1806	Unitrode	Pulse Width Modulator	SS	BNL	$6x10^{-4}$	8	Transients recorded in Static Mode	20
UC1825A	Unitrode	PWM	-	LBL	$1x10^{-2}$	1		19
UC1845A	UTR	PWM	CM	LBL	$2x10^{-4}$	1		19
UCC1802	Unitrode	PWM Controller	CM	LBL	$5x10^{-4}$	1		19

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