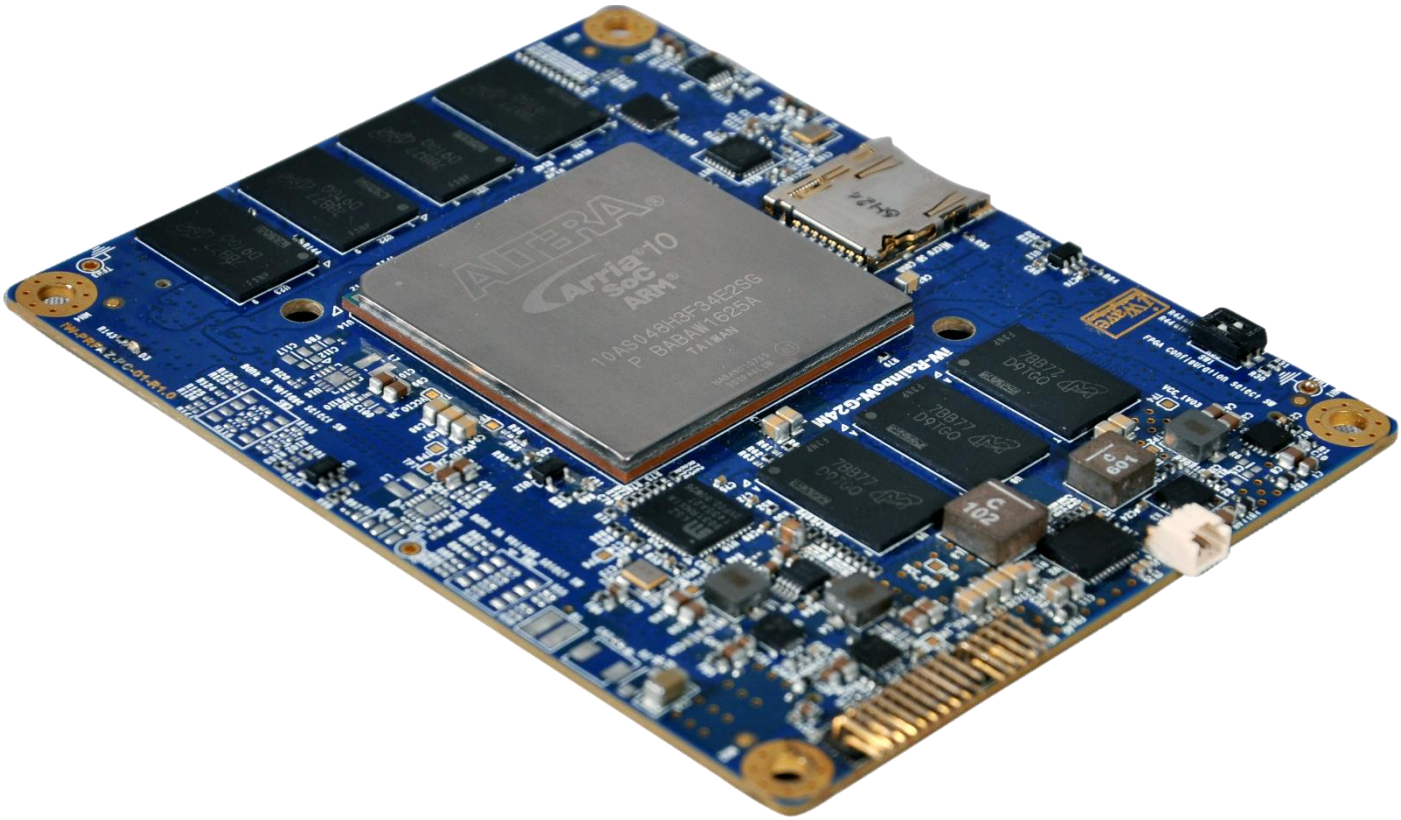
iW-RainboW-G24M
Arria10 SoC/FPGA SOM
Hardware User Guide



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1.1	22nd Jan 2018	Updated Version
1.2	23rd Feb 2018	• Block Diagram and SOM Images are updated. • **Table 7** FPGA AS Header termination details are added. • Expansion Connector2 pinout details are updated in **Table 11** for Pin 31, 46, 48, 69 and 71. • Arria10 SoC HPS IOMUX **Table 12** pinout details are updated for I2C0 and GPIO 12 and 13.

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Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Arria10 SoC/FPGA System On Module based on the Intel's Arria10 SoC or FPGA. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Arria10 SoC/FPGA SOM from a Hardware Systems perspective.

1.2 Overview

The Arria10 SoC/FPGA SOM is an extension of Arria10 SoC/FPGA. The Arria10 SoC/FPGA SOM has a form factor of 95mm x 75mm and provides the functional requirements for an embedded application. Two 240pin high speed ruggedized terminal strip connectors provide the carrier board interface to carry all the I/O signals to and from the Arria10 SoC/FPGA SOM.

1.3 List of Acronyms

The following acronyms is used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
AS	Active serial
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
FPP	Fast Passive Parallel
GB	Giga Byte
Gbps	Gigabits per sec
GHz	Giga Hertz
GPIO	General Purpose Input Output
HPS	Hard Processor System
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
PCB	Printed Circuit Board
PS	Passive Serial

Acronyms	Abbreviations
ROHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SD	Secure Digital
SoC	System On Chip
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Arria10 Device Handbook
- Arria10 Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Arria10 SoC/FPGA SOM features and Hardware architecture with high level block diagram. Also this section provides detailed information about two Expansion connector's pin assignment and usage.

2.1 Arria10 SoC/FPGA SOM Block Diagram

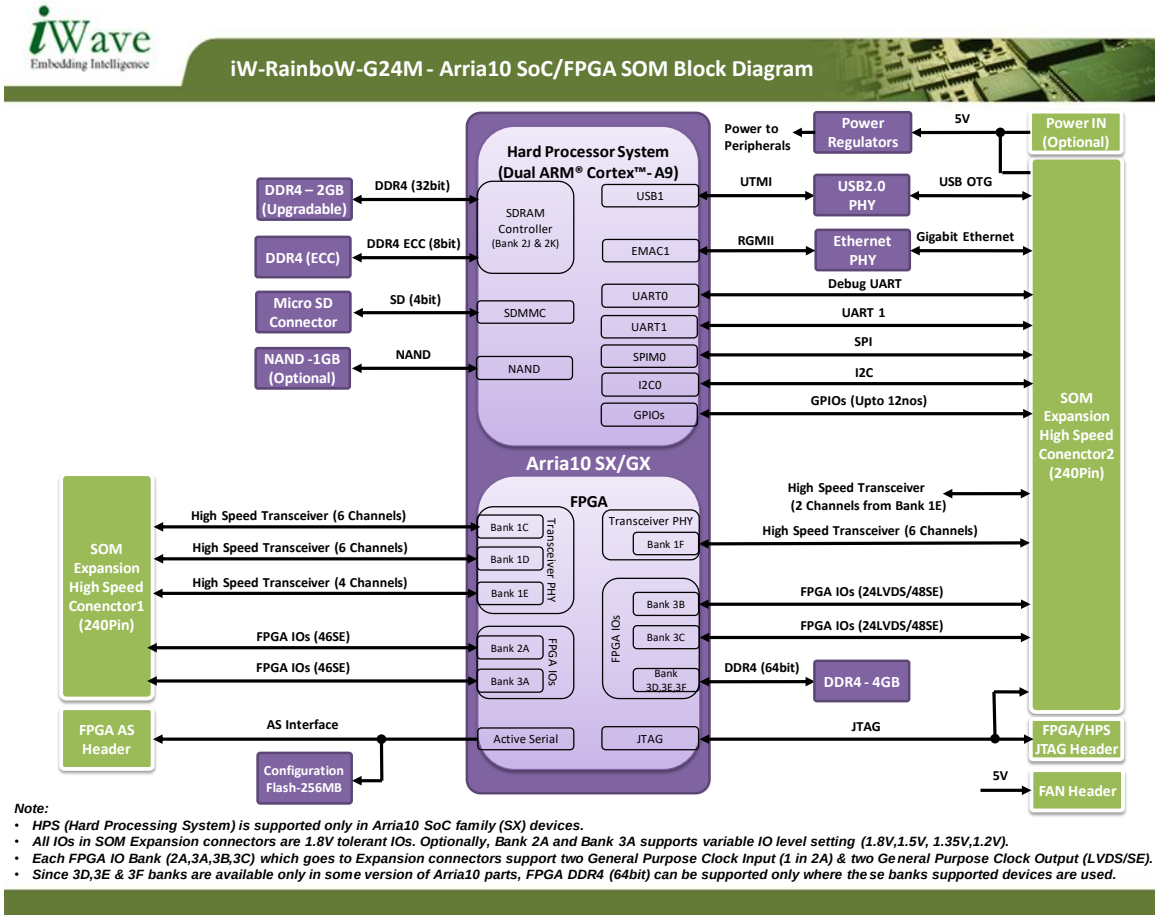

Figure 1: Arria10 SoC/FPGA SOM Block Diagram

2.2 Arria10 SoC/FPGA SOM Features

The Arria10 SoC/FPGA SOM supports the following features.

SoC/FPGA

- Intel's Arria10 SoC/FPGA
  - Compatible Arria10 SoC Family - SX270, SX320, SX480, SX570, SX660
    With upto 660K Logic Elements, 24 High Speed Transceivers and integrated Dual Core ARM Cortex –A9 @ upto 1.5 GHz/Core Hard Processor System (HPS).
  - Compatible Arria10 FPGA Family - GX270, GX320, GX480, GX570, GX660, GX900, GX1150
    With upto 1150K Logic Elements and 24 High Speed transceivers
- FPGA Configuration Selection Switch

Memory

- 2GB DDR4 SDRAM (32bit) with ECC for HPS (Expandable) [1, 2]
- 4GB DDR4 RAM (64bit) from FPGA [3]
- MicroSD Connector for HPS booting [1, 4]
- NAND Flash for HPS booting (Optional) [1, 4]
- Configuration Flash for FPGA (Optional)

Other On-SOM Features

- JTAG Header
- FAN Header
- FPGA AS Header

Expansion Connector1 Interfaces

- FPGA High Speed Transceivers (upto 17.4Gbps) x 18
- FPGA IOs & General Purpose Clocks - Bank2A
  - Upto 46 Single Ended IOs
  - One General Purpose Clock Input LVDS Pair/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended
- FPGA IOs & General Purpose Clocks – Bank3A
  - Upto 47 Single Ended IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended

Expansion Connector2 Interfaces

From HPS Block: [1, 5]

- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY)
- USB OTG x 1 Port (through On-SOM USB ULPI PHY)
- Debug UART (UART0) x 1 Port
- Data UART (UART1) x 1 Port (With CTS & RTS)
- SPI x 1 Port
- I2C x 1 Port
- HPS GPIOs
- HPS Warm Reset

From FPGA Block:

- FPGA High Speed Transceivers (upto 17.4Gbps) x 6
- FPGA IOs & General Purpose Clocks – Bank3B
  - Upto 24 LVDS IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended
- FPGA IOs & General Purpose Clocks – Bank3C
  - Upto 24 LVDS IOs
  - Two General Purpose Clock Input LVDS Pairs/Single Ended
  - Two General Purpose Clock Output LVDS Pairs/Single Ended
- JTAG Interface

General Specification

- Power Supply : 5V
- Form Factor : 95mm x 75mm

[1] In Arria10 SoC/FPGA SOM, these interfaces can be supported only if Arria10 "SoC" family devices are used which supports Hard Processor System (HPS).

[2] In Arria10 SoC/FPGA SOM, if Arrai10 SoC family device is not used and FPGA family device is used, then also 32bit DDR4 can be supported from FPGA fabric.

[3] This FPGA DDR4 interface is not supported in lower device configurations of Arria10 SoC/FPGA devices (SX270, GX270, SX320 and GX320) based SOM.

[4] In Arria10 SoC/FPGA SOM, these interfaces can be supported only if Arria10 "SoC" family devices are used because these interfaces are supported through Dedicated I/O pins of Hard Processor System (HPS).

[5] In Arria10 SoC/FPGA SOM, if Arrai10 "SoC" family device is not used and "FPGA" only family device is used, then these Shared I/O interfaces cannot be used. But the same pins can be used as FPGA Bank2L from FPGA fabric.

2.3 Arria10 SoC/FPGA

The Arria10 SoC/FPGA SOM is based on Intel's Arria10 family devices with F34 package (1,152 pins, 35 mm x 35 mm). Intel's Arria10 family devices comes with FPGA alone devices and FPGA + HPS supported devices (which is called as SoC). The Arria10 SoC/FPGA comes with three different FPGA fabric speed grade supported devices and different power options. Also its high speed transceivers comes with four different speed grade supported devices.

The Arria10 SoC devices supports Dual Core ARM Cortex-A9 core up to 1.5 GHz speed/core. The Dual ARM Cortex-A9 core with FPGA fabric allows greater flexibility for the system designers and helps lower the system cost and power consumption. This improved logic integration with a rich feature set of embedded peripherals, hardened floating point variable precision DSP blocks, embedded high speed transceivers, hard memory controllers and protocol intellectual property controllers which is ideal for cost-sensitive high end applications. The Block Diagram of Arria10 SoC from the datasheet is shown below for reference.

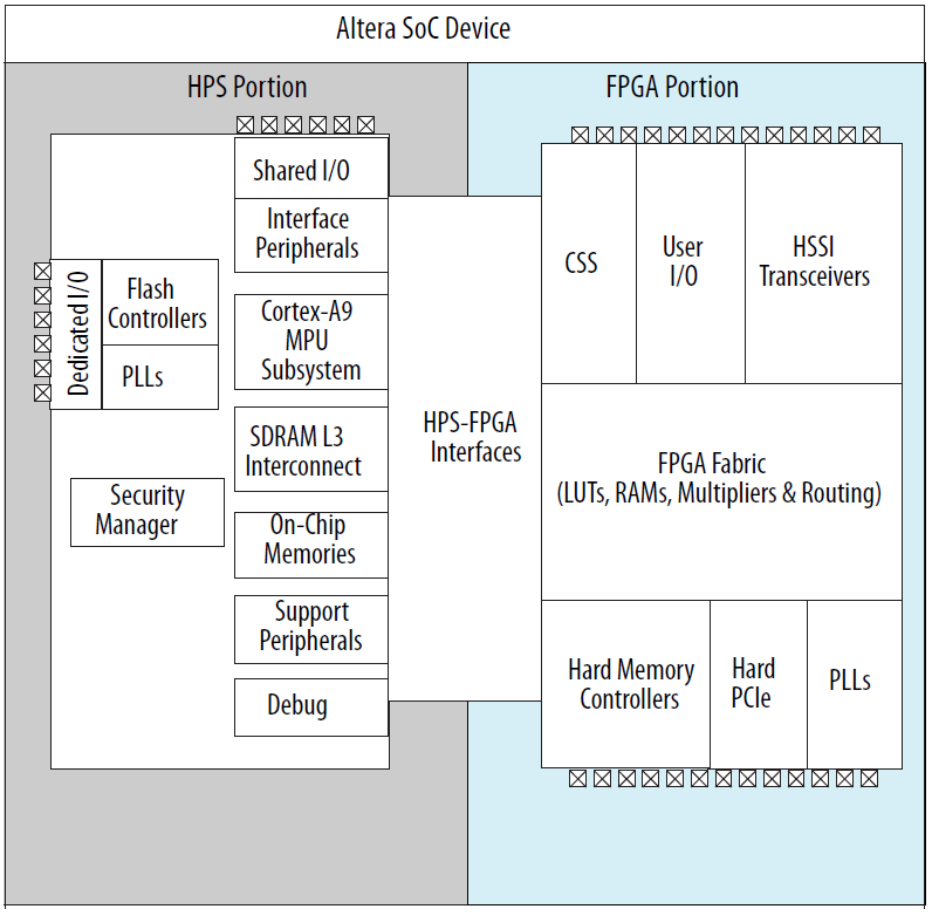

Figure 2: Arria10 SoC Simplified Block Diagram

Note: Please refer the latest Arria10 SoC/FPGA datasheet from Intel website for Electrical & Switching characteristics which may be revised from time to time.

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2.3.1 Arria10 SoC/FPGA Reference Clocks

The Arria10 SoC/FPGA SOM supports on board clock oscillators for reference clock input to different blocks of Arria10 SoC/FPGA. These reference clock details are mentioned in the below table.

Table 3: Arria10 SoC/FPGA SOM Reference Clocks

Sl No	On-SOM Oscillator Frequency	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
1	25MHz	HPS_CLK1/ B16	1.8V, LVCMOS	25Mhz single ended reference clock for HPS.
2	200Mhz/ 267MHz/ 300MHz	CLK_2K_1p/E23 & CLK_2K_1n/E24	1.8V, LVDS	LVDS reference clock for HPS DDR4. *Note: Reference clock will vary depend upon the speed grade of FPGA and so please check with iWave for exact reference clock used in the particular SOM.*
3	50MHz	CLK_2A_1p/ AM15	1.8V, LVCMOS	25Mhz single ended reference clock for FPGA. This is connected to Bank2A General Purpose Clock Input pin.
4	100MHz	CLKUSR/ AK16	1.8V, LVCMOS	100Mhz single ended reference clock for FPGA High Speed Transceiver. This is connected to Bank2A CLKUSR pin.
5	200Mhz/ 267MHz/ 300MHz	CLK_3E_1p/F6 & CLK_3E_1n/F5	1.8V, LVDS	LVDS reference clock for FPGA DDR4. This is connected to Bank3E General Purpose Clock Input pin. *Note: Reference clock will vary depend upon the speed grade of FPGA and so please check with iWave for exact reference clock used in the particular SOM.*

2.3.2 Arria10 SoC/FPGA Power & Reset

In Arria10 SoC/FPGA SOM, Core voltage & Periphery circuitry power supply of Arrai10 HPS & FPGA (VCC, VCCP, VCCERAM & VCCL_HPS) is fixed to 0.95V. The HPS I/O voltage (VCCIO_HPS) is fixed to 1.8V. The I/O voltage details of each FPGA Bank & High speed transceiver is mentioned in the corresponding section.

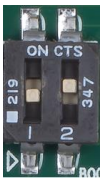
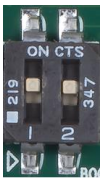
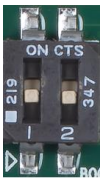
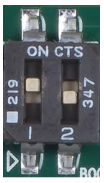
The Arria10 SoC/FPGA SOM supports on board Power On Reset circuit for HPS block POR and connected to HPS_nPOR pin. By default, standard POR delay is supported in Arria10 SoC/FPGA SOM. Also the same POR is connected to FPGA Bank3A AN7 pin for FPGA fabric usage if needed.

2.3.3 Arria10 SoC/FPGA Configuration Scheme

The Arria10 SoC/FPGA supports different configuration schemes JTAG-based configuration, AS Fast or Standard POR configuration and PS/FPP Fast or Standard POR configuration. These configuration scheme is selected using the MSEL pin setting.

The Arria10 SoC/FPGA SOM supports FPGA Configuration Selection Switch (SW1) to set the required FPGA configuration scheme. This Configuration Selection Switch features are shown below.

Table 4: Configuration Selection Switch Truth Table

Arria10 SoC/FPGA Configuration Scheme	POR Delay	SW1 (2 Position Switch)		
		POS1 (MSEL0)	POS2 (MSEL1)	Image
AS (x1 and x4)	Fast	OFF	ON	
AS (x1 and x4)	Standard	ON	ON	
PS and FPP (x8, x16, and x32)	Fast	OFF	OFF	
PS and FPP (Configuration Via HPS) **(Default)**	Standard	ON	OFF	
JTAG-based configuration	-	-	-	Use any of the above valid MSEL pin settings
OFF – Low (0)		ON – High (1)		

Note: MSEL2 pin is fixed to 0 (Low) in the Arria10 SoC/FPGA SOM hardware.

2.4 Memory

2.4.1 DDR4 SDRAM with ECC for HPS/FPGA

The Arria10 SoC SOM supports 32bit, 2GB DDR4 SDRAM from HPS. Two 16bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 2GB for HPS. Also Arria10 SoC SOM supports 8bit ECC for RAM memory. In Arria10 SoC SOM, Bank2J & Bank2K is used for HPS DDR4 interface. DDR4 devices operates at 1.2V voltage level and so I/O voltage for Bank2J & Bank2K is fixed to 1.2V. The Arria10 SoC SOM supports LVDS Oscillator on board for HPS DDR4 reference clock. DDR4-SDRAM ICs are physically located on top side of the SOM. In Arria10 FPGA only SOM (where HPS is not available), DDR4 can still be used from FPGA fabric through Bank2J & Bank2K.

Note: The RAM size can be expandable in Arria10 SoC/FPGA SOM and contact iWave for more details.

2.4.2 DDR4 SDRAM for FPGA

The Arria10 SoC/FPGA SOM supports 64bit DDR4 SDRAM through FPGA fabric. Four 16bit DDR4 SDRAM ICs are used to support RAM memory. These DDR4-SDRAM ICs are physically located on top side of the SOM. The Arria10 SoC/FPGA SOM supports LVDS Oscillator on board for FPGA DDR4 reference clock and connected to Bank3E F5 & F6 dedicated clock input pins.

These DDR4 ICs are connected to FPGA Banks 3D, 3E & 3F of Arria10 SoC/FPGA and hence are only supported in higher device configurations of Arria10 SoC/FPGA devices (SX480/GX480, SX570/GX570, SX660/GX660, GX900, GX1150). The DDR4 SDRAM devices operates at 1.2V voltage level and so I/O voltage for Banks 3D, 3E & 3F is fixed to 1.2V.

2.4.3 MicroSD Connector for HPS booting

The Arria10 SoC has dedicated I/O pins for boot devices and other commonly-used peripherals from HPS. The Arria10 SoC SOM uses these dedicated I/O pins to connect MicroSD connector for default boot device. If Micro SD is not required as boot media, then same dedicated pins can be used to connect the NAND Flash for boot.

MicroSD Card connector (J2) is connected to SD Controller of the Arria10 SoC through dedicated pins. It also supports card detect feature using HPS Dedicated IO “GPIO2_IO13”. The main power to MicroSD Connector is 3.3V Voltage. A voltage Level translator is used to translate the SoC compatible 1.8V signals to 3.3V signals on MicroSD connector. Micro SD connector is physically located on topside of the SOM as shown below.

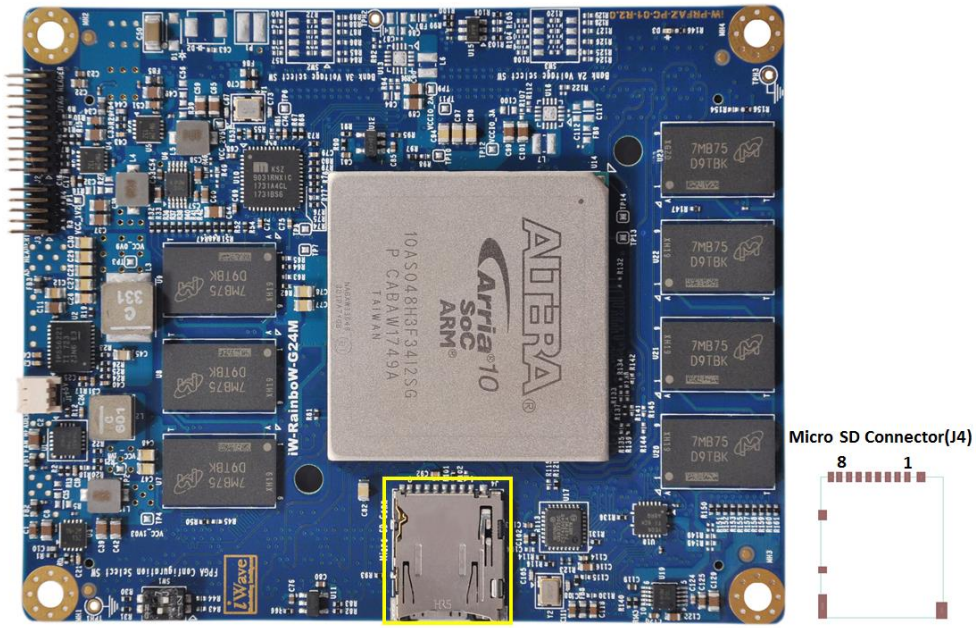


Figure 3: Micro SD Connector

2.4.4 NAND Flash for HPS booting (Optional)

The Arria10 SoC SOM supports NAND Flash as an optional boot device. This is connected to NAND Flash controller of the Arria10 SoC through dedicated pins and operates at 1.8V Voltage level. The NAND Flash memory is physically located on the bottom side of the SOM. This is the optional feature and will not be populated in the default configuration.

2.4.5 Configuration Flash for FPGA

The Arria10 SoC/FPGA SOM supports Serial Flash for FPGA configuration. This configuration Flash is connected to Active Serial (AS) memory interface of the Arria10 SoC/FPGA and operating at 1.8V Voltage level. It supports AS x1 and AS x4 modes and can be programmed using the AS programming interface or JTAG interface.

Using the AS programming interface, the configuration data is programmed into the configuration Flash by the Quartus Prime software or any supported third-party software. Using the JTAG interface, an Altera IP called the SFL IP core must be downloaded into the Arria10 device to form a bridge between the JTAG interface and the configuration Flash which allows the configuration Flash to be programmed directly using the JTAG interface. The configuration Flash is physically located on bottom of the SOM.

2.5 On-SOM Features

2.5.1 JTAG Header

The Arria10 SoC/FPGA SOM supports a customized 20-pin ARM JTAG connector for JTAG debug interface. Arria10 SoC/FPGA's JTAG interface pins are 1.8V tolerant and so 1.8V reference power is provided to pin1 of the JTAG connector. This allows the JTAG tool to automatically configure the logic signals to the right voltage.

The Arria10 HPS and FPGA share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Arria10 device. During power on-reset, the JTAG and all debug fuses are read by the Configuration subsystem to determine if the JTAG to the FPGA or HPS is bypassed. These JTAG interface signals are also connected to Expansion connector2 to access from carrier board. The JTAG connector (J2) is physically located on topside of the SOM as shown below.

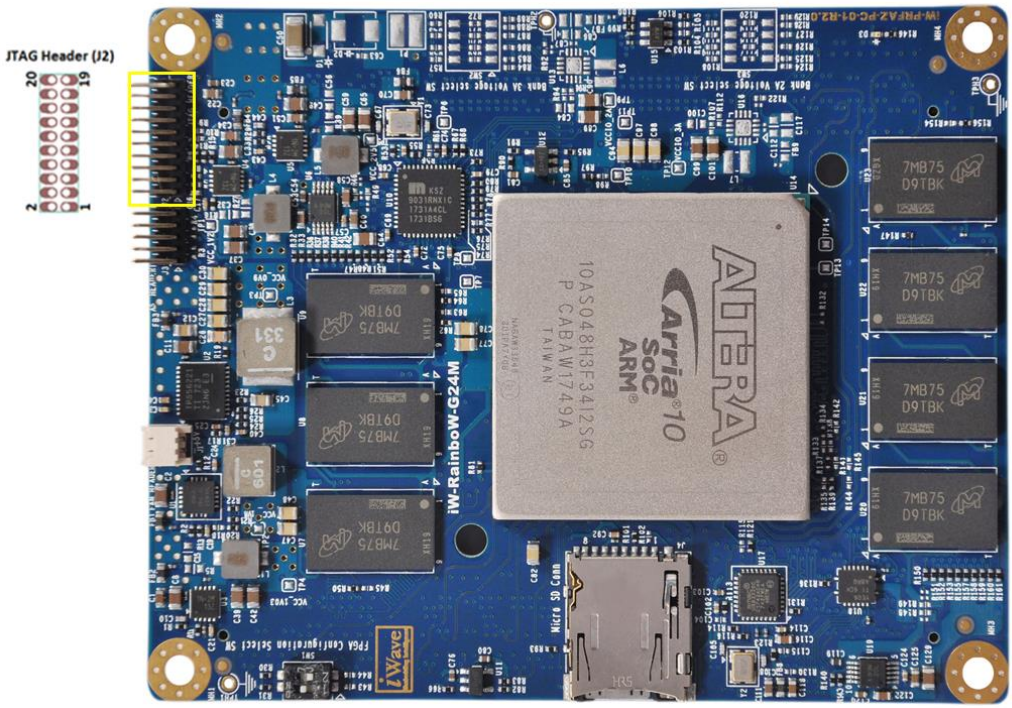


Figure 4: JTAG Header

Number of Pins	- 20
Connector Part	- GRPB102MWCN-RC from Sullins Connector Solutions
Mating Connector	- LPPB102CFFN-RC from Sullins Connector Solutions

Table 5: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_1V8	O, 1.8V Power	VTREF Voltage Reference.
2	VCC_1V8	O, 1.8V Power	Supply Voltage.
3	CSS_TRST	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground.
5	CSS_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
6	GND	Power	Ground.
7	CSS_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground.
9	CSS_TCK	I, 1.8V CMOS	JTAG test Clock.
10	GND	Power	Ground.
11	-	-	NC.
12	GND	Power	Ground.
13	CSS_TDO	O, 1.8V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 1.8V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	I, 1.8V CMOS/ 10K PU	This pin is just pulled up.
18	GND	Power	Ground.
19	-	-	Default NC.
20	GND	Power	Ground.

2.5.2 Fan Header

The Arria10 SoC/FPGA SOM supports a Fan Header to connect cooling Fan if required. Also in SOM there are mounting holes in either side of the Arria10 SoC/FPGA device which can be used to fix the Fan. This Fan Header (J1) is physically located at the top of the board as shown below.

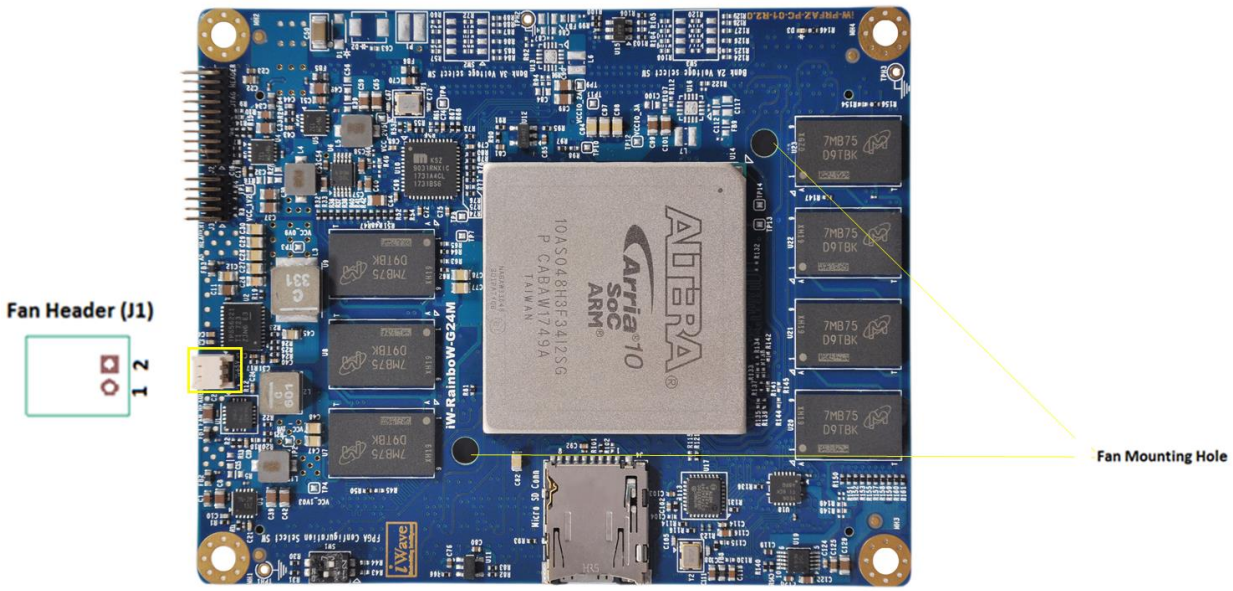


Figure 5: Fan Header

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

Compatible FAN (Example) - AFB0505MB from Delta Electronics

Table 6: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.5.3 FPGA AS Header

The Arria10 SoC/FPGA SOM supports FPGA AS header for Active Serial Interface. This Active Serial Interface can be used to program the FPGA configuration Flash. Using this AS header, the external programmer serially transmits the operation commands and configuration bits to the configuration flash on Data0 using the download cable. During the verification, DATA1 transfers the programming data back to the download cable. This FPGA AS Header (J3) is physically located at the top of the board as shown below.

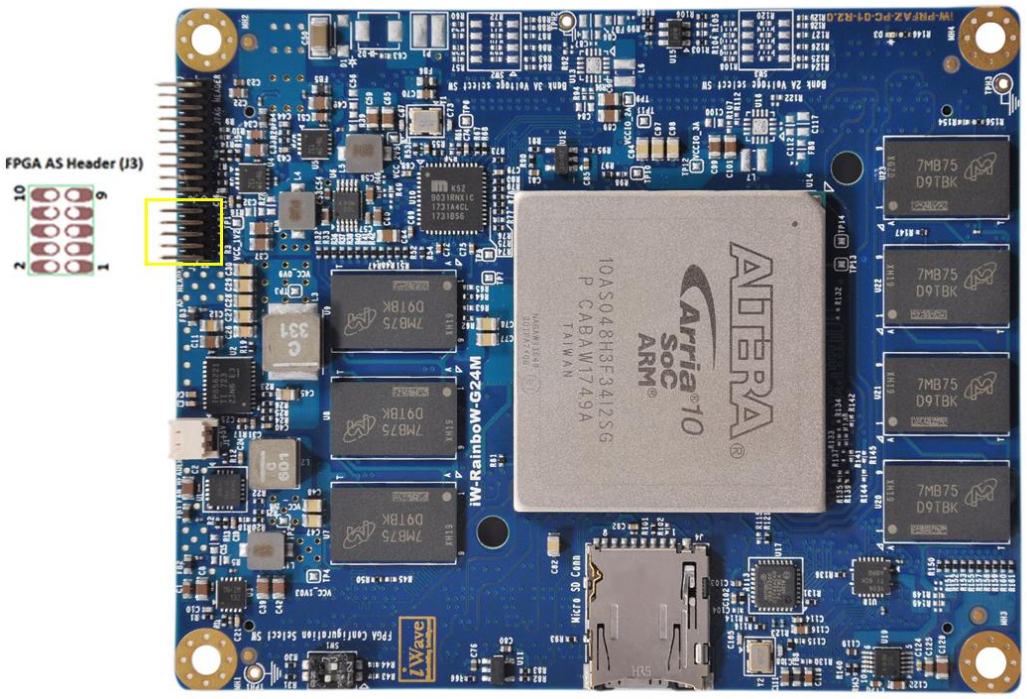


Figure 6: FPGA AS Header

Number of Pins - 10

Connector Part - GRPB052MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB052CFFN-RC from Sullins Connector Solutions

Table 7: FPGA AS Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	CSS_DCLK	I, 1.8V CMOS/10K PD	Dedicated Serial clock to configure flash.
2	GND	Power	Ground.
3	AS_CONFIG_DONE	IO, 1.8V OD/10K PU	Configuration status IO to Arria10 SoC/FPGA.
4	VCC_1V8	O,1.8V Power	Supply Voltage.
5	AS_CONFIG	I, 1.8V CMOS/10K PU	Configuration input to Arria10 SoC/FPGA.
6	CSS_nCE	I, 1.8V CMOS/10K PU	Chip Enable input to Arria10 SoC/FPGA.
7	CSS_AS_DATA0	I, 1.8V CMOS	Serial Data input to Configuration flash.
8	CSS_NCSO0	I, 1.8V CMOS/10K PU	Chip select input to configuration flash.
9	CSS_AS_DATA1	O, 1.8V CMOS	Serial Data output from configuration flash.
10	GND	Power	Ground.

2.6 Expansion Connector1 Interfaces

The Arria10 SoC/FPGA SOM supports two 240pin High speed ground plane ruggedized terminal strip connectors for interfaces expansion. All the effort is made in Arria10 SoC/FPGA SOM design to provide the maximum interfaces of Arria10 SoC/FPGA to the carrier board by adding these two expansion connectors.

The interfaces which are available at Expansion Connector1 are explained in following sections.

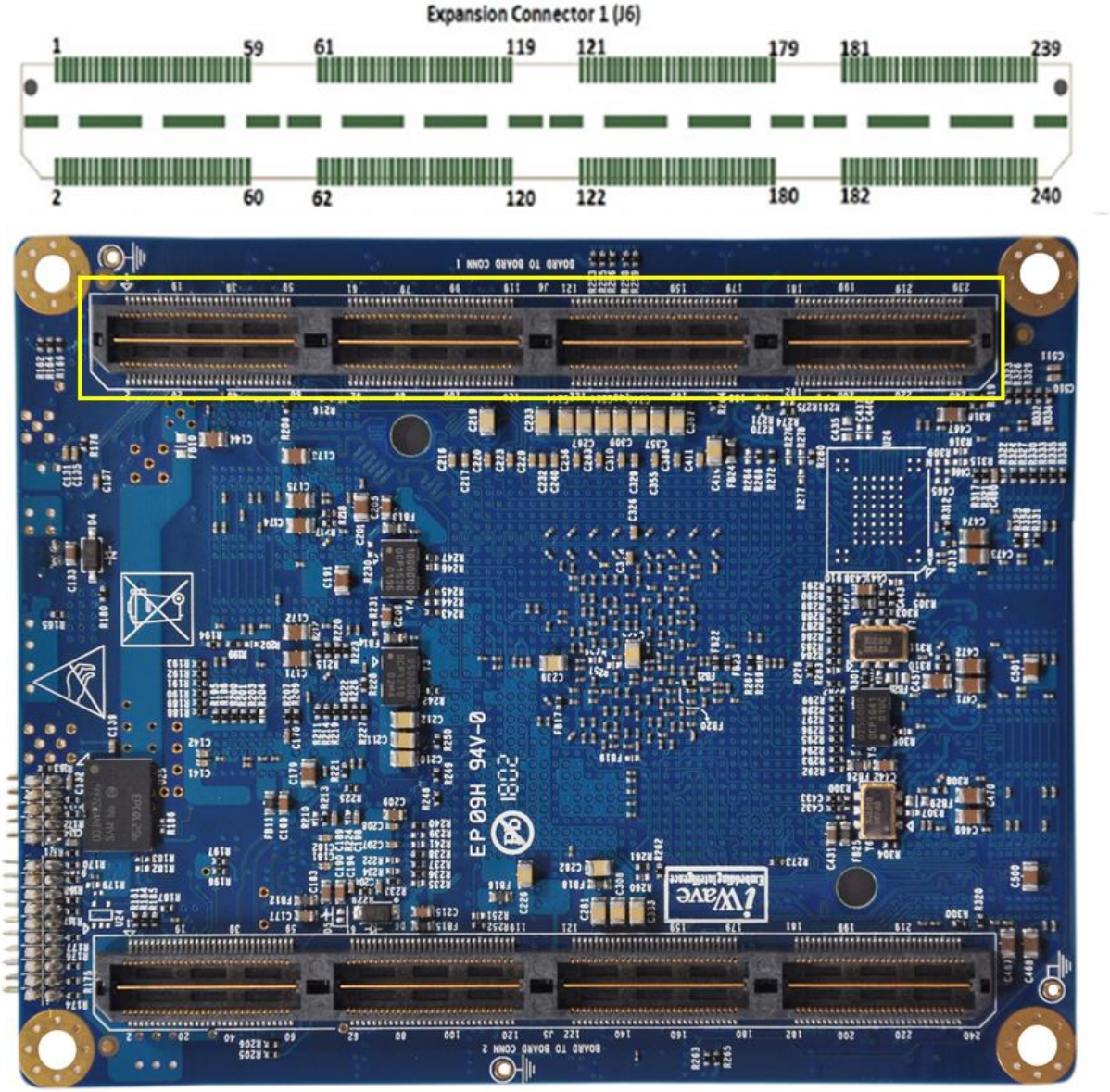


Figure 7: Expansion Connector1

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A

Mating Connector - QSH-120-01-L-D-A from Samtech

Staking Height - 5mm

2.6.1 FPGA High Speed Transceivers

The Arria10 SoC/FPGA SOM supports 24 high speed transceivers on Expansion connectors from Arria10 FPGA fabric. The Arria10 SoC/FPGA has four high speed transceiver banks (1C, 1D, 1E & 1F) and each transceiver bank has six high speed transmit and receive channels. Also each high speed transceiver bank supports two reference clock input pairs. Transceiver data rate performance is based on the transceiver speed grade of the Arria10 SoC/FPGA as mentioned in the below table.

Table 8: Arria10 SoC/FPGA Transceiver data rate performance

Description	Transceiver Speed Grade 1 (Gbps)	Transceiver Speed Grade 2 (Gbps)	Transceiver Speed Grade 3 (Gbps)	Transceiver Speed Grade 4 (Gbps)
Chip-to-Chip	17.4	15	14.2	12.5
Backplane	12.5	12.5	12.5	10.3125

The Arria10 SoC/FPGA SOM supports 16 high speed transceiver channels (6 from Bank1C, 6 from Bank1D & 4 from Bank1E) along with two reference clock input pairs of each bank (Bank1C, Bank1D & Bank1E) on Expansion connector1 and 8 high speed transceiver channels (2 from Bank1E & 6 from Bank1F) along with two reference clock input pairs of Bank1F on Expansion conenctor2. In Arria10 SoC/FPGA SOM, on board termination and AC coupling capacitor are not supported on transceiver lines. So it has to be taken care in the carrier board if required.

In Arria10 SoC/FPGA SOM, Transceiver power to Arria10 SoC/FPGA is fixed to 1.03V. Also it supports 100MHz Oscillator on board for transceiver reference clock and connected to Bank2A AK16 CLKUSR pin. This CLKUSR pin can be used for configuration and transceiver calibration simultaneously. For transceiver calibration, CLKUSR must be a free-running clock running between 100 MHz to 125 MHz at power-up for PS/FPP configuration scheme. Transceiver calibration starts utilizing the CLKUSR during device configuration and may continue to use it even when the device enters user mode.

For more details, refer Expansion connector1 pins 3, 4, 5, 6, 9, 11, 15, 17, 21, 23, 37, 39, 43, 45, 49, 51, 55, 57, 63, 64, 65, 66, 69, 71, 75, 77, 81 & 83 for Transceiver Bank1C, 97, 98, 99, 100, 103, 105, 109, 111, 115, 117, 123, 125, 129, 131, 135, 137, 141, 143, 157, 158, 159, 160, 163, 165, 169, 171, 175 & 177 for Transceiver Bank1D, 183, 184, 185, 186, 189, 191, 195, 197, 201, 203, 217, 218, 219, 220, 223, 225, 229, 231, 235 & 237 for Transceiver Bank1E on ***Table 9.***

2.6.2 FPGA IOs & General Purpose Clocks – Bank2A

The Arria10 SoC/FPGA SOM supports upto 46 Single Ended IOs from Arria10 FPGA Bank2A on Expansion connector1. These Bank2A signals on Expansion connector1 is routed as single ended IOs in the board. If the LVDS IOs are required in these pins, it may also be configured even though the signals are routed as single ended IO. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Arria10 SoC/FPGA SOM, upon these 46 IOs from Arria10 FPGA Bank2A, one General Purpose Clock input LVDS pair and two General Purpose Clock Output LVDS pairs are supported on Expansion connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General Purpose single ended clock.

In Arria10 SoC/FPGA SOM, I/O voltage for Bank2A is fixed to 1.8V. It optionally supports variable I/O voltage for Bank2A pins through external variable voltage regulator and can support 1.8V, 1.5V, 1.35V and 1.2V I/O voltage. This variable voltage can be set through on board 4bit DIP switch option. This variable I/O voltage support for Bank2A is only the optional feature and will not be populated in the default configuration.

For more details, refer Expansion connector1 pins 128, 134, 136, 138, 147, 148, 149, 150, 151, 152, 153, 154, 164, 166, 168, 170, 172, 176, 178, 190, 192, 194, 196, 198, 202, 204, 207, 208, 209, 210, 211, 212, 213, 214, 224, 226, 228, 230, 236 & 238 for Bank2A IOs, 124, 126, 142 & 144 for Bank2A General Purpose Clock Output LVDS pairs, 130 & 132 for Bank2A General Purpose Clock input LVDS pair on ***Table 9.***

2.6.3 FPGA IOs & General Purpose Clocks – Bank3A

The Arria10 SoC/FPGA SOM supports upto 47 Single Ended IOs from Arria10 FPGA Bank3A on Expansion connector1. These Bank3A signals on Expansion connector1 is routed as single ended IOs in the board. If the LVDS IOs are required in these pins, it may also be configured even though the signals are routed as single ended IO. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps.

In Arria10 SoC/FPGA SOM, upon these 47 IOs from Arria10 FPGA Bank3A, two General Purpose Clock input LVDS pairs and two General Purpose Clock Output LVDS pairs are supported on Expansion connector1. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General Purpose single ended clock.

In Arria10 SoC/FPGA SOM, I/O voltage for Bank3A is fixed to 1.8V. It optionally supports variable I/O voltage for Bank3A pins through external variable voltage regulator and can support 1.8V, 1.5V, 1.35V and 1.2V I/O voltage. This variable voltage can be set through on board 4bit DIP switch option. This variable I/O voltage support for Bank3A is only the optional feature and will not be populated in the default configuration.

For more details, refer Expansion connector1 pins 10, 12, 14, 16, 18, 27, 28, 29, 30, 31, 32, 33, 34, 38, 40, 42, 44 ,46, 48, 50, 52, 70, 72, 74, 76, 78, 87, 88, 89, 90, 91, 92, 93, 94, 104, 106, 108, 110 & 112 for Bank3A IOs, 22, 24, 116 & 118 for General Purpose Clock Output LVDS pairs, 56, 58, 82 & 84 for General Purpose Clock input LVDS pairs on ***Table 9.***

Table 9: Expansion Connector1 Pin Assignment

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	NA	Power	Ground.
2	GND	NA	Power	Ground.
3	GXBL1C_TX_CH0p	GXBL1C_TX_CH0p/ AP32	O, DIFF	Bank1C High speed positive differential transmitter channel0. If unused leave this pin floating.
4	REFCLK_GXBL1C_CHTp	REFCLK_GXBL1C_CHTp /AD28	I, DIFF	Bank1C High speed differential reference clock positive receiver channel T. If unused connect this pin to GND.
5	GXBL1C_TX_CH0n	GXBL1C_TX_CH0n/ AP31	O, DIFF	Bank1C High speed negative differential transmitter channel0. If unused leave this pin floating.
6	REFCLK_GXBL1C_CHTn	REFCLK_GXBL1C_CHTn /AD27	I, DIFF	Bank1C High speed differential reference clock negative receiver channel T. If unused connect this pin to GND.
7	GND	NA	Power	Ground.
8	GND	NA	Power	Ground.
9	GXBL1C_TX_CH1p	GXBL1C_TX_CH1p/ AM32	O, DIFF	Bank1C High speed positive differential transmitter channel1. If unused leave this pin floating.
10	FPGA_AM7_LVDS3A_24n	LVDS3A_24n/ AM7	IO, 1.8V LVCMOS	Bank 3A User I/O Single ended pin.
11	GXBL1C_TX_CH1n	GXBL1C_TX_CH1n/ AM31	O, DIFF	Bank1C High speed negative differential transmitter channel1. If unused leave this pin floating.
12	FPGA_AM1_LVDS3A_16p	LVDS3A_16p/ AM1	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel16.
13	GND	NA	Power	Ground.
14	FPGA_AM2_LVDS3A_16n	LVDS3A_16n/ AM2	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel16.
15	GXBL1C_RX_CH1n	GXBL1C_RX_CH1n/ AJ29	I, DIFF	Bank1C High speed negative differential receiver channel1. If unused connect this pin to GND.
16	FPGA_AP4_LVDS3A_18p	LVDS3A_18p/ AP4	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel18.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
17	GXBL1C_RX_CH1p	GXBL1C_RX_CH1p/ AJ30	I, DIFF	Bank1C High speed positive differential receiver channel1. If unused connect this pin to GND.
18	FPGA_AN4_LVDS3A_18n	LVDS3A_18n/ AN4	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel18.
19	GND	NA	Power	Ground.
20	GND	NA	Power	Ground.
21	GXBL1C_RX_CH0n	GXBL1C_RX_CH0n/ AL29	I, DIFF	Bank1C High speed negative differential receiver channel0. If unused connect this pin to GND.
22	FPGA_AL3_LVDS3A_15n/CLKOUT_0n	LVDS3A_15n/ AL3	O, 1.8V LVDS	Bank3A Clock Output differential negative channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
23	GXBL1C_RX_CH0p	GXBL1C_RX_CH0p/ AL30	I, DIFF	Bank1C High speed positive differential receiver channel0. If unused connect this pin to GND.
24	FPGA_AM3_LVDS3A_15p/ CLKOUT_0p	LVDS3A_15p/ AM3	O, 1.8V LVDS	Bank3A Clock Output differential positive channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
25	GND	NA	Power	Ground.
26	GND	NA	Power	Ground.
27	FPGA_AM6_LVDS3A_17p	LVDS3A_17p/ AM6	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel17.
28	FPGA_AP6_LVDS3A_20n	LVDS3A_20n/ AP6	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel20.
29	FPGA_AM5_LVDS3A_17n	LVDS3A_17n/ AM5	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel17.
30	FPGA_AP7_LVDS3A_20p	LVDS3A_20p/ AP7	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel20.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
31	FPGA_AP5_LVDS3A_19p	LVDS3A_19p/ AP5	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel19.
32	FPGA_AL6_LVDS3A_14p	LVDS3A_14p/ AL6	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel14.
33	FPGA_AN5_LVDS3A_19n	LVDS3A_19n/ AN5	IO, 1.8V LVDS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel19.
34	FPGA_AK6_LVDS3A_14n	LVDS3A_14n/ AK6	IO, 1.8V LVDS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel14.
35	GND	NA	Power	Ground.
36	GND	NA	Power	Ground.
37	GXBL1C_TX_CH2p	GXBL1C_TX_CH2p/ AK32	O, DIFF	Bank1C High speed positive differential transmitter channel2. If unused leave this pin floating.
38	FPGA_AK7_LVDS3A_9p	LVDS3A_9p/ AK7	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel9.
39	GXBL1C_TX_CH2n	GXBL1C_TX_CH2n/ AK31	O, DIFF	Bank1C High speed negative differential transmitter channel2. If unused leave this pin floating.
40	FPGA_AK8_LVDS3A_9n	LVDS3A_9n/ AK8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel9.
41	GND	NA	Power	Ground.
42	FPGA_AJ6_LVDS3A_11n	LVDS3A_11n/ AJ6	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel11.
43	GXBL1C_TX_CH3p	GXBL1C_TX_CH3p/ AH32	O, DIFF	Bank1C High speed positive differential transmitter channel3. If unused leave this pin floating.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
44	FPGA_AJ7_LVDS3A_11p	LVDS3A_11p/ AJ7	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel11.
45	GXBL1C_TX_CH3n	GXBL1C_TX_CH3n/ AH31	O, DIFF	Bank1C High speed negative differential transmitter channel3. If unused leave this pin floating.
46	FPGA_AH7_LVDS3A_8p	LVDS3A_8p/ AH7	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel8.
47	GND	NA	Power	Ground.
48	FPGA_AG7_LVDS3A_8n	LVDS3A_8n/ AG7	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel8.
49	GXBL1C_RX_CH3n	GXBL1C_RX_CH3n/ AF31	I, DIFF	Bank1C High speed negative differential receiver channel3. If unused connect this pin to GND.
50	FPGA_AH8_LVDS3A_7p	LVDS3A_7p/ AH8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel7.
51	GXBL1C_RX_CH3p	GXBL1C_RX_CH3p/ AF32	I, DIFF	Bank1C High speed positive differential receiver channel3. If unused connect this pin to GND.
52	FPGA_AG8_LVDS3A_7n	LVDS3A_7n_/ AG8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel7.
53	GND	NA	Power	Ground.
54	GND	NA	Power	Ground.
55	GXBL1C_RX_CH2n	GXBL1C_RX_CH2n/ AG29	I, DIFF	Bank1C High speed negative differential receiver channel2. If unused connect this pin to GND.
56	FPGA_AL4_LVDS3A_13n/CLKIN_0n	LVDS3A_13n/ AL4	I, 1.8V LVDS	Bank3A Clock Input differential negative channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
57	GXBL1C_RX_CH2p	GXBL1C_RX_CH2p/ AG30	I, DIFF	Bank1C High speed positive differential receiver channel2. If unused connect this pin to GND.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
58	FPGA_AL5_LVDS3A_13p/CLKIN_0p	LVDS3A_13p/ AL5	I, 1.8V LVDS	Bank3A Clock Input differential positive channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
59	GND	NA	Power	Ground.
60	GND	NA	Power	Ground.
61	GND	NA	Power	Ground.
62	GND	NA	Power	Ground.
63	GXBL1C_TX_CH4p	GXBL1C_TX_CH4p/ AN34	O, DIFF	Bank1C High speed positive differential transmitter channel4. If unused leave this pin floating.
64	REFCLK_GXBL1C_CHBp	REFCLK_GXBL1C_CHBp /AF28	I, DIFF	Bank1C High speed differential reference clock positive receiver channel B. If unused connect this pin to GND.
65	GXBL1C_TX_CH4n	GXBL1C_TX_CH4n/ AN33	O, DIFF	Bank1C High speed negative differential transmitter channel3. If unused leave this pin floating.
66	REFCLK_GXBL1C_CHBn	REFCLK_GXBL1C_CHBn /AF27	I, DIFF	Bank1C High speed differential reference clock negative receiver channel B. If unused connect this pin to GND.
67	GND	NA	Power	Ground.
68	GND	NA	Power	Ground.
69	GXBL1C_TX_CH5p	GXBL1C_TX_CH5p/ AL34	O, DIFF	Bank1C High speed positive differential transmitter channel5. If unused leave this pin floating.
70	FPGA_AG10_LVDS3A_4p	LVDS3A_4p/ AG10	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel4.
71	GXBL1C_TX_CH5n	GXBL1C_TX_CH5n/ AL33	O, DIFF	Bank1C High speed negative differential transmitter channel5. If unused leave this pin floating.
72	FPGA_AF10_LVDS3A_4n	LVDS3A_4n/ AF10	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel4.
73	GND	NA	Power	Ground.
74	FPGA_AN8_LVDS3A_21p	LVDS3A_21p/ AN8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel21.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
75	GXBL1C_RX_CH5n	GXBL1C_RX_CH5n/ AD31	I, DIFF	Bank1C High speed negative differential receiver channel5. If unused connect this pin to GND.
76	FPGA_AM8_LVDS3A_21n	LVDS3A_21n/ AM8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel21.
77	GXBL1C_RX_CH5p	GXBL1C_RX_CH5p/ AD32	I, DIFF	Bank1C High speed positive differential receiver channel5. If unused connect this pin to GND.
78	FPGA_AL9_LVDS3A_23p	LVDS3A_23p/ AL9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin.
79	GND	NA	Power	Ground.
80	GND	NA	Power	Ground.
81	GXBL1C_RX_CH4n	GXBL1C_RX_CH4n/ AE29	I, DIFF	Bank1C High speed negative differential receiver channel4. If unused connect this pin to GND.
82	FPGA_AK9_LVDS3A_12n/CLKIN_1n	LVDS3A_12n/ AK9	I, 1.8V LVDS	Bank3A Clock Input differential negative channel1. Same pin can be configured as Single Ended Clock Input or User I/O.
83	GXBL1C_RX_CH4p	GXBL1C_RX_CH4p/ AE30	I, DIFF	Bank1C High speed positive differential receiver channel4. If unused connect this pin to GND.
84	FPGA_AJ9_LVDS3A_12p/CLKIN_1p	LVDS3A_12p/ AJ9	I, 1.8V LVDS	Bank3A Clock Input differential positive channel1. Same pin can be configured as Single Ended Clock Input or User I/O.
85	GND	NA	Power	Ground.
86	GND	NA	Power	Ground.
87	FPGA_AF9_LVDS3A_1p	LVDS3A_1p/ AF9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel1.
88	FPGA_AN9_LVDS3A_22n	LVDS3A_22n/ AN9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel22.
89	FPGA_AE9_LVDS3A_1n	LVDS3A_1n/ AE9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel1.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
90	FPGA_AP9_LVDS3A_22p	LVDS3A_22p/ AP9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel22.
91	FPGA_AF8_LVDS3A_2p	LVDS3A_2p/ AF8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel2.
92	FPGA_AH10_LVDS3A_3p	LVDS3A_3p/ AH10	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel3.
93	FPGA_AE8_LVDS3A_2n	LVDS3A_2n/ AE8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel2.
94	FPGA_AH9_LVDS3A_3n	LVDS3A_3n/ AH9	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel3.
95	GND	NA	Power	Ground.
96	GND	NA	Power	Ground.
97	GXBL1D_TX_CH0p	GXBL1D_TX_CH0p/ AJ34	O, DIFF	Bank1D High speed positive differential transmitter channel0. If unused leave this pin floating.
98	REFCLK_GXBL1D_CHTp	REFCLK_GXBL1D_CHTp /Y28	I, DIFF	Bank1D High speed differential reference clock positive receiver channel T. If unused connect this pin to GND.
99	GXBL1D_TX_CH0n	GXBL1D_TX_CH0n/ AJ33	O, DIFF	Bank1D High speed negative differential transmitter channel0. If unused leave this pin floating.
100	REFCLK_GXBL1D_CHTn	REFCLK_GXBL1D_CHTn /Y27	I, DIFF	Bank1D High speed differential reference clock negative receiver channel T. If unused connect this pin to GND.
101	GND	NA	Power	Ground.
102	GND	NA	Power	Ground.
103	GXBL1D_TX_CH1p	GXBL1D_TX_CH1p/ AG34	O, DIFF	Bank1D High speed positive differential transmitter channel1. If unused leave this pin floating.
104	FPGA_AL8_LVDS3A_23n	LVDS3A_23n/ AL8	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
105	GXBL1D_TX_CH1n	GXBL1D_TX_CH1n/ AG33	O, DIFF	Bank1D High speed negative differential transmitter channel1. If unused leave this pin floating.
106	FPGA_AG11_LVDS3A_5n	LVDS3A_5n/ AG11	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel5.
107	GND	NA	Power	Ground.
108	FPGA_AF11_LVDS3A_5p	LVDS3A_5p/ AF11	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel5.
109	GXBL1D_RX_CH1n	GXBL1D_RX_CH1n/ AB31	I, DIFF	Bank1D High speed negative differential receiver channel1. If unused connect this pin to GND.
110	FPGA_AE11_LVDS3A_6n	LVDS3A_6n/ AE11	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel6.
111	GXBL1D_RX_CH1p	GXBL1D_RX_CH1p/ AB32	I, DIFF	Bank1D High speed positive differential receiver channel1. If unused connect this pin to GND.
112	FPGA_AE12_LVDS3A_6p	LVDS3A_6p/ AE12	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel6.
113	GND	NA	Power	Ground.
114	GND	NA	Power	Ground.
115	GXBL1D_RX_CH0n	GXBL1D_RX_CH0n/ AC29	I, DIFF	Bank1D High speed negative differential receiver channel0. If unused connect this pin to GND.
116	FPGA_AH5_LVDS3A_10n/CLKOUT_1n	LVDS3A_10n/ AH5	O, 1.8V LVDS	Bank3A Clock Output differential negative channel1. Same pin can be configured as Single Ended Clock Output or User I/O.
117	GXBL1D_RX_CH0p	GXBL1D_RX_CH0p/ AC30	I, DIFF	Bank1D High speed positive differential receiver channel0. If unused connect this pin to GND.
118	FPGA_AJ5_LVDS3A_10p/CLKOUT_1p	LVDS3A_10p/ AJ5	O, 1.8V LVDS	Bank3A Clock Output differential positive channel1. Same pin can be configured as Single Ended Clock Output or User I/O.
119	GND	NA	Power	Ground.
120	GND	NA	Power	Ground.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
121	GND	NA	Power	Ground.
122	GND	NA	Power	Ground.
123	GXBL1D_TX_CH2p	GXBL1D_TX_CH2p/ AE34	O, DIFF	Bank1D High speed positive differential transmitter channel2. If unused leave this pin floating.
124	FPGA_AG17_LVDS2A_15p/ CLKOUT_0p	LVDS2A_15p/ AG17	O, 1.8V LVDS	Bank2A Clock Output differential positive channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
125	GXBL1D_TX_CH2n	GXBL1D_TX_CH2n/ AE33	O, DIFF	Bank1D High speed negative differential transmitter channel2. If unused leave this pin floating.
126	FPGA_AH17_LVDS2A_15n/ CLKOUT_0n	LVDS2A_15n/ AH17	O, 1.8V LVDS	Bank2A Clock Output differential negative channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
127	GND	NA	Power	Ground.
128	FPGA_AD19_LVDS2A_21p	LVDS2A_21p/ AD19	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin.
129	GXBL1D_TX_CH3p	GXBL1D_TX_CH3p/ AC34	O, DIFF	Bank1D High speed positive differential transmitter channel3. If unused leave this pin floating.
130	FPGA_AH18_LVDS2A_13p/ CLKIN_0p	LVDS2A_13p/ AH18	I, 1.8V LVDS	Bank2A Clock Input differential negative channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
131	GXBL1D_TX_CH3n	GXBL1D_TX_CH3n/ AC33	O, DIFF	Bank1D High speed negative differential transmitter channel3. If unused leave this pin floating.
132	FPGA_AH19_LVDS2A_13n/ CLKIN_0n	LVDS2A_13n/ AH19	I, 1.8V LVDS	Bank2A Clock Input differential positive channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
133	GND	NA	Power	Ground.
134	FPGA_AE18_LVDS2A_21n	LVDS2A_21n/ AE18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin.
135	GXBL1D_RX_CH3n	GXBL1D_RX_CH3n/ Y31	I, DIFF	Bank1D High speed negative differential receiver channel3. If unused connect this pin to GND.
136	FPGA_AJ17_LVDS2A_16p	LVDS2A_16p/ AJ17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel16.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
137	GXBL1D_RX_CH3p	GXBL1D_RX_CH3p/ Y32	I, DIFF	Bank1D High speed positive differential receiver channel3. If unused connect this pin to GND.
138	FPGA_AK17_LVDS2A_16n	LVDS2A_16n/ AK17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel16.
139	GND	NA	Power	Ground.
140	GND	NA	Power	Ground.
141	GXBL1D_RX_CH2n	GXBL1D_RX_CH2n/ AA29	I, DIFF	Bank1D High speed negative differential receiver channel2. If unused connect this pin to GND.
142	FPGA_AM16_LVDS2A_10n /CLKOUT_0n	LVDS2A_10n/ AM16	O, 1.8V LVDS	Bank2A Clock Output differential negative channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
143	GXBL1D_RX_CH2p	GXBL1D_RX_CH2p/ AA30	I, DIFF	Bank1D High speed positive differential receiver channel2. If unused connect this pin to GND.
144	FPGA_AL16_LVDS2A_10p/ CLKOUT_0p	LVDS2A_10p/ AL16	O, 1.8V LVDS	Bank2A Clock Output differential positive channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
145	GND	NA	Power	Ground.
146	GND	NA	Power	Ground.
147	FPGA_AP16_LVDS2A_2p	LVDS2A_2p/ AP16	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel2.
148	FPGA_AP12_LVDS2A_5n	LVDS2A_5n/ AP12	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel5.
149	FPGA_AP17_LVDS2A_2n	LVDS2A_2n/ AP17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel2.
150	FPGA_AN12_LVDS2A_5p	LVDS2A_5p/ AN12	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel5.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
151	FPGA_AL18_LVDS2A_11n	LVDS2A_11n/ AL18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel11.
152	FPGA_AH15_LVDS2A_17n	LVDS2A_17n/ AH15	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel17.
153	FPGA_AK18_LVDS2A_11p	LVDS2A_11p/ AK18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel11.
154	FPGA_AJ15_LVDS2A_17p	LVDS2A_17p/ AJ15	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel17.
155	GND	NA	Power	Ground.
156	GND	NA	Power	Ground.
157	GXBL1D_TX_CH4p	GXBL1D_TX_CH4p/ AA34	I, DIFF	Bank1D High speed positive differential transmitter channel4. If unused leave this pin floating.
158	REFCLK_GXBL1D_CHBp	REFCLK_GXBL1D_CHBp /AB28	I, DIFF	Bank1D High speed differential reference clock positive receiver channel B. If unused connect this pin to GND.
159	GXBL1D_TX_CH4n	GXBL1D_TX_CH4n/ AA33	I, DIFF	Bank1D High speed negative differential transmitter channel4. If unused leave this pin floating.
160	REFCLK_GXBL1D_CHBn	REFCLK_GXBL1D_CHBn /AB27	I, DIFF	Bank1D High speed differential reference clock negative receiver channel B. If unused connect this pin to GND.
161	GND	NA	Power	Ground.
162	GND	NA	Power	Ground.
163	GXBL1D_TX_CH5p	GXBL1D_TX_CH5p/ W34	O, DIFF	Bank1D High speed positive differential transmitter channel5. If unused leave this pin floating.
164	FPGA_AG16_LVDS2A_20p	LVDS2A_20p/ AG16	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel20.
165	GXBL1D_TX_CH5n	GXBL1D_TX_CH5n/ W33	O, DIFF	Bank1D High speed negative differential transmitter channel5. If unused leave this pin floating.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
166	FPGA_AF16_LVDS2A_20n	LVDS2A_20n/ AF16	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel20.
167	GND	NA	Power	Ground.
168	FPGA_AE17_LVDS2A_19n	LVDS2A_19n/ AE17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel19.
169	GXBL1D_RX_CH5n	GXBL1D_RX_CH5n/ V31	I, DIFF	Bank1D High speed negative differential receiver channel5. If unused connect this pin to GND.
170	FPGA_AE16_LVDS2A_19p	LVDS2A_19p/ AE16	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel19.
171	GXBL1D_RX_CH5p	GXBL1D_RX_CH5p/ V32	I, DIFF	Bank1D High speed positive differential receiver channel5. If unused connect this pin to GND.
172	FPGA_AC17_LVDS2A_24p/ NANDWP	LVDS2A_24p/ AC17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. LVDS2A_24p is connected to this pin through resistor and default populated. *Note: Optionally same is also connected to on board NAND flash (for Write Protect) through resistor and default not populated.*
173	GND	NA	Power	Ground.
174	GND	NA	Power	Ground.
175	GXBL1D_RX_CH4n	GXBL1D_RX_CH4n/ W29	I, DIFF	Bank1D High speed negative differential receiver channel4. If unused connect this pin to GND.
176	FPGA_AH14_LVDS2A_14n	LVDS2A_14n/ AH14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel14.
177	GXBL1D_RX_CH4p	GXBL1D_RX_CH4p/ W30	I, DIFF	Bank1D High speed positive differential receiver channel4. If unused connect this pin to GND.
178	FPGA_AJ14_LVDS2A_14p	LVDS2A_14p/ AJ14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel14.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
179	GND	NA	Power	Ground.
180	GND	NA	Power	Ground.
181	GND	NA	Power	Ground.
182	GND	NA	Power	Ground.
183	GXBL1E_TX_CH0p	GXBL1E_TX_CH0p/ U34	O, DIFF	Bank1E High speed positive differential transmitter channel0. If unused leave this pin floating.
184	REFCLK_GXBL1E_CHTp	REFCLK_GXBL1E_CHTp/ T28	I, DIFF	Bank1E High speed differential reference clock positive receiver channel T. If unused connect this pin to GND.
185	GXBL1E_TX_CH0n	GXBL1E_TX_CH0n/ U33	O, DIFF	Bank1E High speed negative differential transmitter channel0. If unused leave this pin floating.
186	REFCLK_GXBL1E_CHTn	REFCLK_GXBL1E_CHTn/ T27	I, DIFF	Bank1E High speed differential reference clock negative receiver channel T. If unused connect this pin to GND.
187	GND	NA	Power	Ground.
188	GND	NA	Power	Ground.
189	GXBL1E_TX_CH1p	GXBL1E_TX_CH1p/ R34	O, DIFF	Bank1E High speed positive differential transmitter channel1. If unused leave this pin floating.
190	FPGA_AD17_LVDS2A_24n/ NANDLOCK	LVDS2A_24n/ AD17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin.
191	GXBL1E_TX_CH1n	GXBL1E_TX_CH1n/ R33	O, DIFF	Bank1E High speed negative differential transmitter channel1. If unused leave this pin floating.
192	FPGA_AE19_LVDS2A_22n	LVDS2A_22n/ AE19	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel22.
193	GND	NA	Power	Ground.
194	FPGA_AF19_LVDS2A_22p	LVDS2A_22p/ AF19	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel22.
195	GXBL1E_RX_CH1n	GXBL1E_RX_CH1n/ T31	I, DIFF	Bank1E High speed negative differential receiver channel1. If unused connect this pin to GND.
196	FPGA_AF18_LVDS2A_23p	LVDS2A_23p/ AF18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel23.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
197	GXBL1E_RX_CH1p	GXBL1E_RX_CH1p/ T32	I, DIFF	Bank1E High speed positive differential receiver channel1. If unused connect this pin to GND.
198	FPGA_AG18_LVDS2A_23n	LVDS2A_23n/ AG18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel23.
199	GND	NA	Power	Ground.
200	GND	NA	Power	Ground.
201	GXBL1E_RX_CH0n	GXBL1E_RX_CH0n/ U29	I, DIFF	Bank1E High speed negative differential receiver channel0. If unused connect this pin to GND.
202	FPGA_AN17_LVDS2A_8n	LVDS2A_8n/ AN17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel8.
203	GXBL1E_RX_CH0p	GXBL1E_RX_CH0p/ U30	I, DIFF	Bank1E High speed positive differential receiver channel0. If unused connect this pin to GND.
204	FPGA_AM17_LVDS2A_8p	LVDS2A_8p/ AM17	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel8.
205	GND	NA	Power	Ground.
206	GND	NA	Power	Ground.
207	FPGA_AP15_LVDS2A_3n	LVDS2A_3n/ AP15	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel3.
208	FPGA_AP14_LVDS2A_6n	LVDS2A_6n/ AP14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel6.
209	FPGA_AN15_LVDS2A_3p	LVDS2A_3p/ AN15	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel3.
210	FPGA_AN14_LVDS2A_6p	LVDS2A_6p/ AN14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel6.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
211	FPGA_AM18_LVDS2A_7p	LVDS2A_7p/ AM18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel7.
212	FPGA_AL14_LVDS2A_9p	LVDS2A_9p/ AL14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel9.
213	FPGA_AN18_LVDS2A_7n	LVDS2A_7n/ AN18	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel7.
214	FPGA_AK14_LVDS2A_9n	LVDS2A_9n/ AK14	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel9.
215	GND	NA	Power	Ground.
216	GND	NA	Power	Ground.
217	GXBL1E_TX_CH2p	GXBL1E_TX_CH2p/ N34	O, DIFF	Bank1E High speed positive differential transmitter channel2. If unused leave this pin floating.
218	REFCLK_GXBL1E_CHBp	REFCLK_GXBL1E_CHBp /V28	I, DIFF	Bank1E High speed differential reference clock positive receiver channel B. If unused connect this pin to GND.
219	GXBL1E_TX_CH2n	GXBL1E_TX_CH2n/ N33	O, DIFF	Bank1E High speed negative differential transmitter channel2. If unused leave this pin floating.
220	REFCLK_GXBL1E_CHBn	REFCLK_GXBL1E_CHBn /V27	I, DIFF	Bank1E High speed differential reference clock negative receiver channel B. If unused connect this pin to GND.
221	GND	NA	Power	Ground.
222	GND	NA	Power	Ground.
223	GXBL1E_TX_CH3p	GXBL1E_TX_CH3p/ L34	O, DIFF	Bank1E High speed positive differential transmitter channel3. If unused leave this pin floating.
224	FPGA_AL15_LVDS2A_12n	LVDS2A_12n/ AL15	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin.
225	GXBL1E_TX_CH3n	GXBL1E_TX_CH3n/ L33	O, DIFF	Bank1E High speed negative differential transmitter channel3. If unused leave this pin floating.

Pin No	Signal Name	Arria10 Ball Name/ Pin Number	Signal Type/ Termination	Description
226	FPGA_AK13_LVDS2A_1n	LVDS2A_1n/ AK13	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel1.
227	GND	NA	Power	Ground.
228	FPGA_AL13_LVDS2A_1p	LVDS2A_1p/ AL13	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel1.
229	GXBL1E_RX_CH3n	GXBL1E_RX_CH3n/ P31	I, DIFF	Bank1E High speed negative differential receiver channel3. If unused connect this pin to GND.
230	FPGA_AJ16_LVDS2A_18p	LVDS2A_18p/ AJ16	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin.
231	GXBL1E_RX_CH3p	GXBL1E_RX_CH3p/ P32	I, DIFF	Bank1E High speed positive differential receiver channel3. If unused connect this pin to GND.
232	NC	NA	NA	NC.
233	GND	NA	Power	Ground.
234	GND	NA	Power	Ground.
235	GXBL1E_RX_CH2n	GXBL1E_RX_CH2n/ R29	I, DIFF	Bank1E High speed negative differential receiver channel2. If unused connect this pin to GND.
236	FPGA_AM13_LVDS2A_4n	LVDS2A_4n/ AM13	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential negative channel4.
237	GXBL1E_RX_CH2p	GXBL1E_RX_CH2p/ R30	I, DIFF	Bank1E High speed positive differential receiver channel2. If unused connect this pin to GND.
238	FPGA_AN13_LVDS2A_4p	LVDS2A_4p/ AN13	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. Same pin can be configured as true LVDS receiver/transmitter differential positive channel4.
239	GND	NA	Power	Ground.
240	GND	NA	Power	Ground.

2.7 Expansion Connector2 Interfaces

The Arria10 SoC/FPGA SOM supports two 240pin High speed ground plane ruggedized terminal strip connectors for interfaces expansion. The interfaces which are available at 240pin Expansion connector2 from Arria10 HPS and FPGA fabric are explained in the following sections.

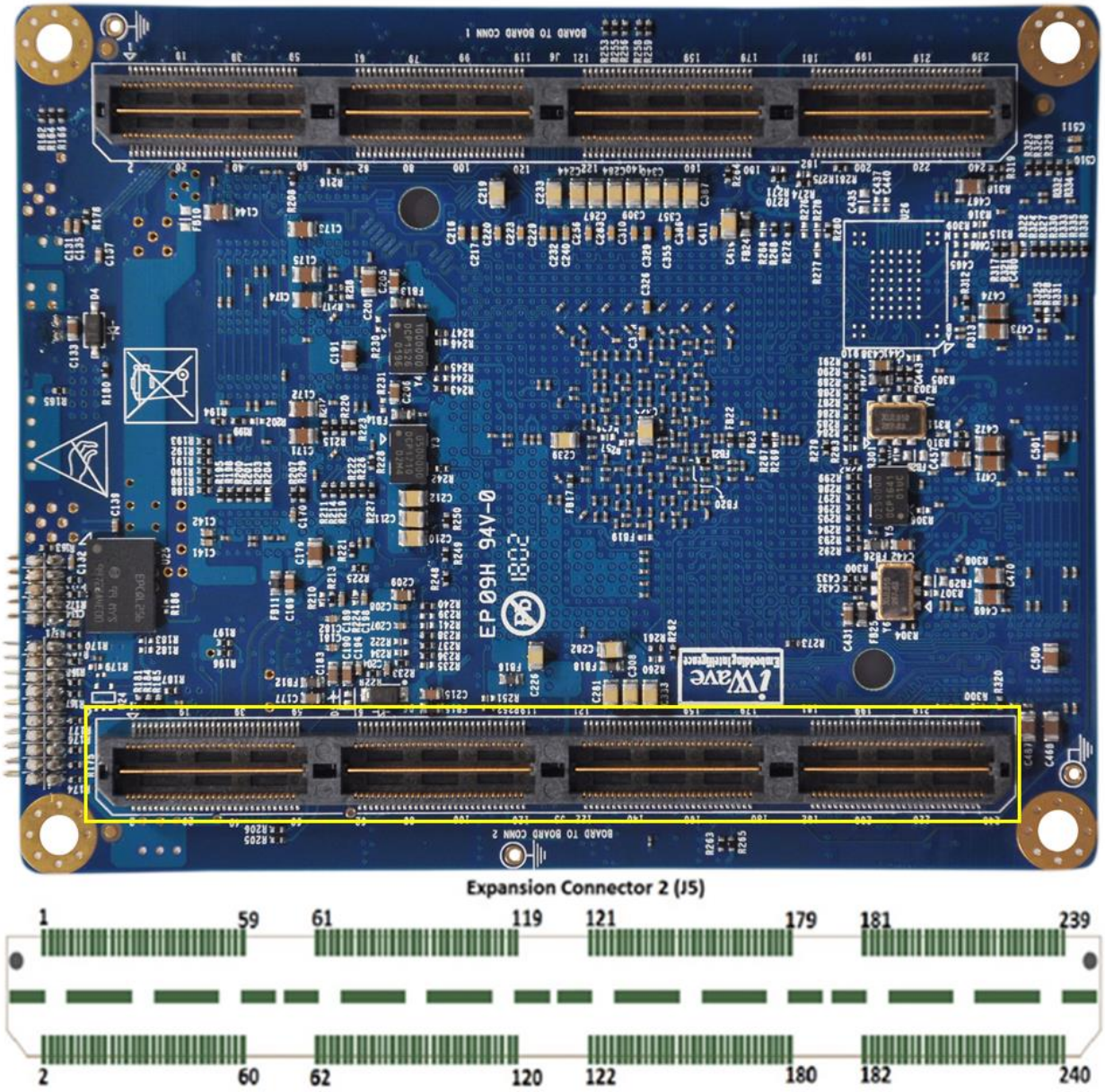


Figure 8: Expansion Connector2

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A

Mating Connector - QSH-120-01-L-D-A from Samtech

Staking Height - 5mm

2.7.1 HPS Gigabit Ethernet

The Arria10 SoC SOM supports one 10/100/1000Mbps Ethernet interface on Expansion connector2 through EMAC1 interface from HPS shared I/O pins. The MAC is integrated in the Arria10 SoC's HPS and connected to the external Ethernet PHY on SOM. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. Arria10 SoC SOM also supports Link and Activity indication LED control signals to Expansion Connector2.

The Arria10 SoC SOM supports "KSZ9031RNX" Ethernet PHY from Microchip. This PHY is interfaced with Arria10 HPS's Ethernet Media Access controller and works at 3.3V IO voltage level. Since this PHY doesn't recommend connecting any power source to magnetic centre tap pins, CTREF voltage to Expansion Connector2 is not supported on SOM. It is recommended that centre tap pins of magnetics should be separated from one another and connected through separate 0.1uF common mode capacitors to ground. This PHY has on-chip termination on differential pairs and so no need to add any termination externally. The below table provides some of the compatible magnetics recommended by the PHY Manufacturer.

For more details, refer Expansion connector2 pins 39, 41, 45, 47, 51, 53, 57, 58, 59 & 60 on ***Table 11***.

Table 10: Compatible Magnetics

Part Description	Part Number	Manufacturer	Temperature
Gigabit Ethernet Discrete Transformer	TG1G-E001NZRL	HALO	-40°C to 85°C
Gigabit Ethernet Discrete Transformer	HX5008NL	Pulse	-40°C to 85°C
Gigabit Ethernet Discrete Transformer	000-7093-37R-LF1	Wurth	0°C to 70°C
RJ45 Magjack with two Green LED	JK0654219NL	Pulse	0°C to 70°C
RJ45 Magjack with two Green LED	0826-1G1T-23-F	Bel Fuse	0°C to 70°C

2.7.2 HPS USB2.0 OTG interface

The Arria10 SoC SOM supports one USB2.0 OTG interface on Expansion connector2 through HPS shared I/O pins. Arria10 SoC HPS's USB1 OTG Controller is used for USB2.0 OTG interface. This USB OTG Controller supports a single USB port connected through a USB 2.0 Transceiver Macrocell Plus Low Pin Interface compliant PHY. Also this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

The Arria10 SoC SOM supports "USB3320" ULPI transceiver from Microchip. The ULPI interface from HPS USB1 OTG controller is connected to this PHY. USB3320 PHY uses the industry standard UTMI+ Low Pin Interface to connect the USB Transceiver to the link. The Arria10 SoC SOM supports active high power enable signal on Expansion conenctor2 from this USB PHY for external Vbus power control. Also it supports USB ID input and USB Vbus from Expansion conenctor2 and connected to USB PHY for USB host or device detection. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details, refer Expansion connector2 pins 26, 28, 32, 34 & 36 on ***Table 11***.

2.7.3 HPS Debug UART Interface

The Arria10 SoC HPS supports two UART controllers for asynchronous serial communication. The UART controllers are based on industry standard 16550 UART Controller.

The Arria10 SoC SOM supports these two UART interface on Expansion connector2 for Debug UART interface and Data UART interface through HPS shared I/O pins. Arria10 SoC HPS's UART0 controller is used for Debug UART interface with Transmit & Receive signal on Expansion connector2.

For more details, refer Expansion connector2 pins 54 & 56 on ***Table 11***.

2.7.4 HPS Data UART Interface

The Arria10 SoC SOM supports one UART interface on Expansion connector2 for Data UART interface through HPS shared I/O pins. Arria10 SoC HPS's UART1 controller is used for Data UART interface with hardware flow control for request to send and clear to send signals on Expansion connector2.

The Arria10 HPS UART controllers are based on industry standard 16550 UART Controller. The UART Controller includes 128-byte FIFO buffers to buffer transmit and receive data. FIFO buffer access mode allows the master to write the receive FIFO buffer and to read the transmit FIFO buffer for test purposes. FIFO buffer access mode is enabled with the FIFO access register. Once enabled, the control portions of the transmit and receive FIFO buffers are reset and the FIFO buffers are treated as empty.

For more details, refer Expansion connector2 pins 46, 48, 50 & 52 on ***Table 11***.

2.7.5 HPS SPI Interface

The Arria10 SoC SOM supports one SPI Master interface with one chip select on Expansion connector2 through HPS shared I/O pins. Arria10 HPS's SPI controller is used for SPI Master interface which supports full-duplex synchronous four-wire serial interface with DMA. Each SPI master has a maximum bit rate of 60Mbps.

Arria10 HPS's SPI controller has programmable choice of Serial interface protocols Motorola SPI protocol or Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire. It has transmit and receive FIFO buffers which are 256 words deep. Also it supports DMA controller interface integrated with HPS DMA controller.

For more details, refer Expansion connector2 pins 61, 63, 65 & 67 on ***Table 11***.

2.7.6 HPS I2C Interface

The Arria10 SoC SOM supports one I2C interface on Expansion Connector2 through HPS shared I/O pins. Arria10 SoC HPS's I2C0 controller is used for I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. I2C controller must be programmed to operate in either master or slave mode only. Operating as a master and slave simultaneously is not supported.

For more details, refer Expansion connector2 pins 46 & 48 *on* ***Table 11****.*

2.7.7 HPS GPIO Interface

The Arria10 SoC SOM supports GPIOs on Expansion connector2. The Arria10 SoC's HPS I/O block supports Dedicated I/O and Shared I/O. Dedicated I/O pins are used for HPS boot devices and other key peripherals. Shared I/O pins are used for other HPS interfaces and can be selected through I/O multiplexing. These shared I/O pins are divided into four quadrants of 12 signals per quadrant. Each quadrant can be assigned to either HPS or the FPGA fabric. All the interface pins from HPS Shared I/O pins can be used as GPIO if not used as other interface.

The Arria10 HPS's GPIO module provides general-purpose pins that can be configured as either input or output. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO input can produce interrupt to the HPS core via the interrupt control block when corresponding registers are set. Also it supports digital de-bounce where the external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.

For more details, refer Expansion Connector2 pins 38, 40, 42, 44, 62, 64, 66, 68, 69, 70, 71 & 72 on ***Table 11****.*

2.7.8 HPS Warm Reset

The Arria10 SoC SOM supports Warm reset pin on Expansion connector2. This Warm reset from Expansion conenctor2 is connected to HPS_nRST pin of the Arria10 SoC. This is active low bi-directional pin and can initiate the warm reset when driven low from the carrier board by connecting the reset push button switch. In HPS warm reset, all of the HPS except security manager, POR, Fuse Logic and test access port (TAP) and Debug domains are reset. While HPS cold reset, HPS drives out this pin low.

For more details, refer Expansion Connector2 pin 35 on ***Table 11****.*

2.7.9 FPGA High Speed Transceivers

The Arria10 SoC/FPGA SOM supports 24 high speed transceivers on Expansion connectors from Arria10 FPGA fabric. The Arria10 SoC/FPGA has four high speed transceiver banks (1C, 1D, 1E & 1F) and each transceiver bank has six high speed transmit and receive channels. Also each high speed transceiver bank supports two reference clock input pairs

The Arria10 SoC/FPGA SOM supports 16 high speed transceiver channels (6 from 1C bank, 6 from 1D bank & 4 from 1E bank) on Expansion connector1 and 8 high speed transceiver channels (2 from 1E bank & 4 from 1F bank) on Expansion conenctor2. In Arria10 SoC/FPGA SOM, Transceiver power to Arria10 SoC/FPGA is fixed to 1.03V. Also it supports 100MHz Oscillator on board for transceiver reference clock and connected to Bank2A AK16 CLKUSR pin.

For more details, refer Expansion connector2 pins 229, 230, 231, 232, 235, 236, 237 & 238 for Transceiver Bank1E, 187, 188, 189, 190, 193, 194, 195, 196, 199, 200, 201, 202, 205, 206, 207, 208, 211, 212, 213, 214, 217, 218, 219, 220, 223, 224, 225 & 226 for Transceiver Bank1F on ***Table 11***.

2.7.10FPGA IOs & General Purpose Clocks – Bank3B

The Arria10 SoC/FPGA SOM supports upto 24 LVDS IO pairs from Arria10 FPGA Bank3B on Expansion connector2. These Bank3B signals on Expansion connector2 is routed as LVDS IO pairs in the board. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps. If the Single Ended IOs are required in these pins, it may also be configured even though the signals are routed as LVDS IOs.

In Arria10 SoC/FPGA SOM, upon these 24 LVDS IO pairs from Arria10 FPGA Bank3B, two General Purpose Clock input LVDS pairs and two General Purpose Clock Output LVDS pairs are supported on Expansion connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General Purpose single ended clock. In Arria10 SoC/FPGA SOM, I/O voltage for Bank3B is fixed to 1.8V.

For more details, refer Expansion connector2 pins 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 121, 122, 123, 124, 125, 126, 127 & 128 for Bank3B LVDS IO pairs, 110, 112, 115 & 117 for Bank3B General Purpose Clock Output LVDS pairs, 109, 111, 116 & 118 for Bank3B General Purpose Clock input LVDS pairs on ***Table 11***.

2.7.11FPGA IOs & General Purpose Clocks – Bank3C

The Arria10 SoC/FPGA SOM supports upto 24 LVDS IO pairs from Arria10 FPGA Bank3C on Expansion connector2. These Bank3C signals on Expansion connector2 is routed as LVDS IO pairs in the board. Every LVDS pair can be configured as receiver or transmitter and works upto 1.6 Gbps. If the Single Ended IOs are required in these pins, it may also be configured even though the signals are routed as LVDS IOs.

In Arria10 SoC/FPGA SOM, upon these 24 LVDS IO pairs from Arria10 FPGA Bank3C, two General Purpose Clock input LVDS pairs and two General Purpose Clock Output LVDS pairs are supported on Expansion connector2. If Single Ended Clock is required instead of LVDS, then the same LVDS clock pins can be configured as General Purpose single ended clock. In Arria10 SoC/FPGA SOM, I/O voltage for Bank3C is fixed to 1.8V.

For more details, refer Expansion connector2 pins 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 181, 182, 183 & 184 for Bank3C LVDS IO pairs, 169, 170, 171 & 172 for Bank3C General Purpose Clock Output LVDS pairs, 175, 176, 177 & 178 for Bank3C General Purpose Clock input LVDS pairs on ***Table 11***.

2.7.12JTAG Interface

The Arria10 SoC/FPGA SOM supports JTAG interface on Expansion connector2. The Arria10 SoC's HPS and FPGA share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Arria10 device. During power- on-reset, the JTAG and all debug fuses are read by the Configuration subsystem to determine if the JTAG to the FPGA or HPS is bypassed. These JTAG interface signals are also connected to on-board JTAG connector.

For more details, refer Expansion Connector2 pins 25, 27, 29, 31 & 33 on ***Table 11***.

Table 11: Expansion Connector2 Pin Assignment

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC	VCC_5V	Power	I, 5V Power
2	VCC	VCC_5V	Power	I, 5V Power
3	VCC	VCC_5V	Power	I, 5V Power
4	VCC	VCC_5V	Power	I, 5V Power
5	VCC	VCC_5V	Power	I, 5V Power
6	VCC	VCC_5V	Power	I, 5V Power
7	VCC	VCC_5V	Power	I, 5V Power
8	VCC	VCC_5V	Power	I, 5V Power
9	VCC	VCC_5V	Power	I, 5V Power
10	VCC	VCC_5V	Power	I, 5V Power
11	VCC	VCC_5V	Power	I, 5V Power
12	VCC	VCC_5V	Power	I, 5V Power
13	VCC	VCC_5V	Power	I, 5V Power
14	VCC	VCC_5V	Power	I, 5V Power
15	VCC	VCC_5V	Power	I, 5V Power
16	VCC	VCC_5V	Power	I, 5V Power
17	VCC	VCC_5V	Power	I, 5V Power
18	VCC	VCC_5V	Power	I, 5V Power
19	VCC	VCC_5V	Power	I, 5V Power
20	VCC	VCC_5V	Power	I, 5V Power
21	GND	NA	Power	Ground.
22	GND	NA	Power	Ground.
23	GND	NA	Power	Ground.
24	GND	NA	Power	Ground.
25	CSS_TRST	CSS_TRST/ AL11	I, 1.8V CMOS/ 10K PU	Dedicated JTAG test reset input pin.
26	USB_OTG_DM	NA	IO, DIFF	USB OTG Data Positive.
27	CSS_TDI	CSS_TDI/ AH13	I, 1.8V CMOS/ 10K PU	Dedicated JTAG test data input pin.
28	USB_OTG_DP	NA	IO, DIFF	USB OTG Data Negative.
29	CSS_TMS	CSS_TMS/ AL10	I, 1.8V CMOS/ 10K PU	Dedicated JTAG test Mode select input pin.
30	GND	NA	Power	Ground.
31	CSS_TCK	CSS_TCK/ AH12	I, 1.8V CMOS	Dedicated JTAG test clock input pin.
32	USB_PWR_EN	NA	O, 3.3V CMOS	USB active high power enable output to control external USB Vbus.
33	CSS_TDO	CSS_TDO/ AJ12	O, 1.8V CMOS	Dedicated JTAG test data output pin.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
34	USB_OTG_ID	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
35	HPS_nRST	HPS_nRST/ L14	IO, 1.8V CMOS/ 1K PU	Warm reset input to HPS block.
36	VBUS_USB	NA	I, Power 5V	USB VBUS Voltage pin.
37	GND	NA	Power	Ground.
38	HPS_GPIO(GPIO0_IO10)	GPIO0_IO10/ L20	IO, 1.8V CMOS	General Purpose Input/Output.
39	GPHY_DTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative.
40	HPS_GPIO/EMAC2_RXD 1(GPIO1_IO19)	GPIO1_IO19/ A21	IO, 1.8V CMOS	General Purpose Input/Output.
41	GPHY_DTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive.
42	HPS_GPIO/EMAC2_RXD 0(GPIO1_IO18)	GPIO1_IO18/ B22	IO, 1.8V CMOS	General Purpose Input/Output.
43	GND	NA	Power	Ground.
44	HPS_GPIO(GPIO0_IO11)	GPIO0_IO11/ M20	IO, 1.8V CMOS	General Purpose Input/Output.
45	GPHY_CTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative.
46	HPS_UART1_CTS_N/I2C 0_SDA	GPIO0_IO4/ M21	IO, 1.8V CMOS/ 4.7K PU	I2C0 Data Signal.
47	GPHY_CTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive
48	HPS_UART1_RTS_N/I2C 0_SCL	GPIO0_IO5/ L21	IO, 1.8V CMOS/ 4.7K PU	I2C0 Clock signal.
49	GND	NA	Power	Ground.
50	HPS_UART1_TX/EMAC2 _MDIO	GPIO0_IO6/ K21	IO, 1.8V CMOS	Data UART1 Transmit data line.
51	GPHY_BTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative.
52	HPS_UART1_RX/EMAC2 _MDC	GPIO0_IO7/ J21	IO, 1.8V CMOS	Data UART1 Receive data line.
53	GPHY_BTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive.
54	HPS_UART0_TX	GPIO0_IO2/ K18	IO, 1.8V CMOS	Debug UART0 Transmit data line.
55	GND	NA	Power	Ground.
56	HPS_UART0_RX	GPIO0_IO3/ L18	IO, 1.8V CMOS	Debug UART0 Receive data line.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
57	GPHY_ATXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative.
58	GPHY_LINK_LED2	NA	O, 3.3V CMOS/ 4.7K PD	Gigabit Ethernet link status LED.
59	GPHY_ATXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.
60	GPHY_ACTIVITY_LED1	NA	O, 3.3V CMOS/ 4.7K PU	Gigabit Ethernet activity status LED.
61	HPS_SPIM0_CLK/EMAC 2_TXD2	GPIO1_IO20/ B21	IO, 1.8V CMOS	SPI Clock output.
62	HPS_GPIO/SDMMC_DA TA3(GPIO1_IO17)	GPIO1_IO17/ A20	IO, 1.8V CMOS	General Purpose Input/Output.
63	HPS_SPIM0_SS0_N/EM AC2_RXD3	GPIO1_IO23/ D19	IO, 1.8V CMOS	SPI Chip select 0.
64	HPS_GPIO/SDMMC_DA TA2(GPIO1_IO16)	GPIO1_IO16/ A19	IO, 1.8V CMOS	General Purpose Input/Output.
65	HPS_SPIM0_MOSI/EMA C2_TXD3	GPIO1_IO21/ B20	IO, 1.8V CMOS	SPI Master output Slave input.
66	HPS_GPIO/SDMMC_DA TA1(GPIO1_IO15)	GPIO1_IO15/ B18	IO, 1.8V CMOS	General Purpose Input/Output.
67	HPS_SPIM0_MISO/EMA C2_RXD2	GPIO1_IO22/ C19	IO, 1.8V CMOS	SPI Master input Slave output.
68	HPS_GPIO/SDMMC_DA TA0(GPIO0_IO0)	GPIO0_IO0/ M17	IO, 1.8V CMOS	General Purpose Input/Output.
69	HPS_I2C1_SDA/EMAC2_ TX_CLK(GPIO1_IO12)	GPIO1_IO12/ C18	IO, 1.8V CMOS	General Purpose Input/Output.
70	HPS_GPIO/SDMMC_CM D(GPIO0_IO1)	GPIO0_IO1/ M18	IO, 1.8V CMOS	General Purpose Input/Output.
71	HPS_I2C1_SCL/EMAC2_ TX_CTL(GPIO1_IO13)	GPIO1_IO13/ D17	IO, 1.8V CMOS	General Purpose Input/Output.
72	HPS_GPIO/SDMMC_CCL K(GPIO1_IO14)	GPIO1_IO14/ A18	IO, 1.8V CMOS	General Purpose Input/Output.
73	GND	NA	Power	Ground.
74	GND	NA	Power	Ground.
75	FPGA_AC10_LVDS3B_9 n	LVDS3B_9n/ AC10	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel9. Same pin can be configured as Single ended I/O.
76	FPGA_AB8_LVDS3B_4p	LVDS3B_4p/ AB8	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel4. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
77	FPGA_AC9_LVDS3B_9p	LVDS3B_9p/ AC9	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel9. Same pin can be configured as Single ended I/O.
78	FPGA_AB7_LVDS3B_4n	LVDS3B_4n/ AB7	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel4. Same pin can be configured as Single ended I/O.
79	FPGA_AF6_LVDS3B_17n	LVDS3B_17n/ AF6	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel17. Same pin can be configured as Single ended I/O.
80	FPGA_AE7_LVDS3B_11n	LVDS3B_11n/ AE7	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel11. Same pin can be configured as Single ended I/O.
81	FPGA_AG6_LVDS3B_17p	LVDS3B_17p/ AG6	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel17. Same pin can be configured as Single ended I/O.
82	FPGA_AE6_LVDS3B_11p	LVDS3B_11p/ AE6	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel11. Same pin can be configured as Single ended I/O.
83	FPGA_AF5_LVDS3B_14n	LVDS3B_14n/ AF5	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel14. Same pin can be configured as Single ended I/O.
84	FPGA_AD6_LVDS3B_8n	LVDS3B_8n/ AD6	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel8. Same pin can be configured as Single ended I/O.
85	FPGA_AG5_LVDS3B_14p	LVDS3B_14p/ AG5	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel14. Same pin can be configured as Single ended I/O.
86	FPGA_AD5_LVDS3B_8p	LVDS3B_8p/ AD5	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel8. Same pin can be configured as Single ended I/O.
87	FPGA_AK4_LVDS3B_22p	LVDS3B_22p/ AK4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel22. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
88	FPGA_AD7_LVDS3B_7p	LVDS3B_7p/ AD7	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel7. Same pin can be configured as Single ended I/O.
89	FPGA_AK3_LVDS3B_22n	LVDS3B_22n/ AK3	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel22. Same pin can be configured as Single ended I/O.
90	FPGA_AC7_LVDS3B_7n	LVDS3B_7n/ AC7	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel7. Same pin can be configured as Single ended I/O.
91	FPGA_AJ4_LVDS3B_21p	LVDS3B_21p/ AJ4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel21. Same pin can be configured as Single ended I/O.
92	FPGA_AH3_LVDS3B_18p	LVDS3B_18p/ AH3	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel18. Same pin can be configured as Single ended I/O.
93	FPGA_AH4_LVDS3B_21n	LVDS3B_21n/ AH4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel21. Same pin can be configured as Single ended I/O.
94	FPGA_AG3_LVDS3B_18n	LVDS3B_18n/ AG3	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel18. Same pin can be configured as Single ended I/O.
95	FPGA_AL1_LVDS3B_24p	LVDS3B_24p/ AL1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel24. Same pin can be configured as Single ended I/O.
96	FPGA_AG2_LVDS3B_19n	LVDS3B_19n/ AG2	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel19. Same pin can be configured as Single ended I/O.
97	FPGA_AK1_LVDS3B_24n	LVDS3B_24n/ AK1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel24. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
98	FPGA_AG1_LVDS3B_19p	LVDS3B_19p/ AG1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel19. Same pin can be configured as Single ended I/O.
99	FPGA_AK2_LVDS3B_23p	LVDS3B_23p/ AK2	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel23. Same pin can be configured as Single ended I/O.
100	FPGA_AE4_LVDS3B_3p	LVDS3B_3p/ AE4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel3. Same pin can be configured as Single ended I/O.
101	FPGA_AJ2_LVDS3B_23n	LVDS3B_23n/ AJ2	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel23. Same pin can be configured as Single ended I/O.
102	FPGA_AD4_LVDS3B_3n	LVDS3B_3n/ AD4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel3. Same pin can be configured as Single ended I/O.
103	FPGA_AJ1_LVDS3B_20p	LVDS3B_20p/ AJ1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel20. Same pin can be configured as Single ended I/O.
104	FPGA_AF1_LVDS3B_16p	LVDS3B_16p/ AF1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel16. Same pin can be configured as Single ended I/O.
105	FPGA_AH2_LVDS3B_20n	LVDS3B_20n/ AH2	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel20. Same pin can be configured as Single ended I/O.
106	FPGA_AE1_LVDS3B_16n	LVDS3B_16n/ AE1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel18. Same pin can be configured as Single ended I/O.
107	GND	NA	Power	Ground.
108	GND	NA	Power	Ground.
109	FPGA_AD10_LVDS3B_12p/CLKIN_1p	LVDS3B_12p/ AD10	IO, 1.8V LVDS	Bank3B Clock Input differential positive channel1. Same pin can be configured as Single Ended Clock Input or User I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
110	FPGA_AC8_LVDS3B_10p/CLKOUT_1p	LVDS3B_10p/ AC8	IO, 1.8V LVDS	Bank3B Clock Output differential positive channel1. Same pin can be configured as Single Ended Clock Output or User I/O.
111	FPGA_AD11_LVDS3B_12n/CLKIN_1n	LVDS3B_12n/ AD11	IO, 1.8V LVDS	Bank3B Clock Input differential negative channel1. Same pin can be configured as Single Ended Clock Input or User I/O.
112	FPGA_AD9_LVDS3B_10n/CLKOUT_1n	LVDS3B_10n/ AD9	IO, 1.8V LVDS	Bank3B Clock Output differential negative channel1. Same pin can be configured as Single Ended Clock Output or User I/O.
113	GND	NA	Power	Ground.
114	GND	NA	Power	Ground.
115	FPGA_AF4_LVDS3B_15p/CLKOUT_0p	LVDS3B_15p/ AF4	IO, 1.8V LVDS	Bank3B Clock Output differential positive channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
116	FPGA_AE2_LVDS3B_13p/CLKIN_0p	LVDS3B_13p/ AE2	IO, 1.8V LVDS	Bank3B Clock Input differential positive channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
117	FPGA_AF3_LVDS3B_15n/CLKOUT_0n	LVDS3B_15n/ AF3	IO, 1.8V LVDS	Bank3B Clock Output differential negative channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
118	FPGA_AE3_LVDS3B_13n/CLKIN_0n	LVDS3B_13n/ AE3	IO, 1.8V LVDS	Bank3B Clock Input differential negative channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
119	GND	NA	Power	Ground.
120	GND	NA	Power	Ground.
121	FPGA_AB11_LVDS3B_1n	LVDS3B_1n/ AB11	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel1. Same pin can be configured as Single ended I/O.
122	FPGA_AD2_LVDS3B_2p	LVDS3B_2p/ AD2	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel2. Same pin can be configured as Single ended I/O.
123	FPGA_AB10_LVDS3B_1p	LVDS3B_1p/ AB10	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel1. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
124	FPGA_AD1_LVDS3B_2n	LVDS3B_2n/ AD1	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel2. Same pin can be configured as Single ended I/O.
125	FPGA_AB5_LVDS3B_5n	LVDS3B_5n/ AB5	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel5. Same pin can be configured as Single ended I/O.
126	FPGA_AC4_LVDS3B_6p	LVDS3B_6p/ AC4	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel6. Same pin can be configured as Single ended I/O.
127	FPGA_AB6_LVDS3B_5p	LVDS3B_5p/ AB6	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel5. Same pin can be configured as Single ended I/O.
128	FPGA_AC5_LVDS3B_6n	LVDS3B_6n/ AC5	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel6. Same pin can be configured as Single ended I/O.
129	GND	NA	Power	Ground.
130	GND	NA	Power	Ground.
131	FPGA_AB1_LVDS3C_24p	LVDS3C_24p/ AB1	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel24. Same pin can be configured as Single ended I/O.
132	FPGA_AC3_LVDS3C_22p	LVDS3C_22p/ AC3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel22. Same pin can be configured as Single ended I/O.
133	FPGA_AA1_LVDS3C_24n	LVDS3C_24n/ AA1	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel24. Same pin can be configured as Single ended I/O.
134	FPGA_AC2_LVDS3C_22n	LVDS3C_22n/ AC2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel22. Same pin can be configured as Single ended I/O.
135	FPGA_AA3_LVDS3C_20p	LVDS3C_20p/ AA3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel20. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
136	FPGA_AB2_LVDS3C_21p	LVDS3C_21p/ AB2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel21. Same pin can be configured as Single ended I/O.
137	FPGA_AA4_LVDS3C_20n	LVDS3C_20n/ AA4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel20. Same pin can be configured as Single ended I/O.
138	FPGA_AB3_LVDS3C_21n	LVDS3C_21n/ AB3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel21. Same pin can be configured as Single ended I/O.
139	FPGA_Y1_LVDS3C_23p	LVDS3C_23p/ Y1	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel23. Same pin can be configured as Single ended I/O.
140	FPGA_AA8_LVDS3C_17p	LVDS3C_17p/ AA8	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel17. Same pin can be configured as Single ended I/O.
141	FPGA_Y2_LVDS3C_23n	LVDS3C_23n/ Y2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel23. Same pin can be configured as Single ended I/O.
142	FPGA_AA9_LVDS3C_17n	LVDS3C_17n/ AA9	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel17. Same pin can be configured as Single ended I/O.
143	FPGA_V3_LVDS3C_9n	LVDS3C_9n/ V3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel9. Same pin can be configured as Single ended I/O.
144	FPGA_Y3_LVDS3C_19p	LVDS3C_19p/ Y3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel19. Same pin can be configured as Single ended I/O.
145	FPGA_U3_LVDS3C_9p	LVDS3C_9p/ U3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel9. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
146	FPGA_Y4_LVDS3C_19n	LVDS3C_19n/ Y4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel19. Same pin can be configured as Single ended I/O.
147	FPGA_V2_LVDS3C_11p	LVDS3C_11p/ V2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel11. Same pin can be configured as Single ended I/O.
148	FPGA_V5_LVDS3C_6p	LVDS3C_6p/ V5	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel6. Same pin can be configured as Single ended I/O.
149	FPGA_U2_LVDS3C_11n	LVDS3C_11n/ U2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel11. Same pin can be configured as Single ended I/O.
150	FPGA_V4_LVDS3C_6n	LVDS3C_6n/ V4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel6. Same pin can be configured as Single ended I/O.
151	FPGA_U6_LVDS3C_5p	LVDS3C_5p/ U6	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel5. Same pin can be configured as Single ended I/O.
152	FPGA_W6_LVDS3C_16p	LVDS3C_16p/ W6	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel16. Same pin can be configured as Single ended I/O.
153	FPGA_U5_LVDS3C_5n	LVDS3C_5n/ U5	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel5. Same pin can be configured as Single ended I/O.
154	FPGA_W7_LVDS3C_16n	LVDS3C_16n/ W7	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel16. Same pin can be configured as Single ended I/O.
155	FPGA_T4_LVDS3C_1p	LVDS3C_1p/ T4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel1. Same pin can be configured as Single ended I/O.
156	FPGA_Y8_LVDS3C_14p	LVDS3C_14p/ Y8	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel14. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
157	FPGA_R4_LVDS3C_1n	LVDS3C_1n/ R4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel1. Same pin can be configured as Single ended I/O.
158	FPGA_Y9_LVDS3C_14n	LVDS3C_14n/ Y9	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel14. Same pin can be configured as Single ended I/O.
159	FPGA_R1_LVDS3C_8p	LVDS3C_8p/ R1	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel8. Same pin can be configured as Single ended I/O.
160	FPGA_R3_LVDS3C_3n	LVDS3C_3n/ R3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel3. Same pin can be configured as Single ended I/O.
161	FPGA_P1_LVDS3C_8n	LVDS3C_8n/ P1	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel8. Same pin can be configured as Single ended I/O.
162	FPGA_T3_LVDS3C_3p	LVDS3C_3p/ T3	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel3. Same pin can be configured as Single ended I/O.
163	FPGA_P2_LVDS3C_7p	LVDS3C_7p/ P2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel7. Same pin can be configured as Single ended I/O.
164	FPGA_P4_LVDS3C_2p	LVDS3C_2p/ P4	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel2. Same pin can be configured as Single ended I/O.
165	FPGA_R2_LVDS3C_7n	LVDS3C_7n/ R2	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel7. Same pin can be configured as Single ended I/O.
166	FPGA_P5_LVDS3C_2n	LVDS3C_2n/ P5	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel2. Same pin can be configured as Single ended I/O.
167	GND	NA	Power	Ground.
168	GND	NA	Power	Ground.
169	FPGA_U1_LVDS3C_10p/ CLKOUT_1p	LVDS3C_10p/ U1	IO, 1.8V LVDS	Bank3C Clock Output differential positive channel1. Same pin can be configured as Single Ended Clock Output or User I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
170	FPGA_W4_LVDS3C_15p /CLKOUT_0p	LVDS3C_15p/ W4	IO, 1.8V LVDS	Bank3C Clock Output differential positive channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
171	FPGA_T1_LVDS3C_10n/ CLKOUT_1n	LVDS3C_10n/ T1	IO, 1.8V LVDS	Bank3C Clock Output differential negative channel1. Same pin can be configured as Single Ended Clock Output or User I/O.
172	FPGA_W5_LVDS3C_15n /CLKOUT_0n	LVDS3C_15n/ W5	IO, 1.8V LVDS	Bank3C Clock Output differential negative channel0. Same pin can be configured as Single Ended Clock Output or User I/O.
173	GND	NA	Power	Ground.
174	GND	NA	Power	Ground.
175	FPGA_W1_LVDS3C_12p /CLKIN_1p	LVDS3C_12p/ W1	IO, 1.8V LVDS	Bank3C Clock Input differential positive channel1. Same pin can be configured as Single Ended Clock Input or User I/O.
176	FPGA_Y6_LVDS3C_13p/ CLKIN_0p	LVDS3C_13p/ Y6	IO, 1.8V LVDS	Bank3C Clock Input differential positive channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
177	FPGA_W2_LVDS3C_12n /CLKIN_1n	LVDS3C_12n/ W2	IO, 1.8V LVDS	Bank3C Clock Input differential negative channel1. Same pin can be configured as Single Ended Clock Input or User I/O.
178	FPGA_Y7_LVDS3C_13n/ CLKIN_0n	LVDS3C_13n/ Y7	IO, 1.8V LVDS	Bank3C Clock Input differential negative channel0. Same pin can be configured as Single Ended Clock Input or User I/O.
179	GND	NA	Power	Ground.
180	GND	NA	Power	Ground.
181	FPGA_T6_LVDS3C_4n	LVDS3C_4n/ T6	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel4. Same pin can be configured as Single ended I/O.
182	FPGA_AA5_LVDS3C_18 p	LVDS3C_18p/ AA5	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel18. Same pin can be configured as Single ended I/O.
183	FPGA_T5_LVDS3C_4p	LVDS3C_4p/ T5	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel4. Same pin can be configured as Single ended I/O.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
184	FPGA_AA6_LVDS3C_18n	LVDS3C_18n/ AA6	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel18. Same pin can be configured as Single ended I/O.
185	GND	NA	Power	Ground.
186	GND	NA	Power	Ground.
187	GXBL1F_RX_CH0p	GXBL1F_RX_CH0P/ L30	IO, 1.8V LVDS	Bank1F High speed positive differential receiver channel0. If unused connect this pin to GND.
188	REFCLK_GXBL1F_CHTp	REFCLK_GXBL1F_CHTp /M28	IO, 1.8V LVDS	Bank1F High speed differential reference clock positive receiver channel T. If unused connect this pin to GND.
189	GXBL1F_RX_CH0n	GXBL1F_RX_CH0n/ L29	IO, 1.8V LVDS	Bank1F High speed negative differential receiver channel0. If unused connect this pin to GND.
190	REFCLK_GXBL1F_CHTn	REFCLK_GXBL1F_CHTn /M27	IO, 1.8V LVDS	Bank1F High speed differential reference clock negative receiver channel T. If unused connect this pin to GND.
191	GND	NA	Power	Ground.
192	GND	NA	Power	Ground.
193	GXBL1F_TX_CH0p	GXBL1F_TX_CH0p/ E34	O, DIFF	Bank1F High speed positive differential transmitter channel0. If unused leave this pin floating.
194	GXBL1F_RX_CH3p	GXBL1F_RX_CH3p/ G30	I, DIFF	Bank1F High speed positive differential receiver channel3. If unused connect this pin to GND.
195	GXBL1F_TX_CH0n	GXBL1F_TX_CH0n/ E33	O, DIFF	Bank1F High speed negative differential transmitter channel0. If unused leave this pin floating.
196	GXBL1F_RX_CH3n	GXBL1F_RX_CH3n/ G29	I, DIFF	Bank1F High speed negative differential receiver channel3. If unused connect this pin to GND.
197	GND	NA	Power	Ground.
198	GND	NA	Power	Ground.
199	GXBL1F_RX_CH1p	GXBL1F_RX_CH1p/ K32	I, DIFF	Bank1F High speed positive differential receiver channel1. If unused connect this pin to GND.
200	GXBL1F_TX_CH3p	GXBL1F_TX_CH3p/ F32	O, DIFF	Bank1F High speed positive differential transmitter channel3. If unused leave this pin floating.
201	GXBL1F_RX_CH1n	GXBL1F_RX_CH1n/ K31	I, DIFF	Bank1F High speed negative differential receiver channel1. If unused connect this pin to GND.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
202	GXBL1F_TX_CH3n	GXBL1F_TX_CH3n/ F31	O, DIFF	Bank1F High speed negative differential transmitter channel3. If unused leave this pin floating.
203	GND	NA	Power	Ground.
204	GND	NA	Power	Ground.
205	GXBL1F_TX_CH1p	GXBL1F_TX_CH1p/ C34	O, DIFF	Bank1F High speed positive differential transmitter channel1. If unused leave this pin floating.
206	GXBL1F_RX_CH4p	GXBL1F_RX_CH4p/ E30	I, DIFF	Bank1F High speed positive differential receiver channel4. If unused connect this pin to GND.
207	GXBL1F_TX_CH1n	GXBL1F_TX_CH1n/ C33	O, DIFF	Bank1F High speed negative differential transmitter channel1. If unused leave this pin floating.
208	GXBL1F_RX_CH4n	GXBL1F_RX_CH4n/ E29	I, DIFF	Bank1F High speed negative differential receiver channel4. If unused connect this pin to GND.
209	GND	NA	Power	Ground.
210	GND	NA	Power	Ground.
211	GXBL1F_RX_CH2p	GXBL1F_RX_CH2p/ J30	I, DIFF	Bank1F High speed positive differential receiver channel2. If unused connect this pin to GND.
212	GXBL1F_TX_CH4p	GXBL1F_TX_CH4p/ D32	O, DIFF	Bank1F High speed positive differential transmitter channel4. If unused leave this pin floating.
213	GXBL1F_RX_CH2n	GXBL1F_RX_CH2n/ J29	I, DIFF	Bank1F High speed negative differential receiver channel2. If unused connect this pin to GND.
214	GXBL1F_TX_CH4n	GXBL1F_TX_CH4n/ D31	O, DIFF	Bank1F High speed negative differential transmitter channel4. If unused leave this pin floating.
215	GND	NA	Power	Ground.
216	GND	NA	Power	Ground.
217	GXBL1F_TX_CH2p	GXBL1F_TX_CH2p/ H32	O, DIFF	Bank1F High speed positive differential transmitter channel2. If unused leave this pin floating.
218	GXBL1F_RX_CH5p	GXBL1F_RX_CH5p/ C30	I, DIFF	Bank1F High speed positive differential receiver channel5. If unused connect this pin to GND.
219	GXBL1F_TX_CH2n	GXBL1F_TX_CH2n/ H31	O, DIFF	Bank1F High speed negative differential transmitter channel2. If unused leave this pin floating.
220	GXBL1F_RX_CH5n	GXBL1F_RX_CH5n/ C29	I, DIFF	Bank1F High speed negative differential receiver channel5. If unused connect this pin to GND.
221	GND	NA	Power	Ground.
222	GND	NA	Power	Ground.

Pin No	Signal Name	Arrai10 Ball Name/ Pin Number	Signal Type/ Termination	Description
223	REFCLK_GXBL1F_CHBp	REFCLK_GXBL1F_CHBp/P28	I, DIFF	Bank1F High speed differential reference clock positive receiver channel B. If unused connect this pin to GND.
224	GXBL1F_TX_CH5p	GXBL1F_TX_CH5p/ B32	O, DIFF	Bank1F High speed positive differential transmitter channel5. If unused leave this pin floating.
225	REFCLK_GXBL1F_CHBn	REFCLK_GXBL1F_CHBn/P27	I, DIFF	Bank1F High speed differential reference clock negative receiver channel B. If unused connect this pin to GND.
226	GXBL1F_TX_CH5n	GXBL1F_TX_CH5n/ B31	O, DIFF	Bank1F High speed negative differential transmitter channel5. If unused leave this pin floating.
227	GND	NA	Power	Ground.
228	GND	NA	Power	Ground.
229	GXBL1E_RX_CH4p	GXBL1E_RX_CH4p/ N30	I, DIFF	Bank1E High speed positive differential receiver channel4. If unused connect this pin to GND.
230	GXBL1E_RX_CH5p	GXBL1E_RX_CH5p/ M32	I, DIFF	Bank1E High speed positive differential receiver channel5. If unused connect this pin to GND.
231	GXBL1E_RX_CH4n	GXBL1E_RX_CH4n/ N29	I, DIFF	Bank1E High speed negative differential receiver channel4. If unused connect this pin to GND.
232	GXBL1E_RX_CH5n	GXBL1E_RX_CH5n/ M31	I, DIFF	Bank1E High speed negative differential receiver channel5. If unused connect this pin to GND.
233	GND	NA	Power	Ground.
234	GND	NA	Power	Ground.
235	GXBL1E_TX_CH4p	GXBL1E_TX_CH4p/ J34	O, DIFF	Bank1E High speed positive differential transmitter channel4. If unused leave this pin floating.
236	GXBL1E_TX_CH5p	GXBL1E_TX_CH5p/ G34	O, DIFF	Bank1E High speed positive differential transmitter channel5. If unused leave this pin floating.
237	GXBL1E_TX_CH4n	GXBL1E_TX_CH4n/ J33	O, DIFF	Bank1E High speed negative differential transmitter channel4. If unused leave this pin floating.
238	GXBL1E_TX_CH5n	GXBL1E_TX_CH5n/ G33	O, DIFF	Bank1E High speed negative differential transmitter channel5. If unused leave this pin floating.
239	GND	NA	Power	Ground.
240	GND	NA	Power	Ground.

2.8 Arria10 SoC HPS Pin Multiplexing on Expansion Connector2

The Arria10 SoC HPS's IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the Arria10 HPS's IO pins can be configured as GPIO if required. The below table provides the details of Arria10 HPS pin connections to the Expansion connector2 with selected pin function highlighted and available alternate functions. This table has been prepared by referring Hard Processor System Pin Information of Arria10 SoC device.

Table 12: Arria10 SoC HPS IOMUX on Expansion Connector2

Interface/ Function	Expansion Connector2 Pin Number	Arria10 SoC HPS Pin Name	HPS Pin Mux Select 15	HPS Pin Mux Select 14	HPS Pin Mux Select 13	HPS Pin Mux Select 12	HPS Pin Mux Select 8	HPS Pin Mux Select 4	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
On-SOM Features from Arria10 HPS												
Micro SD Connector (or) NAND Flash	NA	HPS_DEDICATED_4	GPIO2_IO0	NAND_ADQ0			SDMMC_DATA0	QSPI_CLK				
	NA	HPS_DEDICATED_5	GPIO2_IO1	NAND_ADQ1			SDMMC_CMD	QSPI_IO0				
	NA	HPS_DEDICATED_6	GPIO2_IO2	NAND_WE_N			SDMMC_CCLK	QSPI_SS0				
	NA	HPS_DEDICATED_7	GPIO2_IO3	NAND_RE_N			SDMMC_DATA1	QSPI_IO1				
	NA	HPS_DEDICATED_8	GPIO2_IO4	NAND_ADQ2			SDMMC_DATA2	QSPI_IO2_WPN				
	NA	HPS_DEDICATED_9	GPIO2_IO5	NAND_ADQ3			SDMMC_DATA3	QSPI_IO3_HOLD				
	NA		GPIO2_IO6	NAND_CLE			SDMMC_PWR_EN		SPIM0_SS1_N	SPIS0_MISO		
	NA		GPIO2_IO7	NAND_ALE			QSPI_SS1	CM_PLL_CLK0	SPIM0_CLK			
	NA	HPS_DEDICATED_12	GPIO2_IO8	NAND_RB	UART1_TX		SDMMC_DATA4	CM_PLL_CLK1	SPIM0_MOSI		EMAC1_MDIO	I2C_EMAC1_SDA
	NA	HPS_DEDICATED_13	GPIO2_IO9	NAND_CE_N	UART1_RTS_N		SDMMC_DATA5	CM_PLL_CLK2	SPIM0_MISO		EMAC1_MDC	I2C_EMAC1_SCL
	NA	HPS_DEDICATED_14	GPIO2_IO10	NAND_ADQ4	UART1_CTS_N		SDMMC_DATA6	CM_PLL_CLK3	SPIM0_SS0_N		EMAC2_MDIO	I2C_EMAC2_SDA
	NA	HPS_DEDICATED_15	GPIO2_IO11	NAND_ADQ5	UART1_RX		SDMMC_DATA7	CM_PLL_CLK4		SPIS0_CLK	EMAC2_MDC	I2C_EMAC2_SCL
	NA	HPS_DEDICATED_16	GPIO2_IO12	NAND_ADQ6	UART1_TX		QSPI_SS2			SPIS0_MOSI	EMAC0_MDIO	I2C_EMAC0_SDA
	NA	HPS_DEDICATED_17	GPIO2_IO13	NAND_ADQ7	UART1_RX		QSPI_SS3			SPIS0_SS0_N	EMAC0_MDC	I2C_EMAC0_SCL

Interface/ Function	Expansion Connector2 Pin Number	Arria10 SoC HPS Pin Name	HPS Pin Mux Select 15	HPS Pin Mux Select 14	HPS Pin Mux Select 13	HPS Pin Mux Select 12	HPS Pin Mux Select 8	HPS Pin Mux Select 4	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
EMAC1	NA	HPS_DIRECT_SHARED_Q3_12	GPIO1_IO11	NAND_ADQ7			EMAC1_RXD3			SPIS0_MISO	EMAC0_MDC	I2C_EMAC0_SCL
	NA	HPS_DIRECT_SHARED_Q3_11	GPIO1_IO10	NAND_ADQ6			EMAC1_RXD2			SPIS0_SS0_N	EMAC0_MDIO	I2C_EMAC0_SDA
	NA	HPS_DIRECT_SHARED_Q3_10	GPIO1_IO9	NAND_ADQ5			EMAC1_TXD3			SPIS0_MOSI	EMAC2_MDC	I2C_EMAC2_SCL
	NA	HPS_DIRECT_SHARED_Q3_9	GPIO1_IO8	NAND_ADQ4			EMAC1_TXD2			SPIS0_CLK	EMAC2_MDIO	I2C_EMAC2_SDA
	NA	HPS_DIRECT_SHARED_Q3_8	GPIO1_IO7	NAND_CLE	UART1_RX		EMAC1_RXD1			SPIS1_MISO		I2C1_SCL
	NA	HPS_DIRECT_SHARED_Q3_7	GPIO1_IO6	NAND_ADQ3	UART1_TX		EMAC1_RXD0			SPIS1_SS0_N		I2C1_SDA
	NA	HPS_DIRECT_SHARED_Q3_6	GPIO1_IO5	NAND_ADQ2	UART1_RTS_N		EMAC1_TXD1			SPIS1_MOSI		
	NA	HPS_DIRECT_SHARED_Q3_5	GPIO1_IO4	NAND_WP_N	UART1_CTS_N		EMAC1_TXD0		SPIM1_SS1_N	SPIS1_CLK		
	NA	HPS_DIRECT_SHARED_Q3_4	GPIO1_IO3	NAND_RE_N	UART0_RX		EMAC1_RX_CTL		SPIM1_SS0_N			I2C0_SCL
	NA	HPS_DIRECT_SHARED_Q3_3	GPIO1_IO2	NAND_WE_N	UART0_TX		EMAC1_RX_CLK		SPIM1_MISO			I2C0_SDA
	NA	HPS_DIRECT_SHARED_Q3_2	GPIO1_IO1	NAND_ADQ1	UART0_RTS_N		EMAC1_TX_CTL		SPIM1_MOSI			
	NA	HPS_DIRECT_SHARED_Q3_1	GPIO1_IO0	NAND_ADQ0	UART0_CTS_N		EMAC1_TX_CLK		SPIM1_CLK			
	NA	HPS_DIRECT_SHARED_Q1_10	GPIO0_IO9	NAND_ADQ5			USB0_DATA5	SDMMC_DATA7	SPIM1_MOSI	SPIS1_MOSI	EMAC1_MDC	I2C_EMAC1_SCL
	NA	HPS_DIRECT_SHARED_Q1_9	GPIO0_IO8	NAND_ADQ4			USB0_DATA4	SDMMC_DATA6	SPIM1_CLK	SPIS1_CLK	EMAC1_MDIO	I2C_EMAC1_SDA
USB1	NA	HPS_DIRECT_SHARED_Q2_12	GPIO0_IO23	NAND_ADQ15	UART0_RX		USB1_DATA7	EMAC0_RXD3	SPIM1_SS0_N	SPIS0_MISO		I2C0_SCL
	NA	HPS_DIRECT_SHARED_Q2_11	GPIO0_IO22	NAND_ADQ14	UART0_TX		USB1_DATA6	EMAC0_RXD2	SPIM1_MISO	SPIS0_SS0_N		I2C0_SDA
	NA	HPS_DIRECT_SHARED_Q2_10	GPIO0_IO21	NAND_ADQ13	UART0_RTS_N		USB1_DATA5	EMAC0_TXD3	SPIM1_MOSI	SPIS0_MOSI		I2C1_SCL
	NA	HPS_DIRECT_SHARED_Q2_9	GPIO0_IO20	NAND_ADQ12	UART0_CTS_N		USB1_DATA4	EMAC0_TXD2	SPIM1_CLK	SPIS0_CLK		I2C1_SDA
	NA	HPS_DIRECT_SHARED_Q2_8	GPIO0_IO19	NAND_ADQ11			USB1_DATA3	EMAC0_RXD1	SPIM1_SS1_N			
	NA	HPS_DIRECT_SHARED_Q2_7	GPIO0_IO18	NAND_ADQ10			USB1_DATA2	EMAC0_RXD0				
	NA	HPS_DIRECT_SHARED_Q2_6	GPIO0_IO17	NAND_ADQ9			USB1_NXT	EMAC0_TXD1				
	NA	HPS_DIRECT_SHARED_Q2_5	GPIO0_IO16	NAND_ADQ8			USB1_DATA1	EMAC0_TXD0				
	NA	HPS_DIRECT_SHARED_Q2_4	GPIO0_IO15				USB1_DATA0	EMAC0_RX_CTL				
	NA	HPS_DIRECT_SHARED_Q2_3	GPIO0_IO14	NAND_CE_N			USB1_DIR	EMAC0_RX_CLK				
	NA	HPS_DIRECT_SHARED_Q2_2	GPIO0_IO13	NAND_RB			USB1_STP	EMAC0_TX_CTL				
	NA	HPS_DIRECT_SHARED_Q2_1	GPIO0_IO12	NAND_ALE			USB1_CLK	EMAC0_TX_CLK				

Interface/ Function	Expansion Connector2 Pin Number	Arria10 SoC HPS Pin Name	HPS Pin Mux Select 15	HPS Pin Mux Select 14	HPS Pin Mux Select 13	HPS Pin Mux Select 12	HPS Pin Mux Select 8	HPS Pin Mux Select 4	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
Expansion Connector2 Interfaces from Arria10 HPS												
GPIOs	68	HPS_DIRECT_SHARED_Q1_1	GPIO0_IO0	NAND_ADQ0	UART0_CTS_N		USB0_CLK	SDMMC_DATA0	SPIM0_SS1_N	SPIS0_CLK		
	70	HPS_DIRECT_SHARED_Q1_2	GPIO0_IO1	NAND_ADQ1	UART0_RTS_N		USB0_STP	SDMMC_CMD	SPIM1_SS1_N	SPIS0_MOSI		
	38	HPS_DIRECT_SHARED_Q1_11	GPIO0_IO10	NAND_ADQ6			USB0_DATA6		SPIM1_MISO	SPIS1_SS0_N	EMAC0_MDIO	I2C_EMAC0_SDA
	44	HPS_DIRECT_SHARED_Q1_12	GPIO0_IO11	NAND_ADQ7			USB0_DATA7		SPIM1_SS0_N	SPIS1_MISO	EMAC0_MDC	I2C_EMAC0_SCL
	72	HPS_DIRECT_SHARED_Q4_3	GPIO1_IO14	NAND_CE_N	UART1_TX		EMAC2_RX_CLK	SDMMC_CCLK				
	66	HPS_DIRECT_SHARED_Q4_4	GPIO1_IO15		UART1_RX	Trace_CLK	EMAC2_RX_CTL	SDMMC_DATA1				
	64	HPS_DIRECT_SHARED_Q4_5	GPIO1_IO16	NAND_ADQ8	UART1_CTS_N	QSPI_SS2	EMAC2_TXD0	SDMMC_DATA2				
	62	HPS_DIRECT_SHARED_Q4_6	GPIO1_IO17	NAND_ADQ9	UART1_RTS_N	QSPI_SS3	EMAC2_TXD1	SDMMC_DATA3	SPIM0_SS1_N			
	42	HPS_DIRECT_SHARED_Q4_7	GPIO1_IO18	NAND_ADQ10			EMAC2_RXD0	SDMMC_DATA4	SPIM0_MISO		EMAC1_MDIO	I2C_EMAC1_SDA
	40	HPS_DIRECT_SHARED_Q4_8	GPIO1_IO19	NAND_ADQ11		Trace_CLK	EMAC2_RXD1	SDMMC_DATA5	SPIM0_SS0_N		EMAC1_MDC	I2C_EMAC1_SCL
	71	HPS_DIRECT_SHARED_Q4_2	GPIO1_IO13	NAND_RB			EMAC2_TX_CTL	SDMMC_CMD				I2C1_SCL
	69	HPS_DIRECT_SHARED_Q4_1	GPIO1_IO12	NAND_ALE			EMAC2_TX_CLK	SDMMC_DATA0				I2C1_SDA
SPI	63	HPS_DIRECT_SHARED_Q4_12	GPIO1_IO23	NAND_ADQ15		Trace_D3	EMAC2_RXD3		SPIM0_SS0_N	SPIS1_MISO	EMAC0_MDC	I2C_EMAC0_SCL
	67	HPS_DIRECT_SHARED_Q4_11	GPIO1_IO22	NAND_ADQ14		Trace_D2	EMAC2_RXD2		SPIM0_MISO	SPIS1_SS0_N	EMAC0_MDIO	I2C_EMAC0_SDA
	65	HPS_DIRECT_SHARED_Q4_10	GPIO1_IO21	NAND_ADQ13		Trace_D1	EMAC2_TXD3	SDMMC_DATA7	SPIM0_MOSI	SPIS1_MOSI		I2C_EMAC2_SCL
	61	HPS_DIRECT_SHARED_Q4_9	GPIO1_IO20	NAND_ADQ12		Trace_D0	EMAC2_TXD2	SDMMC_DATA6	SPIM0_CLK	SPIS1_CLK		I2C_EMAC2_SDA
UART1	52	HPS_DIRECT_SHARED_Q1_8	GPIO0_IO7	NAND_CLE	UART1_RX		USB0_DATA3	SDMMC_DATA5	SPIM0_SS0_N		EMAC2_MDC	I2C_EMAC2_SCL
	50	HPS_DIRECT_SHARED_Q1_7	GPIO0_IO6	NAND_ADQ3	UART1_TX		USB0_DATA2	SDMMC_DATA4	SPIM0_MISO		EMAC2_MDIO	I2C_EMAC2_SDA
I2C	48	HPS_DIRECT_SHARED_Q1_6	GPIO0_IO5	NAND_ADQ2	UART1_RTS_N	QSPI_SS3	USB0_NXT	SDMMC_DATA3	SPIM0_MOSI			I2C0_SCL
	46	HPS_DIRECT_SHARED_Q1_5	GPIO0_IO4	NAND_WP_N	UART1_CTS_N	QSPI_SS2	USB0_DATA1	SDMMC_DATA2	SPIM0_CLK			I2C0_SDA
Debug UART0	56	HPS_DIRECT_SHARED_Q1_4	GPIO0_IO3	NAND_RE_N	UART0_RX		USB0_DATA0	SDMMC_DATA1		SPIS0_MISO		I2C1_SCL
	54	HPS_DIRECT_SHARED_Q1_3	GPIO0_IO2	NAND_WE_N	UART0_TX		USB0_DIR	SDMMC_CCLK		SPIS0_SS0_N		I2C1_SDA

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Arria10 SoC/FPGA SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Arria10 SoC/FPGA SOM.

Table 13: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC[1]	4.75V	5V	5.25V	±50mV

[1] The Arria10 SoC/FPGA SOM is designed to work with VCC input power rail from Expansion connector2.

3.1.2 Power Consumption

Table 14: Power Consumption

Task/Status	Power Rail	Current Drawn/Power Consumption
Run Mode Power Consumption		
Ethernet 1000Mbps ping	VCC	1.88A/9.4W
Dhrystone benchmark application	VCC	1.92A/9.6W
USB2.0 Host to Micro SD files transfer.	VCC	1.95A/9.75W
HPS DDR4 Read and Write	VCC	1.98A/9.9W
Typical Maximum Power: • Ethernet 1000Mbps ping. • Dhrystone benchmark application • USB2.0 Host to Micro SD files transfer • HPS DDR4 Read and Write	VCC	2.11A/10.55W

[1] Power consumption measurements have been done in iWave's Arria10 SX480 SOM (iW-G24M-CU2F-4E002G-S008G-LEF) with only HPS enabled.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Arria10 SoC/FPGA SOM.

Table 15: Environmental Specification

Parameters	Min	Max
Operating temperature range - Industrial[1,2]	-40°C	85°C
Operating temperature range - Extended[1,2]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

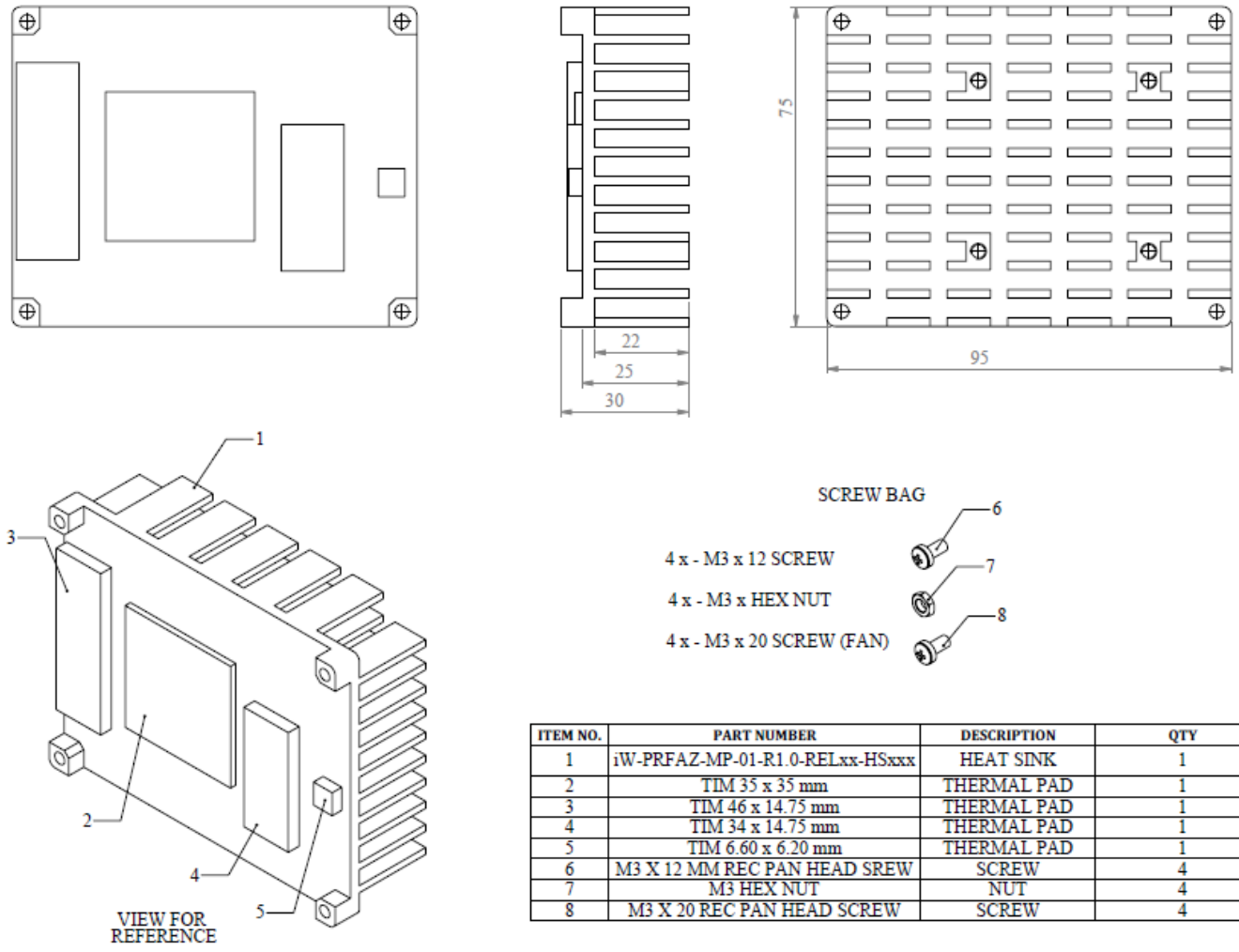
[2]For more information on Thermal solution & Heat spreader refer the following section.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique like Heat spreader, Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the SoC/FPGA.

iWave supports Heat Sink Solution for Arria10 SoC/FPGA SOM. Please refer the below figure for Heat Sink dimension details. For Heat Sink ordering information, refer section 4 **ORDERING INFORMATION**.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY
1	iW-PRFAZ-MP-01-R1.0-RELxx-HSxxx	HEAT SINK	1
2	TIM 35 x 35 mm	THERMAL PAD	1
3	TIM 46 x 14.75 mm	THERMAL PAD	1
4	TIM 34 x 14.75 mm	THERMAL PAD	1
5	TIM 6.60 x 6.20 mm	THERMAL PAD	1
6	M3 X 12 MM REC PAN HEAD SREW	SCREW	4
7	M3 HEX NUT	NUT	4
8	M3 X 20 REC PAN HEAD SCREW	SCREW	4

Figure 9: Heat Sink Dimensions

Note: In high Shock/Vibration environment, it is recommended to use thread-locking fluid on Heat spreader screws.

3.2.3 RoHS Compliance

iWave's Arria10 SoC/FPGA SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's Arria10 SoC/FPGA SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 Arria10 SoC/FPGA SOM Mechanical Dimensions

The Arria10 SoC/FPGA SOM PCB size is 95mm x 75mm x 1.5mm. Its mechanical dimension is shown below.

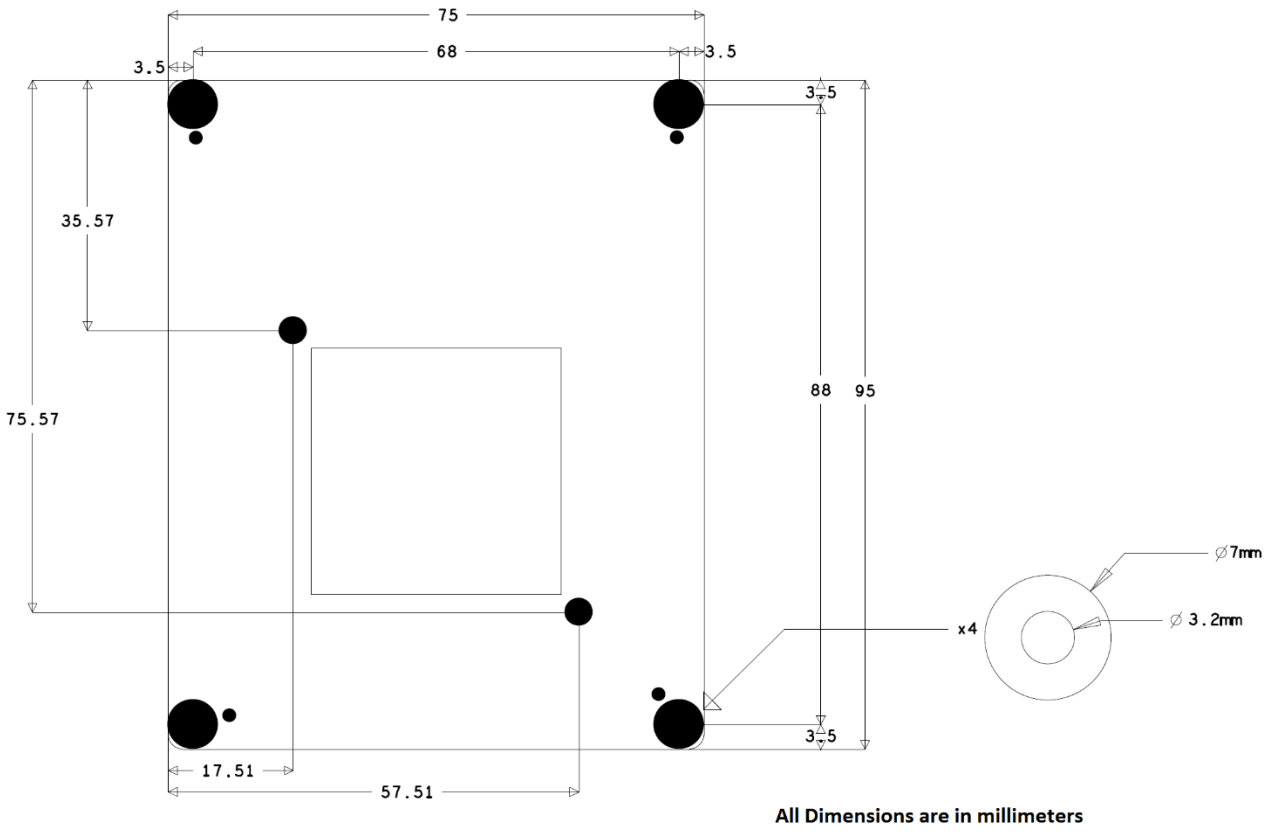


Figure 10: Mechanical dimension of Arria10 SoC/FPGA SOM- Top View

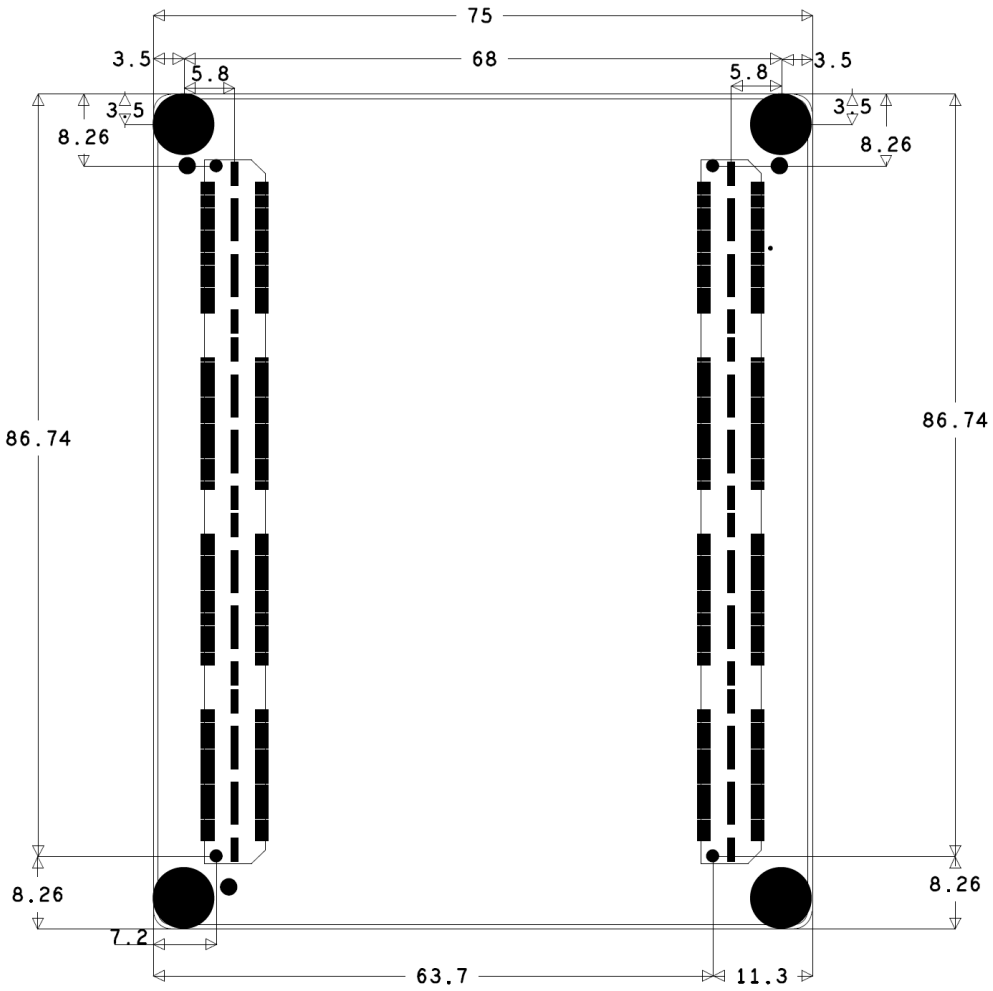


Figure 11: Mechanical dimension of Arria10 SoC/FPGA SOM- Bottom View

Arria10 SoC/FPGA SOM PCB thickness is 1.5mm±0.10mm, top side maximum height component is FAN Header (3.5mm) followed by Arria10 which can vary from 3.2mm to 3.5mm and bottom side maximum height component is expansion connector (4.270mm). For more details, refer the below figure which gives height details of Arria10 SoC/FPGA SOM.

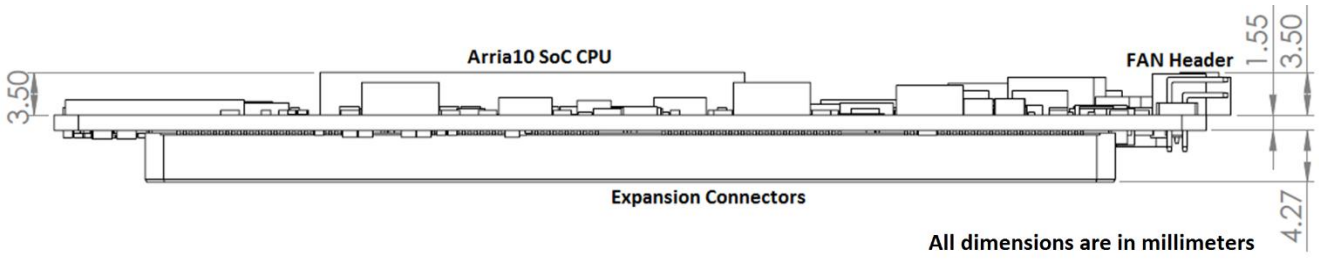


Figure 12: Mechanical dimension of Arria10 SoC/FPGA SOM- Side View

3.3.2 Guidelines to insert the Arria10 SoC/FPGA SOM into Carrier board

- Make sure to use anti-static work environment and wear the anti-static wristband while handling the boards.
- Make sure that the carrier board is completely powered off.
- Insert the Arria10 SoC/FPGA SOM in to the expansion connectors as shown below in first photo.
- Check the position of Expansion connector 1 and Expansion connector 2 of Arria10 SoC/FPGA SOM is proper while inserting.
- Once the Arria10 SoC/FPGA SOM is inserted to the Expansion connector 1 and Expansion connector 2 properly, press the board vertically down such that the board is fixed firmly into the expansion connectors as shown below in second photo.

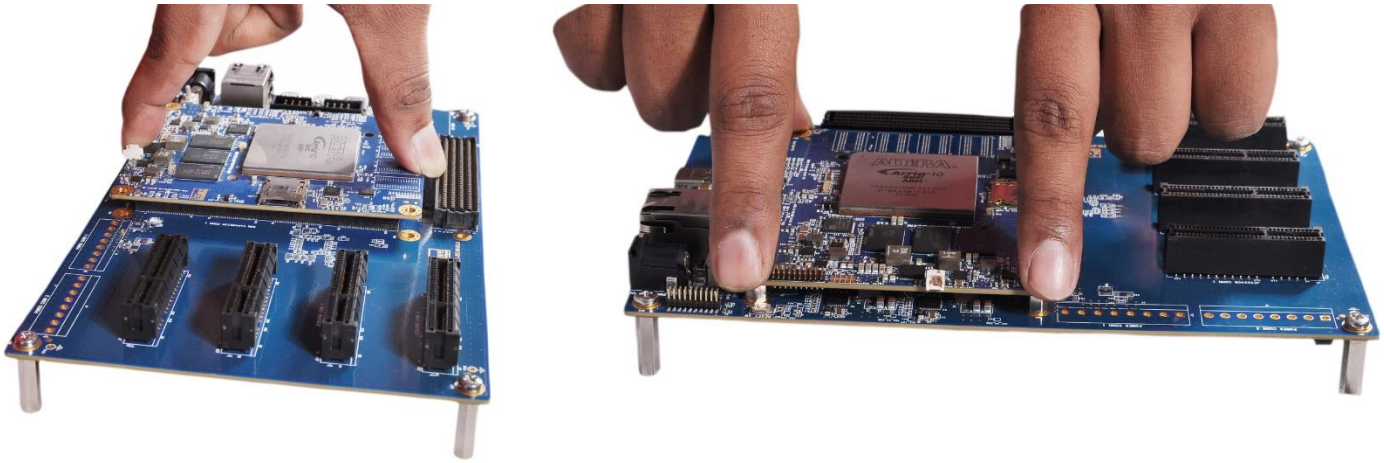


Figure 13: Arria10 SoC/FPGA SOM Insertion procedure

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Arria10 SoC/FPGA SOM variations. Please contact iWave if the desired part number is not listed in below table or if any custom configuration part number is required.

Table 16: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Arria10 SoC/FPGA SOM		
iW-G24M-CU2F-4E002G-S000G-NIF	With Arria10 SX480 SoC (10AS048H3F34I2SG), 2GB HPS DDR4 with ECC, 4GB FPGA DDR4, 480K Logic Elements, FPGA Fabric Speed Grade 2, Transceiver Speed Grade 3	Industrial
iW-G24M-CU2F-4E002G-S000G-NEF	With Arria10 SX480 SoC (10AS048H3F34E2SG), 2GB HPS DDR4 with ECC, 4GB FPGA DDR4, 480K Logic Elements, FPGA Fabric Speed Grade 2, Transceiver Speed Grade 3	Extended
Heat Sink		
iW-HSKALU-CLASLR-CU01	Heat Sink for Arria10 SoC/FPGA SOM	-

Important Note: Please contact iWave for orderable part number of higher density Arria10 SoC/FPGA, higher speed grade Arria10 SoC/FPGA or higher RAM memory size supported SOMs.

Note: For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX I

5.1 Arria10 SoC/FPGA SOM Development Platform

iWave Systems supports iW-RainboW-G24D – Arria10 SoC/FPGA SOM Development Platform which is targeted for quick validation of Arria10 SoC/FPGA based SOM and its features. The carrier board is packed with necessary interfaces & on-board connectors to validate Arria10 SoC/FPGA features.

For more details on Arria10 SoC/FPGA SOM Development Platform, visit the below web link.

http://www.iwavesystems.com/product/cpu-modules/arria-10-soc-system-on-module/altera-arria-10-soc-som-module.html

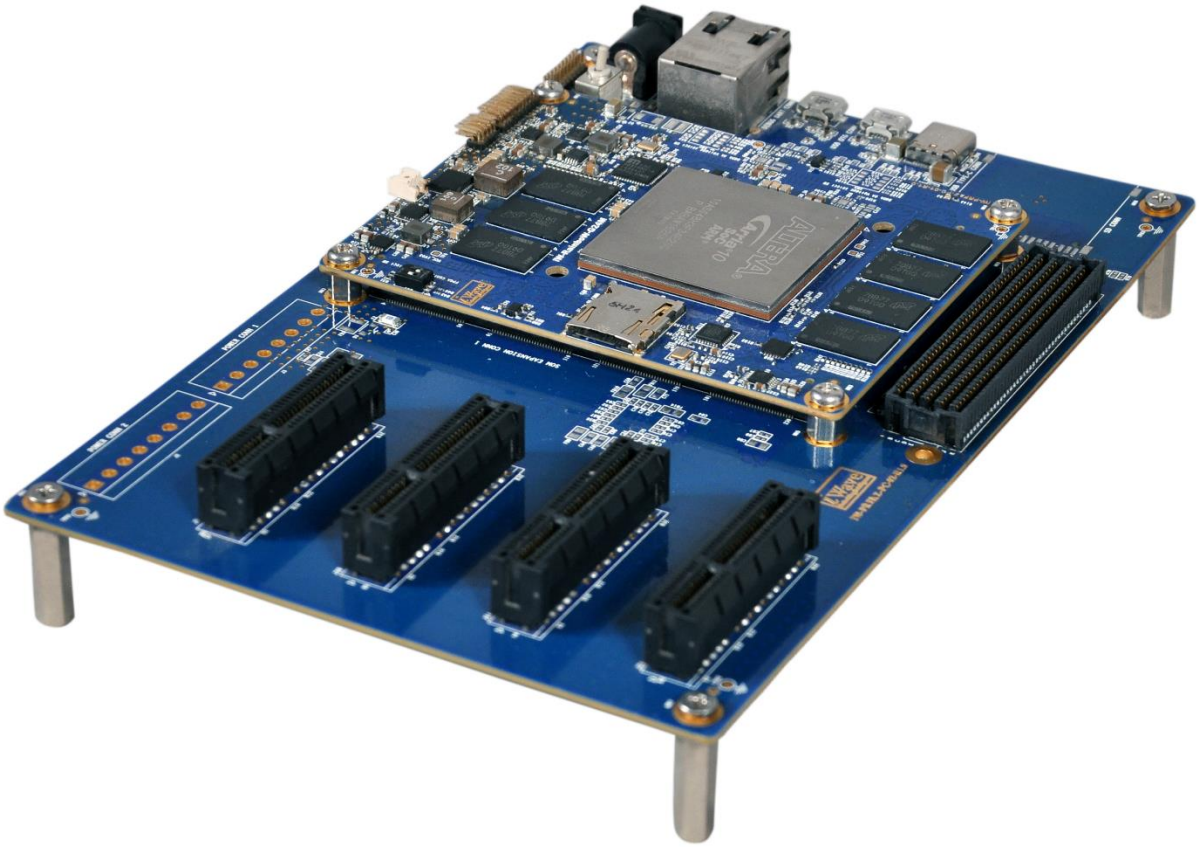


Figure 14: Arria10 SoC/FPGA SOM Development Platform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