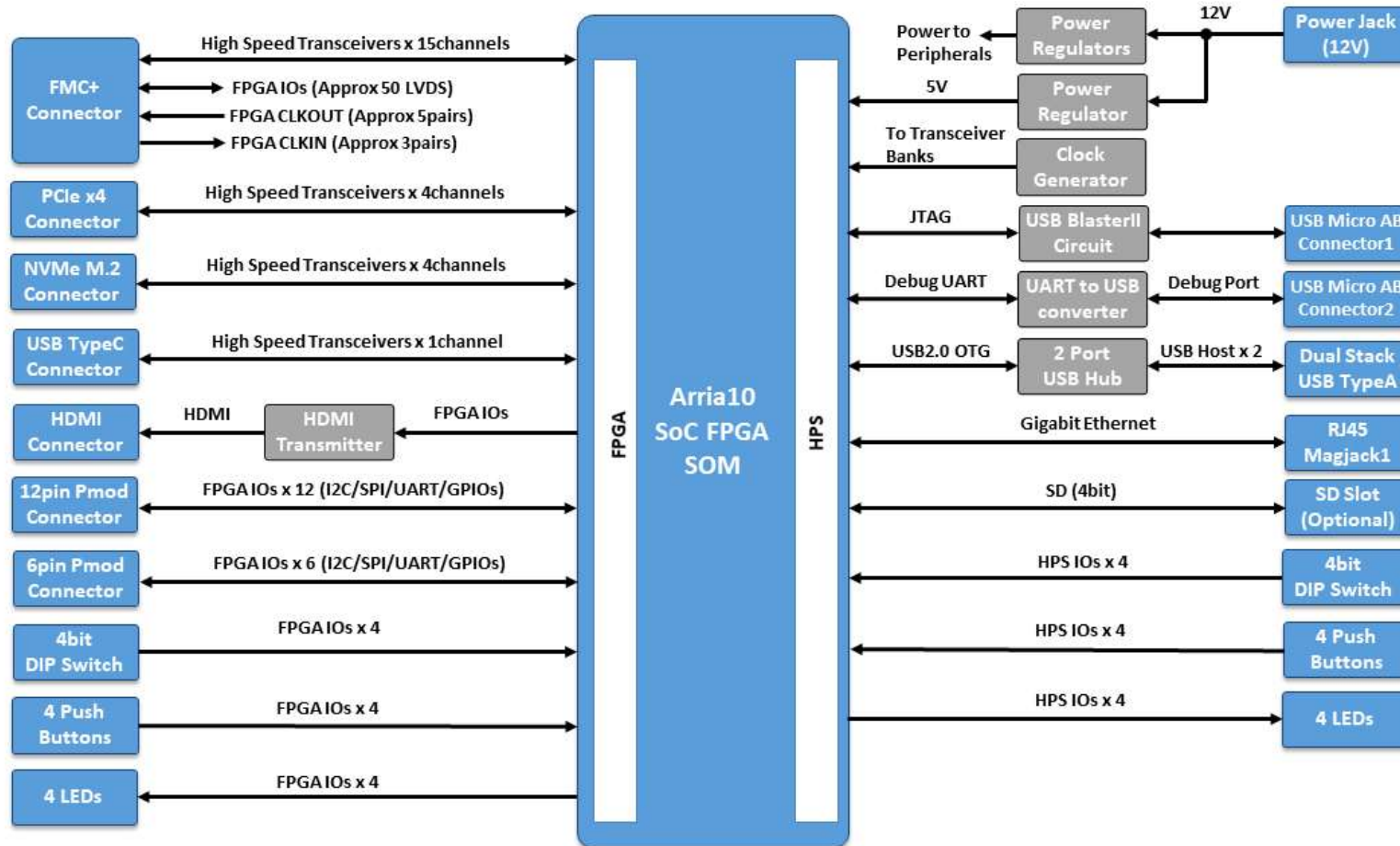


Arria10 SoC FPGA SOM - Carrier Board Refresh Block Diagram



INDEX

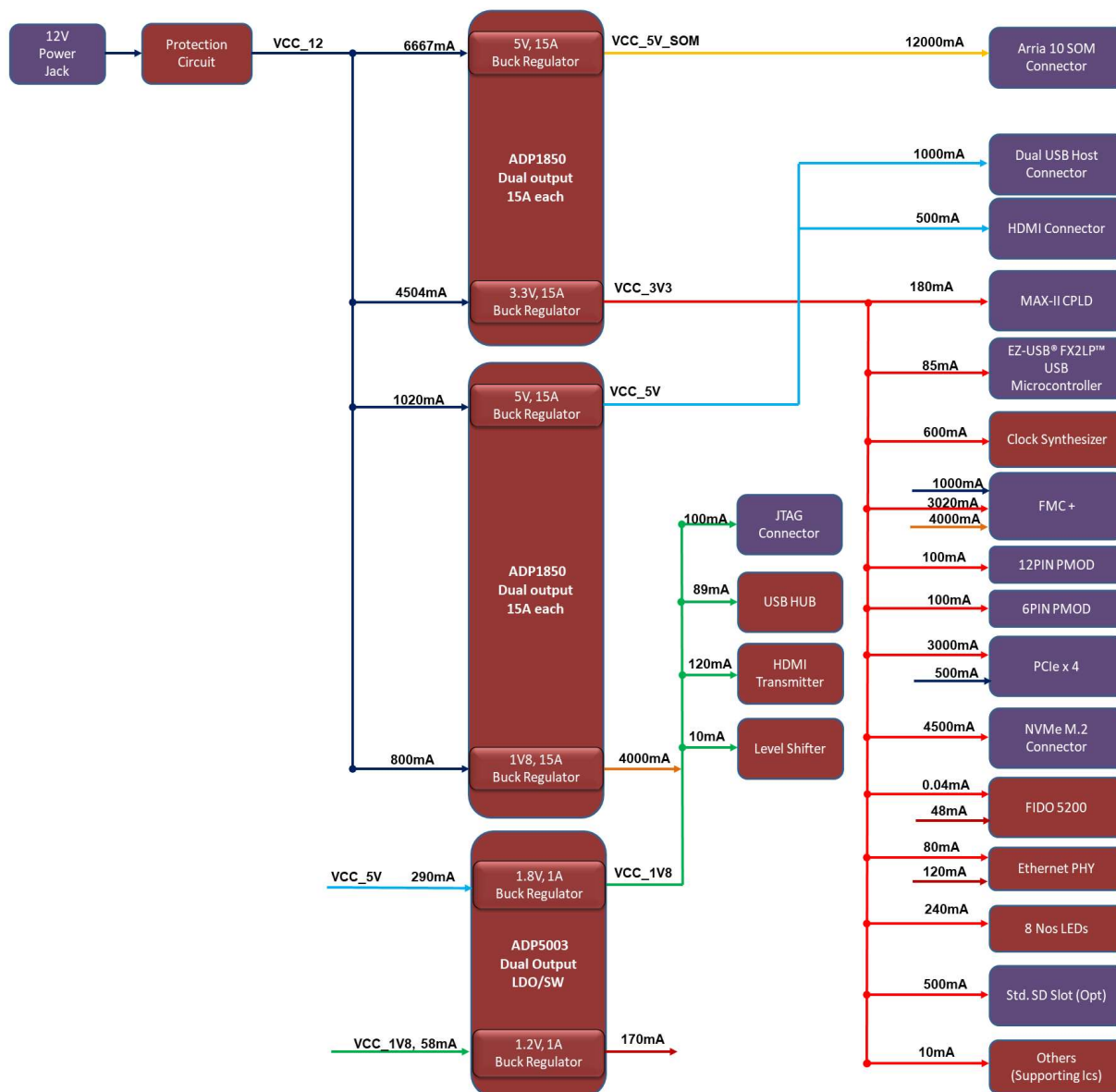
- 01: INDEX & BLOCK DIAGRAM
- 02: POWER TREE & POWER SEQUENCE
- 03: POWER IN, REGULATORS
- 04: BOARD TO BOARD CONN
- 05: UART TO USB,SD,ETHERNET
- 06: CLOCK SYNTHESIZER
- 07: HDMI TRANSMITTER
- 08: PCIe4,M2 KEYM CON,PMOD,I2C
- 09: USB HUB2.0, USB CONN
- 10: FMC PLUS POWER CONTROL
- 11: FMC PLUS CONNECTOR, JTAG
- 12:MAX10-USB BLASTER-II
- 13:LED,PUSH BUTTON,SLIDE SWITCH
- 14: REVISION HISTORY

Custom Carrier Board Arria10 SOM

Title INDEX & BLOCK DIAGRAM

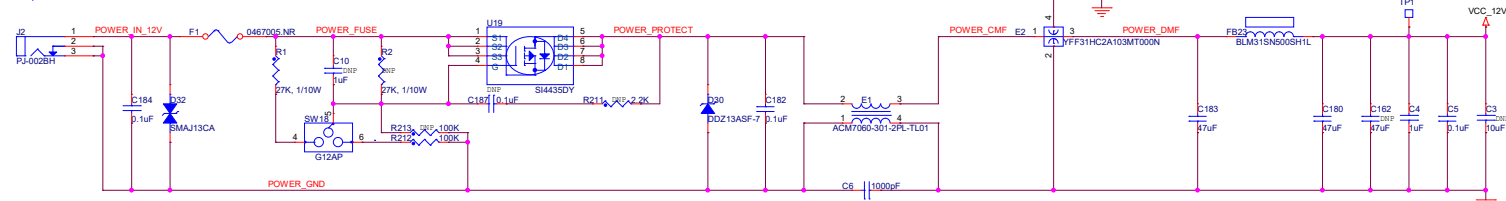
Size	Document Number	Rev
Custom	IW-PRFXR-CS-01-R1.0	0.13
Date:	Thursday, January 31, 2019	Sheet 1 of 16

Arria10 Carrier Board Power Tree Diagram

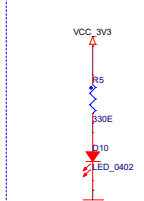


Power Sequence Table			
REGULATORS	VOLTAGE	REMARK	BOOT TIMING
VCC_12V	12V	Board Main Power Input	Always ON
VCC_5V_SOM	5V	SOM Main Power Input	
VCC_5V	5V	Carrier Board Interfaces	
VCC_3V3	3.3V	Carrier Board Interfaces	
VCC_FMC_ADJ	1.8V/3.3V	FMC+ I/O	
VCC_1V8	1.8V	HDMI Trasmitter, Level Shifter	
VCC_1V2	1.2V	FIDO, Ethernet PHY	

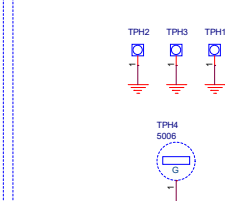
12V,5A Power IN



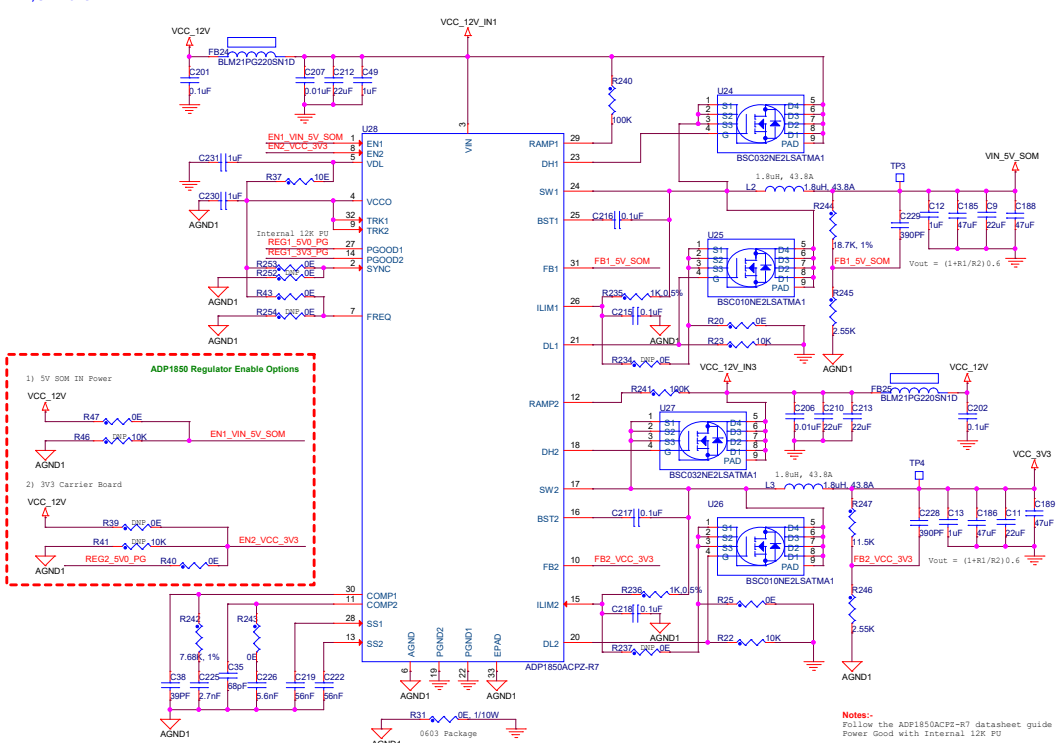
POWER STATUS LED



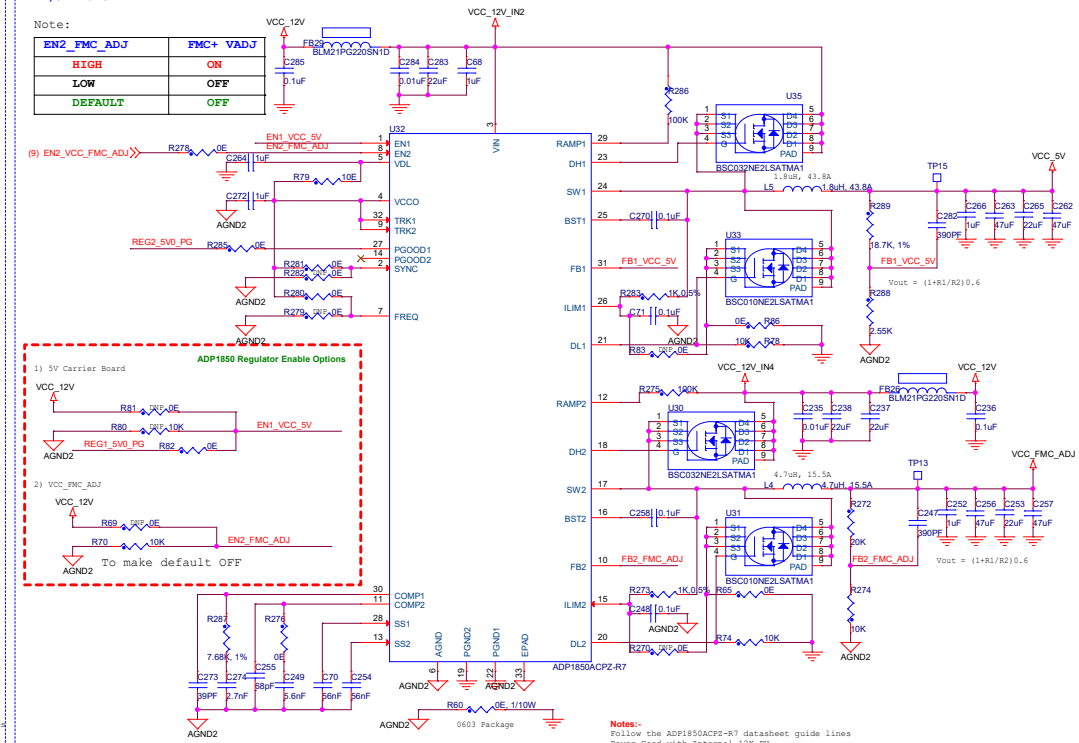
GND Test Points



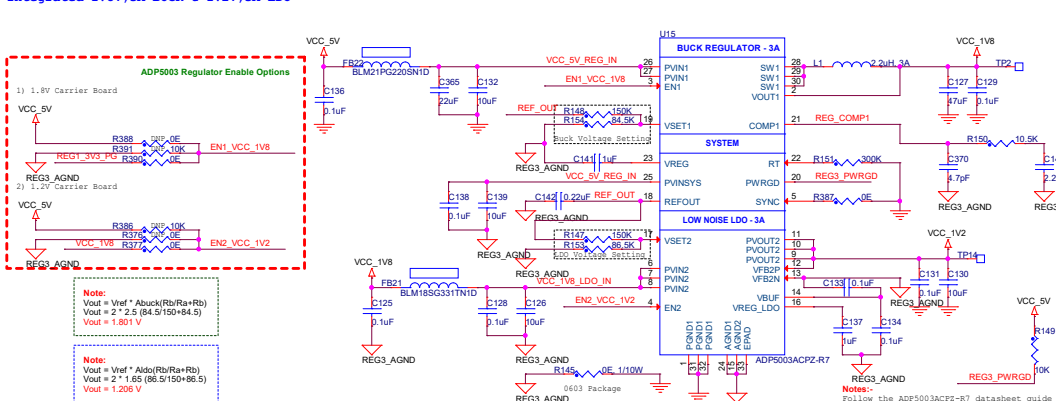
12V,5A Power IN



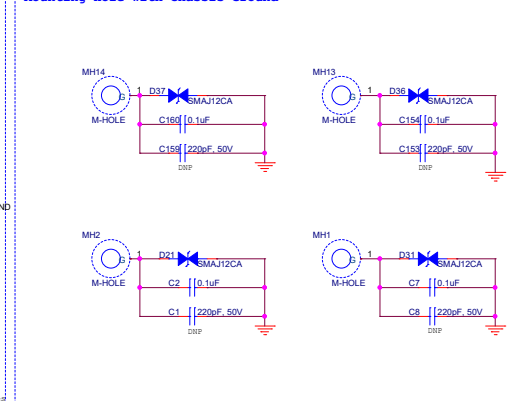
12V,5A Power IN



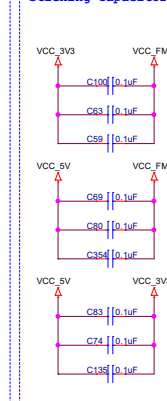
Integrated 1.8V,3A BUCK & 1.2V,3A LDO



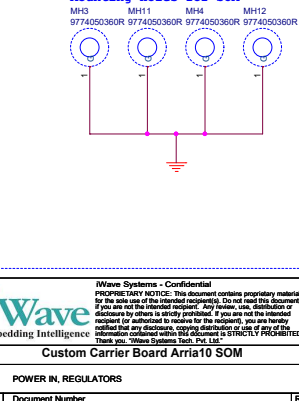
Mounting Hole with Chassis Ground



Stitching Capacitors



Mounting Holes for SOM



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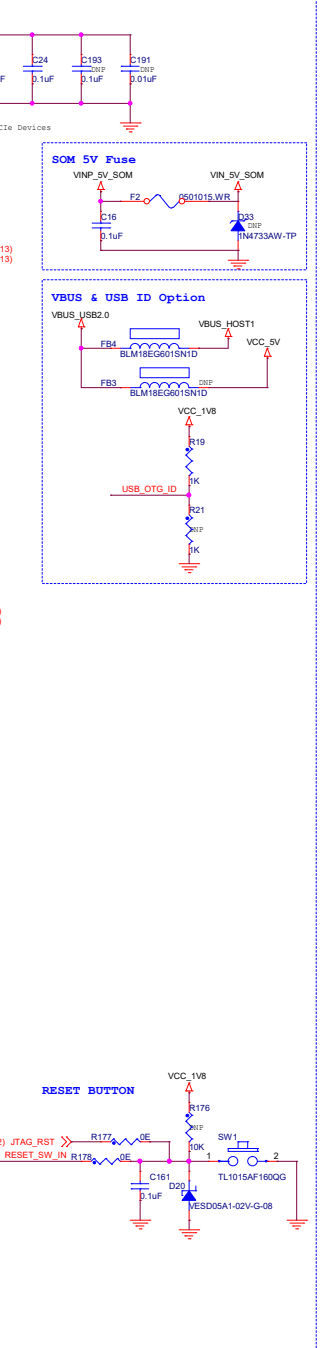
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Custom Carrier Board Arria10 SOM

Size	Document Number	Rev
Custom	IW-PRPKR-CS-01-R1.0	0.13

File: POWER IN, REGULATORS

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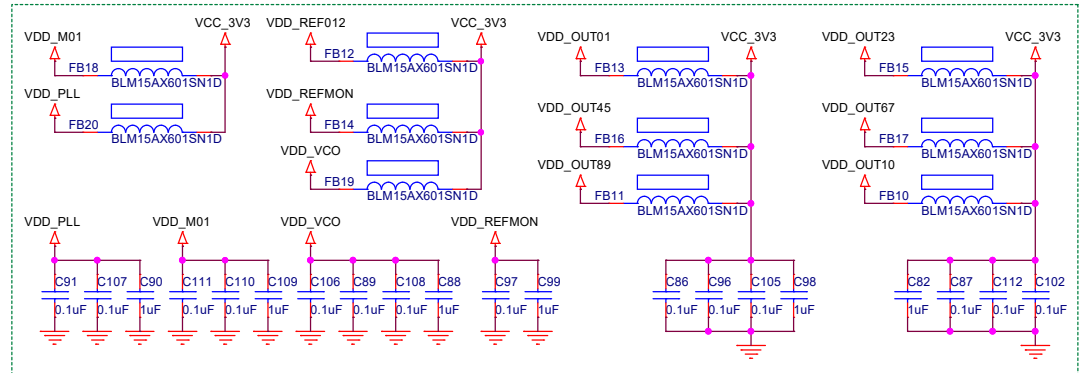
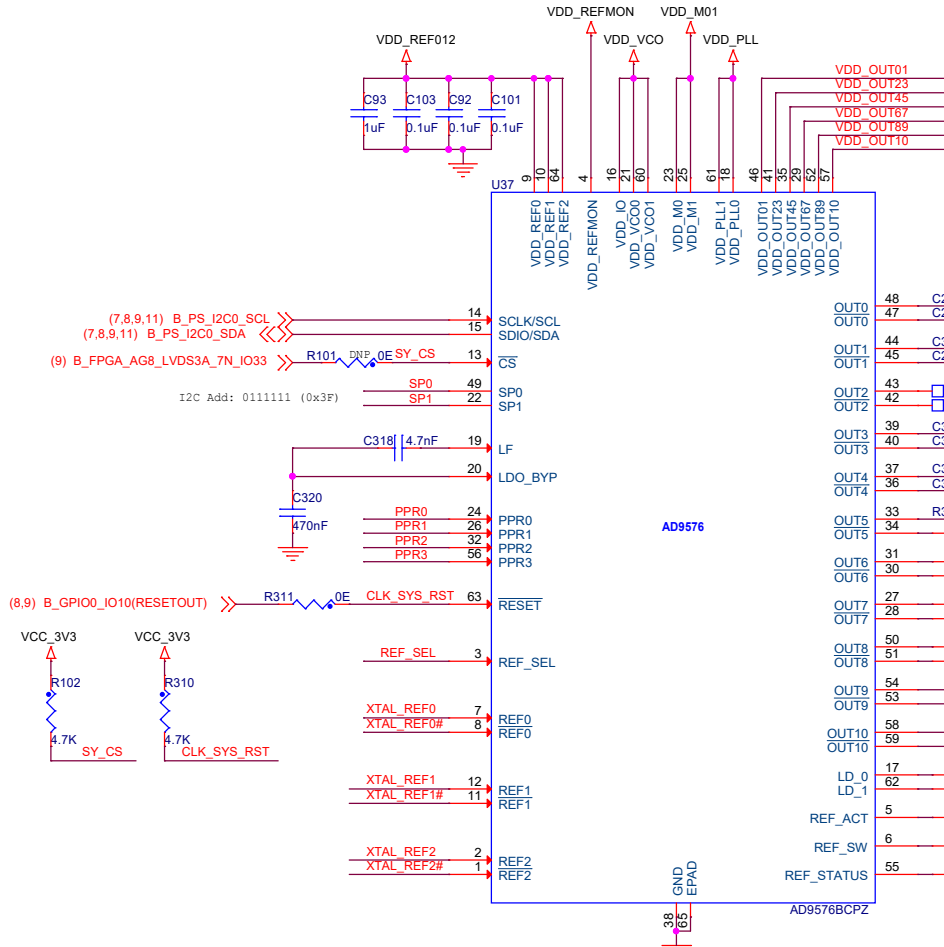


(5) DBUG_UART_RX (4) → R9 → OE → HPS_UART0_RX (4)
 (5) DBUG_UART_TX (4) → R10 → OE → HPS_UART0_TX (4)
 (5) DBUG_UART_RX (4) → R11 → OE → HPS_UART1_RX/EMAC2_MDC (4)
 (5) DBUG_UART_TX (4) → R8 → OE → HPS_UART1_TX/EMAC2_MDIO (4)

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	Thank you, "iWave Systems Pte. Ltd."			
	Custom Carrier Board Arria10 SOM			
Title BOARD TO BOARD CONN				
Size	Document Number			Rev
Customer	HW-PPRFR-JCS-01-R1.0			0.13
Date:	Thursday, January 01, 2010	ISheet	A of	16

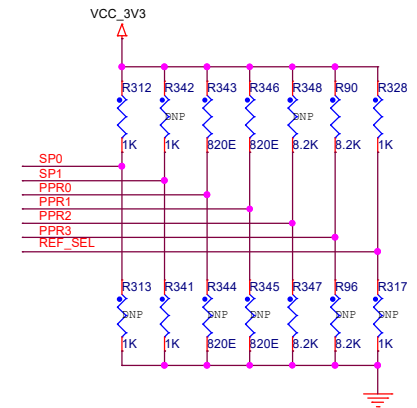
The schematic diagram illustrates the debug UART to USB conversion circuit. It features two main integrated circuits: the APB3025ESGC-F01 (U1) and the USB to UART module (U2). The APB3025ESGC-F01 module is configured with VCC_1V8, VCC_3V3, and VCCIO_DBG_OUT. It has four pins for debug UART RX and TX, and two pins for debug UART TX and RX. The USB to UART module (U2) is configured with VCCIO_DBG_OUT, VCCIO_DBG_5V, and V_DBG_5V. It has four pins for USB DM, DP, ID, and GND. The circuit is powered by VCC_1V8, VCC_3V3, VCCIO_DBG_OUT, VCCIO_DBG_5V, and V_DBG_5V. The USB connector J3 provides the USB interface. Key components include resistors (R217, R218, R215, R216, R3, R4, R17, R221), capacitors (C196, C197, C19, C205, C23, C20, C211, C18, C17, C14), and LEDs (D9, D11, D12).

CLOCK SYNTHESIZER

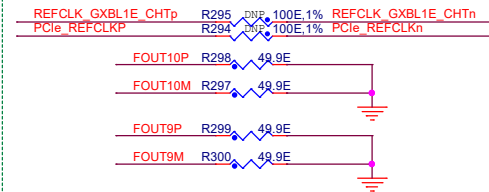


Clock Synthesizer Configuration

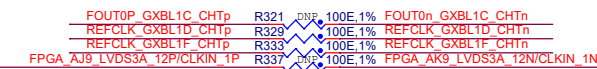
PIN NAME	SETTINGS
SP0, SP1	1, 0 (I2C as Serial Port)
PPR0	State = 4 (820E tied to VDD)
PPR1	State = 4 (820E tied to VDD)
PPR2	State = 3 (8.2K tied to GND)
PPR3	State = 7 (8.2K tied to VDD)




LVDS & HCSL Termination



LVDS Termination



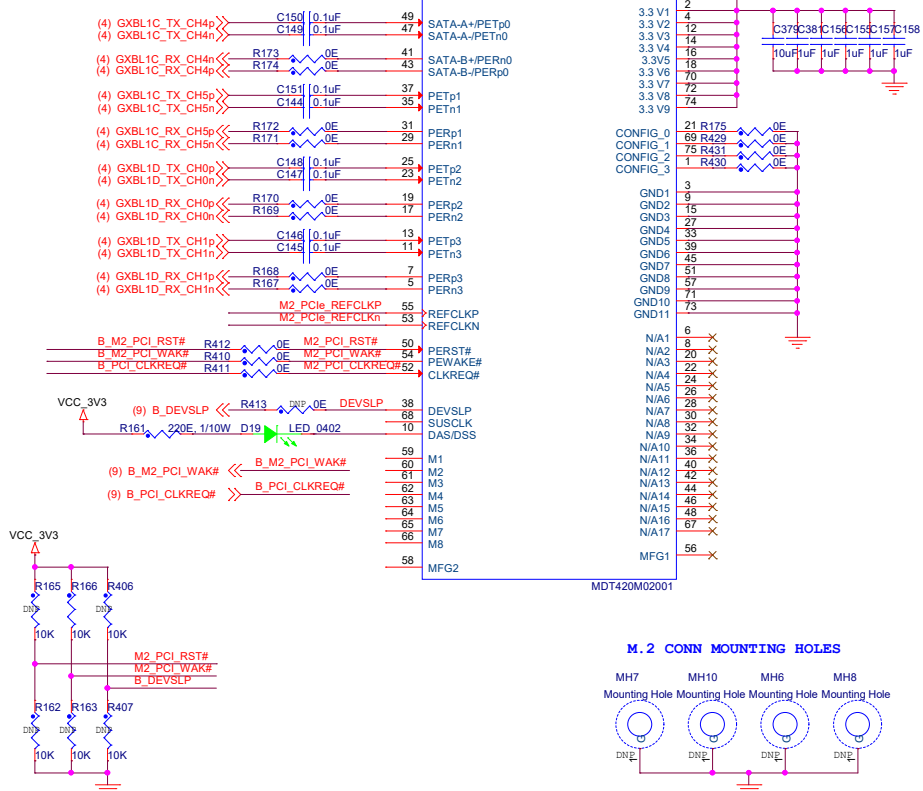


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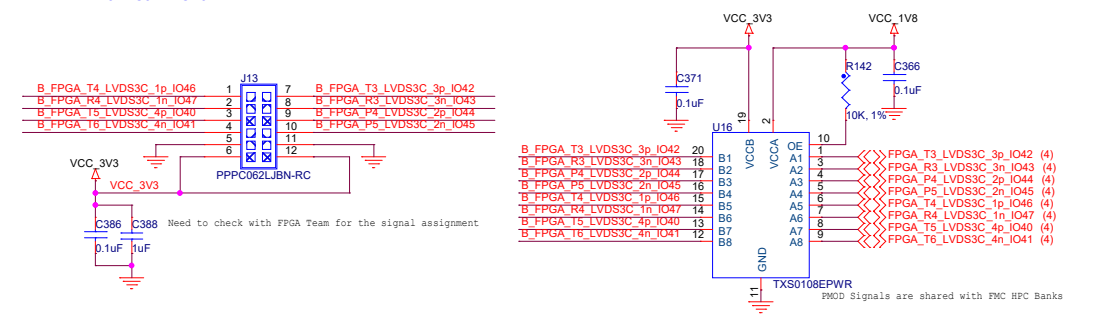
Custom Carrier Board Arria10 SOM

Title	CLOCK SYNTHESIZER	
Size	Document Number	Rev
Custom	miW-PRFXR-CS-01-R1.0	0.13
Date:	Thursday, January 31, 2019	Sheet 6 of 16

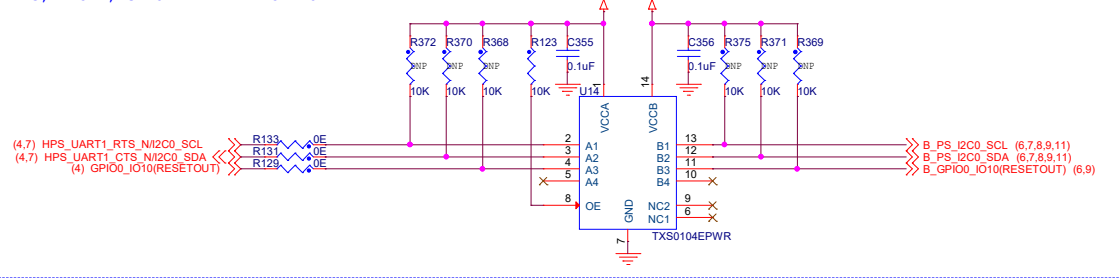
M2-PCI CONNECTOR



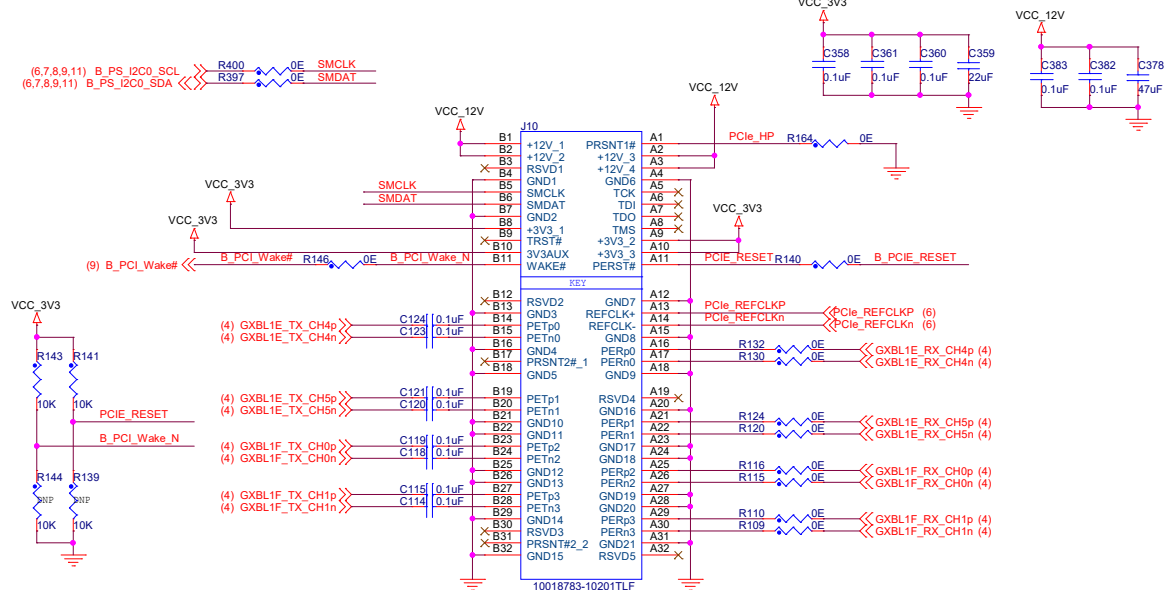
12 PIN PMOD CONNECTOR



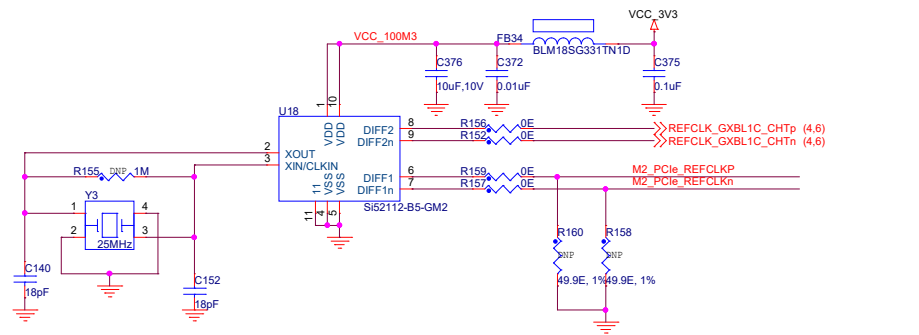
I2C, RESET, GPIO LEVEL TRANSLATOR



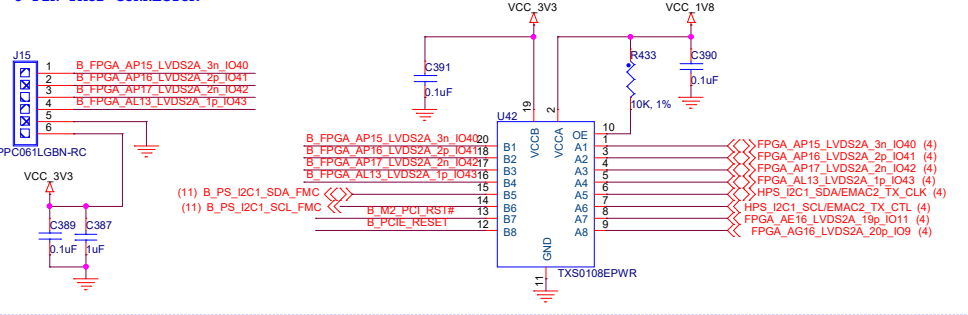
PCIe x4 CONNECTOR



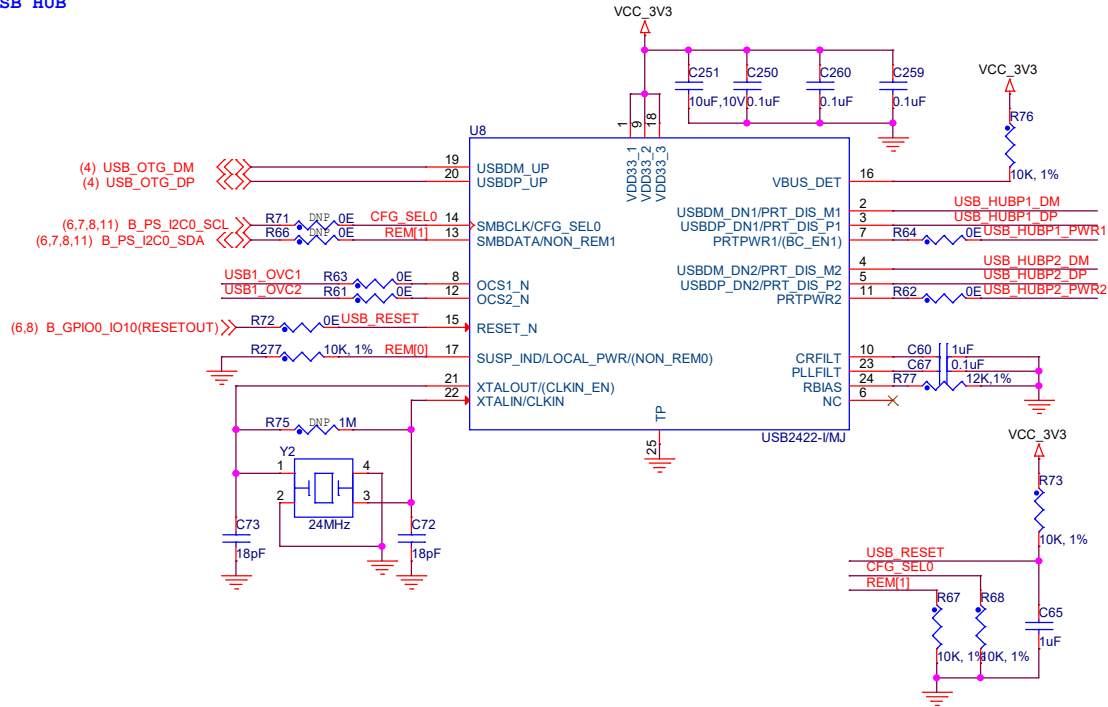
Clock Source for M.2



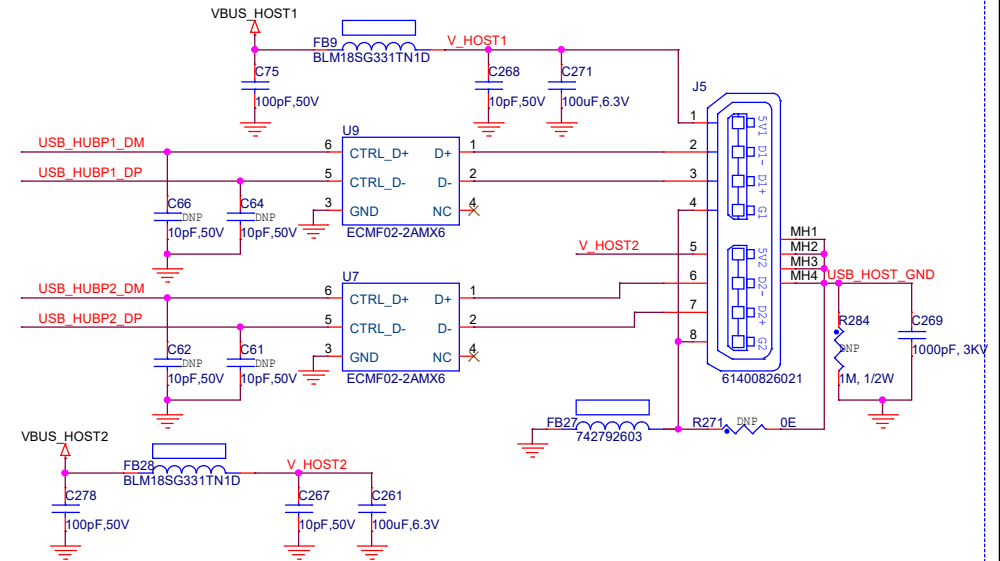
6 PIN PMOD CONNECTOR



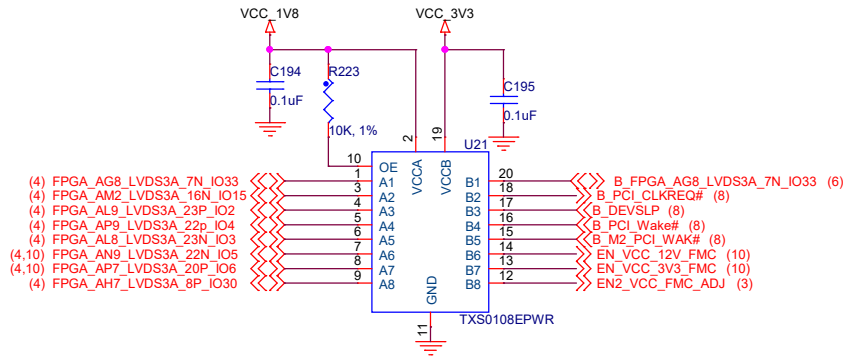
USB HUB



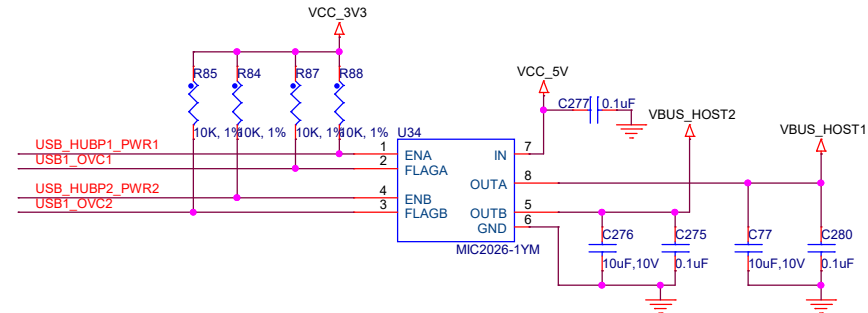
USB 2.0 HOST CONNECTOR



Level Shifter



USB HOST POWER CONTROL



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Custom Carrier Board Arria10 SOM


Title: USB HUB, USB CONN

Size: Document Number: IW-PRFXR-CS-01-R1.0 Rev: 0.13

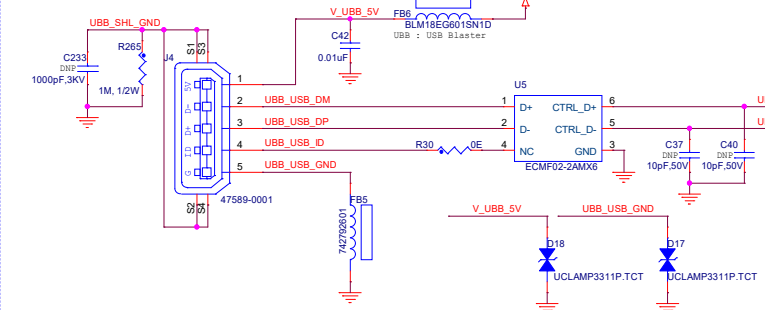
Date: Thursday, January 31, 2019 Sheet: 9 of 16

Figure 10: Custom Carrier Board Arisio10 SOM. The figure contains several circuit diagrams and a table. The diagrams show power supply connections for VDD_1T8G, VDD_3V3, VDD_1V8, VDD_FMC_ADJ, VDD_FMC_1V8, and VDD_3V3_FMC. They include components like resistors, capacitors, and jumpers. A table titled '12 FMC PLUS CONNECTOR_1T8G' lists GAL, GA0, and EEPROM I2C Address values. A note mentions 'FPGA AD17_LVDS0A_24V_1019' and 'FPGA AD17_LVDS0A_24V_1019'.

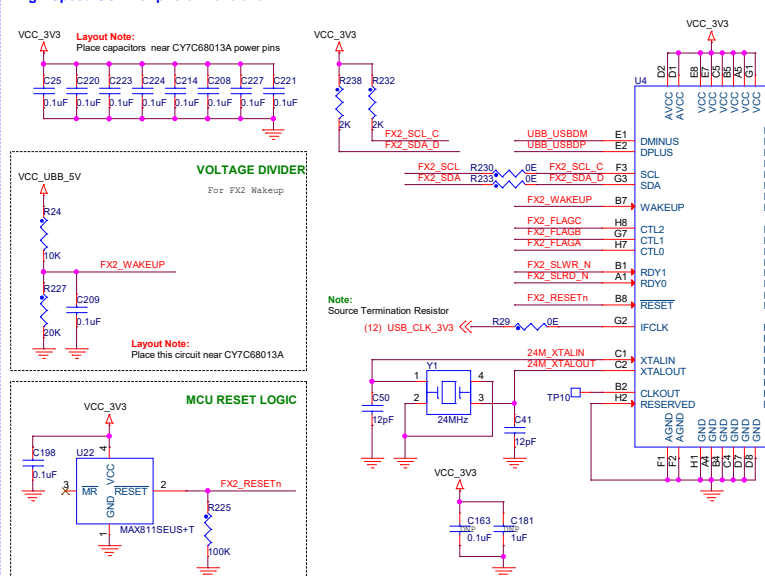
GAL	GA0	EEPROM I2C Address
0	0	0b101 0000
0	1	0b101 0001
1	0	0b101 0010
1	1	0b101 0011

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<p align="center">Custom Carrier Board Attach SOM</p>			
<p>Title 12: FMC PLUS CONNECTOR_ITTAG</p>			
Date	Document Number	Revised	Rev
04/06	HW-PRFR-CB-01-R1.0	1.1	0.13

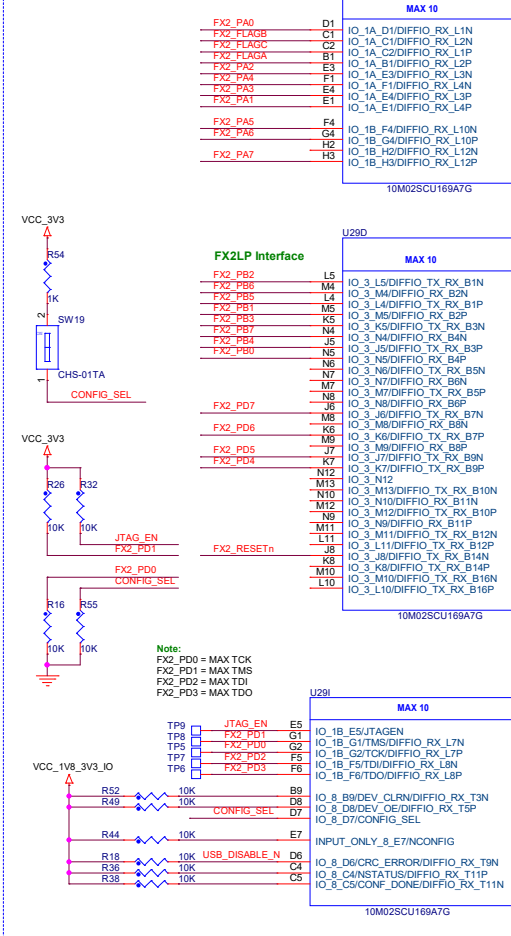
MAX 10 BASED USB BLASTER II



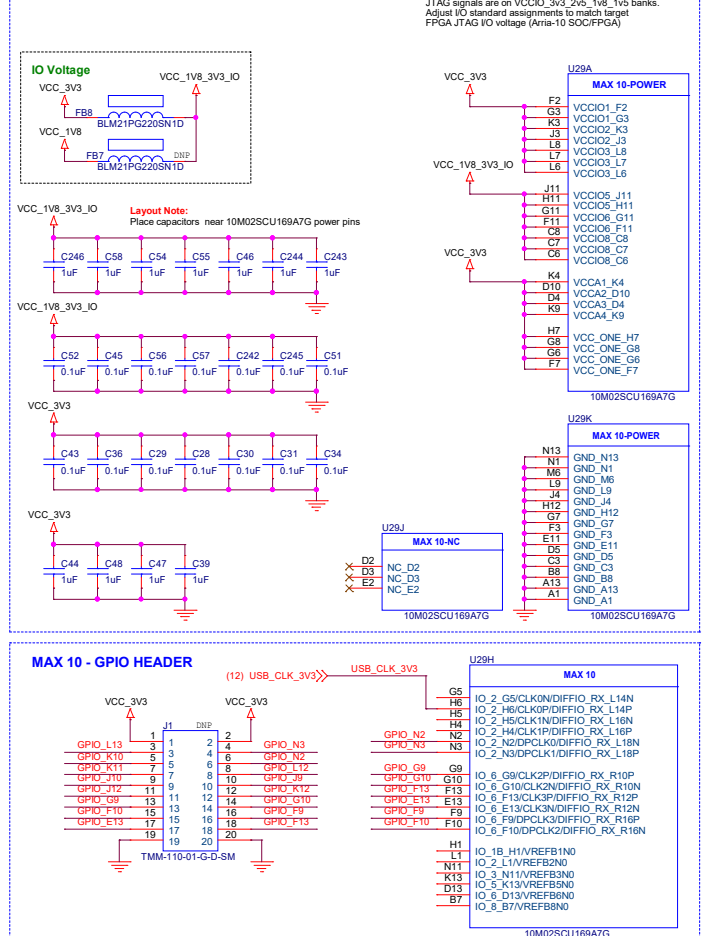
High-Speed USB Peripheral Controller



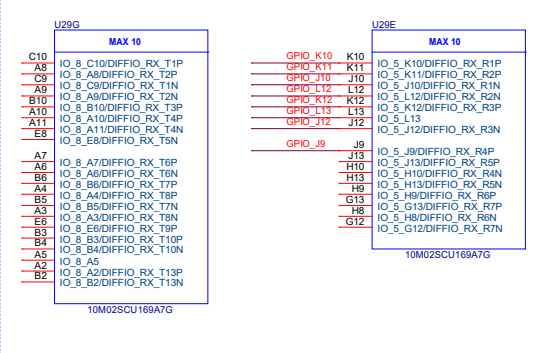
MAX 10 - FX2 Interface



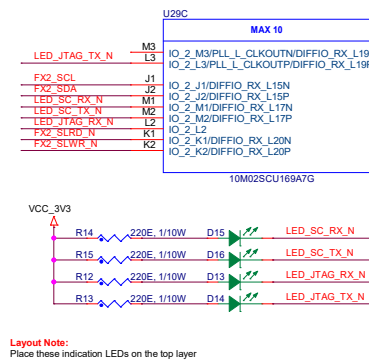
MAX 10 - POWER



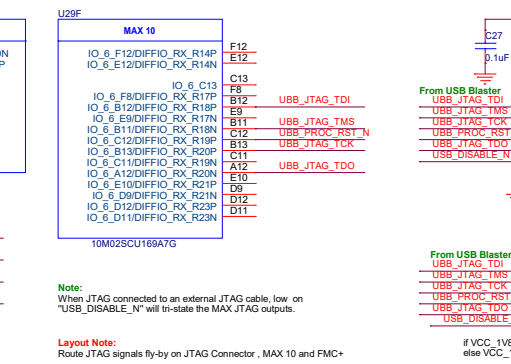
MAX 10 - GPIO



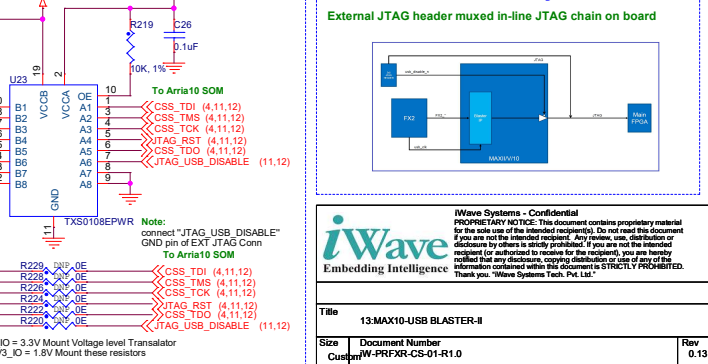
JTAG INTERFACE



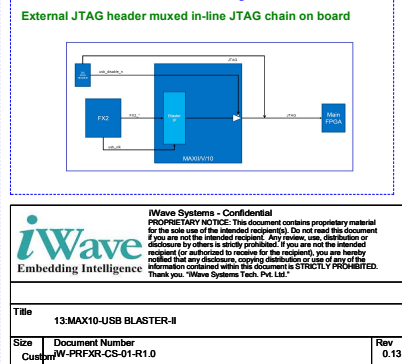
MAX 10 - JTAG Interface



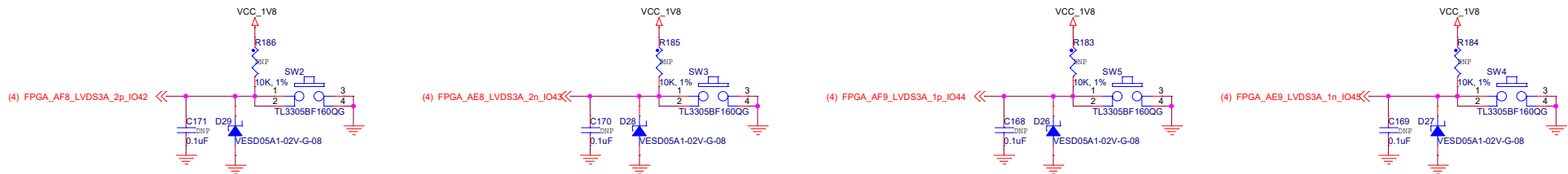
MAX 10 - GPIO HEADER



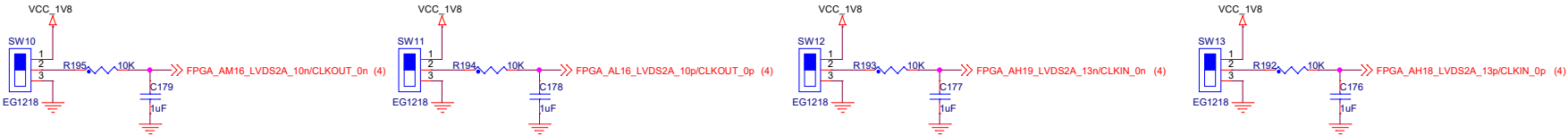
USB BLASTER II - Block Diagram



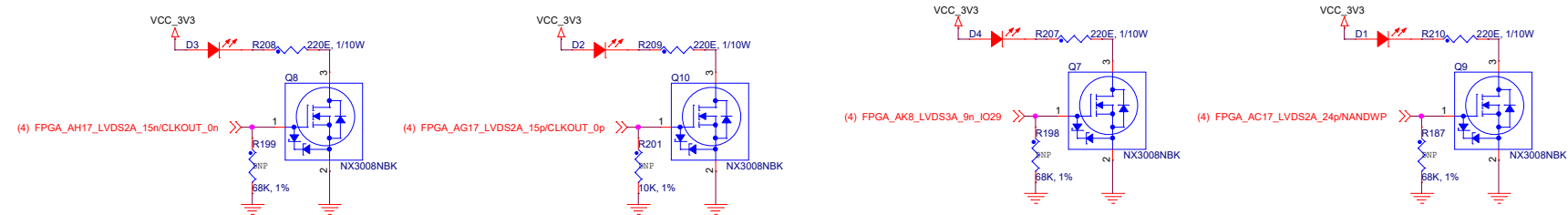
FPGA Push Button



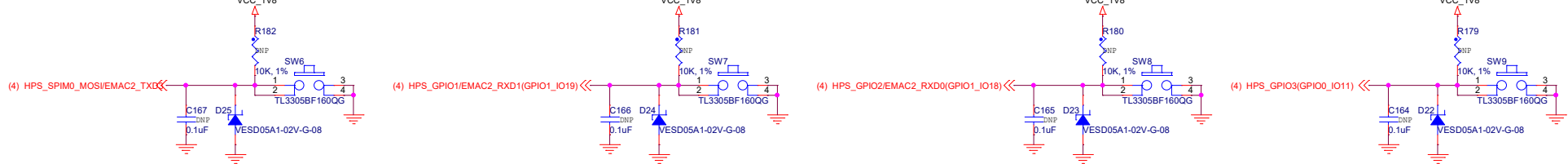
FPGA Slide Switch



FPGA LEDs



HPS Push Button

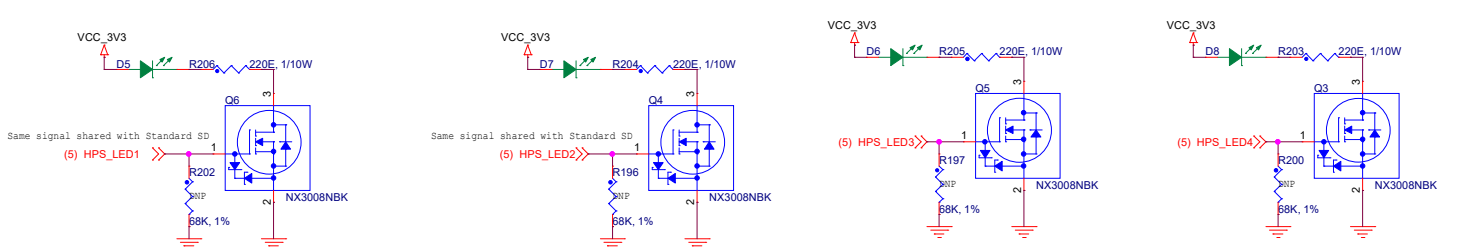


HPS Slide Switch



SD signals shared with HSP Slide Switch


HPS LEDs



iWave Embedding Intelligence Custom Carrier Board for Arria 10 SOM		
Title 14:LED,PUSH BUTTON,SLIDE SWITCH		
Size Document Number CustomW-PRFXR-CS-01-R1.0		
Date Thursday, January 31, 2019		
Sheet 13 of 16		
Rev 0.13		

5	4	3	2	1	
Rev.No	Details of changes with reason	Done by	Done date	Approved by	Approved date
0.12	* Gerber Relased Schematic	Mr.Azlum	14-Jan-2019	Mr.Immanuel	14-Jan-2019
0.13	* Alternate parts updated GRM1555C1H680JZ01D Changed to 04025A680JAT2A 0402YA390JAT4A Changed to 04023A390JAT2A C0402C563K4RACTU Changed to CL05B563K05NNNC CGJ2B2X7R1C472K050BA Changed to CGJ2B2X7R1E472K050BA GRM155R61A474KE15D Changed to CC0402KRX5R6BB474 FA-12824.0000MB-W Changed to FA-128 24.0000MF10Z-W3	Mr.Azlum	31-Jan-2019	Mr.Immanuel	31-Jan-2019

Note: Add PCB details and heat Spreader details while generating BOM.



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Custom Carrier Board Arria10 SOM

Title

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