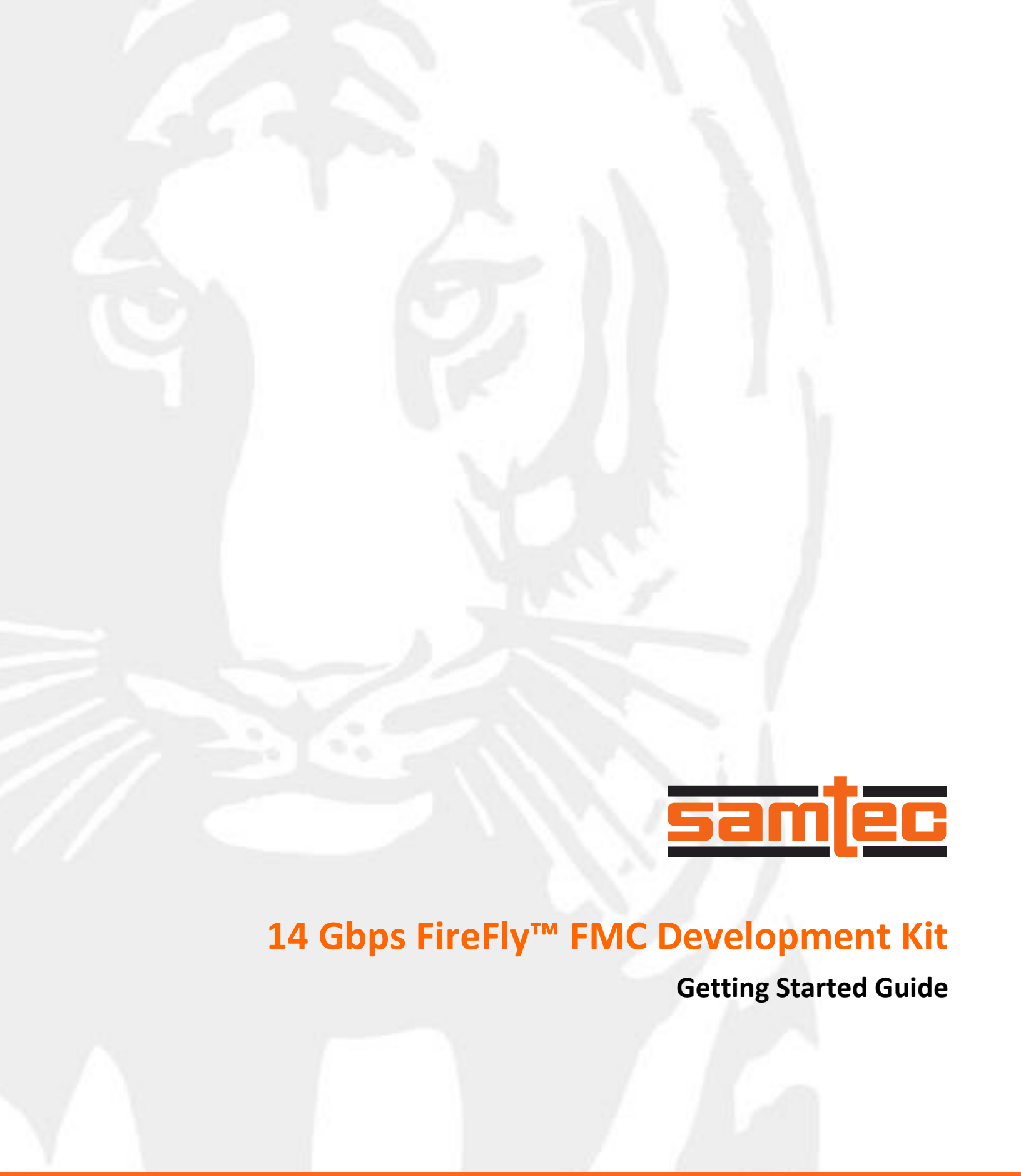

# 14 Gbps FireFly™ FMC Development Kit

## Getting Started Guide

DECEMBER **2017**

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## Updated Documentation

Please visit www.samtec.com/standards/fmc to get access to the latest FMC documentation and resources.

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# Revision History

| Revision # | Reason | Author | Date |
|---|---|---|---|
| **Release 00** | Initial Release | Dylan Lang/Matt Burns | 05/26/2017 |
| **Release 01** | Updated Figures 16 & 20, Added Section 6 | Matt Burns | 10/9/2017 |
| **Release 02** | Updated Figure 18 | Matt Burns | 12/5/2017 |
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# 1 Introduction

In an effort to help speed up time-to-revenue solutions over a wide variety of applications, many developers have implemented Field Programmable Gate Arrays (FPGA) in their designs. These boards offer a flexible and versatile approach in testing and designing electrical systems. Companies such as Xilinx, Intel Altera and Microsemi feature some of the industry's most comprehensive offerings in FPGA and Design Services.

Samtec, in accordance with VITA 57.1 and VITA 57.4, offers FMC (FPGA Mezzanine Card) solutions as an expansion to the traditional FPGA architecture.

The FMC+ and FMC connectors are Application Specific Product (ASP) versions of Samtec's SEARAY™ High-Speed Array system. These FMC connectors are available direct from Samtec and are scalable to high-performance applications as the user's hardware development efforts demand.

Through implementing the added FMC card equipped with Samtec FireFly™ (14G×12), one is able to test, model, troubleshoot, and demonstrate clear 14 Gbps optical connections over 8 SERDES lanes.

This Getting Started Guide is intended to show how to setup one of our supported FPGA boards, the Xilinx® KCU105, as well as achieve the desired results of a clean, rapid signal over optical cables using Xilinx® provided FPGA software, Vivado®.

In addition, this guide will also consider various solutions to potential problems as well as additional diagnostics that can be run through Tera Term to isolate and resolve issues. Throughout the guide, proper installation and programming of the FPGA will be shown in a step by step format with accompanying graphics.

**Note:** This guide can be used with a variety of different FPGAs, not just the KCU105.

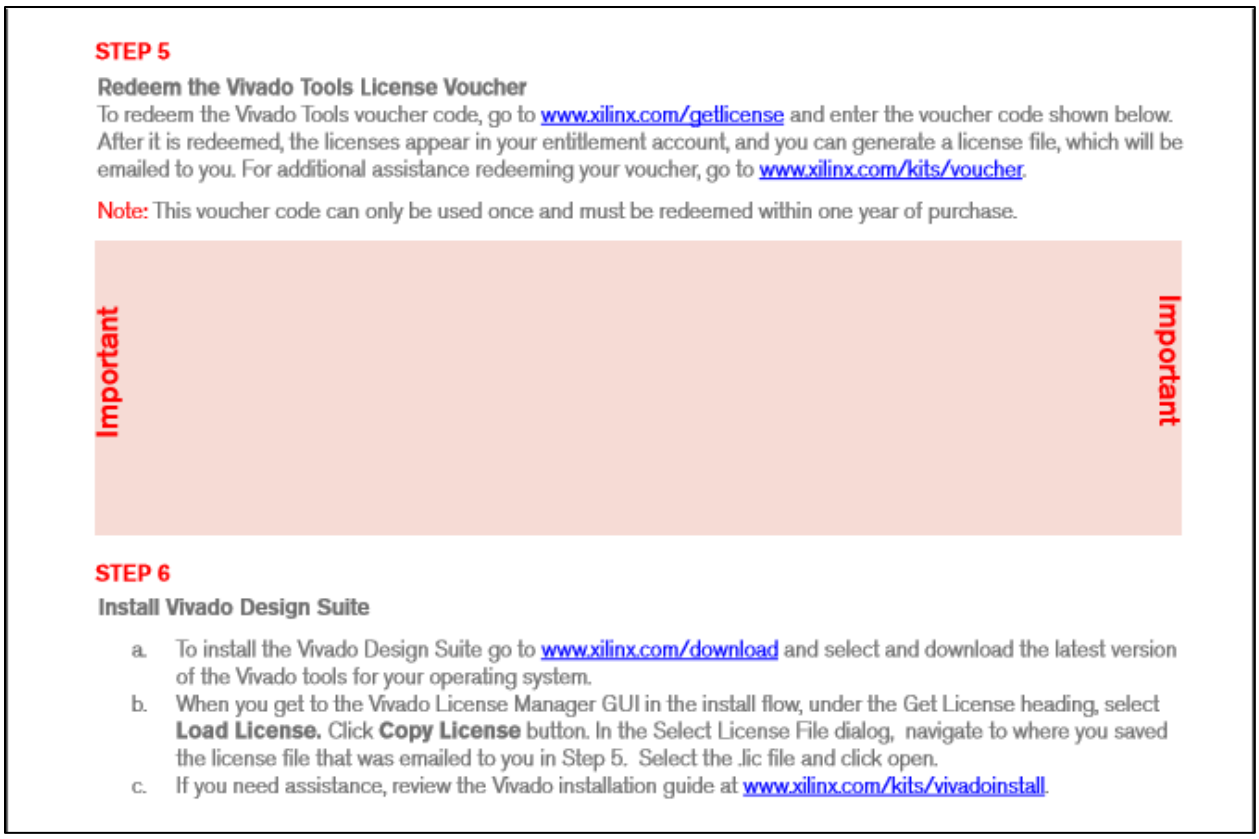
# 2 Getting Started

## 2.1 *Register with Xilinx*

Before you can gain access to the necessary software, you must register the FPGA with Xilinx®. To begin, locate the included KCU105 Quick Start Guide in the box and follow steps 5 and 6 regarding as how to properly register the board and gain access to Vivado®.

**Note:** Code will be indicated inside the box below on the back page of the included guide.

**Note 2:** Due to the nature of the FPGA & FMC, download **version 2015.4** of Vivado® for best results.



**STEP 5**

**Redeem the Vivado Tools License Voucher**

To redeem the Vivado Tools voucher code, go to www.xilinx.com/getlicense and enter the voucher code shown below. After it is redeemed, the licenses appear in your entitlement account, and you can generate a license file, which will be emailed to you. For additional assistance redeeming your voucher, go to www.xilinx.com/kits/voucher.

Note: This voucher code can only be used once and must be redeemed within one year of purchase.

Important

Important

**STEP 6**

**Install Vivado Design Suite**

a. To install the Vivado Design Suite go to www.xilinx.com/download and select and download the latest version of the Vivado tools for your operating system.
b. When you get to the Vivado License Manager GUI in the install flow, under the Get License heading, select **Load License.** Click **Copy License** button. In the Select License File dialog, navigate to where you saved the license file that was emailed to you in Step 5. Select the .lic file and click open.
c. If you need assistance, review the Vivado installation guide at www.xilinx.com/kits/vivadoinstall.

**Figure 1 – KCU105 Quick Start Registration Steps 5, 6**

## 2.2 FPGA Board Prep

Once the FPGA has been successfully registered and Vivado® installed, additional on-board steps must be taken to prep for this specific demonstration. Once all of the components have been unpacked, follow the procedures below as well as download the drivers for the JTAG-USB cables here needed to communicate between the hardware and software.

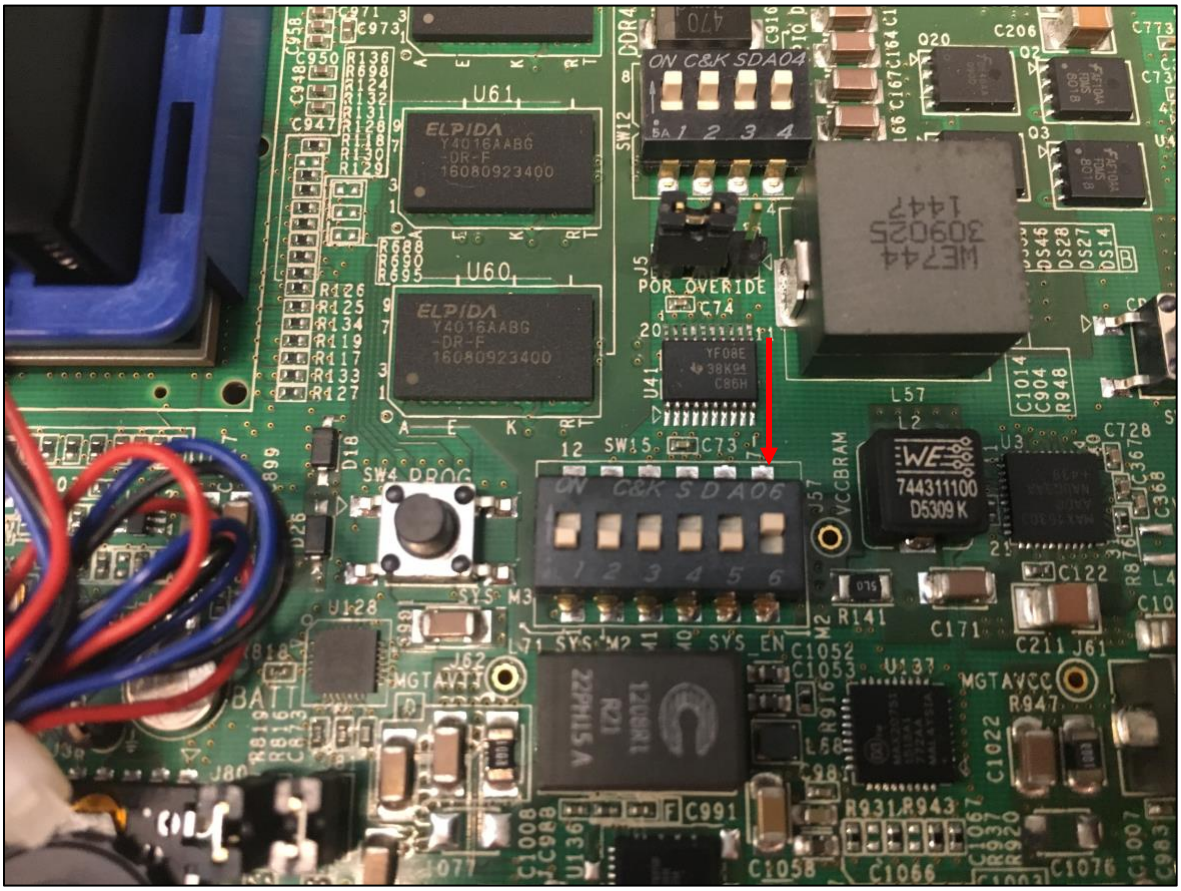



**Figure 2 – DIP Switch SW15 Position 6 Should Be ON**

**Note:** DIP Switches 1-5 should be **OFF**

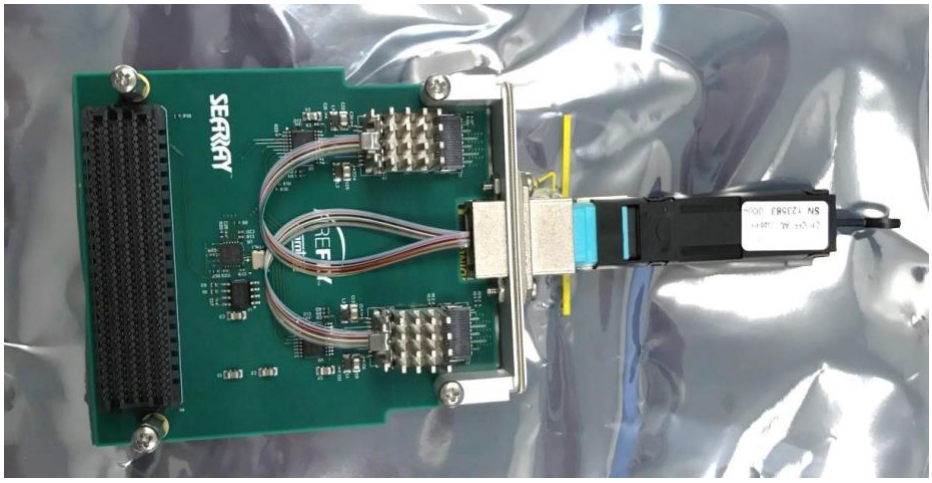



**Figure 3 - Plug Optical Loopback into FMC**

**Note:** Once plugged in, you should hear an audible click from the spring mechanism on the optical loopback module.

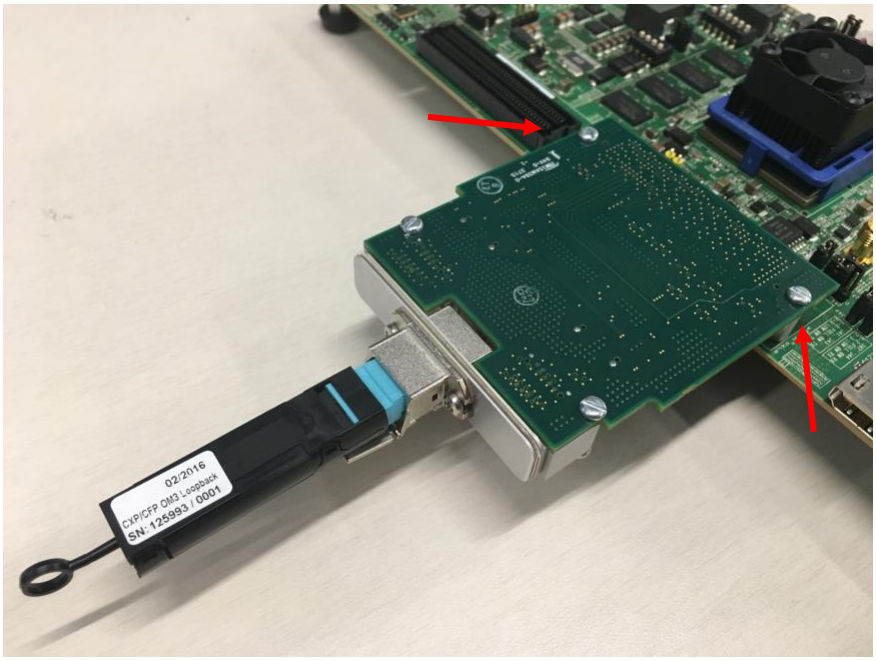



**Figure 4 - Mate Assembly with SEARAY™ using Standoffs**

**Note:** Use included standoffs to carefully mate the FMC to the FPGA to avoid damages. Make sure to mate the assembly to the **connector directly in front of the fan and closest to the HDMI port**.

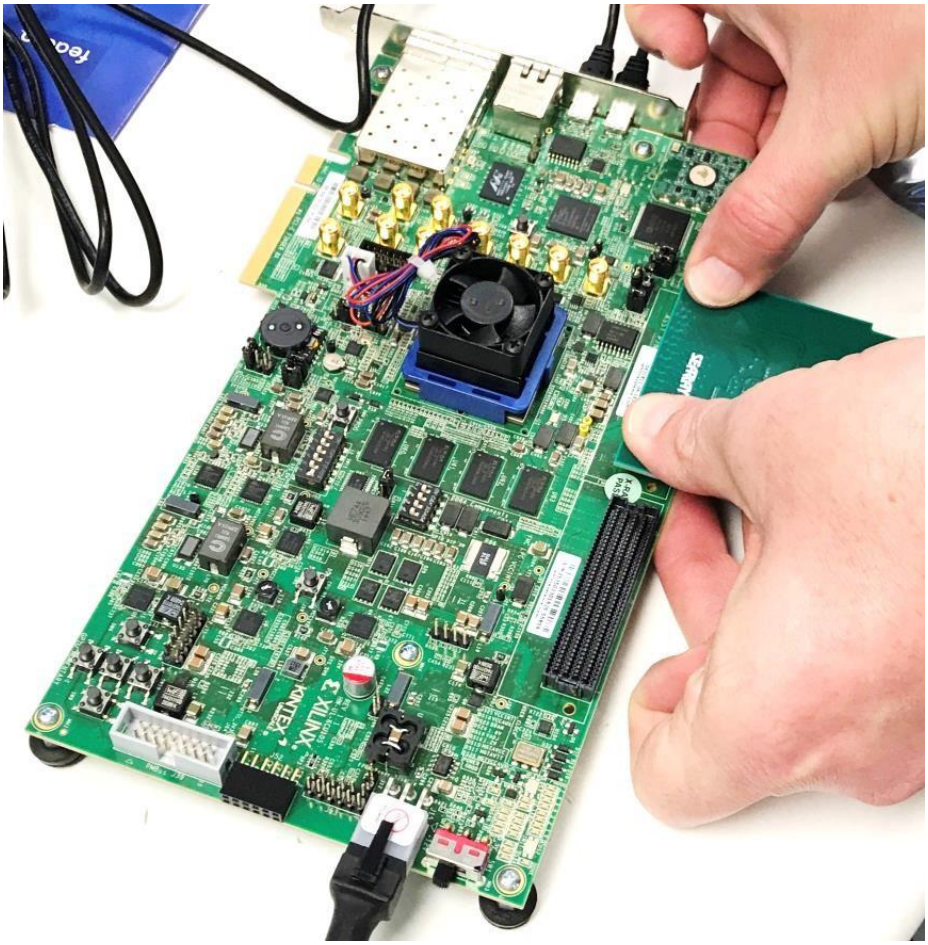


**Figure 5 - Connect JTAG USBs and Power Cables**

**Note:** Under the **Device Manager**, you should notice two new COM ports available once the USB cables are plugged into a PC/laptop and the drivers installed;
**Silicon Laboratories Standard & Enhanced COM**.

**Note 2:** To check the functionality of the FPGA itself, additional details are found under section 5.2 Testing FPGA Functionality with GPIO.

The last step is to power on the KCU105 and begin working in Vivado®.

# 3 Working in Vivado®

Start by opening Vivado® 2015.4, then navigating to the “ofmc_ibert project” under the Open Project tab.

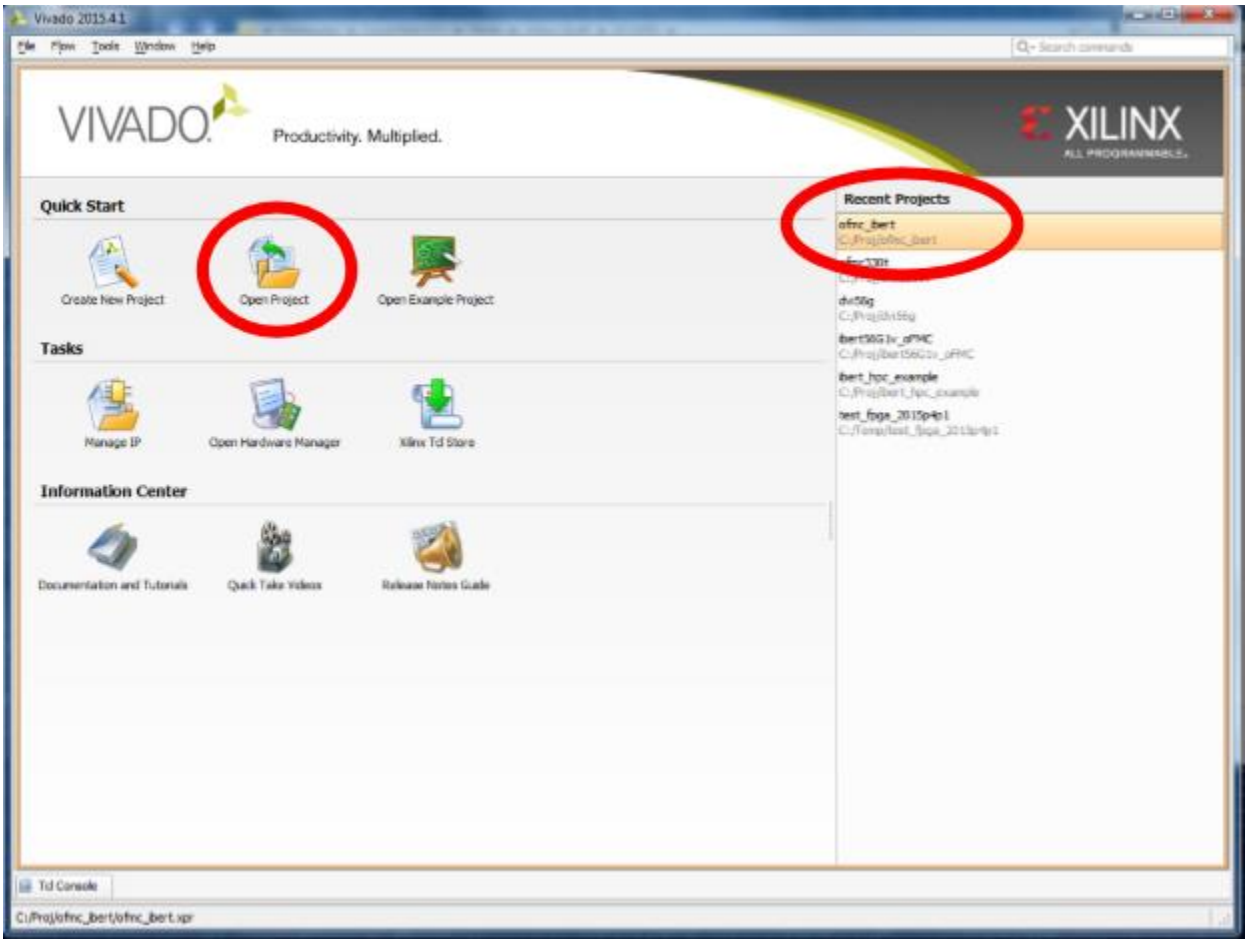



**Figure 6 – Vivado® Quick Start Screen**

## 3.1 *Finding the Target*

The first step in running the optical test is to find the target, in this case, the KCU105 (see **Figure 7** below). Click on "Open Target" then "Auto Connect." Your machine should automatically locate the FPGA and be ready for programming.

**Note:** Notice the statements under the "Design Runs" section of the screen, **synth_design Complete!** and **write_bitstream Complete!** This confirms that the project was successfully loaded into Vivado®.

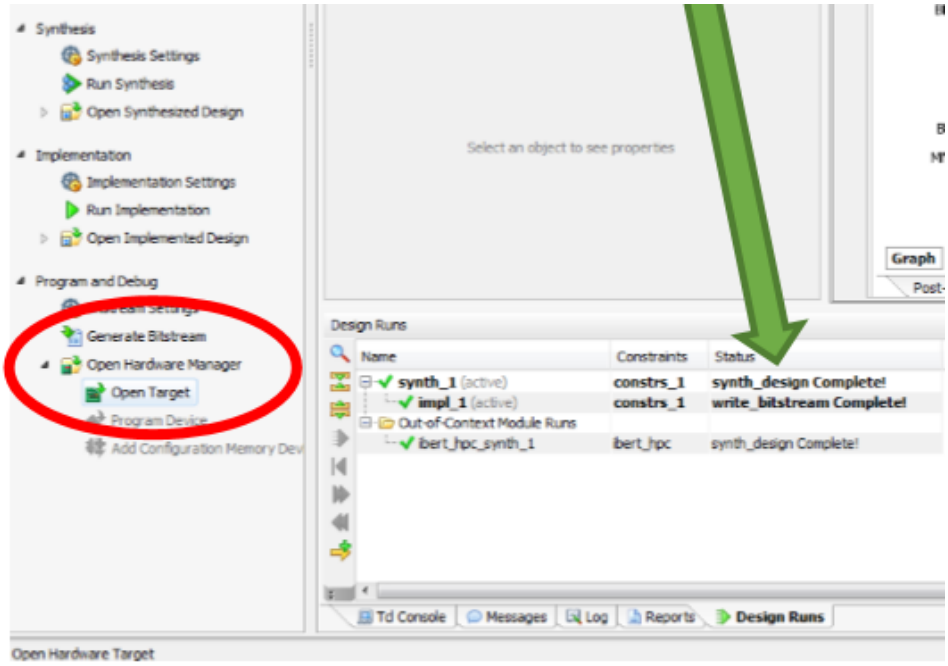



**Figure 7 - Open Target and Successful Program Implementation**

## 3.2 *Programming the FPGA*

Now that Vivado® is able to see the location of the BIT files, these files need to be programmed into the actual board itself. Click **Program Device** directly below "Open Target", select **xcku040_0** FPGA and follow the prompts from the figure below and click "Program."

**Note: DO NOT** change the file paths of either the Bitstream or Debug probe files. This will severely complicate FPGA programming. Vivado® will remember all previously entered information the next time an instance of the program is opened allowing for quicker, more efficient access to the FPGA.

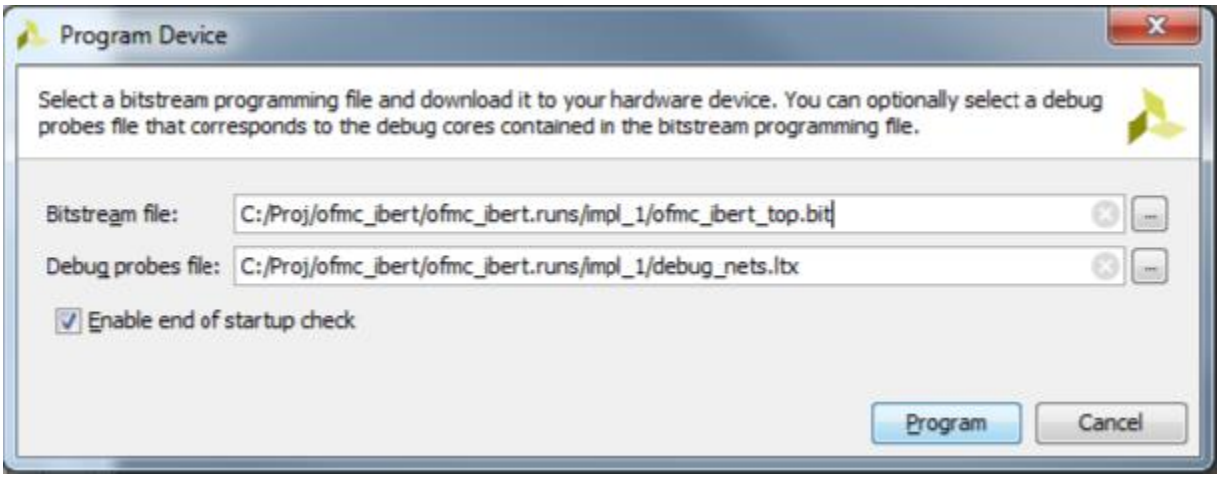



**Figure 8 - Program Device Window**

## 3.3 *Displaying Results*

After the FPGA has been successfully programmed, the board and Vivado® are able to "talk" to each other over the 8 SERDES lanes as shown in the Serial I/O Lanes section of the screen. Results should clearly show the 14 Gbps speeds of the FMC over the dual FireFly™ optical cables. Granted, results may vary from exactly 14.00 Gbps to around 14.02, 14.07 etc. See results in **Figure 9** below.

**Note: If 14 Gbps is not appearing**, due to the extended amount of time to configure both the software and the results, it may be helpful to try the following: To display accurate BER results for each channel, the user should perform a **global reset of the Tx channels**, followed by a **global reset of the Rx channels**. This ensures the Tx and Rx SerDes are properly initialized. Clicking **BERT Reset** will reset and initialize the error counters in the FPGA Rx channels. This resets the error count to zero, and restarts the BER measurement.

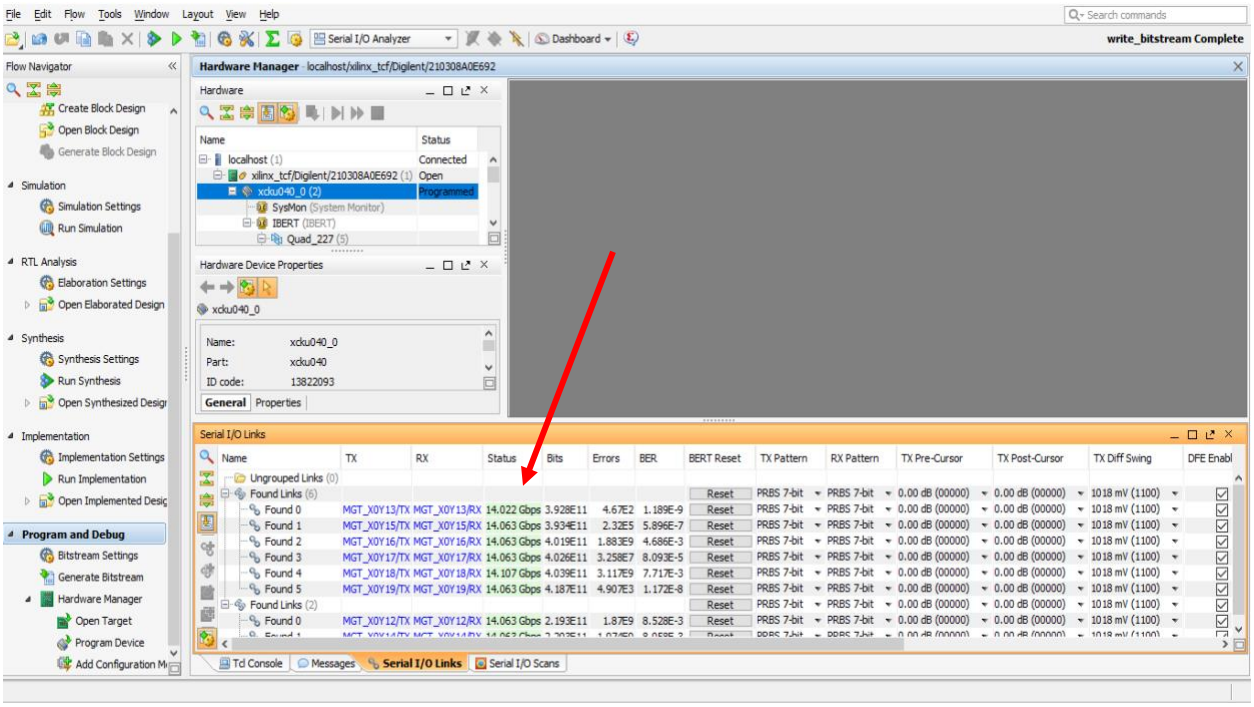



**Figure 9 - SERDES Results Displayed**

# 4 Producing an Eye Scan

At this point, Vivado® has successfully identified, programmed, and displayed the desired BER test results from the FMC Loopback Module. In addition to a BER measurement, it is also helpful to generate an eye scan, as measured at the FPGA Rx SerDes. When evaluating system SI (signal integrity), the goal is to not only establish an error-free link, but to also verify that the received signal has a high degree of voltage and timing margin at the Rx. The eye scan confirms this. An eye scan is generated by sweeping the voltage and timing sampling points in the Rx SerDes, while measuring the BER at each point. The result is a graphical, color graded representation of the BER contour at various sampling points of voltage and time, within the eye. A full, "open" eye indicates a higher degree of available voltage and timing margin at the Rx, whereas a "closed" eye indicates the opposite.

## 4.1 *Create Eye Scan*

To generate an eye scan, select any of the 8 channels of interest and click on **"Create Scan"** near the bottom of the vertical tool ribbon left of the SERDES Lanes. Select the desired options then click OK to generate the scan. The scan may take a few minutes to complete, depending on the user selected settings.

Notice the open eye in the figure below, which shows a wide-eye contour and a high degree of BER margin after the signal completes the round-trip path through OFMC.

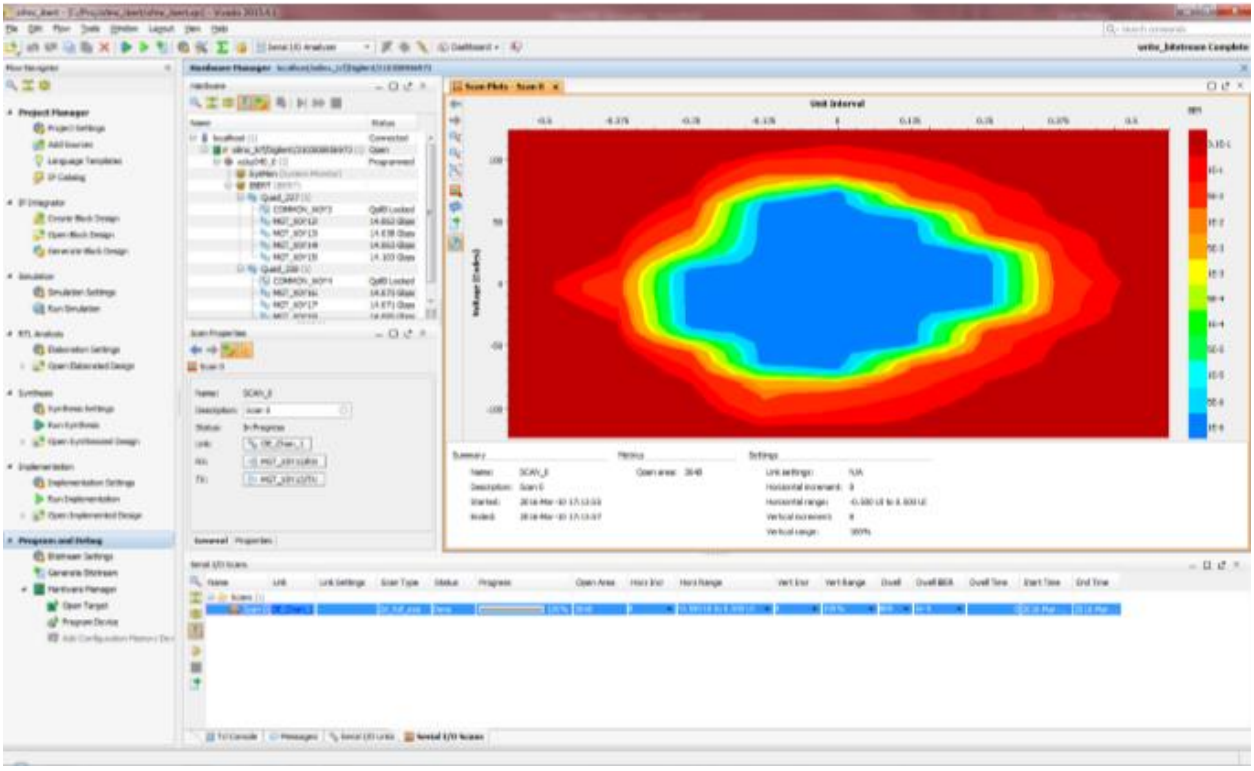


**Figure 10 - Generated Eye Diagram**

**Note:** If channel settings are changed, you will need to re-scan the channel to display the updated eye diagram.

# 5 Additional Resources

Vivado® is an extremely detailed and in-depth piece of software, especially when used in tandem with Xilinx® full line of FPGA solutions. In addition to simply observing the data within the program, this guide also contains various other resources and troubleshooting guidelines that may be helpful when working through this demonstration.

## 5.1 *Using Tera Term to Access OFMC Applications*

Tera Term can be used as an OFMC Control Application to observe, adjust, and display changes of the FMC over FireFly™. The following are a few of the resources you can use within Tera Term to change the optical engine settings.

1. Before accessing the various features of Tera Term, make sure **Vivado® is initialized** with the FPGA as shown above and that the **board is connected and programmed to the PC/Laptop over JTAG USB.**

2. You should notice that on the opening menu screen, it should display both JTAG COM ports as referenced earlier. If you have the option, **select the Standard COM port** and press enter to proceed.

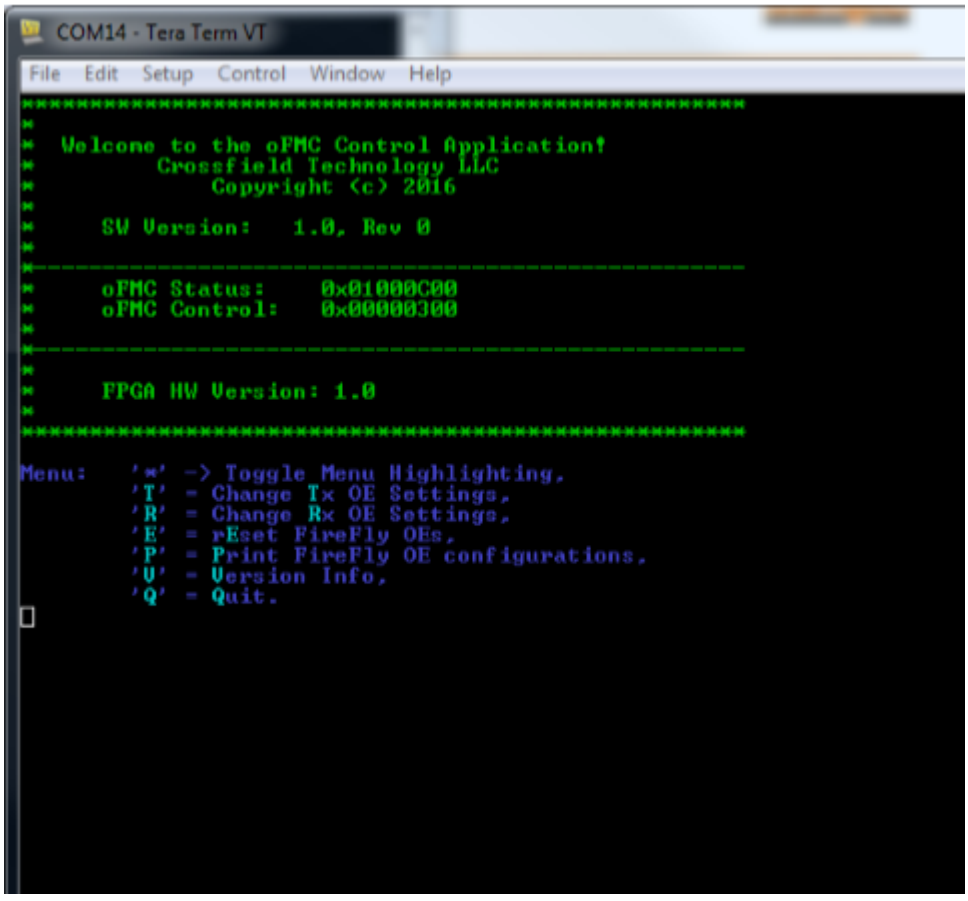



**Figure 11 - Tera Term Opening Menu**

3. Notice the various options in Figure 11; hit any of the designated keys to receive a detailed report or further options on how to edit these features.

4. As an example, try hitting “V” to display the current build as seen below in Figure 12.

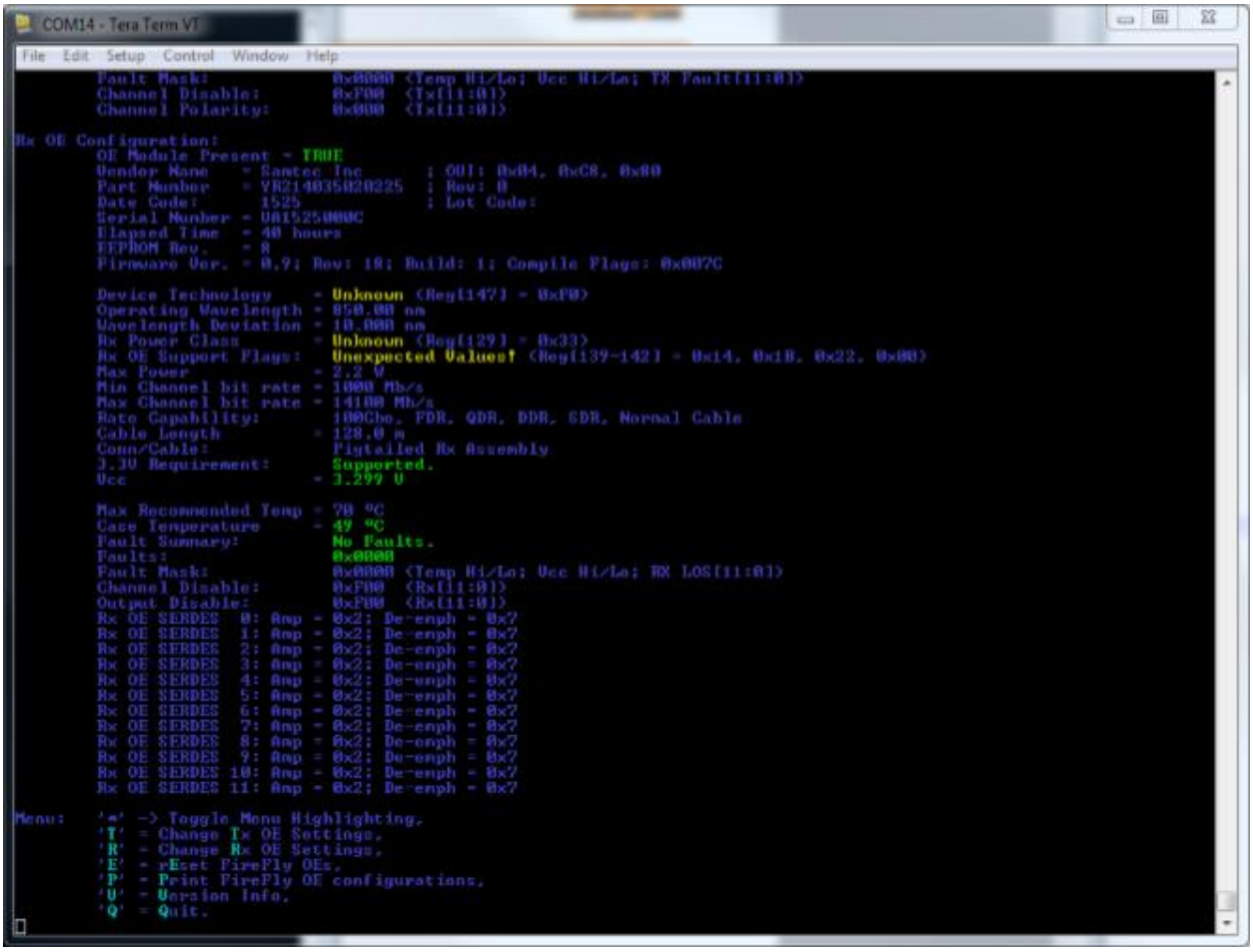



**Figure 12 - Rx Data**

4a. Next, try changing the Rx data above by pressing the “R” key. For example, if you wanted to change the data on Channel 6 to 0×4, hit “S” to change the SERDES Amplitude/Emphasis settings, then “6” to select Channel 6, “A” to select amplitude, then “4” to change the amplitude from 7, as shown in Figure 12, to 4 as shown in Figure 13.

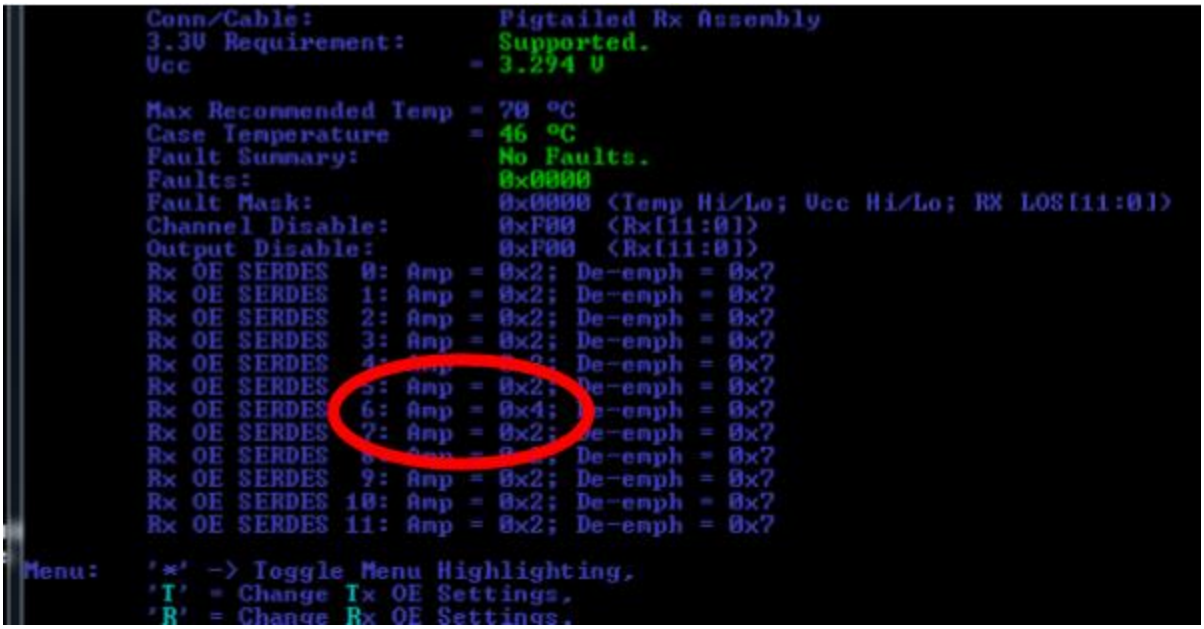



**Figure 13 - Adjusted Rx Amplitude**

To observe the full spectrum of the applied changes, re-open Vivado® and notice the various differences in SERDES Lane data and eye diagrams.

**Note:** Tera Term **does not control** the IBERT core of the FPGA, it is only a tool to communicate with the OFMC.

## 5.2 *Testing FPGA Functionality with GPIO*

In the case of initial board setup or troubleshooting, it is helpful to review the built-in functionality checks by using the GPIO (General Purpose Input/Output). See the examples below.

- LED GPIO Test
  - This test is useful to determine if the board has been recognized by the software and that the system is functioning properly.
  - Observing the LEDs below, note the difference when SW7 (middle switch of the North, South, East, West configuration is pressed)
  - LED Status:
    - 0. Program is Running
    - 1. HPC FMC Module Detected
    - 2. Tx OE Present on FMC module
    - 3. Rx OE Present on FMC module
    - 4. Tx OE INT_L is not asserted
    - 5. Rx OE INT_L is not asserted
    - 6. Test Only (DIP SW12 has a switch high)
    - 7. Test Only (Center PB SW, SW7, is depressed)

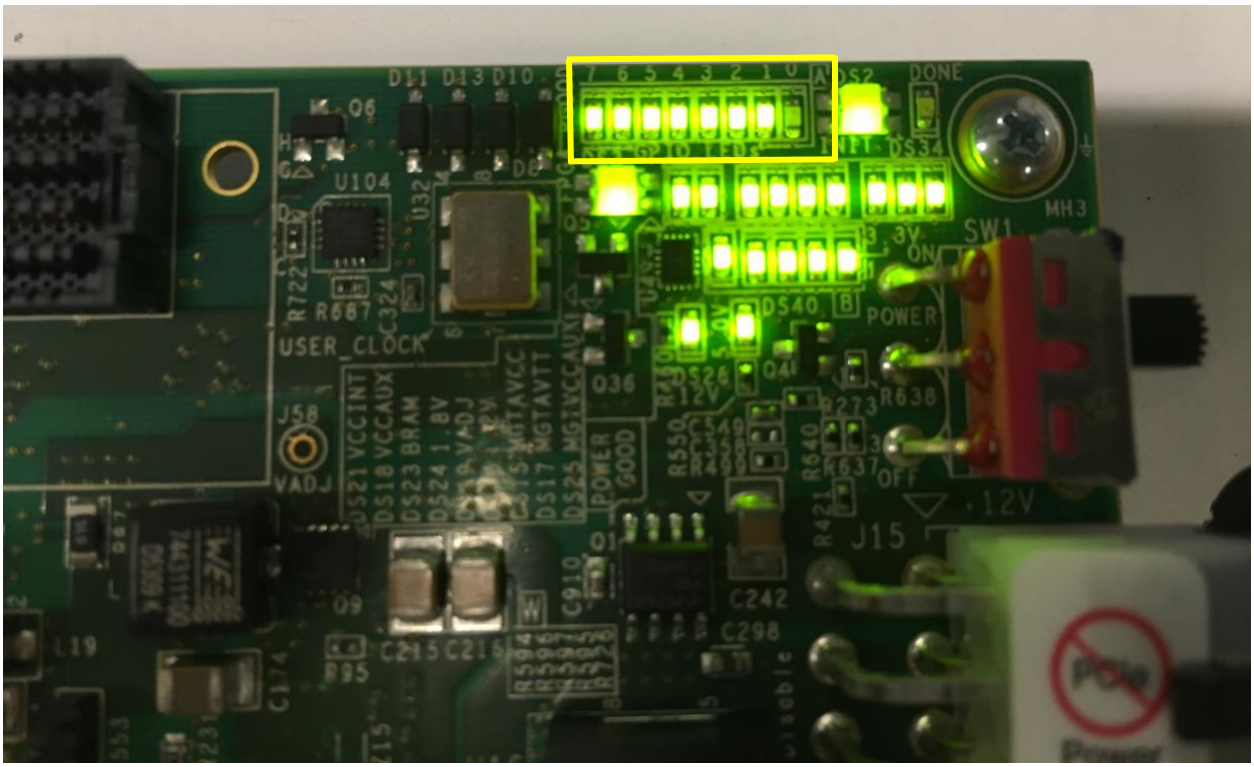



**Figure 14 - GPIO LEDs**

**Note:** In Figure 14 above, Vivado® is **not initialized**, hence why LED 0 is LOW.

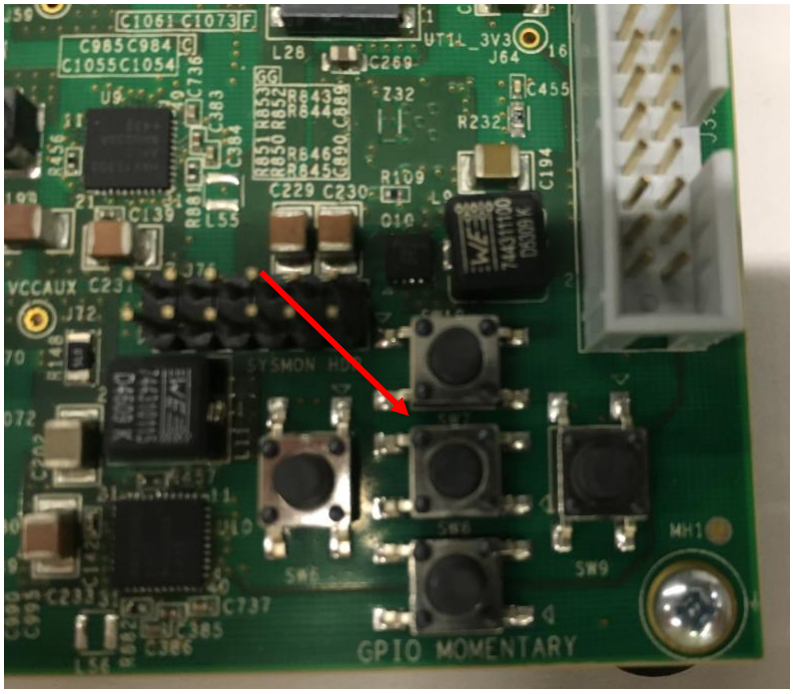



**Figure 15 - GPIO SW 7**

## 5.3 *Troubleshooting*

Due to the massive size and high data rates processed through Vivado®, bugs, crashes, and data errors are all too common. The following section contains a brief list of issues when running the OFMC Demo and troubleshooting solutions.

- If Terminal window seems unresponsive, see if push-button switch illuminates the LED #7, as described above. Perhaps the SiLabs VCP driver is not functioning or the FPGA Bitstream programming failed?
- If Program seems to be responsive, but it is not communicating correctly with OEs (e.g. Module Present LEDs or message indicating Modules are not present), use KCU105 System Console to ensure that it is properly reading EEPROM on FMC card and that VADJ = 1.8V.
    - Perhaps the FMC board needs to be re-seated properly on the KCU105 HPC FMC connector; ensure it is completely engaged by employing the included standoffs.
    - Ensure that FireFly™ OEs are completely seated on Optical FMC circuit board.
- Start seeing bit errors in Vivado® after pro-longed use without a fan blowing on OFMC board
    - Either use a fan for long-term use
    - You can use Tera Term, using the “P” command to Print FireFly OE configurations to determine the current Rx and Tx OE module temperatures. Firefly modules with pin fin heatsink require air flow and an external fan, due to heat conduction caused by the “chimney effect” from nearby heat generators on the board. Keep the FPGA and OFMC module in a relatively controlled temperature range for best results.
    - Further tweaking of SERDES settings (both on Rx OE, and in Vivado® Serial I/O Tool analyzer and Eye Scans) may improve performance at higher temperatures without a fan.
- FMC connected correctly, VADJ is correct & Terminal window is properly communicating with Oes, but Rx LOS faults are occurring or Vivado® indicates “No Link” on all, or specific channels
    - Ensure the Optical Loopback module is properly installed and engaged fully
    - Do changes to Vivado® SERDES settings (Tx Precursor, Postcursor, Diff Swing, DFE Enable, etc.) affect things? Reset IBERT Core (or individual Lanes)?
    - Can improvement be seen with changes to Rx OE SERDES settings (Amplitude or De-emphasis)?

**Note:** If none of these solutions resolve the problem, visit Section 9 Technical Support.

## 5.4 *Tips for Working in Vivado®*

This section contains a few brief tips and reminders to smooth out the process of working with your FPGA in Vivado®.

- When downloading Vivado®, choose **version 15.4**. Due to the dated nature of the Xilinx® KCU105 FPGA, it responds better to the older versions of the software. This will reduce latency and increase workflow when programming the board.
- Check that the FMC is properly mated to the FPGA via the **SEARAY™ connector closest to the HDMI port (HPC Slot 1)** and by **using the two standoffs**.
- Ensure that the Silicon Laboratories **Standard COM port is selected** when analysing with Tera Term.
- **Do not leave the FPGA running for a long time**, the constant use of the built-in fan may cause errors and overheating.
- When working with the FPGA, try to **avoid contact with surfaces which may transmit noise or electrical interference of any kind**. The included FPGA box provides a solid service for stationing the KCU105.
- Reset IBERT on all channels as necessary if expected speeds are not present.
- Remember to **"Create Scan" again after any SERDES channel is updated** to display the correct eye diagram.

# 6 Reprogramming Clock Frequencies

In some use cases, the user may desire to reprogram the default clock frequencies found within the clock generator on the 14 Gbps FireFly™ FMC Module. The output frequency for the GBTCLK0 and GBTCLK1 clocks is 100 MHz. The clock generator attaches to the same I2C bus that programs the FireFly™ optical engines. The clock signals can be enabled and reprogrammed through that interfaces via register 0x70.

A text file (Si5338B-Bxxxxx-GM V2.txt) providing additional details for enabling and reprogramming the clock generator on the 14 Gbps FireFly™ FMC Module is available from http://sog.sharefile.com. Please contact Samtec optical applications engineers at FireFly@samtec.com for more details.

# 7 Block Diagram

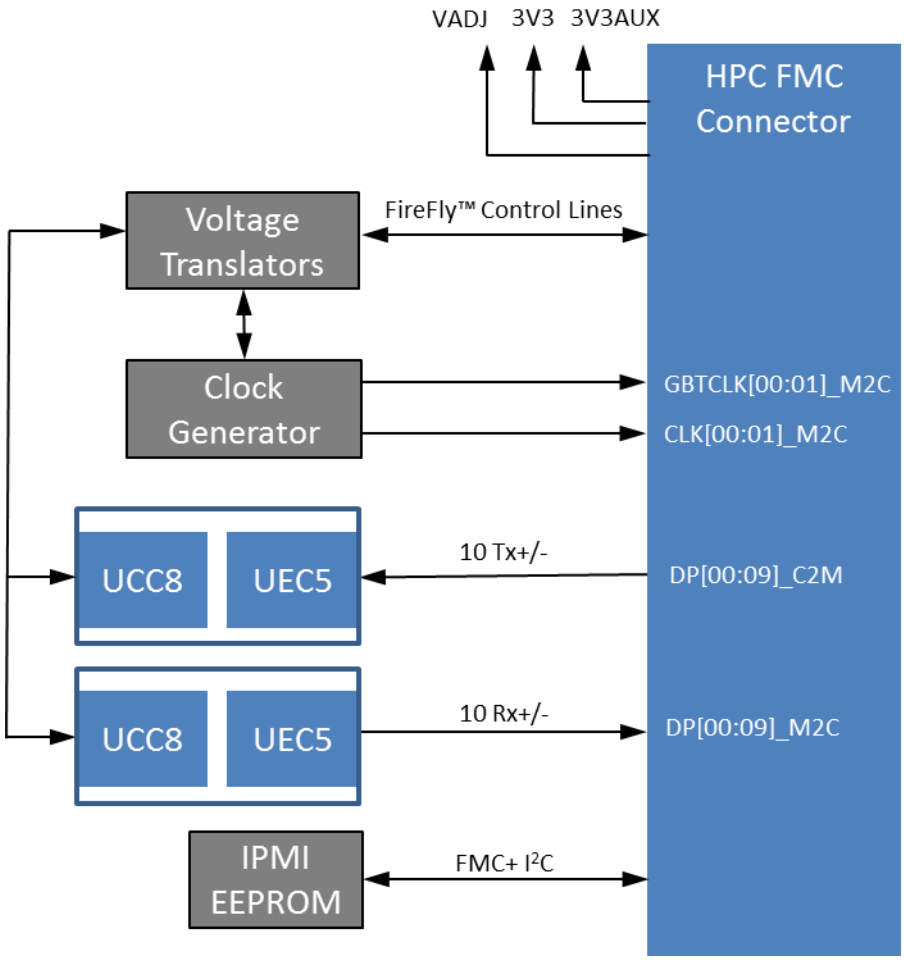



**Figure 16 - 14 Gbps FireFly™ FMC Module Block Diagram**

# 8 Schematic

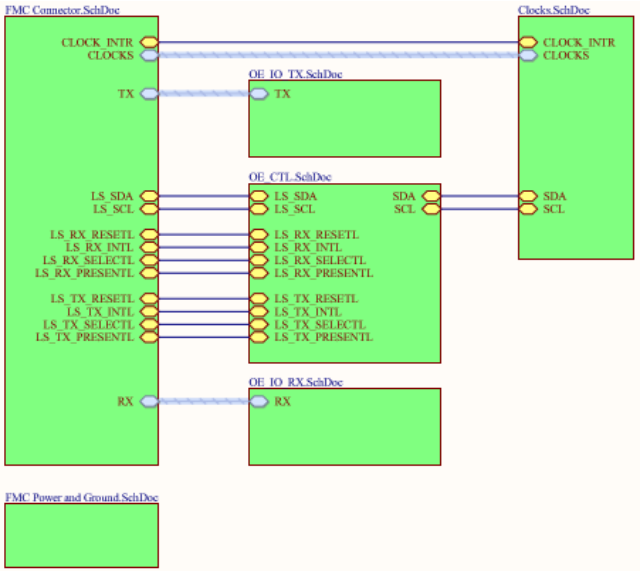



**Figure 17 - Optical FMC Module Top Layer**

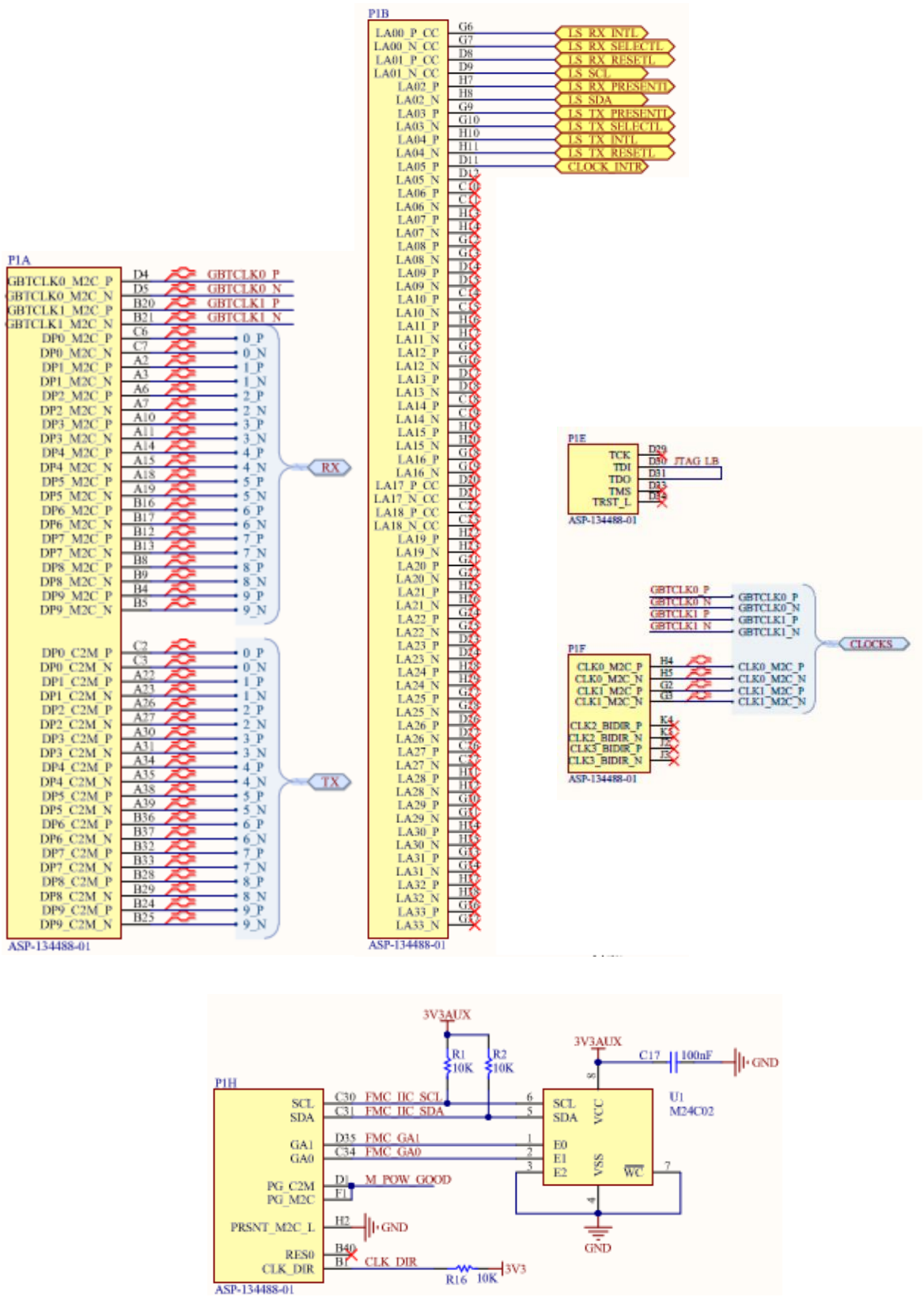



**Figure 18 - FMC Connector**

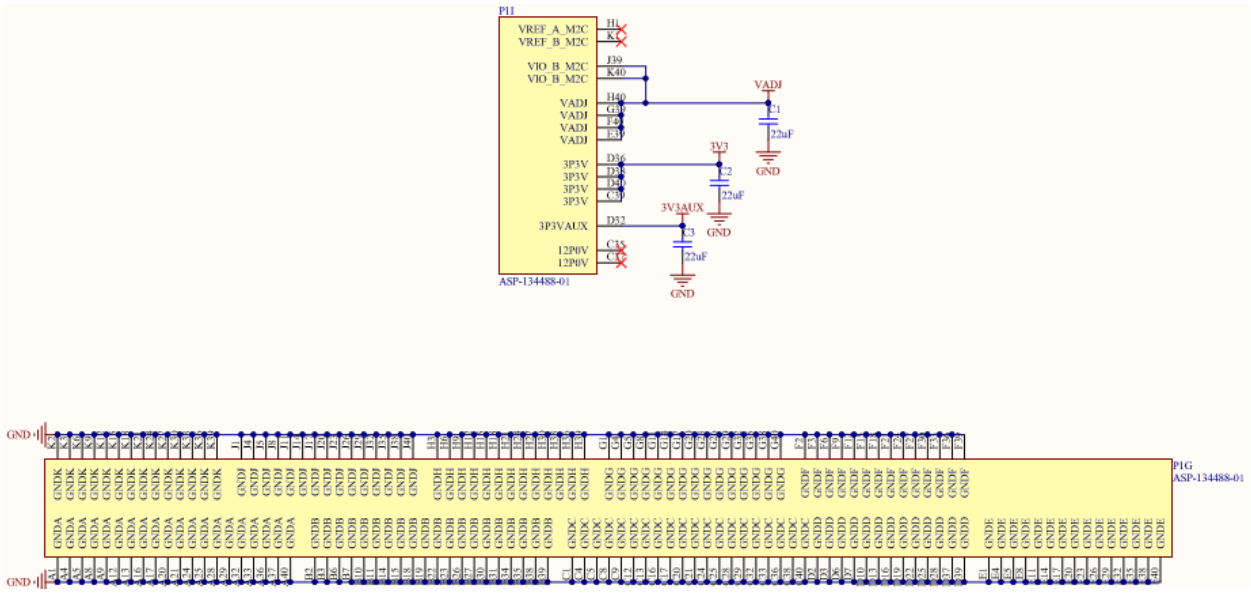



**Figure 19 - FMC Power and Ground**

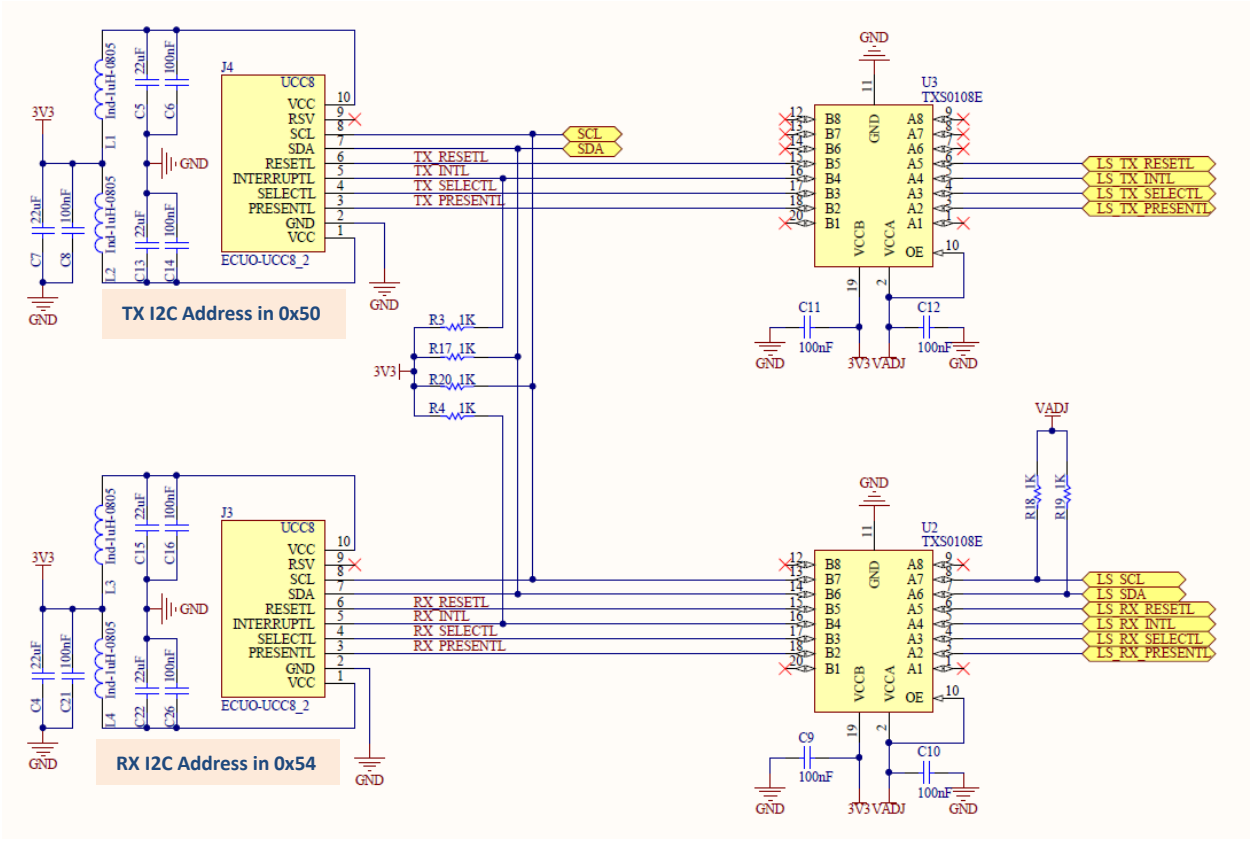



**Figure 20 - Optical Engine Control Signals**

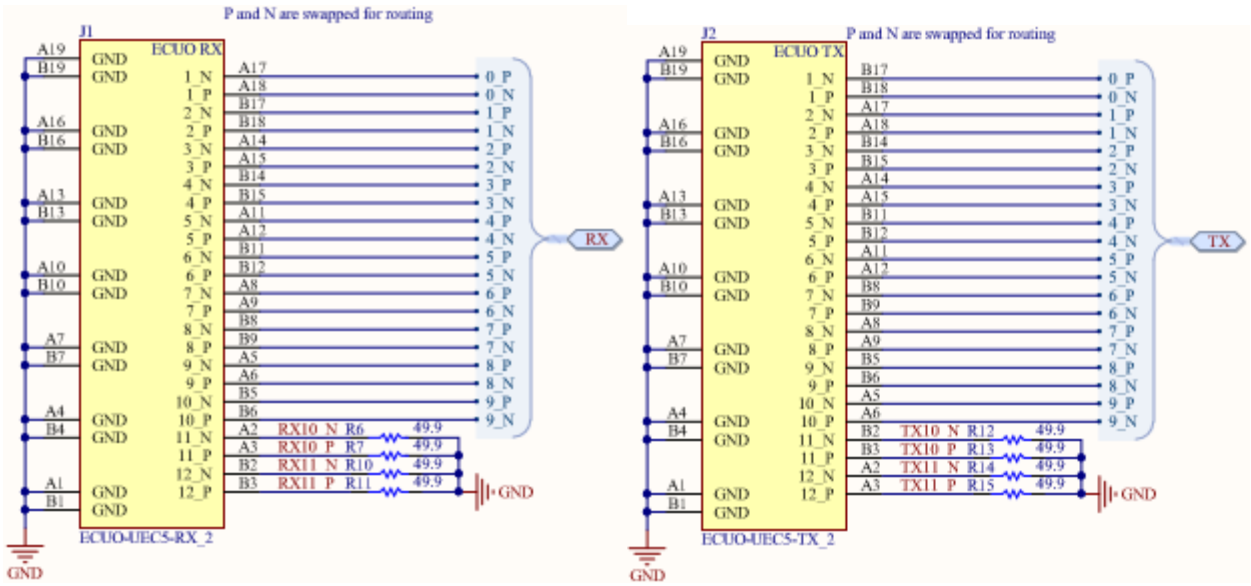



**Figure 21 - Optical Engine Rx and Tx**

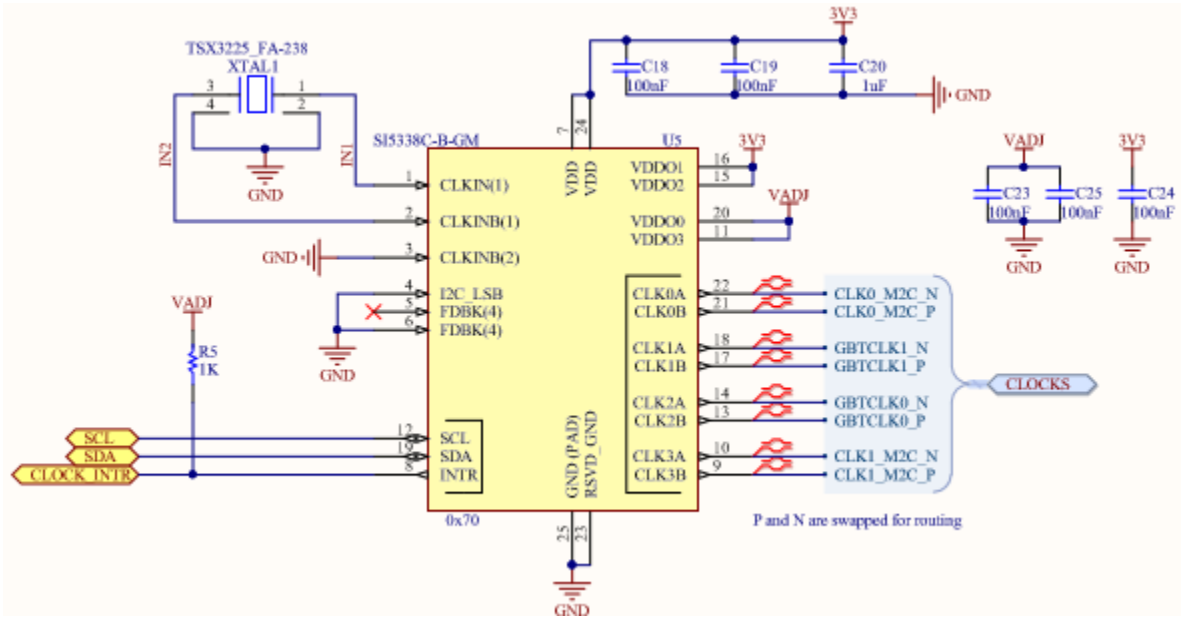



**Figure 22 - Clocks**

# 9 Mechanical and Optical

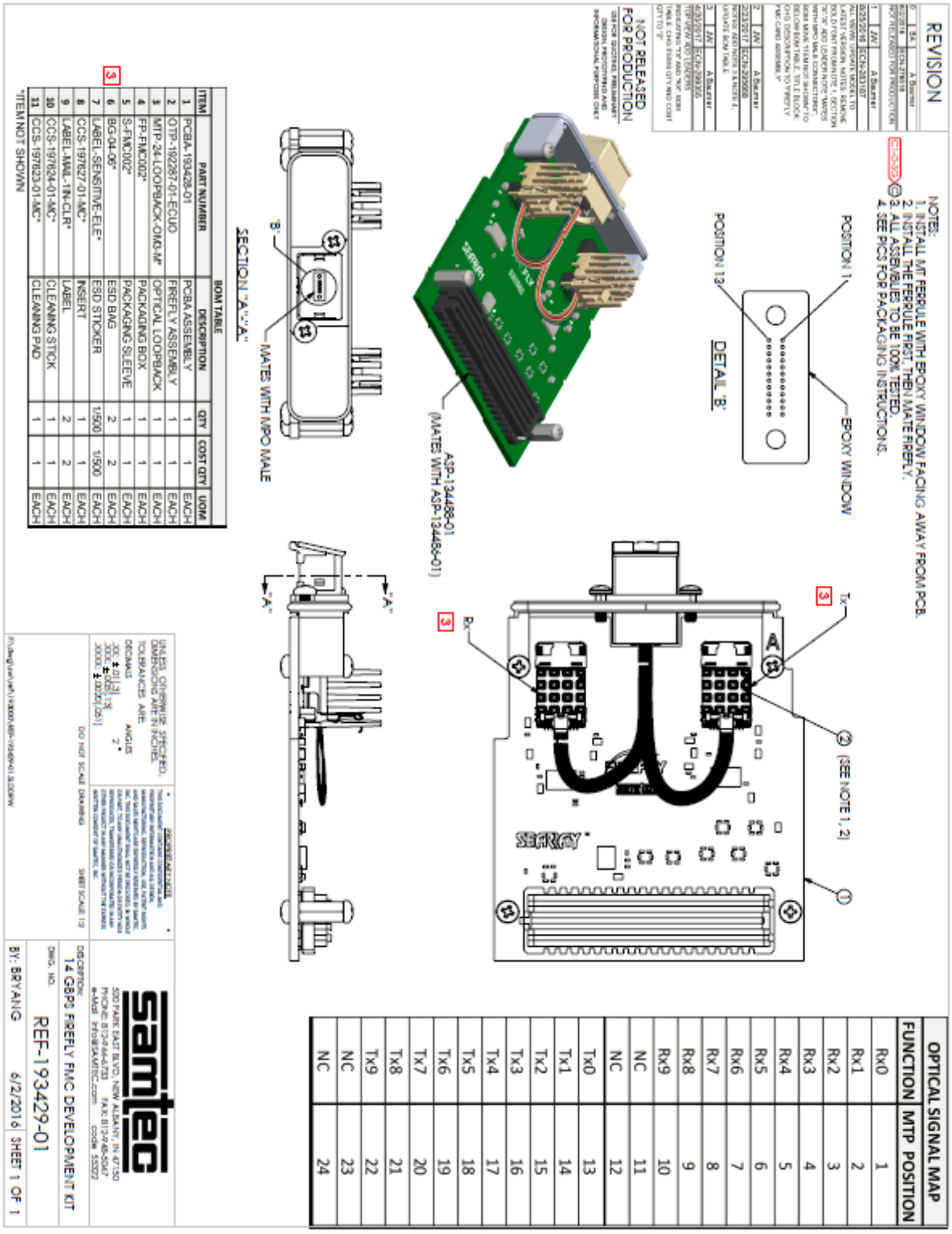



**Figure 23 - Mechanical and Optical Details**

# 10 Technical Support

If the Troubleshooting section was unable to resolve any of the issues you may be facing, please contact the available resources below:

- Samtec Kits and Boards Technical Support: KitsAndBoards@samtec.com
- Xilinx Technical Support: Xilinx Contact Support Page
- Tera Term Technical Support: Tera Term Ticket List

# 11 Glossary

| Acronym | Definition |
|---|---|
| ASP | Application Specific Product |
| BERT | Bit Error Rate Tester |
| COM | Communication Port |
| EEPROM | Read Only Memory |
| FAE | Field Application Engineer |
| FMC | FPGA Mezzanine Card |
| FPGA | Field Programmable Gate Array |
| GBps | Gigabytes Per Second |
| GPIO | General Purpose Input/Output |
| HDMI | High Definition Media Interface |
| JTAG | Joint Test Action Group |
| OE | Optical Engine |
| OFMC | Optical FPGA Mezzanine Card |
| Rx | Receiver |
| SERDES | Serializer/Deserializer |
| SI | Signal Integrity |
| Tx | Transmitter |
| USB | Universal Serial Bus |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P.O. Box 1147 • New Albany, IN 47151-1147 USA
+1-800-SAMTEC-9 (+1-800-726-8329) USA & Canada
Tel: +1-812-944-6733 • Fax: +1-812-948-5047
Email: info@samtec.com

**SAMTEC NORTHERN CALIFORNIA**
2323 Owen St., Ste 120 • Santa Clara, CA 95054
+1-800-726-8329 (USA & Canada)
Tel: +1-812-944-6733 • Fax: +1-408-217-5171
Email: samtecsiliconvalley@samtec.com

**SAMTEC SOUTHERN CALIFORNIA**
5410 Trabuco Road • Suite 120 • Irvine, CA 92620
Tel: +1-800-726-8329
Email: samtecsoutherncalifornia@samtec.com

**SAMTEC SOUTH AMERICA**
Rua Alagoas Nr 1460 • Sala 805 • Bairro Savassi
Belo Horizonte - Minas Gerais 30130-160 • Brazil
Tel: +55 31 9 9146 4447
Email: brazilsales@samtec.com

**SAMTEC UNITED KINGDOM**
11 Mollins Court • Westfield, Cumbernauld • Scotland G68 9HP
Tel: +44 01236 739292 • Fax: +44 01236 727113
Email: scotland@samtec.com

**SAMTEC GERMANY**
Streiflacher Str. 7 • 82110 Germering • Germany
+0800 SAMTEC9 (+0800 / 72 68 329) Germany only
Tel: +49 (0) 89 / 89460-0 • Fax: +49 (0) 89 / 89460-299
Email: germany@samtec.com

**SAMTEC FRANCE**
Val d' Europe Park • 11, rue du Courtalin - Bâtiment B
77700 Magny le Hongre • France
Tel: +33 1 60 95 06 60 • Fax: +33 1 60 95 06 61
Email: france@samtec.com

**SAMTEC ITALY**
Via Colleoni 25 • Centro Direzionale Colleoni
Palazzo Pegaso Ingresso 3
20864 Agrate Brianza-Monza Brianza (MB) • Italy
Tel: +39 039 6890337 • Fax: +39 039 6890315
Email: italy@samtec.com

**SAMTEC NORDIC/BALTIC**
Solkraftsvägen 25 • 13570 Stockholm • Sweden
Tel: +46 8 4477280 • Fax: +46 8 7420413
Email: scandinavia@samtec.com

**SAMTEC BENELUX**
11 Mollins Court • Westfield, Cumbernauld • Scotland G68 9HP
Tel: +44 01236 739292 • Fax: +44 01236 727113
Email: benelux@samtec.com

**SAMTEC ISRAEL**
21 Bar-Kochva St. • Concord Tower
B'nei Brak, Israel 51260
Tel: +972 3 7526600 • Fax: +972 3 7526690
Email: israel@samtec.com

**SAMTEC INDIA**
#11, 2nd Floor, Chetana, Dattatreya Road
Basavanagudi • Bangalore • 560 004 India
Tel: +91 80 3272 1612 • Fax: +91 80 2662 0967
Email: india@samtec.com

**SAMTEC ANZ**
2A San Antonio Court • Mentone 3194 • Victoria, Australia
Tel: +613 9580 0683 • Fax: +613 9580 0684
Email: australia@samtec.com

**SAMTEC SINGAPORE**
1 Kallang Sector #05-01/02 • Kolam Ayer Industrial Park
Singapore 349276
Tel: +65 6745 5955 • Fax: +65 6841 1502
Email: singapore@samtec.com

**SAMTEC JAPAN**
Nisso No. 16 Bldg. • 3-8-8, Shinyokohama, Kohoku-ku
Yokohama-shi, Kanagawa 222-0033 Japan
Tel: +81 45 475 1385 • Fax: +81 45 475 1340
Email: japan@samtec.com

**SAMTEC SHANGHAI**
Unit 601, Qilai Building • No 889 Yishan Road
Shanghai, China 200233
Tel: +86 21 6083 3766 • Fax: +86 21 5423 4575
Email: china@samtec.com

**SAMTEC SHENZHEN**
Rm 906B 9/F New World Center Tower
Yi Tian Road, Fu Tian District • Shenzhen, China 518026
Tel: +86 755 83776780 • Fax: +86 755 83776767
Email: hongkong@samtec.com

**SAMTEC TAIWAN**
Room D, Floor B1, No. 205, Sec. 3 • Beixin Rd.
Xindian District • New Taipei City 23143 • Taiwan
Tel: +886 2 7727 4060 • Fax: +886 2 7727 4179
Email: taiwan@samtec.com

**SAMTEC HONG KONG**
Room 18, 13/F, Shatin Galleria • 18-24 Shan Mei Street
Fo Tan, Shatin, Hong Kong
Tel: +852 26904858 • Fax: +852 26904842
Email: hongkong@samtec.com

**SAMTEC KOREA**
RM#705, 109 Gwanggyo-ro
Yeongtong-gu, Suwon-si, Gyeonggi-Do • 16229 South Korea
Tel: +82 31 717 5685 • Fax: +82 70 7500 0246
Email: korea@samtec.com


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