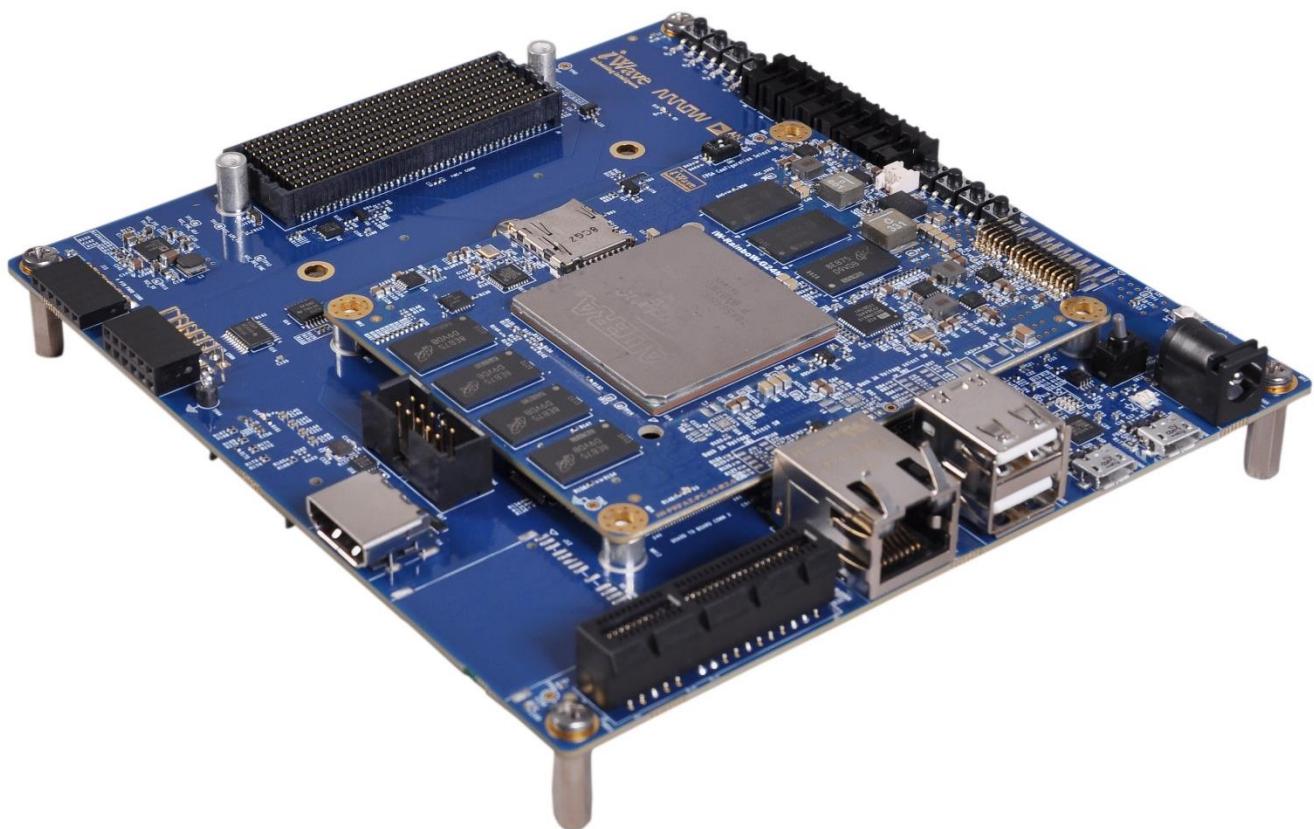


Arria10 SoC/FPGA Custom Development Platform

Hardware User Guide



iWave
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Document Revision History

Document Number		iW-PRFXR-Arria10_SoC_FPGA_DevKit-HardwareUserGuide-REL0.1
Revision	Date	Change Description
0.1	11 th May 2019	Draft Release Version

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1. INTRODUCTION

1.1 Purpose

The Arria10 SoC/FPGA Custom Development platform incorporates Arria10 SoC/FPGA based SOM and Highs-peed Carrier board for complete validation of Arria10 SoC/FPGA functionality. This document is the Hardware User Guide for the Arria10 SoC/FPGA custom Carrier Board and provides detailed information on the overall design & usage of the Carrier Board from a Hardware Systems perspective. The details about the Arria10 SoC/FPGA SOM hardware is explained in iW-Rainbow-G24M-Arria10_SoC_FPGA_SOM-HardwareUserGuide.

1.2 Overview

Arria10 SoC/FPGA Custom Development platform incorporates Arria10 SoC/FPGA SOM which is based on Intel's high performance Arria10 SoC and Highs-peed Carrier Board. With the 150mmx140mm size, carrier board is packed with all the necessary on-board connectors to validate the features of Arria10 SoC/FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor Signal
CPU	Central Processing Unit
FMC+	FPGA Mezzanine Card
GPIO	General Purpose Input Output
HPC	High Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PTH	Plated Through hole
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
TMDS	Transition-Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Arria10 SoC SOM Hardware User Guide
- Intel's CPU Hardware User Manual

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Arria10 SoC/FPGA Custom Development Platform carrier board features with high level block diagram and detailed information about each block.

2.1 Arria10 SoC/FPGA Custom Carrier Board Block Diagram

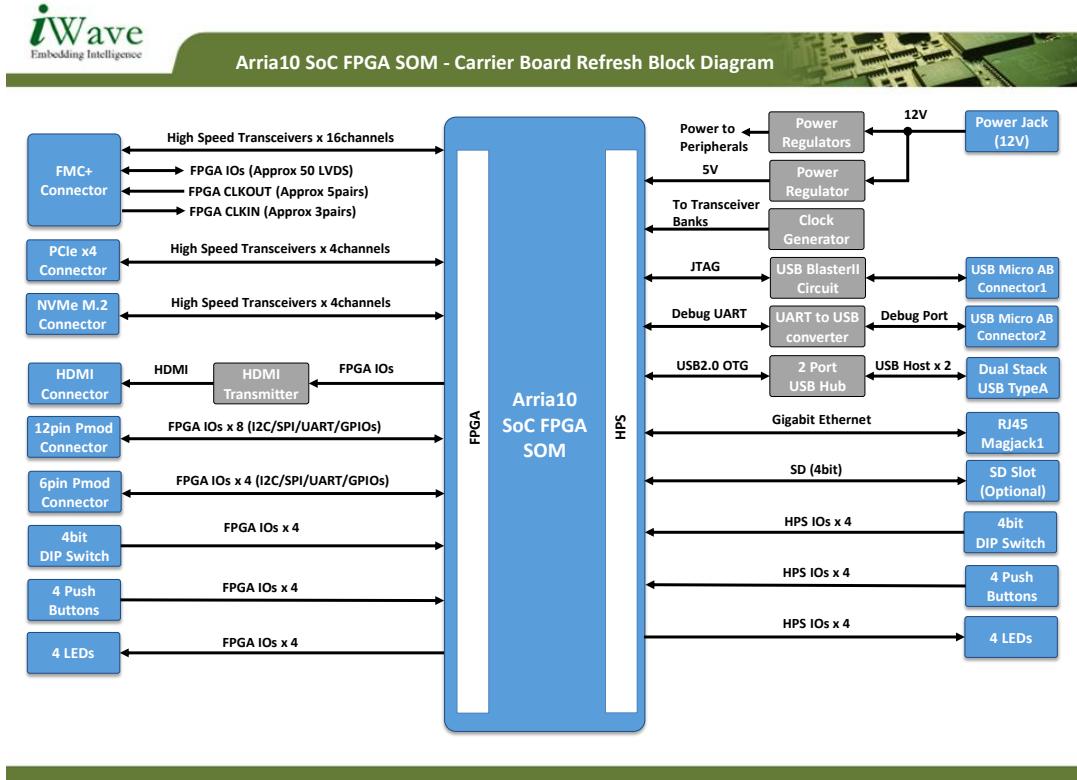


Figure 1:Arria10 SoC/FPGA Custom Carrier Board Block Diagram

2.2 Arria10 SoC/FPGA custom carrier board Features

The Arria10 SoC/FPGA custom carrier board supports the following features to validate the Arria10 SoC/FPGA SOM Expansion connector1 and 2 Interfaces.

Serial Interface Features

- Debug UART through USB MicroAB Connector

Communication Features

- Gigabit Ethernet through RJ45MagJack x 1
- USB2.0 Host x 2 Ports through Dual Stack Type A Connector x 1
- On-Board USB-Blaster™ II Interface through MicroAB Connector x 1

Expansion Connectors

- VITA 57.4 FMC++ High Pin Count (HPC) Connector x 1
 - 16 Transceivers from BANK 1C, BANK 1D, BANK 1E, BANK 1F
 - 42 LVDS pairs IOs from BANK 3B, BANK 3C
 - 28 Single Ended (SE) IOs from BANK3A
- 12pin PMOD Host Port Connector x 1
 - 8 Single ended (SE) IOs
- 6pin PMOD Host Port Connector x 1
 - 4 Single ended (SE) IOs

High Speed Communication Connectors

- PCIe x 4 Connector x 1
- NVMe M.2 Connector (through PCIe Interface) x 1

Display Features

- ADV7511 HDMI 1.4a Transmitter (through FPGA IOs)
- HDMI Type A Receptacle Connector

User Interface Features

- FPGA slide switch x 4 Nos
- FPGA push button x 4 Nos
- FPGA LED x 4 Nos
- HPS slide switch x 4 Nos
- HPS push button x 4 Nos
- HPS LED x 4 Nos

Additional Features

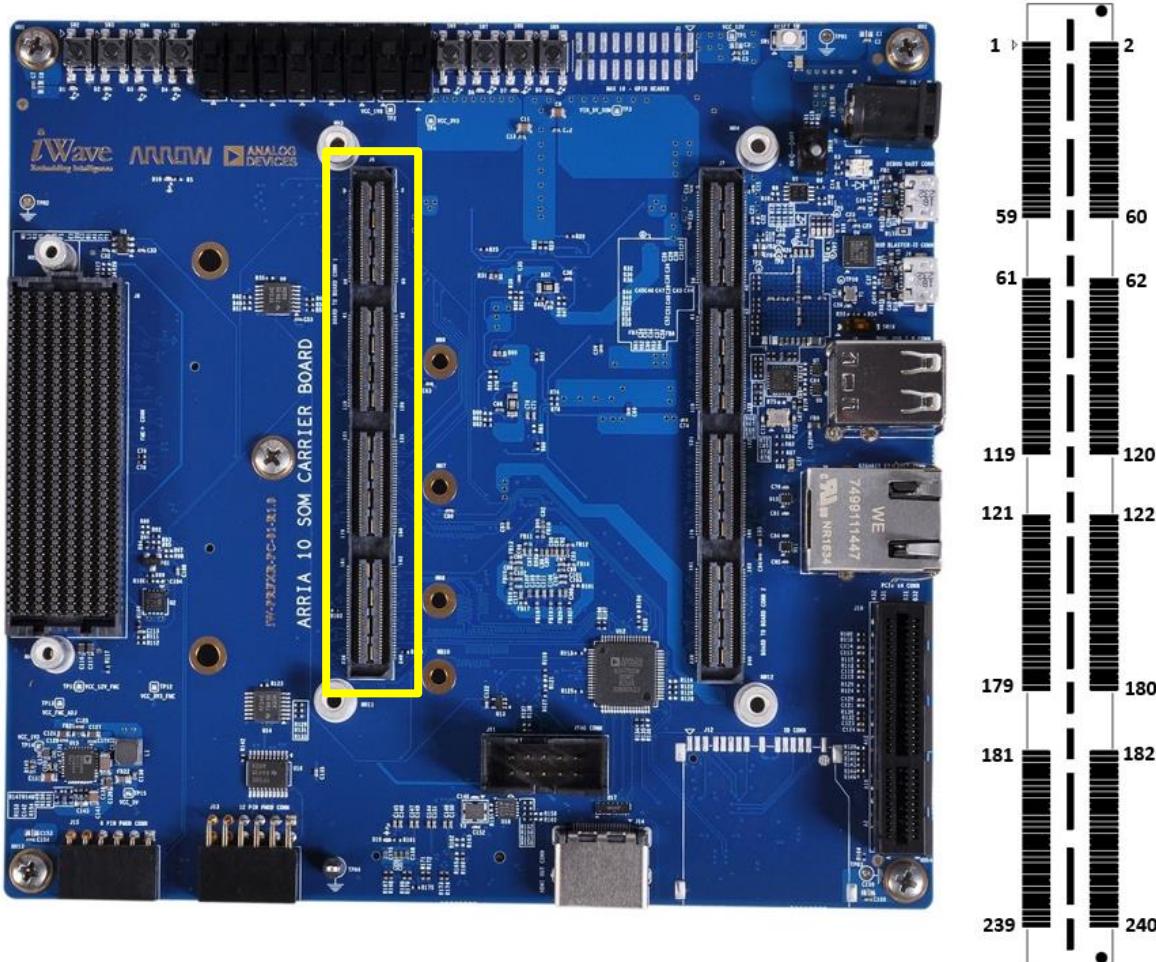
- JTAG Connector x 1
- Power ON/OFF Toggle Switch x 1
- Reset Push-button Switch x 1

General Specification

- Power Supply : 12V Power Input Jack
- Form Factor : 150mm X 140mm

2.3 Board to Board Connector1

The Arria10 SoC/FPGA custom carrier board supports 240Pin Board to Board Connector for mating with Arria10 SoC/FPGA SOM. This 240Pin Expansion connector1 is capable of handling high-speed signals. The SOM Expansion Connector1 (J6) is physically located at the top of the board as shown below.



Board to Board Connector1 (J6)

Figure 2: SOM Expansion Connector1

Table 3: Board to Board Connector1

Pin No	Signal Name	Signal Type/Termination	Description
1	GND	Power	Ground.
2	GND	Power	Ground.
3	GXBL1C_TX_CH0p	I, DIFF	Bank1C High speed positive differential transmitter channel0. This pin is connected to C2 nd pin of HPC FMC+ Connector (J8).
4	REFCLK_GXBL1C_CHTp	O, DIFF	Bank1C High speed differential reference clock positive receiver channel T. This pin is connected from 100MHz PCIe Clock source.
5	GXBL1C_TX_CH0n	I, DIFF	Bank1C High speed negative differential transmitter channel0. This pin is connected to C3 th pin of HPC FMC+ Connector (J8).
6	REFCLK_GXBL1C_CHTn	O, DIFF	Bank1C High speed differential reference clock negative receiver This pin is connected from 100MHz PCIe Clock source.
7	GND	Power	Ground.
8	GND	Power	Ground.
9	GXBL1C_TX_CH1p	I, DIFF	Bank1C High speed positive differential transmitter channel1. This pin is connected to A22 th pin of HPC FMC+ Connector (J8).
10	FPGA_AM7_LVDS3A_24n	IO, 1.8V LVCMOS	Bank 3A User I/O Single ended pin. This pin is connected to B1 th pin of HPC FMC+ Connector (J8).
11	GXBL1C_TX_CH1n	I, DIFF	Bank1C High speed negative differential transmitter channel1. This pin is connected to A23 th pin of HPC FMC+ Connector (J8).
12	FPGA_AM1_LVDS3A_16p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J12th pin of HPC FMC+ Connector (J8)
13	GND	Power	Ground.
14	FPGA_AM2_LVDS3A_16n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to 52 th pin of NVMe M.2 Connector (J16).

Pin No	Signal Name	Signal Type/Termination	Description
15	GXBL1C_RX_CH1n	O, DIFF	Bank1C High speed negative differential receiver channel1. This pin is connected to A3 th pin of HPC FMC+ Connector (J8)
16	FPGA_AP4_LVDS3A_18p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E12th pin of HPC FMC+ Connector (J8)
17	GXBL1C_RX_CH1p	I, DIFF	Bank1C High speed positive differential receiver channel1. This pin is connected to A2 th pin of HPC FMC+ Connector (J8)
18	FPGA_AN4_LVDS3A_18n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E13 th pin of HPC FMC+ Connector (J8)
19	GND	Power	Ground.
20	GND	Power	Ground.
21	GXBL1C_RX_CH0n	O, DIFF	Bank1C High speed negative differential receiver channel0. This pin is connected to C7 th pin of HPC FMC+ Connector (J8)
22	FPGA_AL3_LVDS3A_15n/C LKOUT_On	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J3 th pin of HPC FMC+ Connector (J8)
23	GXBL1C_RX_CH0p	O, DIFF	Bank1C High speed positive differential receiver channel0. This pin is connected to C6 th pin of HPC FMC+ Connector (J8)
24	FPGA_AM3_LVDS3A_15p/ CLKOUT_0p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J2 th pin of HPC FMC+ Connector (J8)
25	GND	Power	Ground.
26	GND	Power	Ground.
27	FPGA_AM6_LVDS3A_17p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E9 th pin of HPC FMC+ Connector (J8).
28	FPGA_AP6_LVDS3A_20n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J13 th pin of HPC FMC+ Connector (J8).
29	FPGA_AM5_LVDS3A_17n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E10 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
30	FPGA_AP7_LVDS3A_20p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to VCC_3V3_FMC+ power enable.
31	FPGA_AP5_LVDS3A_19p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F10 th pin of HPC FMC+ Connector (J8).
32	FPGA_AL6_LVDS3A_14p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to H2 th pin of HPC FMC+ Connector (J8).
33	FPGA_AN5_LVDS3A_19n	IO, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to F11 th pin of HPC FMC+ Connector (J8).
34	FPGA_AK6_LVDS3A_14n	IO, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to Z1 th pin of HPC FMC+ Connector (J8).
35	GND	Power	Ground.
36	GND	Power	Ground.
37	GXBL1C_TX_CH2p	I, DIFF	Bank1C High speed positive differential transmitter channel2. This pin is connected to A26 th pin of HPC FMC+ Connector (J8).
38	FPGA_AK7_LVDS3A_9p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to SDIO power select switch.
39	GXBL1C_TX_CH2n	I, DIFF	Bank1C High speed negative differential transmitter channel2. This pin is connected to A27 th pin of HPC FMC+ Connector (J8).
40	FPGA_AK8_LVDS3A_9n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to FPGA LED D4 control pin
41	GND	Power	Ground.
42	FPGA_AJ6_LVDS3A_11n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to K14 th pin of HPC FMC+ Connector (J8).
43	GXBL1C_TX_CH3p	I, DIFF	Bank1C High speed positive differential transmitter channel3. This pin is connected to A30 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
44	FPGA_AJ7_LVDS3A_11p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to K13 th pin of HPC FMC+ Connector (J8).
45	GXBL1C_TX_CH3n	I, DIFF	Bank1C High speed negative differential transmitter channel3. This pin is connected to A31 th pin of HPC FMC+ Connector (J8).
46	FPGA_AH7_LVDS3A_8p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to VCC_FMC+_ADJ enable.
47	GND	Power	Ground.
48	FPGA_AG7_LVDS3A_8n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F14 th pin of HPC FMC+ Connector (J8).
49	GXBL1C_RX_CH3n	O, DIFF	Bank1C High speed negative differential receiver channel3. This pin is connected to A11 th pin of HPC FMC+ Connector (J8).
50	FPGA_AH8_LVDS3A_7p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F13 th pin of HPC FMC+ Connector (J8).
51	GXBL1C_RX_CH3p	O, DIFF	Bank1C High speed positive differential receiver channel3. This pin is connected to A10 th pin of HPC FMC+ Connector (J8).
52	FPGA_AG8_LVDS3A_7n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to chip select of clock synthesizer.
53	GND	Power	Ground.
54	GND	Power	Ground.
55	GXBL1C_RX_CH2n	O, DIFF	Bank1C High speed negative differential receiver channel2. This pin is connected to A7 th pin of HPC FMC+ Connector (J8).
56	FPGA_AL4_LVDS3A_13n/C_LKIN_On	O, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to H5 th pin of HPC FMC+ Connector (J8).
57	GXBL1C_RX_CH2p	O, DIFF	Bank1C High speed positive differential receiver channel2. This pin is connected to A6 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
58	FPGA_AL5_LVDS3A_13p/C LKIN_0p	O, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to H4 th pin of HPC FMC+ Connector (J8).
59	GND	Power	Ground.
60	GND	Power	Ground.
61	GND	Power	Ground.
62	GND	Power	Ground.
63	GXBL1C_TX_CH4p	I, DIFF	Bank1C High speed positive differential transmitter channel4. This pin is connected to transmit0 positive pin of NVMe M.2 connector.
64	REFCLK_GXBL1C_CHBp	O, DIFF	Bank1C High speed differential reference clock positive receiver channel B. This pin is connected to D4 th pin of HPC FMC+ Connector (J8).
65	GXBL1C_TX_CH4n	I, DIFF	Bank1C High speed negative differential transmitter channel3. This pin is connected to transmit0 negative pin of NVMe M.2 connector (J16).
66	REFCLK_GXBL1C_CHBn	O, DIFF	Bank1C High speed differential reference clock negative receiver channel B. This pin is connected to D5 th pin of HPC FMC+ Connector (J8).
67	GND	Power	Ground.
68	GND	Power	Ground.
69	GXBL1C_TX_CH5p	I, DIFF	Bank1C High speed positive differential transmitter channel5. This pin is connected to transmit1 positive pin of NVMe M.2 connector (J16).
70	FPGA_AG10_LVDS3A_4p	IO, 1.8V LVC MOS	Bank3A User I/O Single ended pin. This pin is connected to J15 th pin of HPC FMC+ Connector (J8).
71	GXBL1C_TX_CH5n	I, DIFF	Bank1C High speed negative differential transmitter channel5. This pin is connected to transmit1 negative pin of NVMe M.2 connector (J16).

Pin No	Signal Name	Signal Type/Termination	Description
72	FPGA_AF10_LVDS3A_4n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J16 th pin of HPC FMC+ Connector (J8).
73	GND	Power	Ground.
74	FPGA_AN8_LVDS3A_21p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E15 th pin of HPC FMC+ Connector (J8).
75	GXBL1C_RX_CH5n	O, DIFF	Bank1C High speed negative differential receiver channel5. This pin is connected to receive1 negative pin of NVMe M.2 connector.
76	FPGA_AM8_LVDS3A_21n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to E16 th pin of HPC FMC+ Connector (J8).
77	GXBL1C_RX_CH5p	O, DIFF	Bank1C High speed positive differential receiver channel5. This pin is connected to receive1 positive pin of NVMe M.2 connector (J16).
78	FPGA_AL9_LVDS3A_23p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to DEVSLP pin of NVMe M.2 connector (J16).
79	GND	Power	Ground.
80	GND	Power	Ground.
81	GXBL1C_RX_CH4n	O, DIFF	Bank1C High speed negative differential receiver channel4. This pin is connected to receive0 negative pin of NVMe M.2 connector (J16).
82	FPGA_AK9_LVDS3A_12n/C LKIN_1n	O, 1.8V LVDS	NC. This pin is optionally connected from clock synthesizer.
83	GXBL1C_RX_CH4p	O, DIFF	Bank1C High speed positive differential receiver channel4. This pin is connected to receive0 positive pin of NVMe M.2 connector (J16).
84	FPGA_AJ9_LVDS3A_12p/CL KIN_1p	O, 1.8V LVDS	NC. This pin is optionally connected from clock synthesizer.
85	GND	Power	Ground.
86	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
87	FPGA_AF9_LVDS3A_1p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected from FPGA push button SW5.
88	FPGA_AN9_LVDS3A_22n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to VCC_12V_FMC+ control.
89	FPGA_AE9_LVDS3A_1n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected from FPGA push button SW4.
90	FPGA_AP9_LVDS3A_22p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This signal is connected to WAKE pin of PCIe x4 Connector (J10).
91	FPGA_AF8_LVDS3A_2p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected from FPGA push button SW2.
92	FPGA_AH10_LVDS3A_3p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F16 th pin of HPC FMC+ Connector (J8).
93	FPGA_AE8_LVDS3A_2n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected from FPGA push button SW3.
94	FPGA_AH9_LVDS3A_3n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F17 th pin of HPC FMC+ Connector (J8).
95	GND	Power	Ground.
96	GND	Power	Ground.
97	GXBL1D_TX_CH0p	I, DIFF	Bank1D High speed positive differential transmitter channel0. This pin is connected to transmit2 positive pin of NVMe M.2 connector (J16).
98	REFCLK_GXBL1D_CHTp	O, DIFF	Bank1D High speed differential reference clock positive receiver channel T. This pin is connected from clock synthesizer OUT1 positive pin.

Pin No	Signal Name	Signal Type/Termination	Description
99	GXBL1D_TX_CH0n	I, DIFF	Bank1D High speed negative differential transmitter channel0. This pin is connected to transmit2 negative pin of NVMe M.2 connector (J16).
100	REFCLK_GXBL1D_CHTn	O, DIFF	Bank1D High speed differential reference clock negative receiver channel T. This pin is connected from clock synthesizer OUT1 negative pin.
101	GND	Power	Ground.
102	GND	Power	Ground.
103	GXBL1D_TX_CH1p	I, DIFF	Bank1D High speed positive differential transmitter channel1. This pin is connected to transmit3 positive pin of NVMe M.2 connector (J16).
104	FPGA_AL8_LVDS3A_23n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to PEWAKE# of NVMe M.2 connector (J16)
105	GXBL1D_TX_CH1n	I, DIFF	Bank1D High speed negative differential transmitter channel1. This pin is connected to transmit3 negative pin of NVMe M.2 connector (J16).
106	FPGA_AG11_LVDS3A_5n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J19 th pin of HPC FMC+ Connector (J8).
107	GND	Power	Ground.
108	FPGA_AF11_LVDS3A_5p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to J18 th pin of HPC FMC+ Connector (J8).
109	GXBL1D_RX_CH1n	O, DIFF	Bank1D High speed negative differential receiver channel1. This pin is connected to receiver3 negative pin of NVMe M.2 connector (J16).
110	FPGA_AE11_LVDS3A_6n	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F20 th pin of HPC FMC+ Connector (J8).
111	GXBL1D_RX_CH1p	O, DIFF	Bank1D High speed positive differential receiver channel1. This pin is connected to receiver3 positive pin of NVMe M.2 connector (J16).

Pin No	Signal Name	Signal Type/Termination	Description
112	FPGA_AE12_LVDS3A_6p	IO, 1.8V LVCMOS	Bank3A User I/O Single ended pin. This pin is connected to F19 th pin of HPC FMC+ Connector (J8).
113	GND	Power	Ground.
114	GND	Power	Ground.
115	GXBL1D_RX_CH0n	O, DIFF	Bank1D High speed negative differential receiver channel0. This pin is connected to receiver2 negative pin of NVMe M.2 connector (J16).
116	FPGA_AH5_LVDS3A_10n/C LKOUT_1n	I, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to K17 th pin of HPC FMC+ Connector (J8).
117	GXBL1D_RX_CH0p	O, DIFF	Bank1D High speed positive differential receiver channel0. This pin is connected to receiver2 positive pin of NVMe M.2 connector (J16).
118	FPGA_AJ5_LVDS3A_10p/CL KOUT_1p	I, 1.8V LVDS	Bank3A User I/O Single ended pin. This pin is connected to K16 th pin of HPC FMC+ Connector (J8).
119	GND	Power	Ground.
120	GND	Power	Ground.
121	GND	Power	Ground.
122	GND	Power	Ground.
123	GXBL1D_TX_CH2p	I, DIFF	Bank1D High speed positive differential transmitter channel2. This pin is connected to A34 th pin of HPC FMC+ Connector (J8).
124	FPGA_AG17_LVDS2A_15p/ CLKOUT_0p	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin connected to FPGA LED D2 control.
125	GXBL1D_TX_CH2n	I, DIFF	Bank1D High speed negative differential transmitter channel2. This pin is connected to A35 th pin of HPC FMC+ Connector (J8).
126	FPGA_AH17_LVDS2A_15n/ CLKOUT_0n	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin connected to FPGA LED D3 control.
127	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
128	FPGA_AD19_LVDS2A_21p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D4 th bit of HDMI transmitter chip.
129	GXBL1D_TX_CH3p	I, DIFF	Bank1D High speed positive differential transmitter channel3. This pin is connected to A38 th pin of HPC FMC+ Connector (J8).
130	FPGA_AH18_LVDS2A_13p/CLKIN_0p	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin is connected from FPGA Slide Switch SW13.
131	GXBL1D_TX_CH3n	I, DIFF	Bank1D High speed negative differential transmitter channel3. This pin is connected to A39 th pin of HPC FMC+ Connector (J8).
132	FPGA_AH19_LVDS2A_13n/CLKIN_0n	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin is connected from FPGA Slide Switch SW12.
133	GND	Power	Ground.
134	FPGA_AE18_LVDS2A_21n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D5 th bit of HDMI transmitter chip.
135	GXBL1D_RX_CH3n	O, DIFF	Bank1D High speed negative differential receiver channel3. This pin is connected to A19 th pin of HPC FMC+ Connector (J8).
136	FPGA_AJ17_LVDS2A_16p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D13 th bit of HDMI transmitter chip.
137	GXBL1D_RX_CH3p	O, DIFF	Bank1D High speed positive differential receiver channel3. This pin is connected to A18 th pin of HPC FMC+ Connector (J8).
138	FPGA_AK17_LVDS2A_16n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D14 th bit of HDMI transmitter chip.
139	GND	Power	Ground.
140	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
141	GXBL1D_RX_CH2n	O, DIFF	Bank1D High speed negative differential receiver channel2. This pin is connected to A15 th pin of HPC FMC+ Connector (J8).
142	FPGA_AM16_LVDS2A_10n /CLKOUT_0n	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin is connected to FPGA Slide Switch SW10
143	GXBL1D_RX_CH2p	O, DIFF	Bank1D High speed positive differential receiver channel2. This pin is connected to A14 th pin of HPC FMC+ Connector (J8).
144	FPGA_AL16_LVDS2A_10p/ CLKOUT_0p	IO, 1.8V LVCMOS	LVDS2A User I/O Single ended pin. This pin is connected to FPGA Slide Switch SW11
145	GND	Power	Ground.
146	GND	Power	Ground.
147	FPGA_AP16_LVDS2A_2p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to 2 nd pin of 6pin Pmod connector (J15).
148	FPGA_AP12_LVDS2A_5n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to I2S0 pin of HDMI transmitter chip. differential negative channels5.
149	FPGA_AP17_LVDS2A_2n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to 3 rd pin of 6pin Pmod connector (J15).
150	FPGA_AN12_LVDS2A_5p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D6 th bit of HDMI transmitter chip.
151	FPGA_AL18_LVDS2A_11n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D19 th bit of HDMI transmitter chip.
152	FPGA_AH15_LVDS2A_17n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D12 th bit of HDMI transmitter chip.

Pin No	Signal Name	Signal Type/Termination	Description
153	FPGA_AK18_LVDS2A_11p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D18 th bit of HDMI transmitter chip.
154	FPGA_AJ15_LVDS2A_17p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D11 th bit of HDMI transmitter chip.
155	GND	Power	Ground.
156	GND	Power	Ground.
157	GXBL1D_TX_CH4p	O, DIFF	Bank1D High speed positive differential transmitter channel4. This pin is connected to B36 th pin of HPC FMC+ Connector (J8).
158	REFCLK_GXBL1D_CHBp	O, DIFF	Bank1D High speed differential reference clock positive receiver channel B. This pin is connected to B20th pin of HPC FMC+ Connector (J8).
159	GXBL1D_TX_CH4n	O, DIFF	Bank1D High speed negative differential transmitter channel4. This pin is connected to B37 th pin of HPC FMC+ Connector (J8).
160	REFCLK_GXBL1D_CHBn	O, DIFF	Bank1D High speed differential reference clock negative receiver channel B. This pin is connected to B21 th pin of HPC FMC+ Connector (J8).
161	GND	Power	Ground.
162	GND	Power	Ground.
163	GXBL1D_TX_CH5p	I, DIFF	Bank1D High speed positive differential transmitter channel5. This pin is connected to B32 th pin of HPC FMC+ Connector (J8).
164	FPGA_AG16_LVDS2A_20p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected PClex4 Connector (J10) reset signal.
165	GXBL1D_TX_CH5n	I, DIFF	Bank1D High speed negative differential transmitter channel5. This pin is connected to B33 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
166	FPGA_AF16_LVDS2A_20n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D7 th bit of HDMI transmitter chip.
167	GND	Power	Ground.
168	FPGA_AE17_LVDS2A_19n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D9 th bit of HDMI transmitter chip.
169	GXBL1D_RX_CH5n	O, DIFF	Bank1D High speed negative differential receiver channel5. This pin is connected to B13 th pin of HPC FMC+ Connector (J8).
170	FPGA_AE16_LVDS2A_19p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to NVMe connector (J16) reset signal.
171	GXBL1D_RX_CH5p	O, DIFF	Bank1D High speed positive differential receiver channel5. This pin is connected to B12 th pin of HPC FMC+ Connector (J8).
172	FPGA_AC17_LVDS2A_24p/ NANDWP	IO, 1.8V LVCMOS	This pin is connected to FPGA LED D1.
173	GND	Power	Ground.
174	GND	Power	Ground.
175	GXBL1D_RX_CH4n	O, DIFF	Bank1D High speed negative differential receiver channel4. This pin is connected to B17 th pin of HPC FMC+ Connector (J8).
176	FPGA_AH14_LVDS2A_14n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D16 th bit of HDMI transmitter chip.
177	GXBL1D_RX_CH4p	O, DIFF	Bank1D High speed positive differential receiver channel4. This pin is connected to B16 th pin of HPC FMC+ Connector (J8).
178	FPGA_AJ14_LVDS2A_14p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D15 th bit of HDMI transmitter chip.
179	GND	Power	Ground.
180	GND	Power	Ground.
181	GND	Power	Ground.
182	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
183	GXBL1E_TX_CH0p	I, DIFF	Bank1E High speed positive differential transmitter channel0. This pin is connected to B28 th pin of HPC FMC+ Connector (J8).
184	REFCLK_GXBL1E_CHTp	O, DIFF	Bank1E High speed differential reference clock positive receiver channel T. This pin is connected from Clock Synthesizer OUT9 positive.
185	GXBL1E_TX_CH0n	I, DIFF	Bank1E High speed negative differential transmitter channel0. This pin is connected to B29 th pin of HPC FMC+ Connector (J8).
186	REFCLK_GXBL1E_CHTn	O, DIFF	Bank1E High speed differential reference clock negative receiver channel T. This pin is connected from Clock Synthesizer OUT9 negative
187	GND	Power	Ground.
188	GND	Power	Ground.
189	GXBL1E_TX_CH1p	I, DIFF	Bank1E High speed positive differential transmitter channel1. This pin is connected to B24 th pin of HPC FMC+ Connector (J8).
190	FPGA_AD17_LVDS2A_24n/NANDLOCK	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D1 th pin of HPC FMC+ Connector (J8).
191	GXBL1E_TX_CH1n	I, DIFF	Bank1E High speed negative differential transmitter channel1. This pin is connected to B25 th pin of HPC FMC+ Connector (J8).
192	FPGA_AE19_LVDS2A_22n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D3 th bit of HDMI transmitter chip.
193	GND	Power	Ground.
194	FPGA_AF19_LVDS2A_22p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D2 th bit of HDMI transmitter chip.
195	GXBL1E_RX_CH1n	O, DIFF	Bank1E High speed negative differential receiver channel1. This pin is connected to B5 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
196	FPGA_AF18_LVDS2A_23p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D0 th bit of HDMI transmitter chip.
197	GXBL1E_RX_CH1p	O, DIFF	Bank1E High speed positive differential receiver channel1. This pin is connected to B4 th pin of HPC FMC+ Connector (J8).
198	FPGA_AG18_LVDS2A_23n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D1 th bit of HDMI transmitter chip.
199	GND	Power	Ground.
200	GND	Power	Ground.
201	GXBL1E_RX_CH0n	O, DIFF	Bank1E High speed negative differential receiver channel0. This pin is connected to B9 th pin of HPC FMC+ Connector (J8).
202	FPGA_AN17_LVDS2A_8n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D23 th bit of HDMI transmitter chip.
203	GXBL1E_RX_CH0p	O, DIFF	Bank1E High speed positive differential receiver channel0. This pin is connected to B8 th pin of HPC FMC+ Connector (J8).
204	FPGA_AM17_LVDS2A_8p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D22 th bit of HDMI transmitter chip.
205	GND	Power	Ground.
206	GND	Power	Ground.
207	FPGA_AP15_LVDS2A_3n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to 1 st pin of 6pin Pmod connector J15
208	FPGA_AP14_LVDS2A_6n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to Clock pin of HDMI transmitter chip.
209	FPGA_AN15_LVDS2A_3p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to L/R Audio Clock pin of HDMI transmitter chip.
210	FPGA_AN14_LVDS2A_6p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to Data Enable of HDMI transmitter chip.

Pin No	Signal Name	Signal Type/Termination	Description
211	FPGA_AM18_LVDS2A_7p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to HSYNC of HDMI transmitter chip.
212	FPGA_AL14_LVDS2A_9p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D20 th bit of HDMI transmitter chip.
213	FPGA_AN18_LVDS2A_7n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to VSYNC of HDMI transmitter chip.
214	FPGA_AK14_LVDS2A_9n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D21 th bit of HDMI transmitter chip.
215	GND	Power	Ground.
216	GND	Power	Ground.
217	GXBL1E_TX_CH2p	I, DIFF	Bank1E High speed positive differential transmitter channel2. This pin is connected to Z24 th pin of HPC FMC+ Connector (J8).
218	REFCLK_GXBL1E_CHBp	O, DIFF	Bank1E High speed differential reference clock positive receiver channel B. This pin is connected to L4 th pin of HPC FMC+ Connector (J8).
219	GXBL1E_TX_CH2n	I, DIFF	Bank1E High speed negative differential transmitter channel2. This pin is connected to Z25 th pin of HPC FMC+ Connector (J8).
220	REFCLK_GXBL1E_CHBn	O, DIFF	Bank1E High speed differential reference clock negative receiver channel B. This pin is connected to L5 th pin of HPC FMC+ Connector (J8).
221	GND	Power	Ground.
222	GND	Power	Ground.
223	GXBL1E_TX_CH3p	I, DIFF	Bank1E High speed positive differential transmitter channel3. This pin is connected to Y26 th pin of HPC FMC+ Connector (J8).
224	FPGA_AL15_LVDS2A_12n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D17 th bit of HDMI transmitter chip.

Pin No	Signal Name	Signal Type/Termination	Description
225	GXBL1E_TX_CH3n	I, DIFF	Bank1E High speed negative differential transmitter channel3. This pin is connected to Y27 th pin of HPC FMC+ Connector (J8).
226	FPGA_AK13_LVDS2A_1n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D8 th bit of HDMI transmitter chip.
227	GND	Power	Ground.
228	FPGA_AI13_LVDS2A_1p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to 4 th pin of 6pin Pmod connector J15
229	GXBL1E_RX_CH3n	O, DIFF	Bank1E High speed negative differential receiver channel3. This pin is connected to Z13 th pin of HPC FMC+ Connector (J8).
230	FPGA_AJ16_LVDS2A_18p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to D10th bit of HDMI transmitter chip.
231	GXBL1E_RX_CH3p	O, DIFF	Bank1E High speed positive differential receiver channel3. This pin is connected to Z12 th pin of HPC FMC+ Connector (J8).
232	NC	NA	NC.
233	GND	Power	Ground.
234	GND	Power	Ground.
235	GXBL1E_RX_CH2n	O, DIFF	Bank1E High speed negative differential receiver channel2. This pin is connected to Y11 th pin of HPC FMC+ Connector (J8).
236	FPGA_AM13_LVDS2A_4n	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to SCLK pin of HDMI transmitter chip.
237	GXBL1E_RX_CH2p	O, DIFF	Bank1E High speed positive differential receiver channel2. This pin is connected to Y10 th pin of HPC FMC+ Connector (J8).
238	FPGA_AN13_LVDS2A_4p	IO, 1.8V LVCMOS	Bank2A User I/O Single ended pin. This pin is connected to I2S1 pin of HDMI transmitter chip.
239	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
240	GND	Power	Ground.

2.4 Board to Board Connector2

This 240-pin Board to Board Connector2 is capable of handling high-speed signals. Also, this connector pulls out more interfaces of Arria10 CPU. This Board to Board Connector2 mating connector (J7) is physically located at the top of the board as shown below.

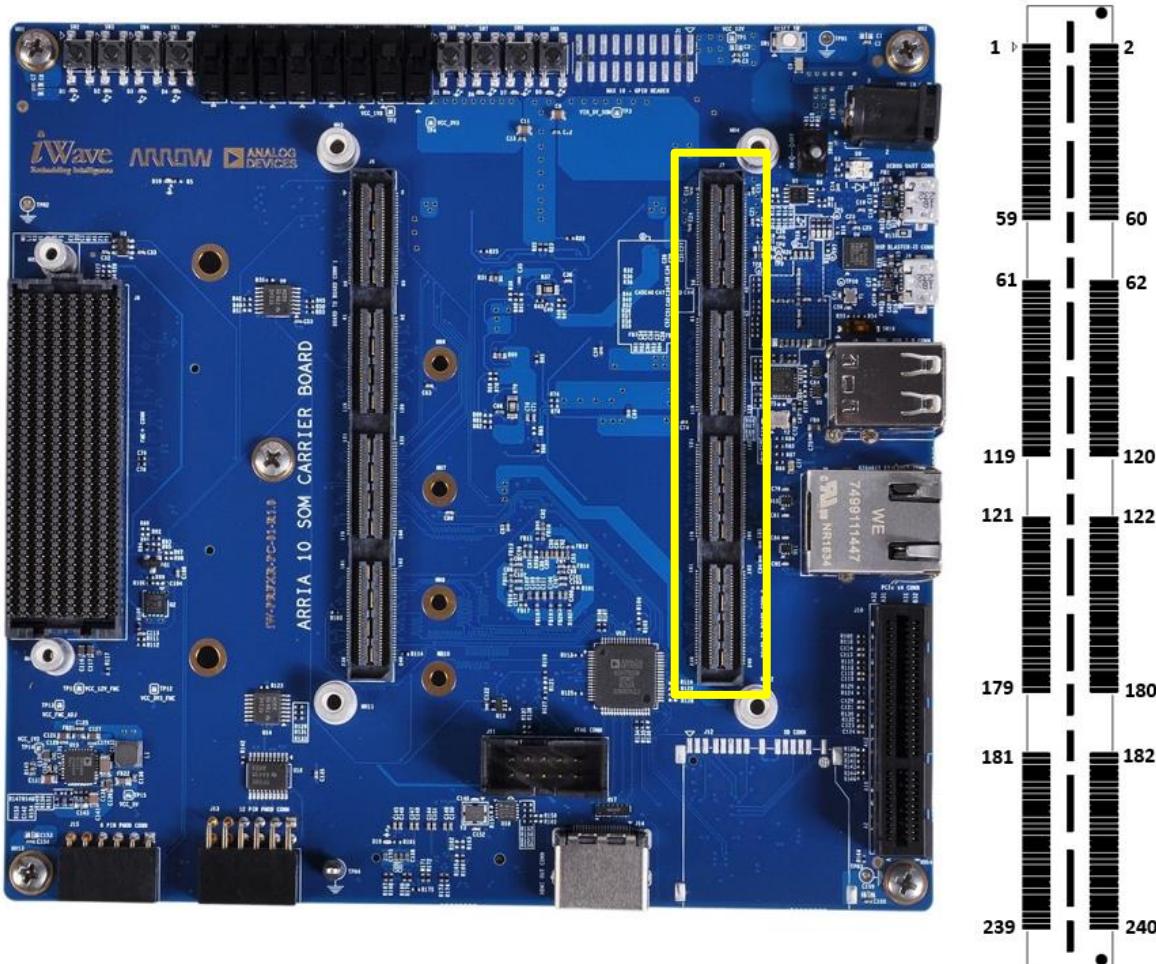


Figure 3 Expansion Connector2

Table 4 : Expansion Connector2 Pin Out

Pin No	Signal Name	Signal Type/Termination	Description
1	VCC	O, 5V Power	Supply Voltage.
2	VCC	O, 5V Power	Supply Voltage.
3	VCC	O, 5V Power	Supply Voltage.
4	VCC	O, 5V Power	Supply Voltage.
5	VCC	O, 5V Power	Supply Voltage.
6	VCC	O, 5V Power	Supply Voltage.
7	VCC	O, 5V Power	Supply Voltage.
8	VCC	O, 5V Power	Supply Voltage.
9	VCC	O, 5V Power	Supply Voltage.
10	VCC	O, 5V Power	Supply Voltage.
11	VCC	O, 5V Power	Supply Voltage.
12	VCC	O, 5V Power	Supply Voltage.
13	VCC	O, 5V Power	Supply Voltage.
14	VCC	O, 5V Power	Supply Voltage.
15	VCC	O, 5V Power	Supply Voltage.
16	VCC	O, 5V Power	Supply Voltage.
17	VCC	O, 5V Power	Supply Voltage.
18	VCC	O, 5V Power	Supply Voltage.
19	VCC	O, 5V Power	Supply Voltage.
20	VCC	O, 5V Power	Supply Voltage.
21	GND	O, 5V Power	Supply Voltage.
22	GND	O, 5V Power	Supply Voltage.
23	GND	O, 5V Power	Supply Voltage.
24	GND	O, 5V Power	Supply Voltage.
25	CSS_TRST	O, 1.8V CMOS/ 10K PU	Dedicated JTAG test reset input pin. This pin is Connected to on Board USB Blaster II, FMC+ and on board JTAG Header.
26	USB_OTG_DM	IO, DIFF	USB OTG Data Positive. This signal is connected to USBDM_UP pin of USB 2.0 Hi-Speed Hub Controller.
27	CSS_TDI	O, 1.8V CMOS/ 10K PU	Dedicated JTAG test data input pin. This signal is connected to on Board USB Blaster II, FMC+ and on board JTAG Header.
28	USB_OTG_DP	IO, DIFF	USB OTG Data Negative. This signal is connected to USBDP_UP pin of USB 2.0 Hi-Speed Hub Controller.

Pin No	Signal Name	Signal Type/Termination	Description
29	CSS_TMS	O, 1.8V CMOS/ 10K PU	Dedicated JTAG test Mode select input pin. This pin is connected to on Board USB Blaster II, FMC+ and on board JTAG Header.
30	GND	Power	Ground.
31	CSS_TCK	O, 1.8V CMOS	Dedicated JTAG test clock input pin. This signal is connected to on Board USB Blaster II, FMC+ and on board JTAG Header.
32	USB_PWR_EN	NA	NC
33	CSS_TDO	I, 1.8V CMOS	Dedicated JTAG test data output pin. This signal is connected to on Board USB Blaster II, FMC+ and on board JTAG Header.
34	USB_OTG_ID	O, 3.3V CMOS/ 1K PU	USB OTG ID input for USB host or device detection. This pin is permanently tied to Pullup 1.8V Level
35	HPS_GPIO3(GPIO0_IO1 1)	IO, 1.8V CMOS/ 1K PU	Warm reset input to HPS block. This pin is connected from Push Button SW1
36	VBUS_USB	O, Power 5V	USB VBUS Voltage pin. This pin is connected from 5V
37	GND	Power	Ground.
38	HPS_GPIO4(GPIO0_IO1 0)	IO, 1.8V CMOS	General Purpose Input/Output. This pin used as reset out from the Arria10 SoC
39	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative. This pin is connected to Ethernet connector (J9)
40	HPS_GPIO1/EMAC2_RX D1(GPIO1_IO19)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Push Button SW7.
41	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive. This pin is connected to Ethernet connector (J9)
42	HPS_GPIO/EMAC2_RXD 0(GPIO1_IO18)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Push Button SW8.
43	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
44	HPS_GPIO(GPIO0_IO11)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Push Button SW9.
45	GPHY_CTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative. This pin is connected to Ethernet connector (J9)
46	HPS_UART1_CTS_N/I2C0_SDA	IO, 1.8V CMOS/4.7K PU	I2C0 Data Signal. This signal is connected to HDMI transmitter chip, Clock Synthesizer and PCIx4 Connector.
47	GPHY_CTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive This pin is connected to Ethernet connector (J9)
48	HPS_UART1_RTS_N/I2C0_SCL	IO, 1.8V CMOS/4.7K PU	I2C0 Clock signal. This signal is connected to HDMI transmitter chip, Clock Synthesizer and PCIx4 Connector
49	GND	Power	Ground.
50	NC	NC	NC
51	GPHY_BTXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative. This pin is connected to Ethernet connector (J9)
52	NC	NC	NC
53	GPHY_BTXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 1 Positive. This pin is connected to Ethernet connector (J9)
54	HPS_UART0_TX	IO, 1.8V CMOS	Debug UART0 Transmit data line. This pin is connected to serial console for Debug console.
55	GND	Power	Ground.
56	HPS_UART0_RX	IO, 1.8V CMOS	Debug UART0 Receive data line. This pin is connected to serial console for Debug console.
57	GPHY_ATXRXM	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative. This pin is connected to Ethernet connector (J9)

Pin No	Signal Name	Signal Type/Termination	Description
58	GPHY_LINK_LED2	I, 3.3V CMOS/4.7K PD	Gigabit Ethernet link status LED. This pin is connected to Ethernet connector (J9)
59	GPHY_ATXRXP	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive. This pin is connected to Ethernet connector (J9)
60	GPHY_ACTIVITY_LED1	I, 3.3V CMOS/4.7K PU	Gigabit Ethernet activity status LED. This pin is connected to Ethernet connector (J9)
61	HPS_SPIM0_CLK/EMAC2_TXD2	IO, 1.8V CMOS	General Purpose Input/Output. This Pin is connected to HPS_LED D8
62	HPS_GPIO/SDMMC_DA TA3(GPIO1_IO17)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Slide Switch SW14
63	HPS_SPIM0_SS0_N/EMAC2_RXD3	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS LED D6
64	HPS_GPIO/SDMMC_DA TA2(GPIO1_IO16)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Slide Switch SW17
65	HPS_SPIM0_MOSI/EMAC2_TXD3	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Push Button SW6
66	HPS_GPIO/SDMMC_DA TA1(GPIO1_IO15)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Slide Switch SW16
67	HPS_SPIM0_MISO/EMAC2_RXD2	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected from Interrupt pin of HDMI transmitter chip.
68	HPS_GPIO/SDMMC_DA TA0(GPIO0_IO0)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS LED D5
69	HPS_I2C1_SDA/EMAC2_TX_CLK(GPIO1_IO12)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to C31 th pin of HPC FMC+ Connector (J8).
70	HPS_GPIO/SDMMC_CM D(GPIO0_IO1)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS LED D7
71	HPS_I2C1_SCL/EMAC2_TX_CTL(GPIO1_IO13)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to C30 th pin of HPC FMC+ Connector (J8).
72	HPS_GPIO/SDMMC_CCL K(GPIO1_IO14)	IO, 1.8V CMOS	General Purpose Input/Output. This pin is connected to HPS Slide Switch SW15

Pin No	Signal Name	Signal Type/Termination	Description
73	GND	Power	Ground.
74	GND	Power	Ground.
75	FPGA_AC10_LVDS3B_9n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel9. This pin is connected to G13 th pin of HPC FMC+ Connector (J8).
76	FPGA_AB8_LVDS3B_4p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel4. This pin is connected to H7 th pin of HPC FMC+ Connector (J8).
77	FPGA_AC9_LVDS3B_9p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel9. This pin is connected to G12 th pin of HPC FMC+ Connector (J8).
78	FPGA_AB7_LVDS3B_4n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel4. This pin is connected to H8 th pin of HPC FMC+ Connector (J8).
79	FPGA_AF6_LVDS3B_17n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel17. This pin is connected to H11 th pin of HPC FMC+ Connector (J8).
80	FPGA_AE7_LVDS3B_11n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel11. This pin is connected to D12 th pin of HPC FMC+ Connector (J8).
81	FPGA_AG6_LVDS3B_17p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel17. This pin is connected to H10 th pin of HPC FMC+ Connector (J8).
82	FPGA_AE6_LVDS3B_11p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel11. This pin is connected to D11 th pin of HPC FMC+ Connector (J8).
83	FPGA_AF5_LVDS3B_14n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel14. This pin is connected to D15 th pin of HPC FMC+ Connector (J8).
84	FPGA_AD6_LVDS3B_8n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel8. This pin is connected to G10 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
85	FPGA_AG5_LVDS3B_14p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel14. This pin is connected to D14 th pin of HPC FMC+ Connector (J8).
86	FPGA_AD5_LVDS3B_8p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel8 This pin is connected to G9 th pin of HPC FMC+ Connector (J8).
87	FPGA_AK4_LVDS3B_22p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel22. This pin is connected to H13 th pin of HPC FMC+ Connector (J8).
88	FPGA_AD7_LVDS3B_7p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel7. This pin is connected to G15 th pin of HPC FMC+ Connector (J8).
89	FPGA_AK3_LVDS3B_22n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel22. This pin is connected to H14 th pin of HPC FMC+ Connector (J8).
90	FPGA_AC7_LVDS3B_7n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel7. This pin is connected to G16 th pin of HPC FMC+ Connector (J8).
91	FPGA_AJ4_LVDS3B_21p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel21. This pin is connected to H16 th pin of HPC FMC+ Connector (J8).
92	FPGA_AH3_LVDS3B_18p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel18. This pin is connected to H19 th pin of HPC FMC+ Connector (J8).
93	FPGA_AH4_LVDS3B_21n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel21. This pin is connected to H17 th pin of HPC FMC+ Connector (J8).
94	FPGA_AG3_LVDS3B_18n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel18. This pin is connected to H20 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
95	FPGA_AL1_LVDS3B_24p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel24. This pin is connected to C10 th pin of HPC FMC+ Connector (J8).
96	FPGA_AG2_LVDS3B_19n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel19. This pin is connected to C19 th pin of HPC FMC+ Connector (J8).
97	FPGA_AK1_LVDS3B_24n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel24. This pin is connected to C11 th pin of HPC FMC+ Connector (J8).
98	FPGA_AG1_LVDS3B_19p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel19. This pin is connected to C18 th pin of HPC FMC+ Connector (J8).
99	FPGA_AK2_LVDS3B_23p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel23. This pin is connected to D17 th pin of HPC FMC+ Connector (J8).
100	FPGA_AE4_LVDS3B_3p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel3. This pin is connected to G21 th pin of HPC FMC+ Connector (J8).
101	FPGA_AJ2_LVDS3B_23n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel23. This pin is connected to D18 th pin of HPC FMC+ Connector (J8).
102	FPGA_AD4_LVDS3B_3n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel3. This pin is connected to G22 th pin of HPC FMC+ Connector (J8).
103	FPGA_AJ1_LVDS3B_20p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel20. This pin is connected to C14 th pin of HPC FMC+ Connector (J8).
104	FPGA_AF1_LVDS3B_16p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel16. This pin is connected to G18 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
105	FPGA_AH2_LVDS3B_20n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel20. This pin is connected to C15 th pin of HPC FMC+ Connector (J8).
106	FPGA_AE1_LVDS3B_16n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel18. This pin is connected to G19 th pin of HPC FMC+ Connector (J8).
107	GND	Power	Ground.
108	GND	Power	Ground.
109	FPGA_AD10_LVDS3B_12p/CLKIN_1p	IO, 1.8V LVDS	Bank3B Clock Input differential positive channel1. This pin is connected to G6 th pin of HPC FMC+ Connector (J8).
110	FPGA_AC8_LVDS3B_10p/CLKOUT_1p	IO, 1.8V LVDS	Bank3B Clock Output differential positive channel1. This pin is connected to C22 th pin of HPC FMC+ Connector (J8).
111	FPGA_AD11_LVDS3B_12n/CLKIN_1n	IO, 1.8V LVDS	Bank3B Clock Input differential negative channel1. This pin is connected to G7 th pin of HPC FMC+ Connector (J8).
112	FPGA_AD9_LVDS3B_10n/CLKOUT_1n	IO, 1.8V LVDS	Bank3B Clock Output differential negative channel1. This pin is connected to C23 th pin of HPC FMC+ Connector (J8).
113	GND	Power	Ground.
114	GND	Power	Ground.
115	FPGA_AF4_LVDS3B_15p/CLKOUT_0p	IO, 1.8V LVDS	Bank3B Clock Output differential positive channel0. This pin is connected to D8 th pin of HPC FMC+ Connector (J8).
116	FPGA_AE2_LVDS3B_13p/CLKIN_0p	IO, 1.8V LVDS	Bank3B Clock Input differential positive channel0. This pin is connected to D20 th pin of HPC FMC+ Connector (J8).
117	FPGA_AF3_LVDS3B_15n/CLKOUT_0n	IO, 1.8V LVDS	Bank3B Clock Output differential negative channel0. This pin is connected to D9 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
118	FPGA_AE3_LVDS3B_13n /CLKIN_0n	IO, 1.8V LVDS	Bank3B Clock Input differential negative channel0. This pin is connected to D21 th pin of HPC FMC+ Connector (J8).
119	GND	Power	Ground.
120	GND	Power	Ground.
121	FPGA_AB11_LVDS3B_1n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel1. This pin is connected to D24 th pin of HPC FMC+ Connector (J8).
122	FPGA_AD2_LVDS3B_2p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel2. This pin is connected to G24 th pin of HPC FMC+ Connector (J8).
123	FPGA_AB10_LVDS3B_1p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel1. This pin is connected to D23 th pin of HPC FMC+ Connector (J8).
124	FPGA_AD1_LVDS3B_2n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel2. This pin is connected to G25 th pin of HPC FMC+ Connector (J8).
125	FPGA_AB5_LVDS3B_5n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel5. This pin is connected to H26 th pin of HPC FMC+ Connector (J8).
126	FPGA_AC4_LVDS3B_6p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel6. This pin is connected to H22 th pin of HPC FMC+ Connector (J8).
127	FPGA_AB6_LVDS3B_5p	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential positive channel5. This pin is connected to H25 th pin of HPC FMC+ Connector (J8).
128	FPGA_AC5_LVDS3B_6n	IO, 1.8V LVDS	Bank3B LVDS receiver/transmitter differential negative channel6. This pin is connected to H23 th pin of HPC FMC+ Connector (J8).
129	GND	Power	Ground.
130	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
131	FPGA_AB1_LVDS3C_24p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel24. This pin is connected to J6 th pin of HPC FMC+ Connector (J8).
132	FPGA_AC3_LVDS3C_22p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel22. This pin is connected to E6 th pin of HPC FMC+ Connector (J8).
133	FPGA_AA1_LVDS3C_24n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel24. This pin is connected to J7 th pin of HPC FMC+ Connector (J8).
134	FPGA_AC2_LVDS3C_22n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel22. This pin is connected to E7 th pin of HPC FMC+ Connector (J8).
135	FPGA_AA3_LVDS3C_20p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel20. This pin is connected to K7 th pin of HPC FMC+ Connector (J8).
136	FPGA_AB2_LVDS3C_21p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel21. This pin is connected to G33 th pin of HPC FMC+ Connector (J8).
137	FPGA_AA4_LVDS3C_20n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel20. This pin is connected to K8 th pin of HPC FMC+ Connector (J8).
138	FPGA_AB3_LVDS3C_21n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel21. This pin is connected to G34 th pin of HPC FMC+ Connector (J8).
139	FPGA_Y1_LVDS3C_23p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel23. This pin is connected to F7 th pin of HPC FMC+ Connector (J8).
140	FPGA_AA8_LVDS3C_17p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel17. This pin is connected to K10 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
141	FPGA_Y2_LVDS3C_23n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel23. This pin is connected to F8 th pin of HPC FMC+ Connector (J8).
142	FPGA_AA9_LVDS3C_17n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel17. This pin is connected to K11 th pin of HPC FMC+ Connector (J8).
143	FPGA_V3_LVDS3C_9n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel9. This pin is connected to C27 th pin of HPC FMC+ Connector (J8).
144	FPGA_Y3_LVDS3C_19p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel19. This pin is connected to H34 th pin of HPC FMC+ Connector (J8).
145	FPGA_U3_LVDS3C_9p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel9. This pin is connected to C26 th pin of HPC FMC+ Connector (J8).
146	FPGA_Y4_LVDS3C_19n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel19. This pin is connected to H35 th pin of HPC FMC+ Connector (J8).
147	FPGA_V2_LVDS3C_11p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel11. This pin is connected to J9 th pin of HPC FMC+ Connector (J8).
148	FPGA_V5_LVDS3C_6p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel6. This pin is connected to H30 th pin of HPC FMC+ Connector (J8).
149	FPGA_U2_LVDS3C_11n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel11. This pin is connected to J10 th pin of HPC FMC+ Connector (J8).
150	FPGA_V4_LVDS3C_6n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel6. This pin is connected to H31 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
151	FPGA_U6_LVDS3C_5p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel5. This pin is connected to G27 th pin of HPC FMC+ Connector (J8).
152	FPGA_W6_LVDS3C_16p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel16. This pin is connected to G36 th pin of HPC FMC+ Connector (J8).
153	FPGA_U5_LVDS3C_5n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel5. This pin is connected to G28 th pin of HPC FMC+ Connector (J8).
154	FPGA_W7_LVDS3C_16n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel16. This pin is connected to G37 th pin of HPC FMC+ Connector (J8).
155	FPGA_T4_LVDS3C_1p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel1. This pin is connected to 1 st pin of 12pin Pmod connector J13
156	FPGA_Y8_LVDS3C_14p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel14. This pin is connected to H31 th pin of HPC FMC+ Connector (J8).
157	FPGA_R4_LVDS3C_1n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel1. This pin is connected to 2 nd pin of 12pin Pmod connector J13
158	FPGA_Y9_LVDS3C_14n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel14. This pin is connected to H32 th pin of HPC FMC+ Connector (J8).
159	FPGA_R1_LVDS3C_8p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel8. This pin is connected to H28 th pin of HPC FMC+ Connector (J8).
160	FPGA_R3_LVDS3C_3n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel3. This pin is connected to 8 th pin of 12pin Pmod connector J13

Pin No	Signal Name	Signal Type/Termination	Description
161	FPGA_P1_LVDS3C_8n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel8. This pin is connected to H29 th pin of HPC FMC+ Connector (J8).
162	FPGA_T3_LVDS3C_3p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel3. This pin is connected to 7 th pin of 12pin Pmod connector J13
163	FPGA_P2_LVDS3C_7p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel7. This pin is connected to D26 th pin of HPC FMC+ Connector (J8).
164	FPGA_P4_LVDS3C_2p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel2. This pin is connected to 9 th pin of 12pin Pmod connector J13.
165	FPGA_R2_LVDS3C_7n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel7. This pin is connected to D27 th pin of HPC FMC+ Connector (J8).
166	FPGA_P5_LVDS3C_2n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel2. This pin is connected to 10 th pin of 12pin Pmod connector J13.
167	GND	Power	Ground.
168	GND	Power	Ground.
169	FPGA_U1_LVDS3C_10p/ CLKOUT_1p	IO, 1.8V LVDS	Bank3C Clock Output differential positive channel10. This pin is connected to K4 th pin of HPC FMC+ Connector (J8).
170	FPGA_W4_LVDS3C_15p/ CLKOUT_0p	IO, 1.8V LVDS	Bank3C Clock Output differential positive channel15. This pin is connected to E2 th pin of HPC FMC+ Connector (J8).
171	FPGA_T1_LVDS3C_10n/ CLKOUT_1n	IO, 1.8V LVDS	Bank3C Clock Output differential negative channel10. This pin is connected to K5 th pin of HPC FMC+ Connector (J8).
172	FPGA_W5_LVDS3C_15n/ CLKOUT_0n	IO, 1.8V LVDS	Bank3C Clock Output differential negative channel15. This pin is connected to E3 th pin of HPC FMC+ Connector (J8).
173	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
174	GND	Power	Ground.
175	FPGA_W1_LVDS3C_12p /CLKIN_1p	IO, 1.8V LVDS	Bank3C Clock Input differential positive channel12. This pin is connected to F4 th pin of HPC FMC+ Connector (J8).
176	FPGA_Y6_LVDS3C_13p/ CLKIN_0p	IO, 1.8V LVDS	Bank3C Clock Input differential positive channel13. This pin is connected to G2 th pin of HPC FMC+ Connector (J8).
177	FPGA_W2_LVDS3C_12n /CLKIN_1n	IO, 1.8V LVDS	Bank3C Clock Input differential negative channel12. This pin is connected to F5 th pin of HPC FMC+ Connector (J8).
178	FPGA_Y7_LVDS3C_13n/ CLKIN_0n	IO, 1.8V LVDS	Bank3C Clock Input differential negative channel13. This pin is connected to G3 th pin of HPC FMC+ Connector (J8).
179	GND	Power	Ground.
180	GND	Power	Ground.
181	FPGA_T6_LVDS3C_4n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel4. This pin is connected to 4 th pin of 12pin Pmod connector J13.
182	FPGA_AA5_LVDS3C_18 p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel18. This pin is connected to H37 th pin of HPC FMC+ Connector (J8).
183	FPGA_T5_LVDS3C_4p	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential positive channel4. This pin is connected to 3 rd pin of 12pin Pmod connector J13.
184	FPGA_AA6_LVDS3C_18 n	IO, 1.8V LVDS	Bank3C LVDS receiver/transmitter differential negative channel18. This pin is connected to H38 th pin of HPC FMC+ Connector (J8).
185	GND	Power	Ground.
186	GND	Power	Ground.
187	GXBL1F_RX_CH0p	O, Diff	Bank1F High speed positive differential receiver channel0. This pin is connected to A25 th pin of PClex4 Connector1 (J10)

Pin No	Signal Name	Signal Type/Termination	Description
188	REFCLK_GXBL1F_CHTp	O, Diff	Bank1F High speed differential reference clock positive receiver channel T. This pin is connected from Clock Synthesizer OUT3 positive.
189	GXBL1F_RX_CH0n	O, Diff	Bank1F High speed negative differential receiver channel0. This pin is connected to A26 th pin of PClex4 Connector1 (J10)
190	REFCLK_GXBL1F_CHTn	O, Diff	Bank1F High speed differential reference clock negative receiver channel T. This pin is connected from Clock Synthesizer OUT3 negative.
191	GND	Power	Ground.
192	GND	Power	Ground.
193	GXBL1F_TX_CH0p	I, DIFF	Bank1F High speed positive differential transmitter channel0. This pin is connected to B23 th pin of PClex4 Connector1 (J10)
194	GXBL1F_RX_CH3p	O, DIFF	Bank1F High speed positive differential receiver channel3. This pin is connected to Z16 th pin of HPC FMC+ Connector (J8).
195	GXBL1F_TX_CH0n	I, DIFF	Bank1F High speed negative differential This pin is connected to B24 th pin of PClex4 Connector1 (J10)
196	GXBL1F_RX_CH3n	O, DIFF	Bank1F High speed negative differential receiver channel3. This pin is connected to Z17 th pin of HPC FMC+ Connector (J8).
197	GND	Power	Ground.
198	GND	Power	Ground.
199	GXBL1F_RX_CH1p	O, DIFF	Bank1F High speed positive differential receiver channel1. This pin is connected to A29 th pin of PClex4 Connector1 (J10)
200	GXBL1F_TX_CH3p	I, DIFF	Bank1F High speed positive differential transmitter channel3. This pin is connected to Y30 th pin of HPC FMC+ Connector (J8).

Pin No	Signal Name	Signal Type/Termination	Description
201	GXBL1F_RX_CH1n	O, DIFF	Bank1F High speed negative differential receiver channel1. This pin is connected to A30 th pin of PClex4 Connector1 (J10)
202	GXBL1F_TX_CH3n	I, DIFF	Bank1F High speed negative differential transmitter channel3. This pin is connected to Y31 th pin of HPC FMC+ Connector (J8).
203	GND	Power	Ground.
204	GND	Power	Ground.
205	GXBL1F_TX_CH1p	I, DIFF	Bank1F High speed positive differential transmitter channel1. This pin is connected to B27 th pin of PClex4 Connector1 (J10).
206	GXBL1F_RX_CH4p	O, DIFF	Bank1F High speed positive differential receiver channel4. This pin is connected to Y18 th pin of HPC FMC+ Connector (J8).
207	GXBL1F_TX_CH1n	I, DIFF	Bank1F High speed negative differential transmitter channel1. This pin is connected to B28 th pin of PClex4 Connector1 (J10).
208	GXBL1F_RX_CH4n	O, DIFF	Bank1F High speed negative differential receiver channel4. This pin is connected to Y19 th pin of HPC FMC+ Connector (J8).
209	GND	Power	Ground.
210	GND	Power	Ground.
211	GXBL1F_RX_CH2p	O, DIFF	Bank1F High speed positive differential receiver channel2. This pin is connected to Y14 th pin of HPC FMC+ Connector (J8).
212	GXBL1F_TX_CH4p	I, DIFF	Bank1F High speed positive differential transmitter channel4. This pin is connected to M18 th pin of HPC FMC+ Connector (J8).
213	GXBL1F_RX_CH2n	O, DIFF	Bank1F High speed negative differential receiver channel2. This pin is connected to Y15 th pin of HPC FMC+ Connector (J8).
214	GXBL1F_TX_CH4n	I, DIFF	Bank1F High speed negative differential transmitter channel4. This pin is connected to M19 th pin of HPC FMC+ Connector (J8).
215	GND	Power	Ground.
216	GND	Power	Ground.

Pin No	Signal Name	Signal Type/Termination	Description
217	GXBL1F_TX_CH2p	I, DIFF	Bank1F High speed positive differential transmitter channel2. This pin is connected to Z28 th pin of HPC FMC+ Connector (J8).
218	GXBL1F_RX_CH5p	O, DIFF	Bank1F High speed positive differential receiver channel5. This pin is connected to Y22 th pin of HPC FMC+ Connector (J8).
219	GXBL1F_TX_CH2n	I, DIFF	Bank1F High speed negative differential transmitter channel2. This pin is connected to Z29 th pin of HPC FMC+ Connector (J8).
220	GXBL1F_RX_CH5n	O, DIFF	Bank1F High speed negative differential receiver channel5. This pin is connected to Y23 th pin of HPC FMC+ Connector (J8).
221	GND	Power	Ground.
222	GND	Power	Ground.
223	REFCLK_GXBL1F_CHBp	O, DIFF	Bank1F High speed differential reference clock positive receiver channel B. This pin is connected to L8 th pin of HPC FMC+ Connector (J8).
224	GXBL1F_TX_CH5p	I, DIFF	Bank1F High speed positive differential transmitter channel5. This pin is connected to M22 th pin of HPC FMC+ Connector (J8).
225	REFCLK_GXBL1F_CHBn	O, DIFF	Bank1F High speed differential reference clock negative receiver channel B. This pin is connected to L9 th pin of HPC FMC+ Connector (J8).
226	GXBL1F_TX_CH5n	I, DIFF	Bank1F High speed negative differential transmitter channel5. This pin is connected to M23 th pin of HPC FMC+ Connector (J8).
227	GND	Power	Ground.
228	GND	Power	Ground.
229	GXBL1E_RX_CH4p	O, DIFF	Bank1E High speed positive differential receiver channel4. This pin is connected to A16 th pin of PClex4 Connector1 (J10)

Pin No	Signal Name	Signal Type/Termination	Description
230	GXBL1E_RX_CH5p	O, DIFF	Bank1E High speed positive differential receiver channel5. This pin is connected to A21 th pin of PClex4 Connector1 (J10)
231	GXBL1E_RX_CH4n	O, DIFF	Bank1E High speed negative differential receiver channel4. This pin is connected to A17 th pin of PClex4 Connector1 (J10)
232	GXBL1E_RX_CH5n	O, DIFF	Bank1E High speed negative differential receiver channel5. This pin is connected to A22 th pin of PClex4 Connector1 (J10)
233	GND	Power	Ground.
234	GND	Power	Ground.
235	GXBL1E_TX_CH4p	I, DIFF	Bank1E High speed positive differential transmitter channel4. This pin is connected to B14 th pin of PClex4 Connector1 (J10)
236	GXBL1E_TX_CH5p	I, DIFF	Bank1E High speed positive differential transmitter channel5. This pin is connected to B19 th pin of PClex4 Connector1 (J10)
237	GXBL1E_TX_CH4n	I, DIFF	Bank1E High speed negative differential transmitter channel4. This pin is connected to B15 th pin of PClex4 Connector1 (J10)
238	GXBL1E_TX_CH5n	I, DIFF	Bank1E High speed negative differential transmitter channel5. This pin is connected to B20 th pin of PClex4 Connector1 (J10)
239	GND	Power	Ground.
240	GND	Power	Ground.

2.5 Serial Interface Features

2.5.1 Debug UART

The Arria10 SoC/FPGA custom carrier board supports debug interface through Arria10 CPU's UART0 interface. This UART0 signals from expansion connector2 is connected to UART to USB Convertor "FT232RQ-REEL" and to USB Micro AB Connector (J3). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

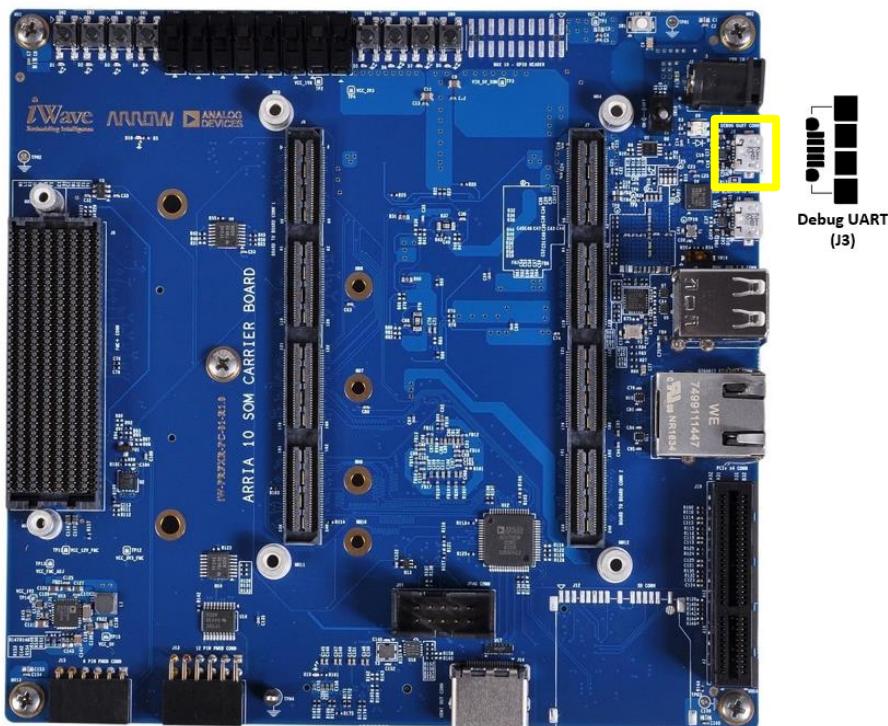


Figure 4: Debug UART

2.6 Communication Features

2.6.1 Gigabit Ethernet Port

The Arria10 SoC/FPGA custom carrier board supports 10/100/1000Mbps Ethernet interface through HPS EMAC1 interface of Arria10 SoC & KSZ9031RNXCA EthernetPhy. Ethernet PHY output signals from Expansion connector2 is directly connected to RJ45 Magjack (J9). The Ethernet supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack connector. This RJ45 Magjack connector (J9) is physically located at the top of the board as shown below.

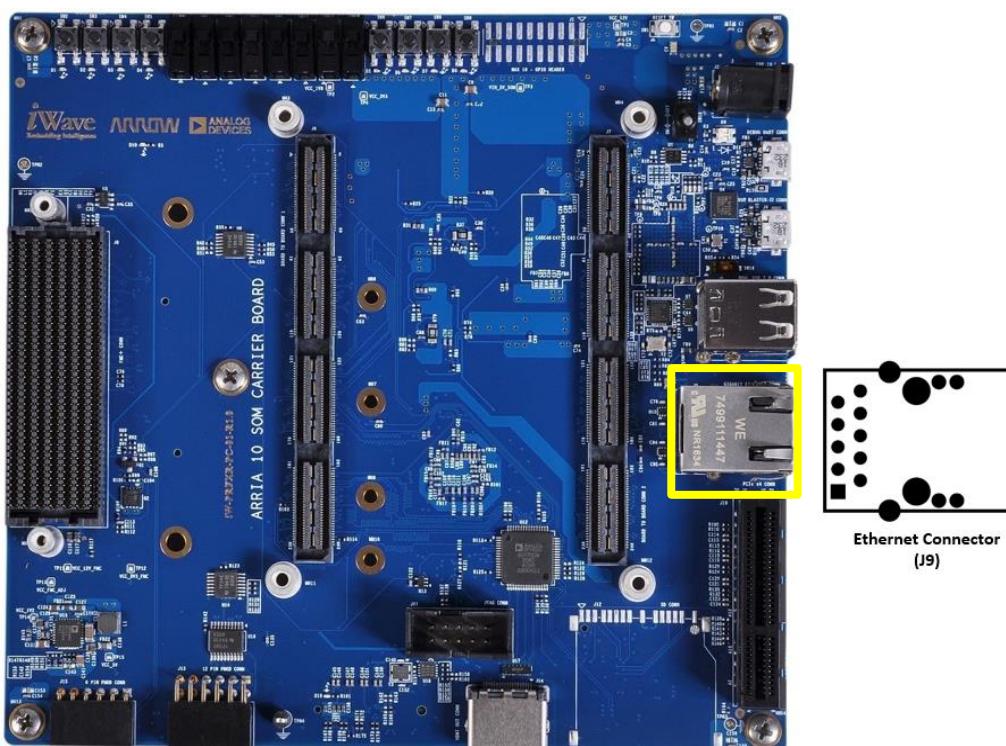


Figure 5: Gigabit Ethernet Connector

2.6.2 Dual Stack USB 2.0 Host Port

The Arria10 SoC/FPGA custom carrier board supports two host interfaces through Arria10 CPU's HPS USB1 interface. HPS USB1 interface signals from Expansion connector2 is connected to 2port USB HUB "USB2422/MJ" to support two USB 2.0 high speed host ports in the carrier board. This Dual Stack USB 2.0 OTG Host connector (J5) is physically located at the top of the board as shown below.

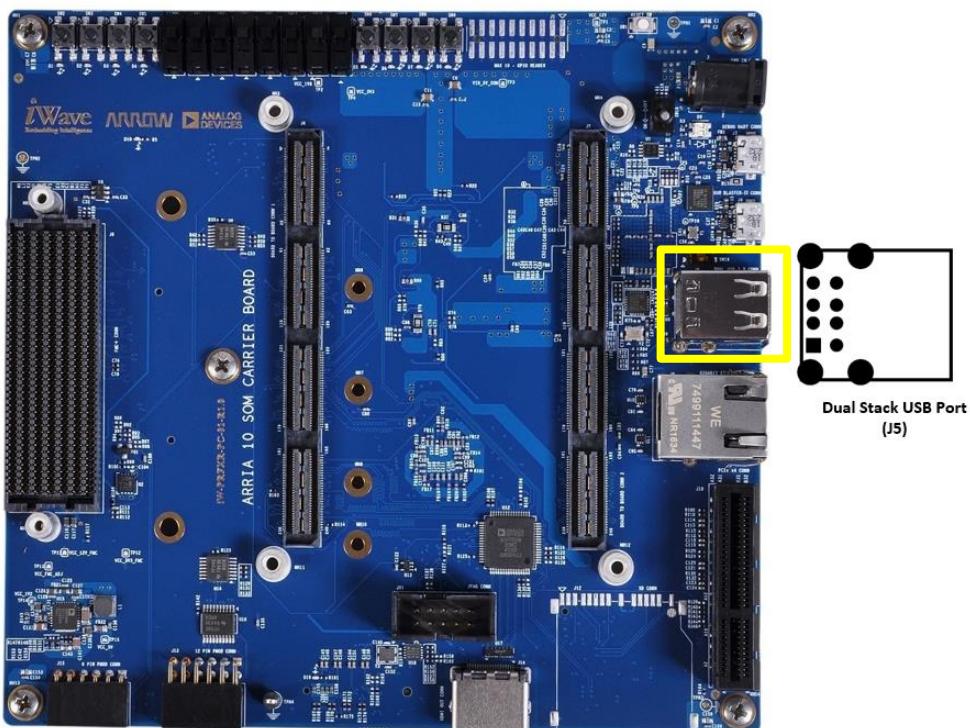


Figure 6: USB OTG Connector

2.6.3 On-board USB Blaster-II Port

The Arria10 SoC/FPGA custom carrier board supports on-board USB Blaster II Interface through JTAG interface of Arria10 SoC for FPGA programming. This JTAG signals from Expansion Connector2 is connected to MAX10 FPGA. The MAX10 device is interfaced to USB 2.0 Microcontroller host CY7C68013A through FX2 interface. Then, USB 2.0 Microcontroller is connected to USB Micro AB connector for programming the Arria10 SoC/FPGA through the host PC using the Micro AB OTG cable. This USB Micro AB connector (J4) is physically located at the top of the board as shown below.

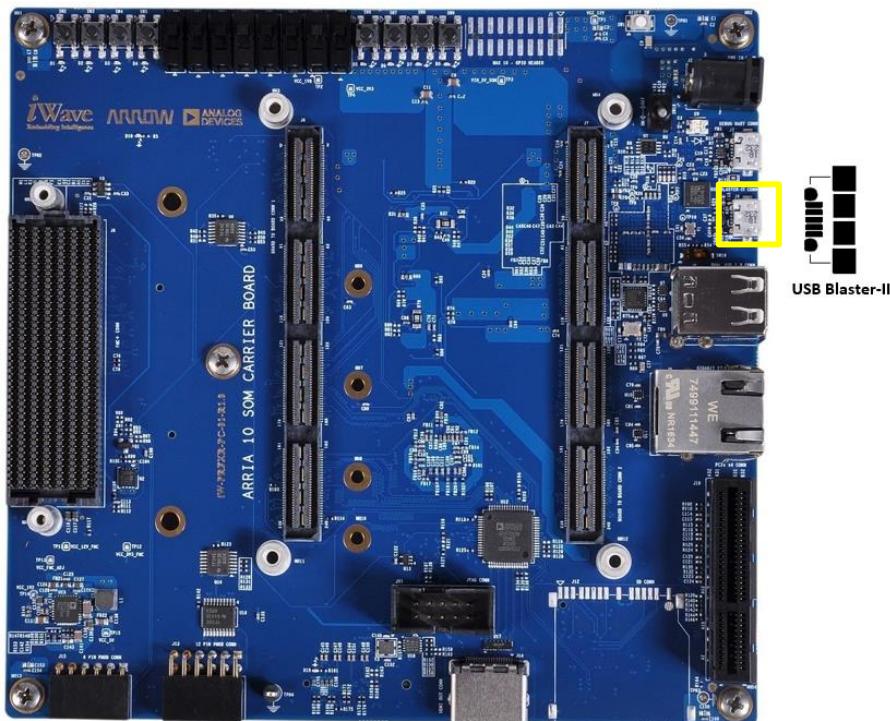


Figure 7: On-Board USB Blaster-II Mirco AB USB connector

2.7 Expansion Connectors

2.7.1 FMC+ Connector

The Arria10 SoC/FPGA custom carrier board supports one 560Pin VITA 57.4 FMC+ HPC connector for FPGA IOs expansion. This 560Pin FMC+ HPC connector (J8) is physically located at the top of the board as shown below.

This FMC+ connector supports

- Up to 16 Transceivers from BANK 1C, BANK 1D, BANK 1E, BANK 1F (each supports 6 Transceivers)
- Up to 42 LVDS IOs from BANK 3B, BANK 3C
- Up to 28 Single Ended (SE) IOs from BANK3A, BANK2A

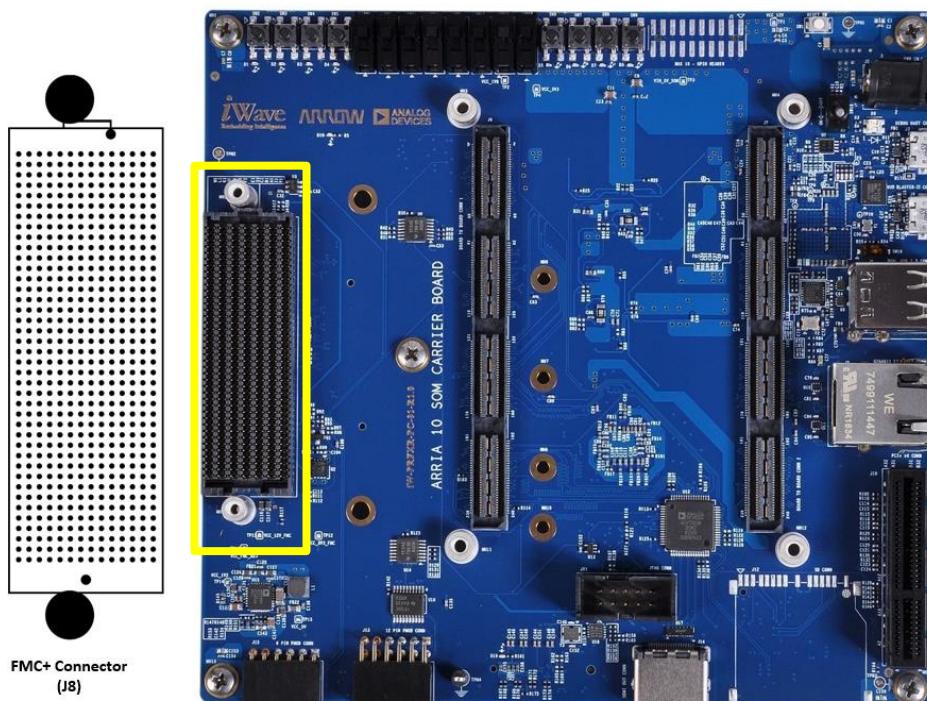


Figure 8: FMC+ HPC Connector

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNTR_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	DP8_M2C_N	GND	DP20_C2N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	DP7_M2C_N	GND	DP11_M2C_N	GND	DP11_M2C_N
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	DP6_M2C_P	GND	DP13_M2C_P	GND	DP13_M2C_N
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP12_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	LA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P	
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	DP9_C2M_N	GND	DP10_C2M_N	GND	DP10_C2M_N
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	GND	DP2_C2M_N	GND	DP11_C2M_N	
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	DP8_C2M_P	GND	DP12_C2M_P	GND	
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	GND	DP6_C2M_N	GND	DP18_M2C_N
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

Figure 9: FMC++ HPC Connector Pin Out

Table 5: FMC+ HPC Connector Pin Out

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	GXBL1C_RX_CH1P	O, DIFF	Bank1C High speed positive differential receiver channel1. This Pin is connected to 17 th pin of Board to Board Connector1 (J6).
A3	DP1_M2C_N	GXBL1C_RX_CH1N	O, DIFF	Bank1C High speed negative differential receiver channel1. This Pin is connected to 15 th pin of Board to Board Connector1 (J6).
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	GXBL1C_RX_CH2P	O, DIFF	Bank1C High speed negative differential receiver channel2. This Pin is connected to 57 th pin of Board to Board Connector1 (J6).
A7	DP2_M2C_N	GXBL1C_RX_CH2N	O, DIFF	Bank1C High speed negative differential receiver channel1. This Pin is connected to 55 th pin of Board to Board Connector1 (J6).
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	GXBL1C_RX_CH3P	O, DIFF	Bank1C High speed positive differential receiver channel3. This Pin is connected to 51 th pin of Board to Board Connector1 (J6).
A11	DP3_M2C_N	GXBL1C_RX_CH3N	O, DIFF	Bank1C High speed negative differential receiver channel3. This Pin is connected to 49 th pin of Board to Board Connector1 (J6).
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	GXBL1D_RX_CH2P	O, DIFF	Bank1D High speed positive differential receiver channel2. This Pin is connected to 143 th pin of Board to Board Connector1 (J6).
A15	DP4_M2C_N	GXBL1D_RX_CH2N	O, DIFF	Bank1D High speed negative differential receiver channel2. This Pin is connected to 141 th pin of Board to Board Connector1 (J6).
A16	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	GXBL1D_RX_CH3P	O, DIFF	Bank1D High speed positive differential receiver channel3. This Pin is connected to 137 th pin of Board to Board Connector1 (J6).
A19	DP5_M2C_N	GXBL1D_RX_CH3N	O, DIFF	Bank1D High speed negative differential receiver channel3. This Pin is connected to 135 th pin of Board to Board Connector1 (J6).
A20	GND	GND	Power	
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	GXBL1C_TX_CH1P	I, DIFF	Bank1C High speed positive differential Transmitter channel3. This Pin is connected to 9 th pin of Board to Board Connector1 (J6).
A23	DP1_C2M_N	GXBL1C_TX_CH1N	I, DIFF	Bank1C High speed negative differential Transmitter channel1. This Pin is connected to 11 th pin of Board to Board Connector1 (J6).
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	GXBL1C_TX_CH2P	I, DIFF	Bank1C High speed positive differential Transmitter channel2. This Pin is connected to 37 th pin of Board to Board Connector1 (J6).
A27	DP2_C2M_N	GXBL1C_TX_CH2N	I, DIFF	Bank1C High speed negative differential Transmitter channel2. This Pin is connected to 39 th pin of Board to Board Connector1 (J6).
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	GXBL1C_TX_CH3P	I, DIFF	Bank1C High speed positive differential Transmitter channel3. This Pin is connected to 43 th pin of Board to Board Connector1 (J6).
A31	DP3_C2M_N	GXBL1C_TX_CH3N	I, DIFF	Bank1C High speed negative differential Transmitter channel3. This Pin is connected to 45 th pin of Board to Board Connector1 (J6).
A32	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	GXBL1D_TX_CH2P	I, DIFF	Bank1D High speed positive differential Transmitter channel2. This Pin is connected to 123 th pin of Board to Board Connector1 (J6).
A35	DP4_C2M_N	GXBL1D_TX_CH2N	I, DIFF	Bank1C High speed negative differential Transmitter channel2. This Pin is connected to 125 th pin of Board to Board Connector1 (J6).
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	GXBL1D_TX_CH3P	I, DIFF	Bank1D High speed positive differential Transmitter channel3. This Pin is connected to 129 th pin of Board to Board Connector1 (J6).
A39	DP5_C2M_N	GXBL1D_TX_CH3N	I, DIFF	Bank1D High speed negative differential Transmitter channel3. This Pin is connected to 131 th pin of Board to Board Connector1 (J6).
A40	GND	GND	Power	Ground.
B1	RES1	CLK_DIR	NA	NC.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	GXBL1E_RX_CH1P	NA	Bank1E High speed positive differential receiver channel1. This Pin is connected to 197 th pin of Board to Board Connector1 (J6).
B5	DP9_M2C_N	GXBL1E_RX_CH1N	NA	Bank1E High speed negative differential receiver channel4. This Pin is connected to 195 th pin of Board to Board Connector1 (J6).
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	GXBL1E_RX_CH0P	NA	Bank1E High speed positive differential receiver channel0. This Pin is connected to 203 th pin of Board to Board Connector1 (J6).

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
B9	DP8_M2C_N	GXBL1E_RX_CH0N	NA	Bank1E High speed negative differential receiver channel0. This Pin is connected to 201 th pin of Board to Board Connector1 (J6).
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	GXBL1D_RX_CH5P	O, DIFF	Bank1D High speed positive differential receiver channel5. This Pin is connected to 171 th pin of Board to Board Connector1 (J6).
B13	DP7_M2C_N	GXBL1D_RX_CH5N	O, DIFF	Bank1D High speed negative differential receiver channel5. This Pin is connected to 169 th pin of Board to Board Connector1 (J6).
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	GXBL1D_RX_CH4P	O, DIFF	Bank1D High speed positive differential receiver channel4. This Pin is connected to 177 th pin of Board to Board Connector1 (J6).
B17	DP6_M2C_N	GXBL1D_RX_CH4N	O, DIFF	Bank1D High speed negative differential receiver channel4. This Pin is connected to 175 th pin of Board to Board Connector1 (J6).
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	REFCLK_GXBL1D_CH_Bp	O, DIFF	Bank1D High speed positive differential receiver Clock. This Pin is connected to 158 th pin of Board to Board Connector1 (J6).
B21	GBTCLK1_M2C_N	REFCLK_GXBL1D_CH_Bn	O, DIFF	Bank1D High speed negative differential receiver Clock. This Pin is connected to 160 th pin of Board to Board Connector1 (J6).
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	GXBL1E_TX_CH1P	NA	Bank1E High speed positive differential transmitter channel1. This Pin is connected to 189 th pin of Board to Board Connector1 (J6).

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
B25	DP9_C2M_N	GXBL1E_TX_CH1N	NA	Bank1E High speed negative differential transmitter channel1. This Pin is connected to 191 th pin of Board to Board Connector1 (J6).
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	GXBL1E_TX_CH0P	NA	Bank1E High speed positive differential transmitter channel0. This Pin is connected to 183 th pin of Board to Board Connector1 (J6).
B29	DP8_C2M_N	GXBL1E_TX_CH0N	NA	Bank1E High speed negative differential transmitter channel0. This Pin is connected to 185 th pin of Board to Board Connector1 (J6).
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	GXBL1D_TX_CH5P	I, DIFF	Bank1D High speed positive differential transmitter channel5. This Pin is connected to 163 th pin of Board to Board Connector1 (J6).
B33	DP7_C2M_N	GXBL1D_TX_CH5N	I, DIFF	Bank1D High speed negative differential transmitter channel5. This Pin is connected to 165 th pin of Board to Board Connector1 (J6).
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	GXBL1D_TX_CH4P	I, DIFF	Bank1D High speed positive differential transmitter channel4. This Pin is connected to 157 th pin of Board to Board Connector1 (J6).
B37	DP6_C2M_N	GXBL1D_TX_CH4N	I, DIFF	Bank1D High speed negative differential transmitter channel4. This Pin is connected to 159 th pin of Board to Board Connector1 (J6).
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NC	NA	NC.
C1	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
C2	DPO_C2M_P	GXBL1C_TX_CH0P	I, DIFF	Bank1D High speed positive differential transmitter channel0. This Pin is connected to 3 rd pin of Board to Board Connector1 (J6).
C3	DPO_C2M_N	GXBL1C_TX_CH0N	I, DIFF	Bank1D High speed negative differential transmitter channel0. This Pin is connected to 5 th pin of Board to Board Connector1 (J6).
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DPO_M2C_P	GXBL1C_RX_CH0P	O, DIFF	Bank1C High speed positive differential receiver channel0. This Pin is connected to 23 rd pin of Board to Board Connector1 (J6).
C7	DPO_M2C_N	GXBL1C_RX_CH0N	O, DIFF	Bank1C High speed negative differential receiver channel0. This Pin is connected to 21 th pin of Board to Board Connector1 (J6).
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	FPGA_AL1_LVDS3B_24P_IO1	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel24. This Pin is connected to 95 th pin of Board to Board Connector2 (J7).
C11	LA06_N	FPGA_AK1_LVDS3B_24N_IO2	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel24. This Pin is connected to 97 st pin of Board to Board Connector2 (J7).
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	FPGA_AJ1_LVDS3B_20P_IO9	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel20. This Pin is connected to 103 th pin of Board to Board Connector2 (J7).
C15	LA10_N	FPGA_AH2_LVDS3B_20N_IO10	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel20. This Pin is connected to 105 th pin of Board to Board Connector2 (J7).
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
C18	LA14_P	FPGA_AG1_LVDS3B_19P_IO11	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel19. This Pin is connected to 98 th pin of Board to Board Connector2 (J7).
C19	LA14_N	FPGA_AG2_LVDS3B_19N_IO12	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel19. This Pin is connected to 96 th pin of Board to Board Connector2 (J7).
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	FPGA_AC8_LVDS3B_10P/CLKOUT_1P	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel10. This Pin is connected to 110 th pin of Board to Board Connector2 (J7).
C23	LA18_N_CC	FPGA_AD9_LVDS3B_10N/CLKOUT_1N	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel10. This Pin is connected to 112 nd pin of Board to Board Connector2 (J7).
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	FPGA_U3_LVDS3C_9P_IO30	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential positive channel9. This Pin is connected to 145 th pin of Board to Board Connector2 (J7).
C27	LA27_N	FPGA_V3_LVDS3C_9N_IO31	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential negative channel9. This Pin is connected to 143 th pin of Board to Board Connector2 (J7).
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	FMC+_SCL	IO, 3.3V LVCMOS	HPC FMC+ I2C Clock Signal.
C31	SDA	FMC+_SDA	IO, 3.3V LVCMOS	HPC FMC+ I2C Data Signal.
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	GA0	1K, PU	MSB of EEPROM I2C Address
C35	12P0V	VCC_12V_FMC+	O, 12V Power	Supply Voltage.
C36	GND	GND	Power	Ground.
C37	12P0V	VCC_12V_FMC+	O, 12V Power	Supply Voltage.
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3_FMC+	O, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
D1	PG_C2M	PG_C2M	I, 3.3V	Power Good Signal from Carrier to FMC+ Module. This Pin is connected to 190 th pin of Board to Board Connector2 (J6).
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	GBTCLK0_M2C_P	REFCLK_GXBL1C_CH_Bp	O, DIFF	GXBL1C High speed differential reference clock positive receiver channel0. This Pin is connected to 64 st pin of Board to Board Connector1 (J6).
D5	GBTCLK0_M2C_N	REFCLK_GXBL1C_CH_Bn	O, DIFF	GXBL1C High speed differential reference clock negative receiver channel0. This Pin is connected to 66 th pin of Board to Board Connector1 (J6).
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	FPGA_AF4_LVDS3B_15P/CLKOUT_OP	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel15. This Pin is connected to 115 th pin of Board to Board Connector2 (J7).
D9	LA01_N_CC	FPGA_AF3_LVDS3B_15N/CLKOUT_ON	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel15. This Pin is connected to 117 th pin of Board to Board Connector2 (J7).
D10	GND	GND	Power	Ground.
D11	LA05_P	FPGA_AE6_LVDS3B_11P_IO27	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel11. This Pin is connected to 82 th pin of Board to Board Connector2 (J7).
D12	LA05_N	FPGA_AE7_LVDS3B_11N_IO28	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel11. This Pin is connected to 80 th pin of Board to Board Connector2 (J7).
D13	GND	GND	Power	Ground.
D14	LA09_P	FPGA_AG5_LVDS3B_14P_IO21	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel14. This Pin is connected to 85 th pin of Board to Board Connector2 (J7).

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
D15	LA09_N	FPGA_AF5_LVDS3B_14N_IO22	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel14. This Pin is connected to 83 th pin of Board to Board Connector2 (J7).
D16	GND	GND	Power	Ground.
D17	LA13_P	FPGA_AK2_LVDS3B_23P_IO3	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel23. This Pin is connected to 99 th pin of Board to Board Connector2 (J7).
D18	LA13_N	FPGA_AJ2_LVDS3B_23N_IO4	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel23. This Pin is connected to 101 th pin of Board to Board Connector2 (J7).
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	FPGA_AE2_LVDS3B_13P/CLKIN_OP	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel13. This Pin is connected to 116 th pin of Board to Board Connector2 (J7).
D21	LA17_N_CC	FPGA_AE3_LVDS3B_13N/CLKIN_ON	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel13. This Pin is connected to 118 th pin of Board to Board Connector2 (J7).
D22	GND	GND	Power	Ground.
D23	LA23_P	FPGA_AB10_LVDS3B_1P_IO47	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel1. This Pin is connected to 123 th pin of Board to Board Connector2 (J7).
D24	LA23_N	FPGA_AB11_LVDS3B_1N_IO48	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel1. This Pin is connected to 121 th pin of Board to Board Connector2 (J7).
D25	GND	GND	Power	Ground.
D26	LA26_P	FPGA_P2_LVDS3C_7P_IO34	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel7. This Pin is connected to 163 th pin of Board to Board Connector2 (J7).
D27	LA26_N	FPGA_R2_LVDS3C_7N_IO35	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel7. This Pin is connected to 165 th pin of Board to Board Connector2 (J7).
D28	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
D29	TCK	CSS_TCK	I, 3.3V LVCMOS	JTAG Test clock. This Pin is connected to 31 th pin of Board to Board Connector2 (J7).
D30	TDI	FMC+_JTAG_TDI	I, 3.3V LVCMOS	JTAG Test Input. This pin connected to FMC+_JTAG_TDO for JTAG chain feature. This pin is connected to 33th. pin of Board to Board Connector2 (J7).
D31	TDO	FMC+_JTAG_TDO	O, 3.3V LVCMOS	JTAG Test output This pin connected to FMC+_JTAG_TDI for JTAG chain feature.
D32	3P3VAUX	3V3_AUX	O, 3.3V Power	Supply Voltage.
D33	TMS	B_CSS_TMS	I, 3.3V LVCMOS	JTAG Test Mode Select This pin is connected to 29th. pin of Board to Board Connector2 (J7).
D34	TRST_L	B_CSS_TRST	I, 3.3V LVCMOS	JTAG Reset This pin is connected to 25th. pin of Board to Board Connector2 (J7).
D35	GA1	GA1	1K, PD	MSB of EEPROM I2C Address
D36	3P3V	VCC_3V3_FMC+	O, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3_FMC+	O, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3_FMC+	O, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	FPGA_W4_LVDS3C_15P/CLKOUT_OP	NA	LVDS3C LVDS receiver/transmitter differential Positive channel15. This Pin is connected to 170 th pin of Board to Board Connector2 (J7).
E3	HA01_N_CC	FPGA_W5_LVDS3C_15N/CLKOUT_ON	NA	LVDS3C LVDS receiver/transmitter differential negative channel15. This Pin is connected to 172 th pin of Board to Board Connector2 (J7).
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
E6	HA05_P	FPGA_AC3_LVDS3C_22P_IO5	NA	LVDS3C LVDS receiver/transmitter differential Positive channel22. This Pin is connected to 132 th pin of Board to Board Connector2 (J7).
E7	HA05_N	FPGA_AC2_LVDS3C_22N_IO6	NA	LVDS3C LVDS receiver/transmitter differential negative channel22. This Pin is connected to 134 th pin of Board to Board Connector2 (J7).
E8	GND	GND	Power	Ground.
E9	HA09_P	FPGA_AM6_LVDS3A_17P_IO12	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 27 th pin of Board to Board Connector1 (J6).
E10	HA09_N	FPGA_AM5_LVDS3A_17N_IO13	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 29 th pin of Board to Board Connector1 (J6).
E11	GND	GND	Power	Ground.
E12	HA13_P	FPGA_AP4_LVDS3A_18P_IO10	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 16 th pin of Board to Board Connector1 (J6).
E13	HA13_N	FPGA_AN4_LVDS3A_18N_IO11	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 18 th pin of Board to Board Connector1 (J6).
E14	GND	GND	Power	Ground.
E15	HA16_P	FPGA_AN8_LVDS3A_21P_IO46	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 74 th pin of Board to Board Connector1 (J6).
E16	HA16_N	FPGA_AM8_LVDS3A_21N_IO47	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 76 th pin of Board to Board Connector1 (J6).
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC.
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.
E39	VADJ	VCC_FMC+_ADJ	O, 1.8V Power	Supply Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	PG_M2C	O,3.3V/ 10K PU	Power Good Signal from FMC+ Module to Carrier. This pin is connected 10K PD in the carrier board.
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	FPGA_W1_LVDS3C_12P/CLKIN_1P	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential Positive channel12. This Pin is connected to 175 th pin of Board to Board Connector2 (J7).
F5	HA00_N_CC	FPGA_W2_LVDS3C_12N/CLKIN_1N	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential Negative channel12. This Pin is connected to 177 th pin of Board to Board Connector2 (J7).
F6	GND	GND	Power	Ground.
F7	HA04_P	FPGA_Y1_LVDS3C_23P_IO3	NA	LVDS3C LVDS receiver/transmitter differential Positive channel23. This Pin is connected to 139 th pin of Board to Board Connector2 (J7).
F8	HA04_N	FPGA_Y2_LVDS3C_23N_IO4	NA	LVDS3C LVDS receiver/transmitter differential Negative channel23. This Pin is connected to 141 th pin of Board to Board Connector2 (J7).
F9	GND	GND	Power	Ground.
F10	HA08_P	FPGA_AP5_LVDS3A_19P_IO8	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 31 th pin of Board to Board Connector1 (J6).
F11	HA08_N	FPGA_AN5_LVDS3A_19N_IO9	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 33 th pin of

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
				Board to Board Connector1 (J6).
F12	GND	GND	Power	Ground.
F13	HA12_P	FPGA_AH8_LVDS3A_7P_IO32	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 50 th pin of Board to Board Connector1 (J6).
F14	HA12_N	FPGA_AG7_LVDS3A_8N_IO31	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 48 th pin of Board to Board Connector1 (J6).
F15	GND	GND	Power	Ground.
F16	HA15_P	FPGA_AH10_LVDS3A_3P_IO40	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 92 th pin of Board to Board Connector1 (J6).
F17	HA15_N	FPGA_AH9_LVDS3A_3N_IO41	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 94 th pin of Board to Board Connector1 (J6).
F18	GND	GND	Power	Ground.
F19	HA19_P	FPGA_AE12_LVDS3A_6P_IO34	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 112 th pin of Board to Board Connector1 (J6).
F20	HA19_N	FPGA_AE11_LVDS3A_6N_IO35	NA	LVDS3A User I/O Single ended pin. This Pin is connected to 110 th pin of Board to Board Connector1 (J6).
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_FMC+_ADJ	O, 1.8V Power	Supply Voltage.
G1	GND	GND	Power	Ground.
G2	CLK1_M2C_P	FPGA_Y6_LVDS3C_13P/CLKIN_OP	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential Positive channel13. This Pin is connected to 176 th pin of Board to Board Connector2 (J7).
G3	CLK1_M2C_N	FPGA_Y7_LVDS3C_13N/CLKIN_ON	IO, 1.8V LVDS	LVDS3C LVDS receiver/transmitter differential Negative channel13. This Pin is connected to 178 th pin of Board to Board Connector2 (J7).
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.
G6	LA00_P_CC	FPGA_AD10_LVDS3B_12P/CLKIN_1P	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel12. This Pin is connected to 109 th pin of Board to Board Connector2 (J7).
G7	LA00_N_CC	FPGA_AD11_LVDS3B_12N/CLKIN_1N	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel12 This Pin is connected to 111 th pin of Board to Board Connector2 (J7).
G8	GND	GND	Power	Ground.
G9	LA03_P	FPGA_AD5_LVDS3B_8P_IO33	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel8. This Pin is connected to 86 th pin of Board to Board Connector2 (J7).
G10	LA03_N	FPGA_AD6_LVDS3B_8N_IO34	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel8. This Pin is connected to 84 th pin of Board to Board Connector2 (J7).
G11	GND	GND	Power	Ground.
G12	LA08_P	FPGA_AC9_LVDS3B_9P_IO31	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel9. This Pin is connected to 77 th pin of Board to Board Connector2 (J7).
G13	LA08_N	FPGA_AC10_LVDS3B_9N_IO32	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel9. This Pin is connected to 75 th pin of Board to Board Connector2 (J7).
G14	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
G15	LA12_P	FPGA_AD7_LVDS3B_7P_IO35	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel7. This Pin is connected to 88 th pin of Board to Board Connector2 (J7).
G16	LA12_N	FPGA_AC7_LVDS3B_7N_IO36	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel7. This Pin is connected to 90 th pin of Board to Board Connector2 (J7).
G17	GND	GND	Power	Ground.
G18	LA16_P	FPGA_AF1_LVDS3B_16P_IO17	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel17. This Pin is connected to 104 th pin of Board to Board Connector2 (J7).
G19	LA16_N	FPGA_AE1_LVDS3B_16N_IO18	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel17. This Pin is connected to 106 th pin of Board to Board Connector2 (J7).
G20	GND	GND	Power	Ground.
G21	LA20_P	FPGA_AE4_LVDS3B_3P_IO43	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel3. This Pin is connected to 100 th pin of Board to Board Connector2 (J7).
G22	LA20_N	FPGA_AD4_LVDS3B_3N_IO44	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel3. This Pin is connected to 102 th pin of Board to Board Connector2 (J7).
G23	GND	GND	Power	Ground.
G24	LA22_P	FPGA_AD2_LVDS3B_2P_IO45	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel2. This Pin is connected to 122 th pin of Board to Board Connector2 (J7).
G25	LA22_N	FPGA_AD1_LVDS3B_2N_IO46	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel2. This Pin is connected to 124 th pin of Board to Board Connector2 (J7).
G26	GND	GND	Power	Ground.
G27	LA25_P	FPGA_U6_LVDS3C_5P_IO38	IO, 1.8V LVCMOS	LVDS3B LVDS receiver/transmitter differential positive channel5. This Pin is connected to 151 th pin of Board to Board Connector2 (J7).

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
G28	LA25_N	FPGA_U5_LVDS3C_5N_IO39	IO, 1.8V LVCMOS	LVDS3B LVDS receiver/transmitter differential negative channel5. This Pin is connected to 153 th pin of Board to Board Connector2 (J7).
G29	GND	GND	Power	Ground.
G30	LA29_P	FPGA_V5_LVDS3C_6P_IO36	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel6. This Pin is connected to 148 th pin of Board to Board Connector2 (J7).
G31	LA29_N	FPGA_V4_LVDS3C_6N_IO37	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel6. This Pin is connected to 150 th pin of Board to Board Connector2 (J7).
G32	GND	GND	Power	Ground.
G33	LA31_P	FPGA_AB2_LVDS3C_21P_IO7	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel21. This Pin is connected to 136 th pin of Board to Board Connector2 (J7).
G34	LA31_N	FPGA_AB3_LVDS3C_21N_IO8	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel21. This Pin is connected to 138 th pin of Board to Board Connector2 (J7).
G35	GND	GND	Power	Ground.
G36	LA33_P	FPGA_W6_LVDS3C_16P_IO17	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel16. This Pin is connected to 152 th pin of Board to Board Connector2 (J7).
G37	LA33_N	FPGA_W7_LVDS3C_16N_IO18	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel16. This Pin is connected to 154 th pin of Board to Board Connector2 (J7).
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_FMC+_ADJ	O, 1.8V Power	Supply Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NC	NC	NC
H2	PRSNT_M2C_L	FPGA_AL6_LVDS3A_14p_IO18	I,3.3V/10K PU	Module Present Signal. This Pin is connected to 32th pin of Board to Board Connector1 (J6).
H3	GND	GND	Power	Ground.

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
H4	CLK0_M2C_P	FPGA_AL5_LVDS3A_13P/CLKIN_OP	NA	LVDS3A single ended I/O. This Pin is connected to 58th pin of Board to Board Connector1 (J6).
H5	CLK0_M2C_N	FPGA_AL4_LVDS3A_13N/CLKIN_ON	NA	LVDS3A single ended I/O. This Pin is connected to 56th pin of Board to Board Connector1 (J6).
H6	GND	GND	Power	Ground.
H7	LA02_P	FPGA_AB8_LVDS3B_4P_IO41	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel4. This Pin is connected to 76 nd pin of Board to Board Connector2 (J7).
H8	LA02_N	FPGA_AB7_LVDS3B_4N_IO42	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel4. This Pin is connected to 78 th pin of Board to Board Connector2 (J7).
H9	GND	GND	Power	Ground.
H10	LA04_P	FPGA_AG6_LVDS3B_17P_IO15	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel17. This Pin is connected to 81 nd pin of Board to Board Connector2 (J7).
H11	LA04_N	FPGA_AF6_LVDS3B_17N_IO16	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel17. This Pin is connected to 79 th pin of Board to Board Connector2 (J7).
H12	GND	GND	Power	Ground.
H13	LA07_P	FPGA_AK4_LVDS3B_22P_IO5	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel22. This Pin is connected to 87 th pin of Board to Board Connector2 (J7).
H14	LA07_N	FPGA_AK3_LVDS3B_22N_IO6	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel22. This Pin is connected to 89 th pin of Board to Board Connector2 (J7).
H15	GND	GND	Power	Ground.
H16	LA11_P	FPGA_AJ4_LVDS3B_21P_IO7	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel21. This Pin is connected to 91 th pin of Board to Board Connector2 (J7).
H17	LA11_N	FPGA_AH4_LVDS3B_	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
		21N_IO8		differential negative channel21. This Pin is connected to 93 th pin of Board to Board Connector2 (J7).
H18	GND	GND	Power	Ground.
H19	LA15_P	FPGA_AH3_LVDS3B_18P_IO13	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel18. This Pin is connected to 92 th pin of Board to Board Connector2 (J7).
H20	LA15_N	FPGA_AG3_LVDS3B_18N_IO14	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel18. This Pin is connected to 94 th pin of Board to Board Connector2 (J7).
H21	GND	GND	Power	Ground.
H22	LA19_P	FPGA_AC4_LVDS3B_6P_IO37	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel6. This Pin is connected to 126 th pin of Board to Board Connector2 (J7).
H23	LA19_N	FPGA_AC5_LVDS3B_6N_IO38	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel6. This Pin is connected to 128 th pin of Board to Board Connector2 (J7).
H24	GND	GND	Power	Ground.
H25	LA21_P	FPGA_AB6_LVDS3B_5P_IO39	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential positive channel5. This Pin is connected to 127 th pin of Board to Board Connector2 (J7).
H26	LA21_N	FPGA_AB5_LVDS3B_5N_IO40	IO, 1.8V LVDS	LVDS3B LVDS receiver/transmitter differential negative channel5. This Pin is connected to 125 th pin of Board to Board Connector2 (J7).
H27	GND	GND	Power	Ground.
H28	LA24_P	FPGA_R1_LVDS3C_8P_IO32	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel8. This Pin is connected to 159 th pin of Board to Board Connector2 (J7).
H29	LA24_N	FPGA_P1_LVDS3C_8N_IO33	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel8. This Pin is connected to 161 th pin of Board to Board Connector2 (J7).
H30	GND	GND	Power	Ground.
H31	LA28_P	FPGA_Y8_LVDS3C_14P_IO21	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel4.

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Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
				This Pin is connected to 156 th pin of Board to Board Connector2 (J7).
H32	LA28_N	FPGA_Y9_LVDS3C_14N_IO22	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel4. This Pin is connected to 158 th pin of Board to Board Connector2 (J7).
H33	GND	GND	Power	Ground.
H34	LA30_P	FPGA_Y3_LVDS3C_19P_IO11	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel9. This Pin is connected to 144 th pin of Board to Board Connector2 (J7).
H35	LA30_N	FPGA_Y4_LVDS3C_19N_IO12	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel9. This Pin is connected to 146 th pin of Board to Board Connector2 (J7).
H36	GND	GND	Power	Ground.
H37	LA32_P	FPGA_AA5_LVDS3C_18P_IO13	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential positive channel18. This Pin is connected to 182 th pin of Board to Board Connector2 (J7).
H38	LA32_N	FPGA_AA6_LVDS3C_18N_IO14	IO, 1.8V LVCMOS	LVDS3C LVDS receiver/transmitter differential negative channel18. This Pin is connected to 184 th pin of Board to Board Connector2 (J7).
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_FMC+_ADJ	O, 1.8V Power	Supply Voltage.
J1	GND	GND	Power	Ground.
J2	CLK3_BIDIR_P	FPGA_AM3_LVDS3A_15P/CLKOUT_0P	IO, 1.8V LVDS	LVDS3A Single ended signal. This Pin is connected to 24 th pin of Board to Board Connector1 (J6).
J3	CLK3_BIDIR_N	FPGA_AL3_LVDS3A_15N/CLKOUT_0N	IO, 1.8V LVDS	LVDS3A Single ended signal. This Pin is connected to 22 th pin of Board to Board Connector1 (J6).
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	FPGA_AB1_LVDS3C_	NA	LVDS3C LVDS receiver/transmitter

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
		24P_IO1		differential positive channel24. This Pin is connected to 131 th pin of Board to Board Connector2 (J7).
J7	HA03_N	FPGA_AA1_LVDS3C_24N_IO2	NA	LVDS3C LVDS receiver/transmitter differential negative channel24. This Pin is connected to 133 th pin of Board to Board Connector2 (J7).
J8	GND	GND	Power	Ground.
J9	HA07_P	FPGA_V2_LVDS3C_11P_IO26	NA	LVDS3C LVDS receiver/transmitter differential positive channel11. This Pin is connected to 147 th pin of Board to Board Connector2 (J7).
J10	HA07_N	FPGA_U2_LVDS3C_11N_IO27	NA	LVDS3C LVDS receiver/transmitter differential negative channel11. This Pin is connected to 149 th pin of Board to Board Connector2 (J7).
J11	GND	GND	Power	Ground.
J12	HA11_P	FPGA_AM1_LVDS3A_16P_IO14	NA	LVDS3A Single ended signal. This Pin is connected to 12 th pin of Board to Board Connector1 (J6).
J13	HA11_N	FPGA_AP6_LVDS3A_20N_IO7	NA	LVDS3A Single ended signal. This Pin is connected to 28 th pin of Board to Board Connector1 (J6).
J14	GND	GND	Power	Ground.
J15	HA14_P	FPGA_AG10_LVDS3A_4P_IO38	NA	LVDS3A Single ended signal. This Pin is connected to 70 th pin of Board to Board Connector1 (J6).
J16	HA14_N	FPGA_AF10_LVDS3A_4N_IO39	NA	LVDS3A Single ended signal. This Pin is connected to 72 th pin of Board to Board Connector1 (J6).
J17	GND	GND	Power	Ground.
J18	HA18_P	FPGA_AF11_LVDS3A_5P_IO36	NA	LVDS3A Single ended signal. This Pin is connected to 108 th pin of Board to Board Connector1 (J6).
J19	HA18_N	FPGA_AG11_LVDS3A_5N_IO37	NA	LVDS3A Single ended signal. This Pin is connected to 106 th pin of Board to Board Connector1 (J6).
J20	GND	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.
J27	HB07_P	NA	NA	NC.
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	NA	NA	NC.
J34	HB15_N	NA	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	VREF_B_M2C	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK2_BIDIR_P	FPGA_U1_LVDS3C_10P/CLKOUT_1P	NA	LVDS3C LVDS receiver/transmitter differential positive channel10. This Pin is connected to 169 th pin of Board to Board Connector2 (J7).
K5	CLK2_BIDIR_N	FPGA_T1_LVDS3C_10N/CLKOUT_1N	NA	LVDS3C LVDS receiver/transmitter differential negative channel10. This Pin is connected to 171 th pin of Board to Board Connector2 (J7).
K6	GND	GND	Power	Ground.
K7	HA02_P	FPGA_AA3_LVDS3C_20P_IO9	NA	LVDS3C LVDS receiver/transmitter differential positive channel20. This Pin is connected to 135 th pin of Board to Board Connector2 (J7).
K8	HA02_N	FPGA_AA4_LVDS3C_20N_IO10	NA	LVDS3C LVDS receiver/transmitter differential negative channel20. This Pin is connected to 137 th pin of Board to Board Connector2 (J7).
K9	GND	GND	Power	Ground.
K10	HA06_P	FPGA_AA8_LVDS3C_	NA	LVDS3C LVDS receiver/transmitter

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
		17P_IO15		differential positive channel17. This Pin is connected to 140 th pin of Board to Board Connector2 (J7).
K11	HA06_N	FPGA_AA9_LVDS3C_17N_IO16	NA	LVDS3C LVDS receiver/transmitter differential negative channel17. This Pin is connected to 142 th pin of Board to Board Connector2 (J7).
K12	GND	GND	Power	Ground.
K13	HA10_P	FPGA_AJ7_LVDS3A_11P_IO24	NA	LVDS3A Single ended signal. This Pin is connected to 44 th pin of Board to Board Connector1 (J6).
K14	HA10_N	FPGA_AJ6_LVDS3A_11N_IO25	NA	LVDS3A Single ended signal. This Pin is connected to 42 th pin of Board to Board Connector1 (J6).
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	FPGA_AJ5_LVDS3A_10P/CLKOUT_1P	NA	LVDS3A Single ended signal. This Pin is connected to 118 th pin of Board to Board Connector1 (J6).
K17	HA17_N_CC	FPGA_AH5_LVDS3A_10N/CLKOUT_1N	NA	LVDS3A Single ended signal. This Pin is connected to 116 th pin of Board to Board Connector1 (J6).
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC.
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.
L1	RES1	NA	NA	NC.
L2	GND2	GND	Power	Ground.
L3	GND3	GND	Power	Ground.
L4	GBTCLK2_M2C_P	REFCLK_GXBL1E_CH Bp	I, Diff	GXBL1E High speed differential reference bottom clock positive receiver channel. This Pin is connected to 218 th pin of Board to Board Connector1 (J6).
L5	GBTCLK2_M2C_N	REFCLK_GXBL1E_CH Bn	I, Diff	GXBL1E High speed differential reference bottom clock negative receiver channel. This Pin is connected to 220 th pin of Board to Board Connector1 (J6).
L6	GND4	GND	Power	Ground.
L7	GND5	GND	Power	Ground.
L8	GBTCLK3_M2C_P	REFCLK_GXBL1F_CH Bp	I, Diff	GXBL1F High speed differential reference bottom clock positive receiver channel. This Pin is connected to 223th pin of Board to Board Connector2 (J7).
L9	GBTCLK3_M2C_N	REFCLK_GXBL1F_CH Bn	I, Diff	GXBL1F High speed differential reference bottom clock negative receiver channel. This Pin is connected to 225th pin of Board to Board Connector2 (J7).
L10	GND6	GND	Power	Ground.
L11	GND7	GND	Power	Ground.
L12	GBTCLK4_M2C_P	NA	NA	NC.
L13	GBTCLK4_M2C_N	NA	NA	NC.
L14	GND8	GND	Power	Ground.
L15	GND9	GND	Power	Ground.
L16	SYNC_C2M_P	NA	NA	NC.
L17	SYNC_C2M_N	NA	NA	NC.
L18	GND10	GND	Power	Ground.
L19	GND11	GND	Power	Ground.
L20	REFCLK_C2M_P	NA	NA	NC.
L21	REFCLK_C2M_N	NA	NA	NC.
L22	GND12	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
L23	GND13	GND	Power	Ground.
L24	REFCLK_M2C_P	NA	NA	NC.
L25	REFCLK_M2C_N	NA	NA	NC.
L26	GND14	GND	Power	Ground.
L27	GND15	GND	Power	Ground.
L28	SYNC_M2C_P	NA	NA	NC.
L29	SYNC_M2C_N	NA	NA	NC.
L30	GND16	GND	Power	Ground.
L31	GND17	GND	Power	Ground.
L32	RES2	NA	NA	NC.
L33	RES3	NA	NA	NC.
L34	GND18	GND	Power	Ground.
L35	GND19	GND	Power	Ground.
L36	12P0V	VCC_12V_FMC+	O, 12V Power	Supply Voltage.
L37	12P0V	VCC_12V_FMC+	O, 12V Power	Supply Voltage.
L38	GND20	GND	Power	Ground.
L39	GND37	GND	Power	Ground.
L40	12P0V	VCC_12V_FMC+	O, 12V Power	Supply Voltage.
M1	GND1	GND	Power	Ground.
M2	DP23_M2C_P	NA	NA	NC.
M3	DP23_M2C_N	NA	NA	NC.
M4	GND2	GND	Power	Ground.
M5	GND3	GND	Power	Ground.
M6	DP22_M2C_P	NA	NA	NC.
M7	DP22_M2C_N	NA	NA	NC.
M8	GND4	GND	Power	Ground.
M9	GND5	GND	Power	Ground.
M10	DP21_M2C_P	NA	NA	NC.
M11	DP21_M2C_N	NA	NA	NC.
M12	GND6	GND	Power	Ground.
M13	GND7	GND	Power	Ground.
M14	DP20_M2C_P	NA	NA	NC.
M15	DP20_M2C_N	NA	NA	NC.
M16	GND8	GND	Power	Ground.
M17	GND9	GND	Power	Ground.
M18	DP14_C2M_P	GXBL1F_TX_CH4p	O, Diff	GXBL1F High speed positive differential Transmitter channel4. This Pin is connected to 212th pin of Board to Board Connector2 (J7).
M19	DP14_C2M_N	GXBL1F_TX_CH4n	O, Diff	GXBL1F High speed positive differential Transmitter channel4. This Pin is connected to 214th pin of

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
				Board to Board Connector2 (J7).
M20	GND10	GND	Power	Ground.
M21	GND11	GND	Power	Ground.
M22	DP15_C2M_P	GXBL1F_TX_CH5p	O, Diff	GXBL1F High speed positive differential Transmitter channel5. This Pin is connected to 224 th pin of Board to Board Connector2 (J7).
M23	DP15_C2M_N	GXBL1F_TX_CH5n	O, Diff	GXBL1F High speed positive differential Transmitter channel5. This Pin is connected to 226th pin of Board to Board Connector2 (J7).
M24	GND12	GND	Power	Ground.
M25	GND13	GND	Power	Ground.
M26	DP16_C2M_P	NA	NA	NC.
M27	DP16_C2M_N	NA	NA	NC.
M28	GND14	GND	Power	Ground.
M29	GND15	GND	Power	Ground.
M30	DP17_C2M_P	NA	NA	NC.
M31	DP17_C2M_N	NA	NA	NC.
M32	GND16	GND	Power	Ground.
M33	GND17	GND	Power	Ground.
M34	DP18_C2M_P	NA	NA	NC.
M35	DP18_C2M_N	NA	NA	NC.
M36	GND18	GND	Power	Ground.
M37	GND19	GND	Power	Ground.
M38	DP19_C2M_P	NA	NA	NC.
M39	DP19_C2M_N	NA	NA	NC.
M40	GND20	GND	Power	Ground.
Y1	GND1	GND	Power	Ground.
Y2	DP23_C2M_P	NA	NA	NC.
Y3	DP23_C2M_N	NA	NA	NC.
Y4	GND2	GND	Power	Ground.
Y5	GND3	GND	Power	Ground.
Y6	DP21_C2M_P	NA	NA	NC.
Y7	DP21_C2M_N	NA	NA	NC.
Y8	GND4	GND	Power	Ground.
Y9	GND5	GND	Power	Ground.
Y10	DP10_M2C_P	GXBL1E_RX_CH2P	I, Diff	GXBL1E High speed positive differential receiver channel2. This Pin is connected to 237 th pin of Board to Board Connector1 (J6).
Y11	DP10_M2C_N	GXBL1E_RX_CH2N	I, Diff	GXBL1E High speed positive differential

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
				receiver channel2. This Pin is connected to 235 th pin of Board to Board Connector1 (J6).
Y12	GND6	GND	Power	Ground.
Y13	GND7	GND	Power	Ground.
Y14	DP12_M2C_P	GXBL1F_RX_CH2p	I, Diff	GXBL1F High speed positive differential receiver channel2. This Pin is connected to 211 th pin of Board to Board Connector2 (J7).
Y15	DP12_M2C_N	GXBL1F_RX_CH2n	I, Diff	GXBL1F High speed positive differential receiver channel2. This Pin is connected to 213 th pin of Board to Board Connector2 (J7).
Y16	GND8	GND	Power	Ground.
Y17	GND9	GND	Power	Ground.
Y18	DP14_M2C_P	GXBL1F_RX_CH4p	I, Diff	GXBL1F High speed positive differential receiver channel4. This Pin is connected to 206 th pin of Board to Board Connector2 (J7).
Y19	DP14_M2C_N	GXBL1F_RX_CH4n	I, Diff	GXBL1F High speed positive differential receiver channel4. This Pin is connected to 208 th pin of Board to Board Connector2 (J7).
Y20	GND10	GND	Power	Ground.
Y21	GND11	GND	Power	Ground.
Y22	DP15_M2C_P	GXBL1F_RX_CH5p	I, Diff	GXBL1F High speed positive differential receiver channel5. This Pin is connected to 218 th pin of Board to Board Connector2 (J7).
Y23	DP15_M2C_N	GXBL1F_RX_CH5n	I, Diff	GXBL1F High speed positive differential receiver channel5. This Pin is connected to 220 th pin of Board to Board Connector2 (J7).
Y24	GND12	GND	Power	Ground.
Y25	GND13	GND	Power	Ground.
Y26	DP11_C2M_P	GXBL1E_TX_CH3p	O, Diff	GXBL1F High speed positive differential Transmitter channel3. This Pin is connected to 223 th pin of Board to Board Connector1 (J6).

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
Y27	DP11_C2M_N	GXBL1E_TX_CH3n	O, Diff	GXBL1F High speed positive differential Transmitter channel3. This Pin is connected to 225 th pin of Board to Board Connector1 (J6).
Y28	GND14	GND	Power	Ground.
Y29	GND15	GND	Power	Ground.
Y30	DP13_C2M_P	GXBL1F_TX_CH3p	O, Diff	GXBL1F High speed positive differential Transmitter channel3. This Pin is connected to 200 th pin of Board to Board Connector2 (J7).
Y31	DP13_C2M_N	GXBL1F_TX_CH3n	O, Diff	GXBL1F High speed positive differential Transmitter channel3. This Pin is connected to 202 th pin of Board to Board Connector2 (J7).
Y32	GND16	GND	Power	Ground.
Y33	GND17	GND	Power	Ground.
Y34	DP17_M2C_P	NA	NA	NC.
Y35	DP17_M2C_N	NA	NA	NC.
Y36	GND18	GND	Power	Ground.
Y37	GND19	GND	Power	Ground.
Y38	DP19_M2C_P	NA	NA	NC.
Y39	DP19_M2C_N	NA	NA	NC.
Y40	GND20	GND	Power	Ground.
Z1	HSPC_PRSNT_M2C_L	FPGA_AK6_LVDS3A_14n_IO19	I,3.3V/10K PU	Module Present Signal. This Pin is connected to 34 th pin of Board to Board Connector1 (J6).
Z2	GND2	GND	Power	Ground.
Z3	GND3	GND	Power	Ground.
Z4	DP22_C2M_P	NA	NA	NC.
Z5	DP22_C2M_N	NA	NA	NC.
Z6	GND6	GND	Power	Ground.
Z7	GND7	GND	Power	Ground.
Z8	DP20_C2M_P	NA	NA	NC.
Z9	DP20_C2M_N	NA	NA	NC.
Z10	GND8	GND	Power	Ground.
Z11	GND9	GND	Power	Ground.
Z12	DP11_M2C_P	GXBL1E_RX_CH3p	I, Diff	GXBL1E High speed positive differential receiver channel3. This Pin is connected to 231 th pin of Board to Board Connector1 (J6).

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
Z13	DP11_M2C_N	GXBL1E_RX_CH3n	I, Diff	GXBL1E High speed positive differential receiver channel3. This Pin is connected to 229 th pin of Board to Board Connector1 (J6).
Z14	GND10	GND	Power	Ground.
Z15	GND11	GND	Power	Ground.
Z16	DP13_M2C_P	GXBL1F_RX_CH3p	I, Diff	GXBL1F High speed positive differential receiver channel3. This Pin is connected to 194 th pin of Board to Board Connector2 (J7).
Z17	DP13_M2C_N	GXBL1F_RX_CH3n	I, Diff	GXBL1F High speed positive differential receiver channel3. This Pin is connected to 196 th pin of Board to Board Connector2 (J7).
Z18	GND12	GND	Power	Ground.
Z19	GND13	GND	Power	Ground.
Z20	GBTCLK5_M2C_P	NA	NA	NC.
Z21	GBTCLK5_M2C_N	NA	NA	NC.
Z22	GND14	GND	Power	Ground.
Z23	GND15	GND	Power	Ground.
Z24	DP10_C2M_P	GXBL1E_TX_CH2p	O, Diff	GXBL1E High speed positive differential Transmitter channel2. This Pin is connected to 217 th pin of Board to Board Connector1 (J6).
Z25	DP10_C2M_N	GXBL1E_TX_CH2n	O, Diff	GXBL1E High speed positive differential Transmitter channel2. This Pin is connected to 219 th pin of Board to Board Connector1 (J6).
Z26	GND16	GND	Power	Ground.
Z27	GND17	GND	Power	Ground.
Z28	DP12_C2M_P	GXBL1F_TX_CH2p	O, Diff	GXBL1F High speed positive differential Transmitter channel2. This Pin is connected to 217 th pin of Board to Board Connector2 (J7).
Z29	DP12_C2M_N	GXBL1F_TX_CH2n	O, Diff	GXBL1F High speed positive differential Transmitter channel2. This Pin is connected to 219 th pin of Board to Board Connector2 (J7).
Z30	GND18	GND	Power	Ground.
Z31	GND19	GND	Power	Ground.

Pin No	FMC+ Connector1 Pin Name	Signal Name	Signal Type/Termination	Description
Z32	DP16_M2C_P	NA	NA	NC.
Z33	DP16_M2C_N	NA	NA	NC.
Z34	GND20	GND	Power	Ground.
Z35	GND21	GND	Power	Ground.
Z36	DP18_M2C_P	NA	NA	NC.
Z37	DP18_M2C_N	NA	NA	NC.
Z38	GND22	GND	Power	Ground.
Z39	GND23	GND	Power	Ground.
Z40	VADJ			

2.7.2 Pmod Host Port Connectors

The Arria10 SoC/FPGA custom carrier board supports one 12pin Pmod and one 6pin Pmod host port connectors for plugging Pmod modules. Pmod interface or Peripheral Module interface is a standard defined by Digilent Inc in the Digilent Pmod Interface Specification for peripherals used with FPGAs or microcontrollers.

Pmod provides multiple digital IO signals which can be configured as different standard serial protocols like SPI, UART, I2C etc. 12pin Pmod Host port connector (J13) and 6pin connector (J15) are physically located at the top of the board as shown below.

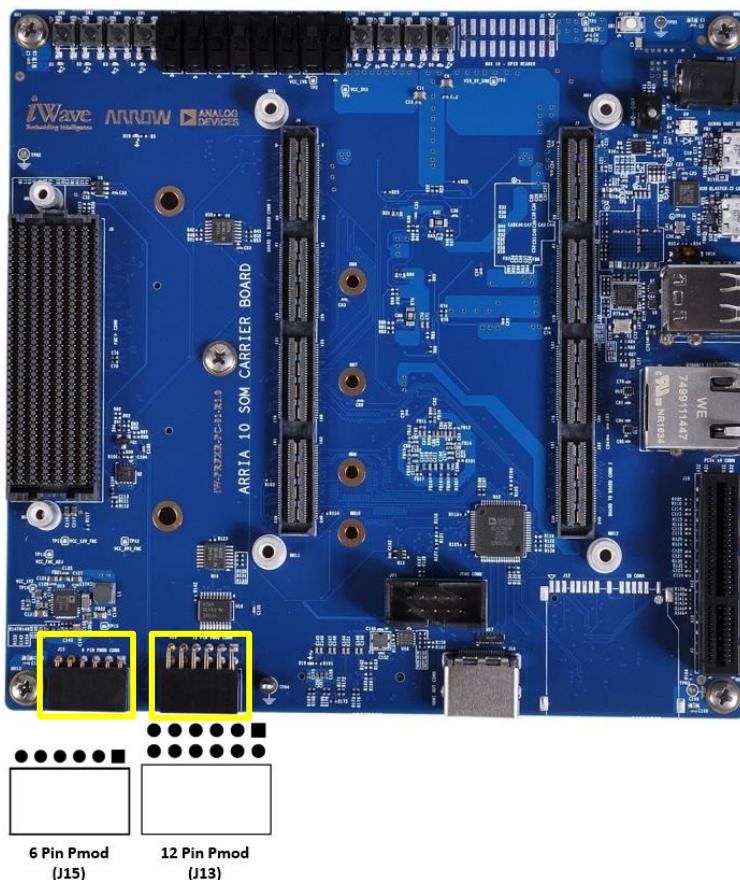


Figure 10: Pmod Host Port Connectors

Table 6: 12Pin Pmod Connector1 Pin Out

Pin No	Signal Name	Signal Type/Termination	Description
1	FPGA_T4_LVDS3C_1p_IO46	IO, 3V3 LVCMOS	General purpose Input Output.
2	FPGA_R4_LVDS3C_1n_IO47	IO, 3V3 LVCMOS	General purpose Input Output.
3	FPGA_T5_LVDS3C_4p_IO40	IO, 3V3 LVCMOS	General purpose Input Output.
4	FPGA_T6_LVDS3C_4n_IO41	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	FPGA_T3_LVDS3C_3p_IO42	IO, 3V3 LVCMOS	General purpose Input Output.
8	FPGA_R3_LVDS3C_3n_IO43	IO, 3V3 LVCMOS	General purpose Input Output.
9	FPGA_P4_LVDS3C_2p_IO44	IO, 3V3 LVCMOS	General purpose Input Output.
10	FPGA_P5_LVDS3C_2n_IO45	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

Table 7: 6Pin Pmod Connector2 Pin Out

Pin No	Signal Name	Signal Type/Termination	Description
1	FPGA_AP15_LVDS2A_3n_I040	IO, 3V3 LVCMOS	General purpose Input Output.
2	FPGA_AP16_LVDS2A_2p_I041	IO, 3V3 LVCMOS	General purpose Input Output.
3	FPGA_AP17_LVDS2A_2n_I042	IO, 3V3 LVCMOS	General purpose Input Output.
4	FPGA_AL13_LVDS2A_1p_I043	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

2.8 High Speed Communication Connectors

2.8.1 PCIe x 4 Connector

The Arria10 SoC/FPGA custom carrier board supports one PCI Express Gen3.0 lane through Arria10 Transceiver BANK 1E and BANK 1F. This Transceiver channels from Board to Board connector 2 is connected to PClex4 lane connector through 0.1uF AC caps. Also, PCIe reference clock from on board clock synthesizer is connected to PClex4 connector. This PClex4 connector (J10) is physically located at the top of the board as shown below.

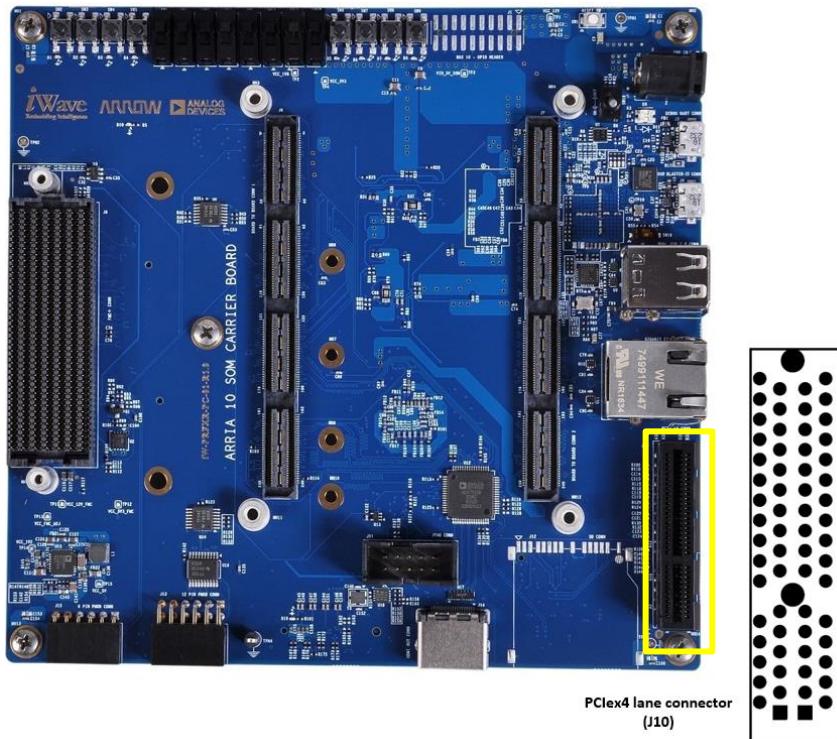


Figure 11 PCIe x 4 Connector

Table 8 PClex4 Connector Pin Out

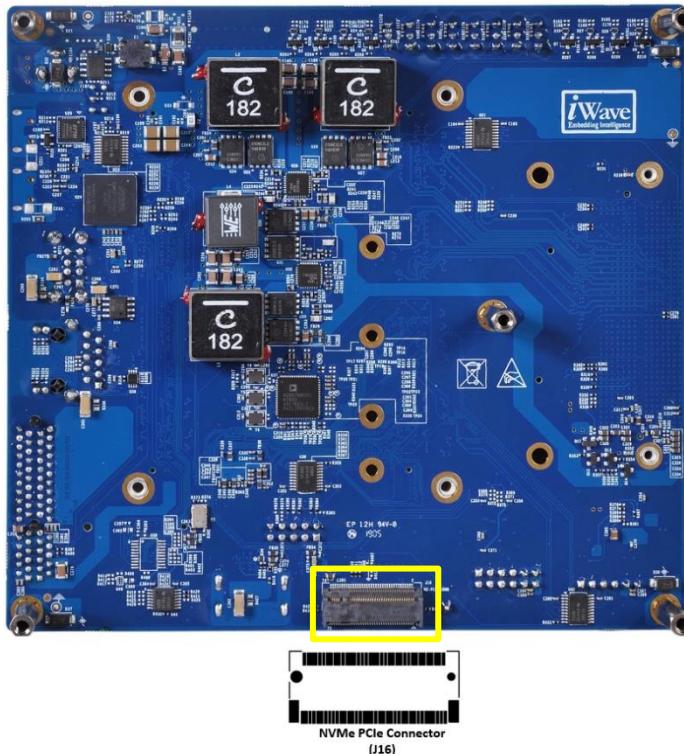
Pin No	Pin Name	Signal Name	Signal Type/Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	RSVD1	NC	-	NC, Reserved Pin.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	I2C0_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.

Pin No	Pin Name	Signal Name	Signal Type/Termination	Description
B6	SMDAT	I2C0_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	FPGA_AG16_LVDS2A_20p_IO9	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	FPGA_AP9_LVDS3A_2_2p_IO4	O, 3.3V CMOS	PCIe WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	REFCLK+	PCIe_REFCLKP	O, DIFF	PCIe Clock positive. This pin is connected from Clock Synthesizer
B13	GND	GND	Power	Ground.
A14	REFCLK-	PCIe_REFCLK_DN	O, DIFF	PCIe Clock negative. This pin is connected from Clock Synthesizer
B14	PCIE0_TX+	GXBL1E_TX_CH4p	O, DIFF	PCIe Port 0 Transmit pair positive.
A15	GND	GND	Power	Ground.
B15	PCIE0_TX-	GXBL1E_TX_CH4n	O, DIFF	PCIe Port 0 Transmit pair negative.
A16	PCIE0_RX+	GXBL1E_RX_CH4p	I, DIFF	PCIe Port 0 Receive pair positive.
B16	GND	GND	Power	Ground.
A17	PCIE0_RX-	GXBL1E_RX_CH4n	I, DIFF	PCIe Port 0 Receive pair negative.
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PCIE1_TX+	GXBL1E_TX_CH5p	-	PCIe Port 1 Transmit pair positive.
A20	GND	GND	Power	Ground.
B20	PCIE1_TX-	GXBL1E_TX_CH5n	-	PCIe Port 1 Transmit pair negative.
A21	PCIE1_RX+	GXBL1E_RX_CH5p	-	PCIe Port 1 Receive pair positive.
B21	GND	GND	Power	Ground.
A22	PCIE1_RX-	GXBL1E_RX_CH5n	-	PCIe Port 1 Receive pair negative.
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PCIE2_TX+	GXBL1F_TX_CH0p	-	PCIe Port 2 Transmit pair positive.
A24	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/Termination	Description
B24	PCIE2_TX-	GXBL1F_TX_CH0n	-	PCIe Port 2 Transmit pair negative.
A25	PCIE2_RX+	GXBL1F_RX_CH0p	-	PCIe Port 2 Receive pair positive.
B25	GND	GND	Power	Ground.
A26	PCIE2_RX-	GXBL1F_RX_CH0n	-	PCIe Port 2 Receive pair negative.
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PCIE3_TX+	GXBL1F_TX_CH1p	-	PCIe Port 3 Transmit pair positive.
A28	GND	GND	Power	Ground.
B28	PCIE3_TX-	GXBL1F_TX_CH1n	-	PCIe Port 3 Transmit pair negative.
A29	PCIE3_RX+	GXBL1F_RX_CH1p	-	PCIe Port 3 Receive pair positive.
B29	GND	GND	Power	Ground.
A30	PCIE3_RX-	GXBL1F_RX_CH1n	-	PCIe Port 3 Receive pair negative.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSNT3#	NC	-	NC.
A32	RSVD	NC	-	NC, Reserved Pin.
B32	GND	GND	Power	Ground.

2.8.2 NVMe M.2 Connector

The Arria10 SoC/FPGA custom carrier board supports one NVMe M.2 interface through Arria10 Transceiver BANK 1C and BANK 1D. This Transceiver channels from Board to Board connector 2 is connected to NVMe M.2 connector through 0.1uF AC caps. Also, NVMe M.2 reference clock from on board clock synthesizer is connected to NVMe M.2 connector. This NVMe M.2 connector (J16) is physically located at the bottom of the board as shown below.



2.9 Display Features

2.9.1 HDMI Output

The Arria10 SoC/FPGA custom carrier board supports Type A HDMI output connector through Arria10 Single Ended FPGA signals from BANK2A. This Single Ended FPGA signals are from Board to Board Connector is connected to ADV7511W HDMI Transmitter chip.

Arria10 SoC CPU's I2C0 interface is connected to HDMI Transmitter for control & configuration. Output of HDMI transmitter is connected to Standard HDMI connector with ESD protection circuitry. HDMI Output connector (J14) is physically located on top of the board as shown below.

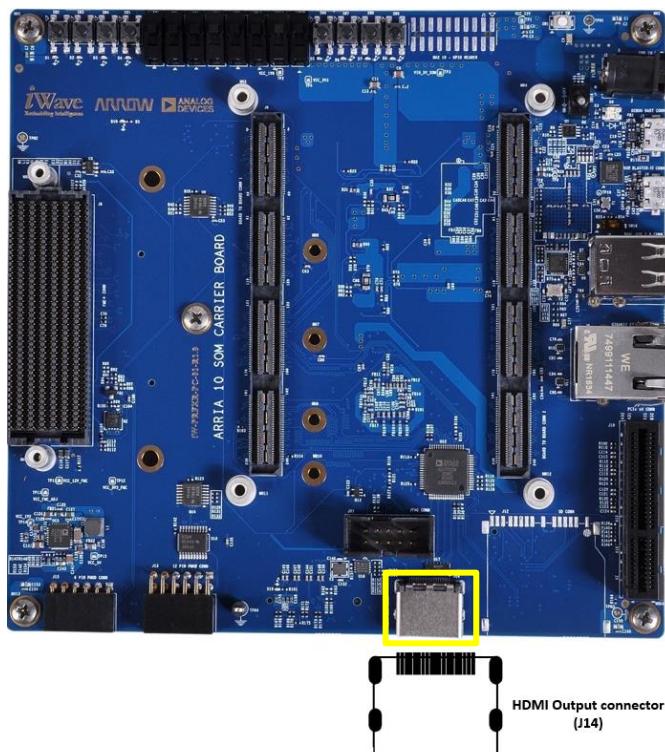


Figure 12 HDMI Type A Connector

Table 9 HDMI Output Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	TMDS_D2+	D2T+	O, TMDS	HDMI data2 pair positive.
2	GND	GND	Power	Red Pair Ground.
3	TMDS_D2-	D2T-	O, TMDS	HDMI data2 pair negative.
4	TMDS_D1+	D1T+	O, TMDS	HDMI data1 pair positive.
5	GND	GND	Power	Green Pair Ground.
6	TMDS_D1-	D1T-	O, TMDS	HDMI data1 pair negative.
7	TMDS_D0+	D0T+	O, TMDS	HDMI data0 pair positive.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
8	GND	GND	Power	Blue Pair Ground.
9	TMDS_D0-	D0T-	O, TMDS	HDMI data0 pair negative.
10	TMDS_CLK+	CLKT+	O, TMDS	Display Clock pair positive.
11	GND	GND	Power	Clock pair Ground.
12	TMDS_CLK-	CLKT-	O, TMDS	Display Clock pair negative.
13	CEC	CEC	IO, 5V CMOS	Consumer Electronic Control.
14	RSV/NC	NC	-	NC.
15	I2C_SCL	SCL	O, 5V CMOS	EDID I2C Clock.
16	I2C_SDA	SDA	IO, 5V CMOS	EDID I2C Data.
17	DDC/CEC_GND	DDC/CEC_GND	Power	Ground.
18	+5V	+5V	O, Power	5V Power Supply.
19	HPD	HPD	I, 5V TTL	HDMI Cable Hot plug detect.

2.10 User Interface Features

2.10.1 FPGA slide switch

The Arria10 SoC/FPGA custom carrier board supports four FPGA Slide Switches through Arria10 FPGA I/Os. This FPGA I/Os from Board to Board Connector is directly connected to FPGA Slide Switches.

FPGA I/Os status can be changed by changing the switch position High or Low. This FPGA Slide switches (SW10, SW11, SW12, SW13) is physically located at the top of the board as shown below.

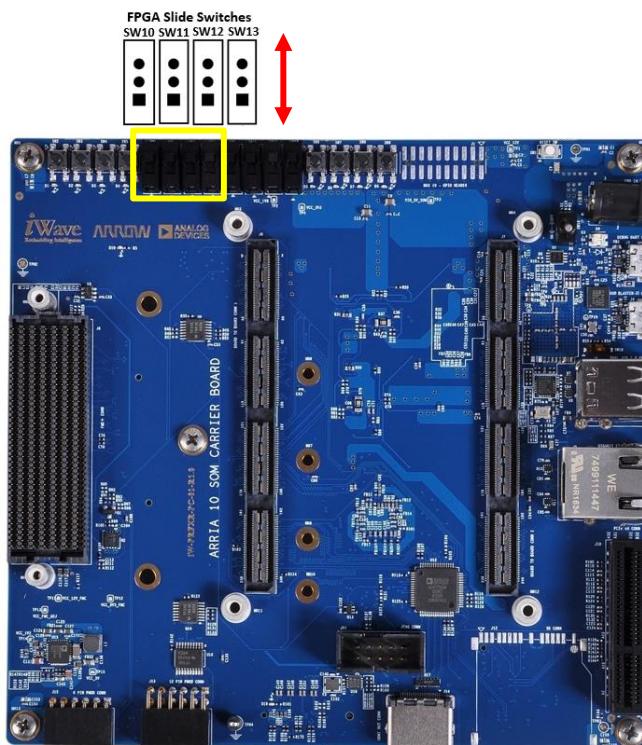


Figure 13 FPGA Sliding Switch

Table 10 FPGA Slide Switch Pin Out

FPGA Sliding Switch	Signal Name	Switch Direction	
		Down	UP
SW10	FPGA_AM16_LVDS2A_10n/CLKOUT_0n	High	Low
SW11	FPGA_AL16_LVDS2A_10p/CLKOUT_0p	High	Low
SW12	FPGA_AH19_LVDS2A_13n/CLKIN_0n	High	Low
SW13	FPGA_AH18_LVDS2A_13p/CLKIN_0p	High	Low

2.10.2 FPGA push button

The Arria10 SoC/FPGA custom carrier board supports four FPGA push buttons through Arria10 FPGA I/Os. This FPGA I/Os from Board to Board Connector is directly connected to FPGA push buttons.

FPGA I/Os status can be changed by changing the push button action. This FPGA push button (SW2, SW3, SW4, SW5) is physically located at the top of the board as shown below.

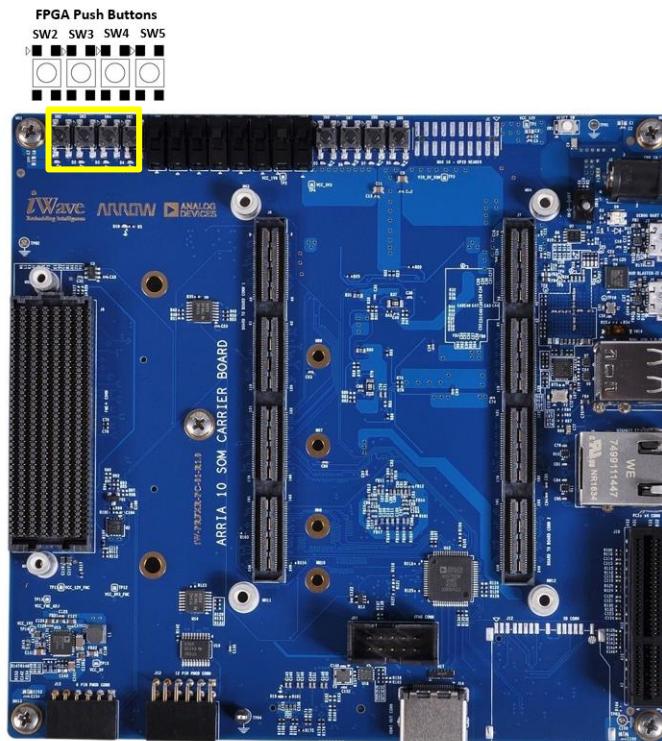


Figure 14 FPGA Push Button

Table 11 FPGA Push Button Pin Out

FPGA Sliding Switch	Signal Name	Switch Direction	
		Down	UP
SW2	FPGA_AF8_LVDS3A_2p_IO42	Low	High
SW3	FPGA_AE8_LVDS3A_2n_IO43	Low	High
SW4	FPGA_AE9_LVDS3A_1n_IO45	Low	High
SW5	FPGA_AF9_LVDS3A_1p_IO44	Low	High

2.10.3 FPGA LED

The Arria10 SoC/FPGA custom carrier board supports four LEDs through Arria10 FPGA I/Os. This FPGA I/Os from Board to Board Connector is connected to LEDs through Mosfet control switch.

LED status can be changed by driving the FPGA I/Os High or Low. These LED's (D1, D2, D3, D4) are physically located at the top of the board as shown below.

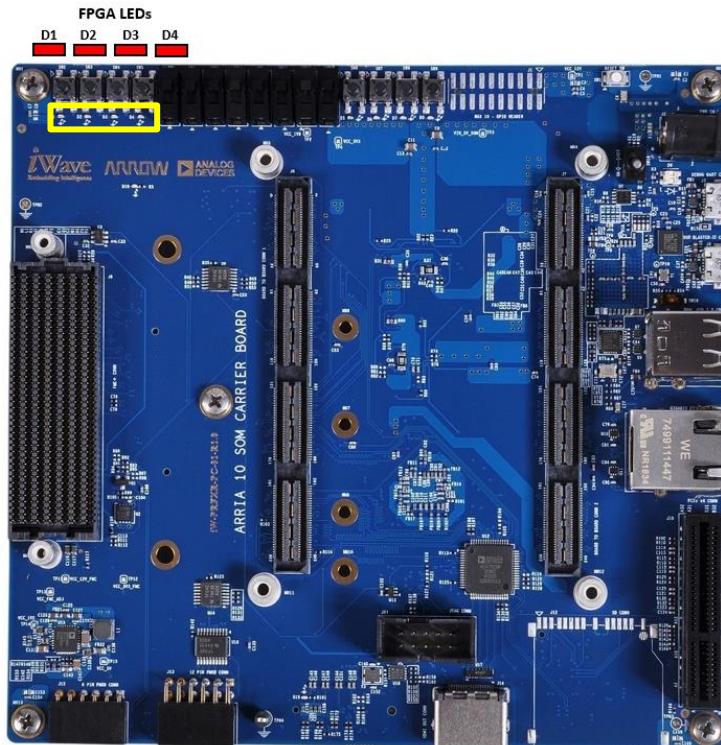


Figure 15 FPGA LED

Table 12 FPGA LED

LED's Name	Net Name	LED Indication	
		LOW	HIGH
D1	FPGA_AC17_LVDS2A_24p/NANDWP	ON	OFF
D2	FPGA_AG17_LVDS2A_15p/CLKOUT_0p	ON	OFF
D3	FPGA_AG17_LVDS2A_15p/CLKOUT_0n	ON	OFF
D4	FPGA_AC17_LVDS2A_24p/NANDWP	ON	OFF

2.10.4 HPS Slide Switch

The Arria10 SoC/FPGA custom carrier board supports four HPS Slide Switches through Arria10 HPS I/Os. This HPS I/Os from Board to Board Connector is directly connected to HPS Slide Switches.

HPS I/Os status can be changed by changing the switch position High or Low. This HPS Slide switches (SW14, SW15, SW16, SW17) is physically located at the top of the board as shown below.

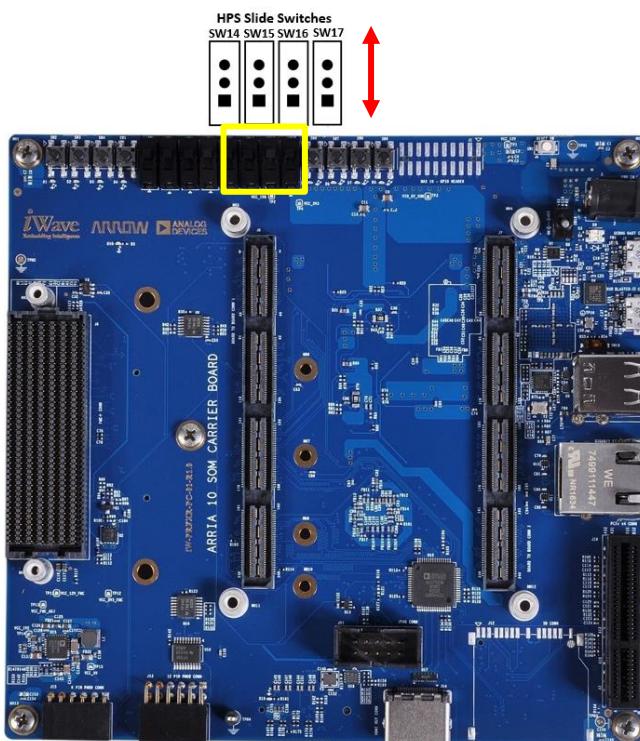


Figure 16 HPS Slide Switch

Table 13 HPS Slide Switch

HPS Sliding Switch	Signal Name	Switch Direction	
		Down	UP
SW14	HPS_SDMMC_DATA3/EMAC2_TXD1	High	Low
SW15	HPS_SDMMC_CCLK/EMAC2_RX_CLK	High	Low
SW16	HPS_SDMMC_DATA1/EMAC2_RX_CTL	High	Low
SW17	HPS_SDMMC_DATA2/EMAC2_TXD0	High	Low

2.10.5 HPS Push Button

The Arria10 SoC/FPGA custom carrier board supports four HPS push buttons through Arria10 HPS I/Os. This HPS I/Os from Board to Board Connector is directly connected to HPS push buttons.

HPS I/Os status can be changed by changing the push button action. This HPS push button (SW6, SW7, SW8, SW9) is physically located at the top of the board as shown below.

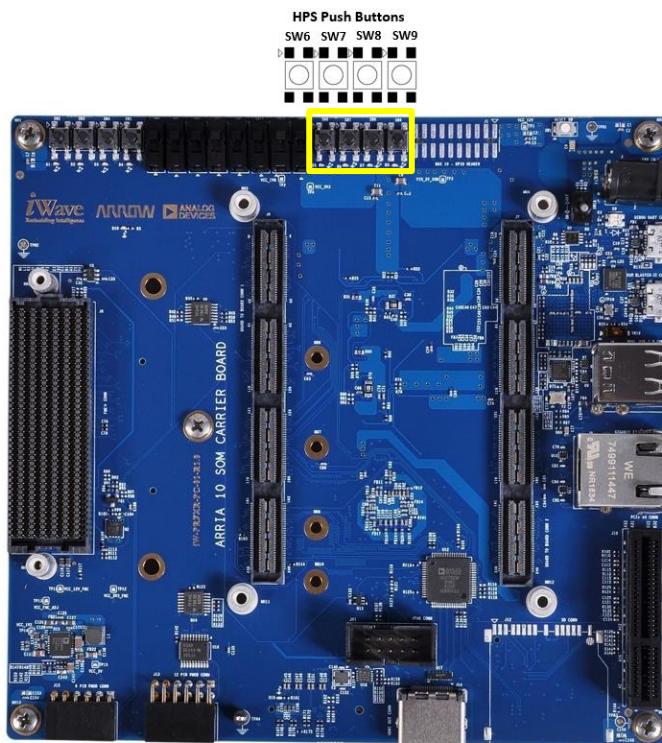


Figure 17 HPS Push Button

Table 14 HPS Push Button

HPS Sliding Switch	Signal Name	Switch Direction	
		Down	UP
SW6	HPS_SPIM0_MOSI/EMAC2_TXD3	Low	High
SW7	HPS_GPIO1/EMAC2_RXD1(GPIO1_IO19)	Low	High
SW8	HPS_GPIO2/EMAC2_RXD0(GPIO1_IO18)	Low	High
SW9	HPS_GPIO3(GPIO0_IO11)	Low	High

2.10.6 HPS LED

The Arria10 SoC/FPGA custom carrier board supports four LEDs through Arria10 HPS I/Os. This HPS I/Os from Board to Board Connector is connected to LEDs through Mosfet control switch.

LED status can be changed by driving the HPS I/Os High or Low. These LED's (D5, D6, D7, D8) are physically located at the top of the board as shown below.

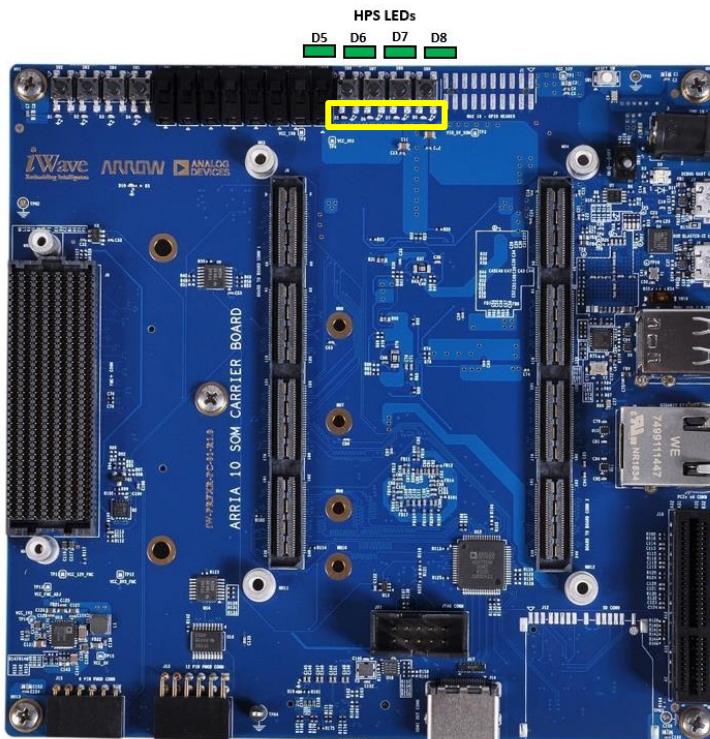


Figure 18 HPS LEDs

Table 15 HPS LEDs

LED's Name	Net Name	LED Indication	
		LOW	HIGH
D5	HPS_SDMMC_DATA0	ON	OFF
D6	HPS_SPIM0_SSO_N/EMAC2_RXD3	ON	OFF
D7	HPS_SDMMC_CMD	ON	OFF
D8	HPS_SPIM0_CLK/EMAC2_TXD2	ON	OFF

2.11 Additional Features

2.11.1 JTAG Connector

A Standard USB Blaster JTAG Header is available in Arria10 SoC/FPGA custom carrier board for debug purpose. JTAG signals from Expansion Connector2 is directly connected to JTAG Header (J11) and same JTAG signals are also connected to FMC+ connector. External USB Blaster-II programming cable can be plugged to this JTAG Header for programming and debugging purpose. This JTAG Header (J11) is physically located at the top of the board as shown below.

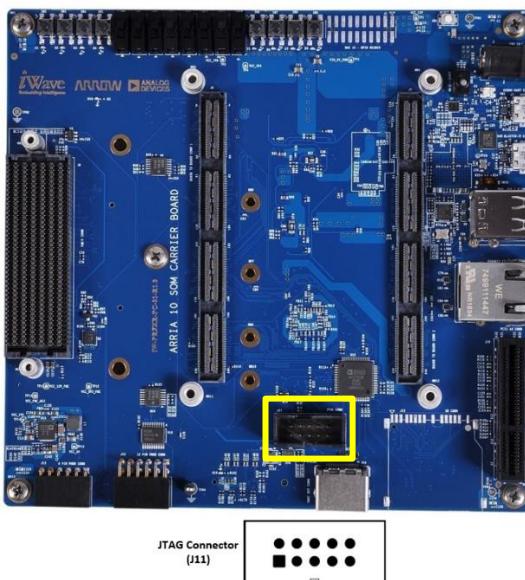


Figure 19 JTAG Header

Table 16: JTAG Header Pin Out

Pin No	Signal Name	Signal Type/ Termination	Description
1	CSS_TCK	I, 3.3V CMOS	JTAG test clock.
2	JTAG_GND	Power	Ground
3	CSS_TDO	O, 3.3V CMOS	JTAG test data Output.
4	JTAG_VCC	Power	3V3 Supply Voltage.
5	CSS_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
6	JTAG_RESETB	I, 3V3 CMOS	JTAG Reset Signal
7	NC	NC	NC
8	NC	NC	NC
9	CSS_TDI	I, 3.3V CMOS	JTAG test data Input.
10	GND	Power	Ground

2.11.2 Power ON/OFF Switch

The Arria10 SoC/FPGA custom carrier board has power ON/OFF switch (SW18) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

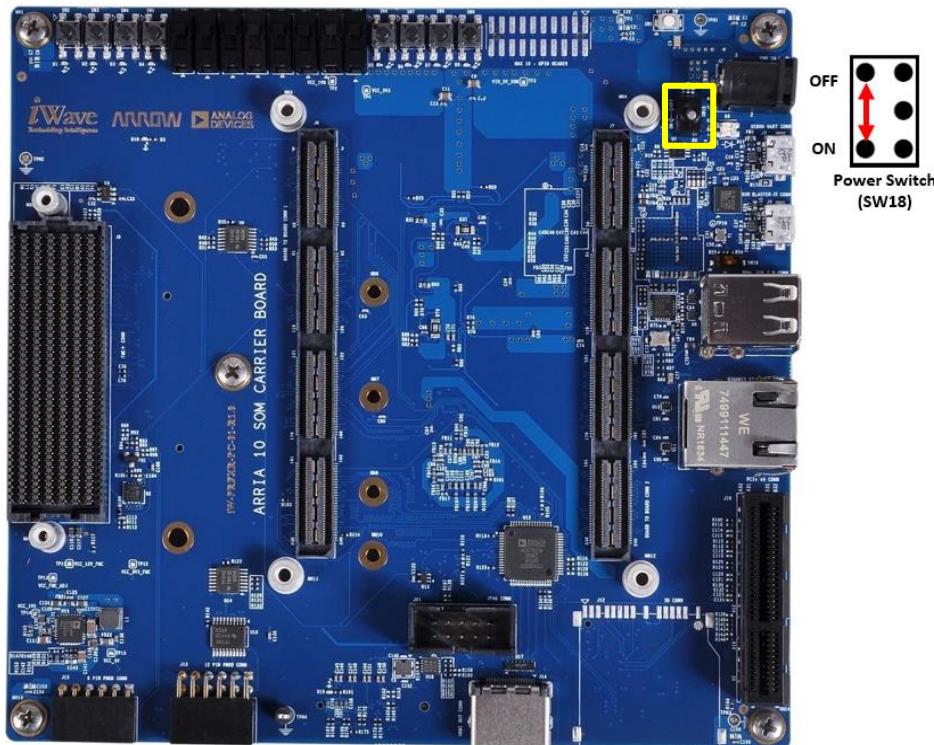


Figure 20: Power On/Off Switch

2.11.3 Reset Switch

The Arria10 SoC/FPGA custom carrier board supports Push button switch (SW1) to reset the Arria10 SoC/FPGA CPU. Reset signal of Expansion connector2 Pin 35 is directly connected from Reset Push button switch. This Reset Push button switch (SW1) is physically located at the top of the board as shown below.

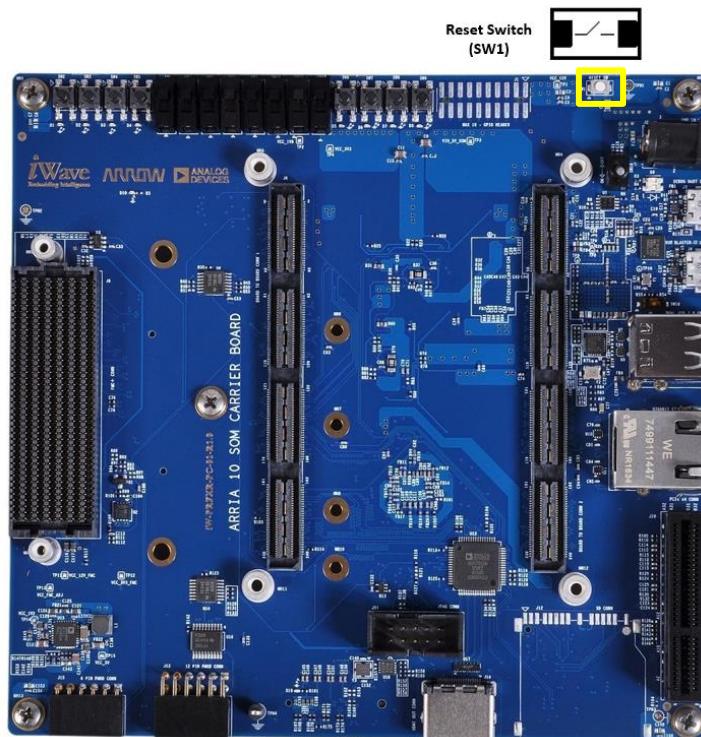


Figure 21: Reset Switch

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Arria10 SoC/FPGA custom carrier board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The Arria10 SoC/FPGA custom carrier board is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V, 5000mA power input from an external power supply is connected to the Arria10 SoC/FPGA custom carrier board through Power Jack (J2). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below

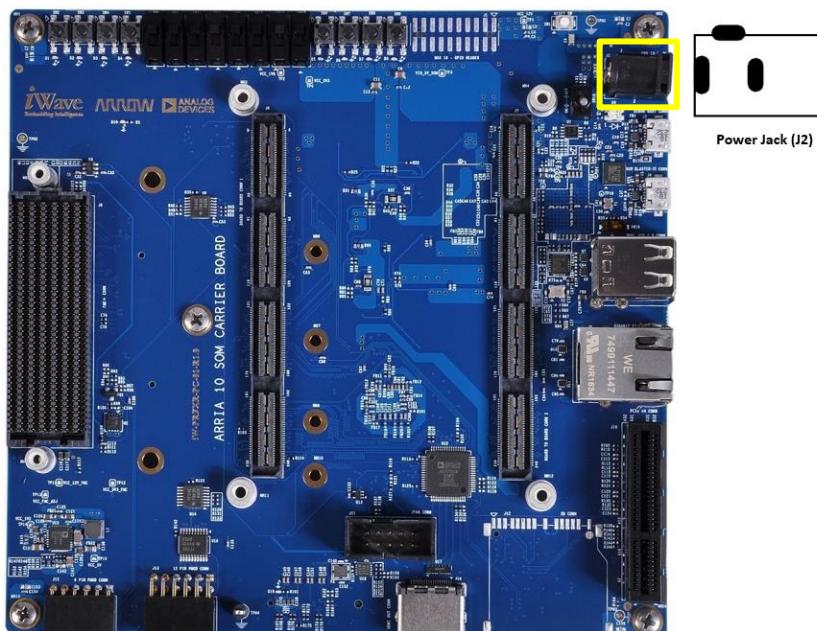


Figure 22: Power Jack

The below table provides the Power Input Requirement Arria10 SoC/FPGA custom carrier board.

Table 17: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Arria10 SoC/FPGA custom Development.

Table 18: Environmental Specification

Parameters	Min	Max
Operating temperature range	0°C	50°C

¹iWave only guarantees the component selection for the given operating temperature.

3.2.2 RoHS Compliance

iWave's Arria10 SoC/FPGA custom Development platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Arria10 SoC/FPGA custom Development platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 Arria10 SoC/FPGA custom carrier board Mechanical Dimensions

The Arria10 SoC/FPGA custom carrier board PCB form factor is 150mm x 140mm and Board mechanical dimension is shown below.

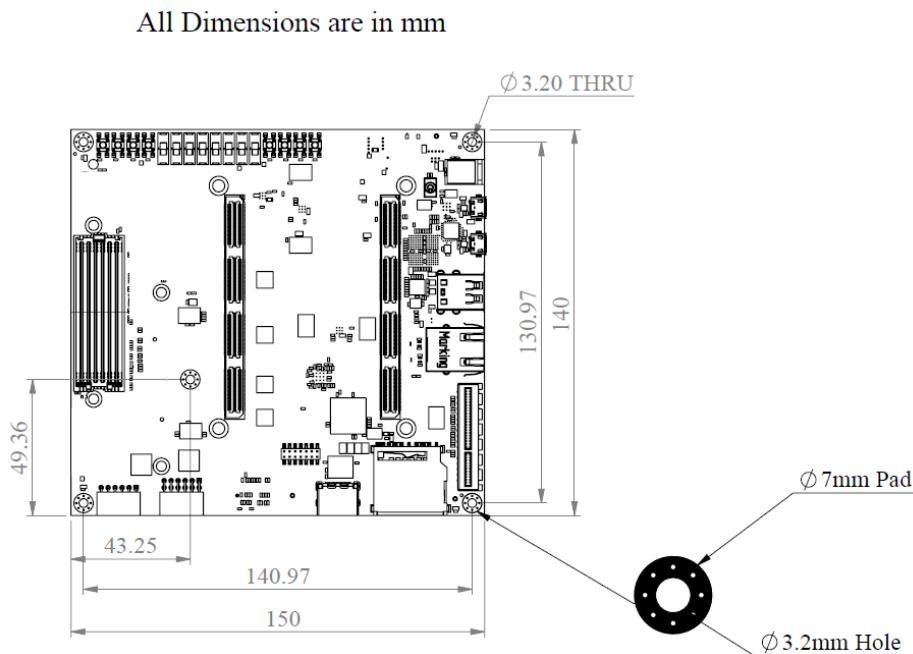


Figure 23: Arria10 SoC/FPGA custom carrier board – Top View

The Arria10 SoC/FPGA custom carrier board PCB thickness is $1.55\text{mm}\pm0.1\text{mm}$, top side maximum height component is Dual Stack USB Connector (15.91mm) and bottom side maximum height component is Inductor (9.50mm). Please refer the below figure for height details of the Arria10 SoC/FPGA custom carrier board.

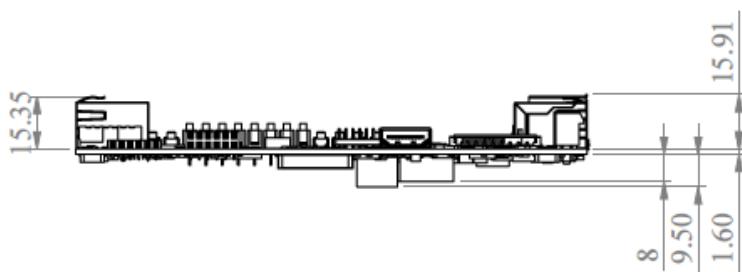


Figure 24: Arria10 SoC/FPGA custom carrier board – Side View

Note: All dimensions are shown in mm

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Arria10 SoC/FPGA custom Development platform which includes Arria10 SoC/FPGA SOM and Arria10 SoC/FPGA custom carrier board.

Table 19: Orderable Product Part Numbers

Product Part Number	Description	Temperature
TBD	TBD	
TBD	TBD	

Important Note: Please contact iWave for orderable part number of higher density/ higher speed grade/ higher memory size supported Arria10 Soc/FPGA SOM based DevKit.

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.

