=Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	1
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Student ID:	18223451

1 References

[1] *7 Series FPGAs Datasheet: Overview*, DS180 (v2.6), Xilinx Inc., 2018

[2] *Vivado Design Suite User Guide – Using the Vivado ISE*, UG893 (v2019.2), Xilinx Inc., 2019

[3] *Vivado Design Suite User Guide – Logic Simulation*, UG900 (v2019.2), Xilinx Inc., 2019

If references such as [1-3] are used, cross-reference them in your text.

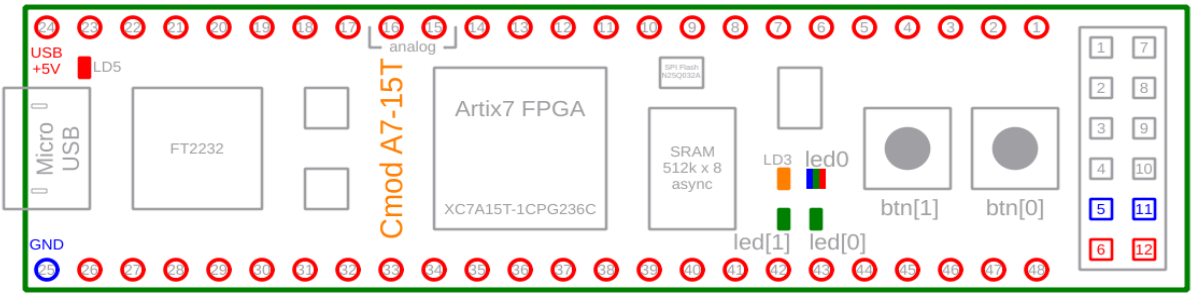

Figure 1 Package Outline Diagram of the Digilent Cmod A7 FPGA module.

2 Lab Challenges

- Challenge 1.1: Pio1=2.09V, pio9=0.41V
- Challenge 1.2: Yes, as the collector input of the BJTs is also being driven by the VDD5+ 5V power supply.
- Challenge 1.3: 1/800ns=1.25MHz
- Challenge 1.4: Segments 1,2,3,4,5,7,10 and 11 of each display have the same component values 5V/100Ω=50mA when the segment is switched on. The remaining segments 12,8 and 9 of each display have base voltage of 0.41V, collector voltage of 5V, and emitter output of 0.72V to the segments for 14.4mA each. With each added segment this totals to 886.4mA total to the displays which is 443.2mA per each fully lit display.
- Challenge 1.5: The
- Challenge 1.6: In this lab challenge I struggled with the measurements tool to more accurately calculate the frequency of the buzzer as the software sees no input to take the frequency measurement from, which I could not understand as shown below is the scope plot I was getting from the buzzer output. My estimated value of the buzzer frequency is 125Hz from the scope plot.

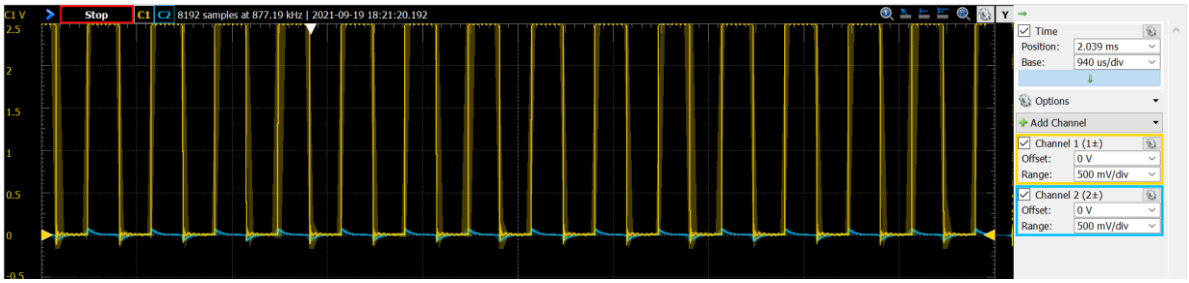

Figure 2 Scope plot of buzzer while pressed.

3 Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.