Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	09/11/2021
Lab Number:	10
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1. References

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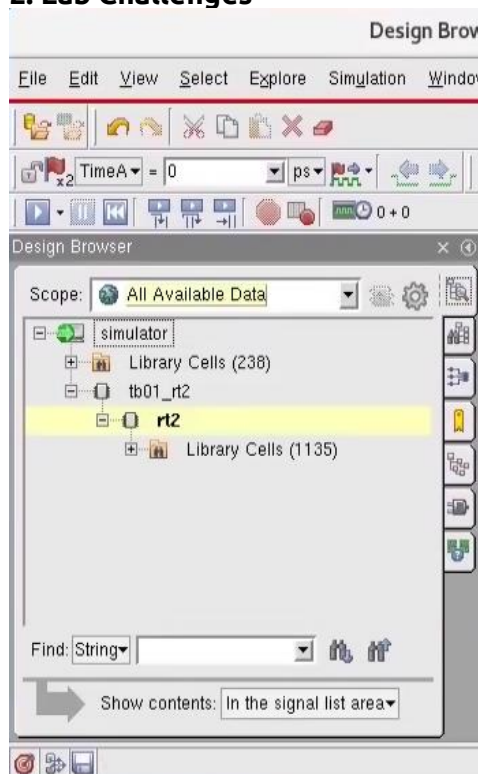
2. Lab Challenges
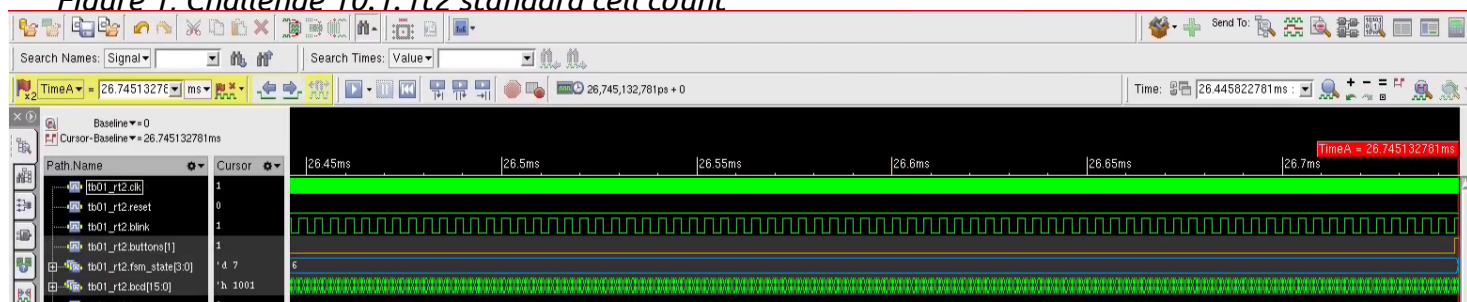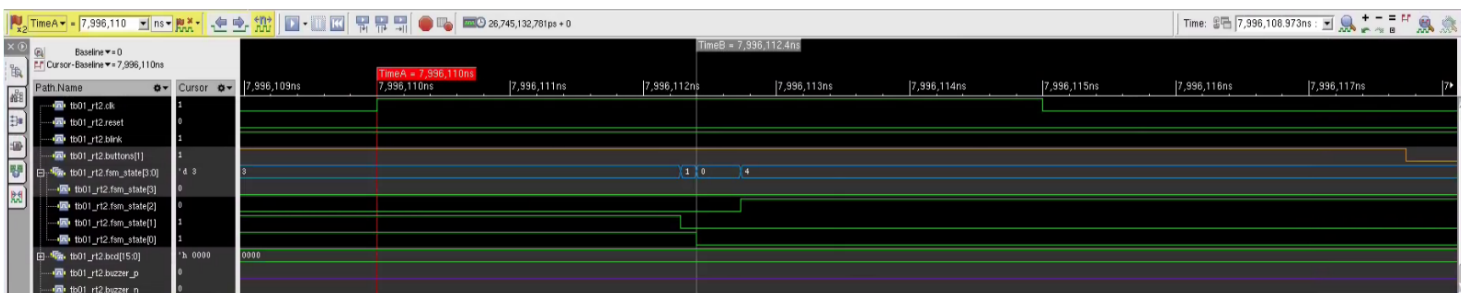

Figure 1. Challenge 10.1: rt2 standard cell count

Figure 2, Post implementation timing simulation signal response

Figure 3, Challenge 10.2 rt2 fsm state and cathodes signal and timing interval

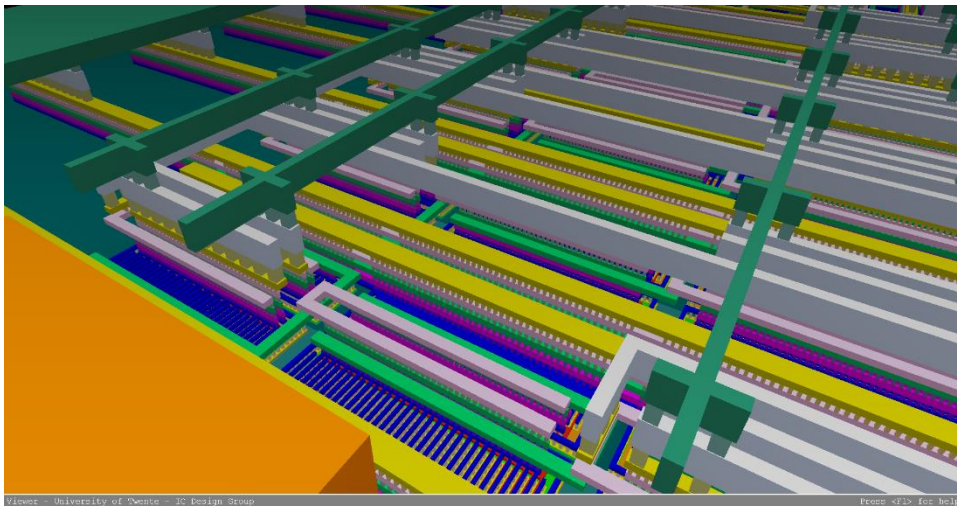*Figure 5, Challenge 10.3 rt2.gds file view in terminal*

Figure 6, GDS3D 3D view of rt2.gds top metal METTPL not shown

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.