=Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	4
Author / Student Name:	Fionn Murray
Student ID:	18223451

1 References

[1] 7 Series FPGAs Datasheet: Overview, DS180 (v2.6), Xilinx Inc., 2018

[2] Artix-7 FPGAs Datasheet: DC and AC Switching Characteristics, DS181 (v1.25), Xilinx Inc., 2018

[3] 7 Series FPGAs Clocking Resources User Guide, UG471 (v1.14), Xilinx Inc., 2018

[4] 7 Series FPGAs Configuration User Guide, UG470 (v1.13.1), Xilinx Inc., 2018 [5] Vivado Design Suite User Guide – Release Notes, Installation and Licensing, UG973 (v2020.1), Xilinx Inc., 2020

[6] Vivado Design Suite User Guide – Using the Vivado ISE, UG893 (v2019.2), Xilinx Inc., 2019

[7] Vivado Design Suite User Guide – System Level Design Entry, UG895 (v2019.2), Xilinx Inc., 2019

[8] Vivado Design Suite User Guide – Using TCL Scripting, UG894 (v2019.2), Xilinx Inc., 2019

[9] Vivado Design Suite User Guide – Logic Simulation, UG900 (v2019.2), Xilinx Inc., 2019

[10] Vivado Design Suite User Guide – Synthesis, UG901 (v2019.2), Xilinx Inc., 2019

[11] Vivado Design Suite User Guide – Implementation, UG904 (v2019.2), Xilinx Inc., 2019

[12] Vivado Design Suite User Guide – Using Constraints, UG903 (v2019.2), Xilinx Inc., 2019

[13] Vivado Design Suite Overview [Online]. Available: https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html

[14] Revision control system git [Online]. Available: https://git-scm.com/

[15] Digilent Inc. (2020, June, 27), Cmod A7 Reference Manual: https://reference.digilentinc.com/reference/programmablelogic/cmod-a7/reference-manual.Lab Challenges

Challenge 4.1:

```
// Info for CmodA7-15T using XC7A15T-1CPG236C
// ================================================
// External clock generator produces 12MHz and delivers schematic signal GCLK to FPGA pin L17 (in Bank 14)
// fclkin=12MHz, translating into Tclkin=83.333ns (attribute .CLKIN1_PERIOD in ps resolution)
//  => .CLKIN1_PERIOD(83.333)
// fvco=600MHz (in order to achieve 100MHz target frequency, and derived frequencies). Can't go higher as M is restricted to 2<=M<=64
```

Challenge 4.2

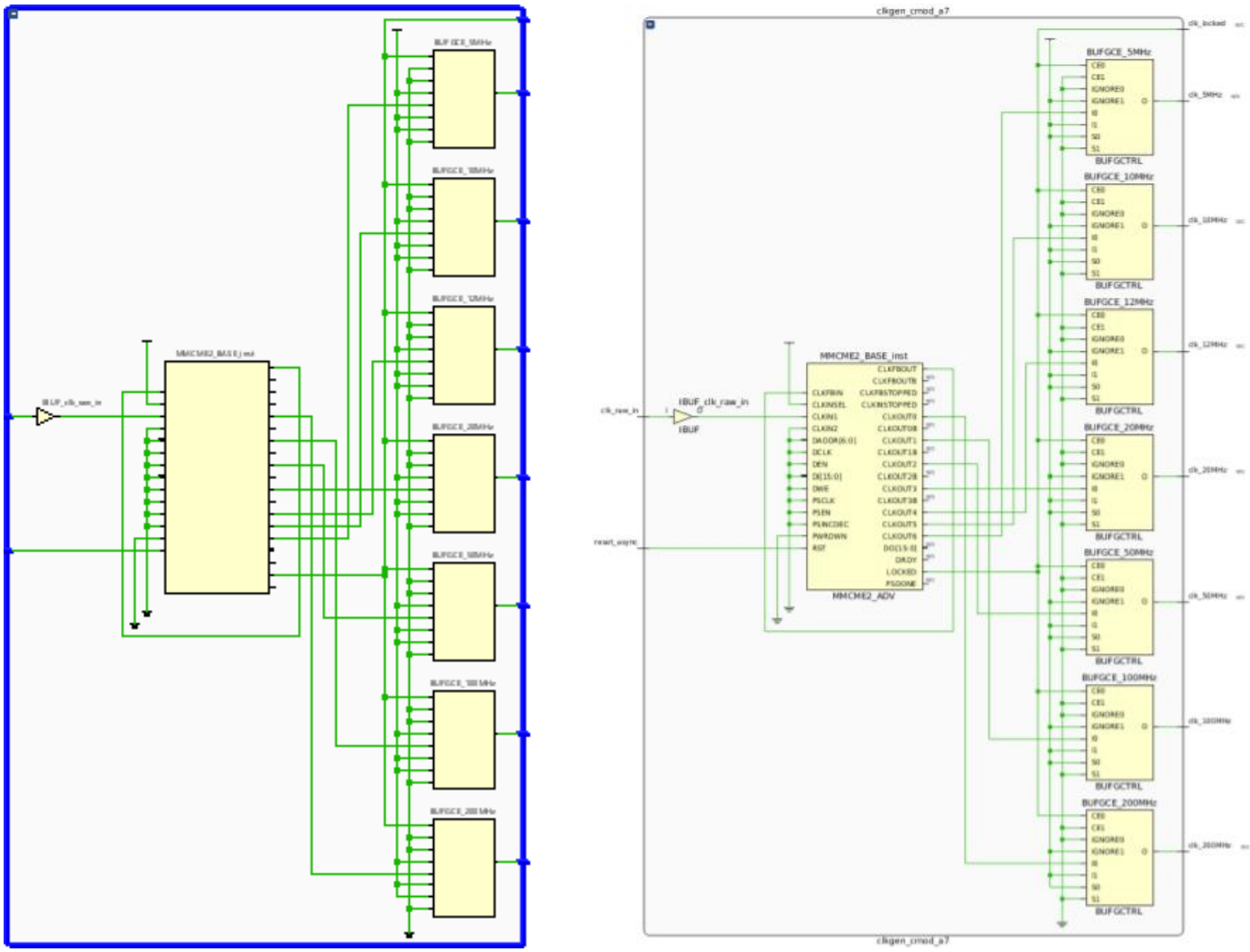
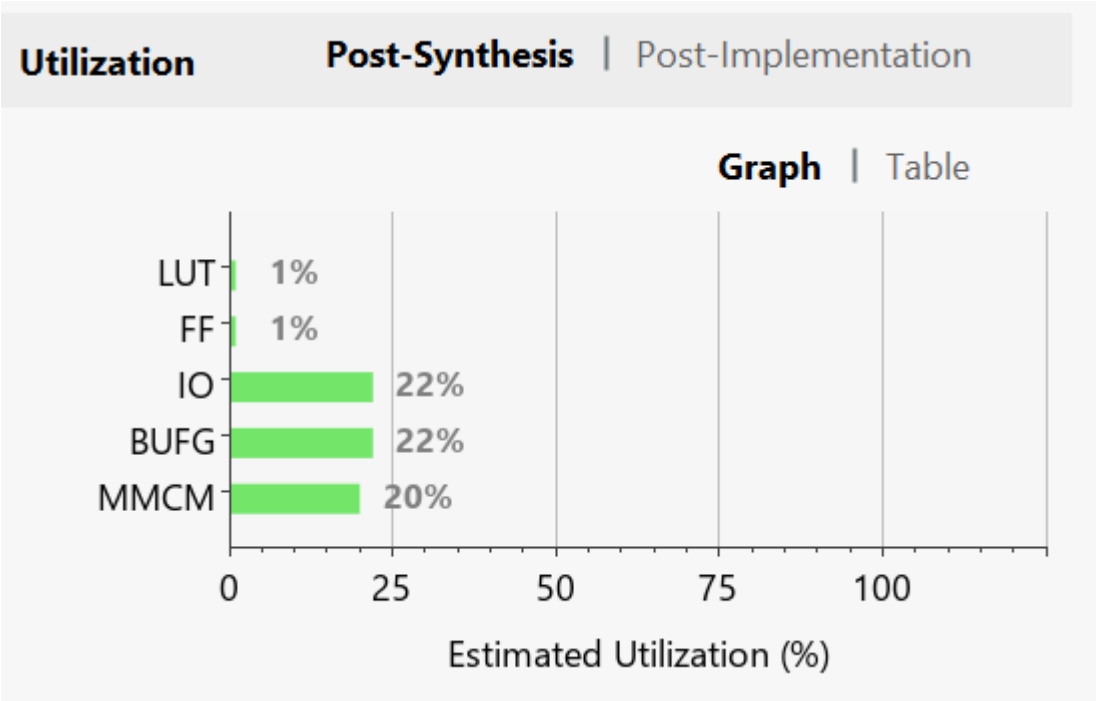
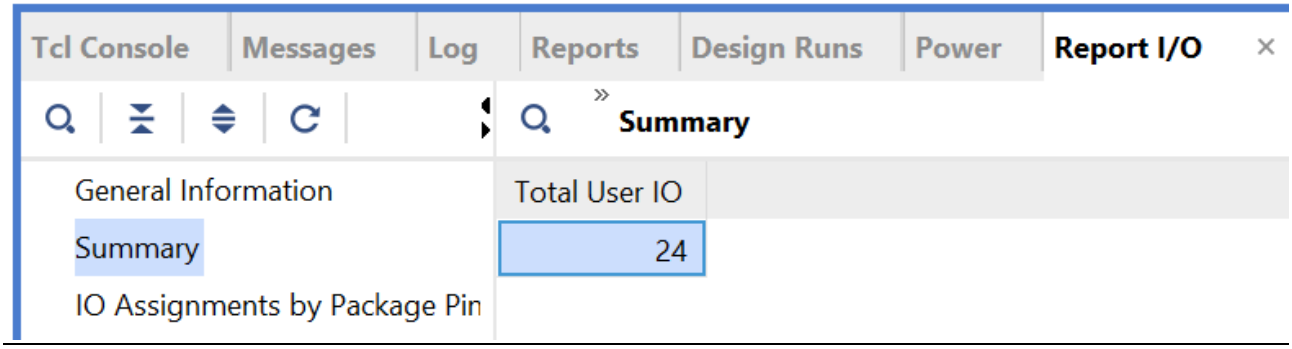


Figure 1, clkgen_cmod_a7 Schematic

Challenge 4.3





24 total ports being used out of 106=22% is correct.

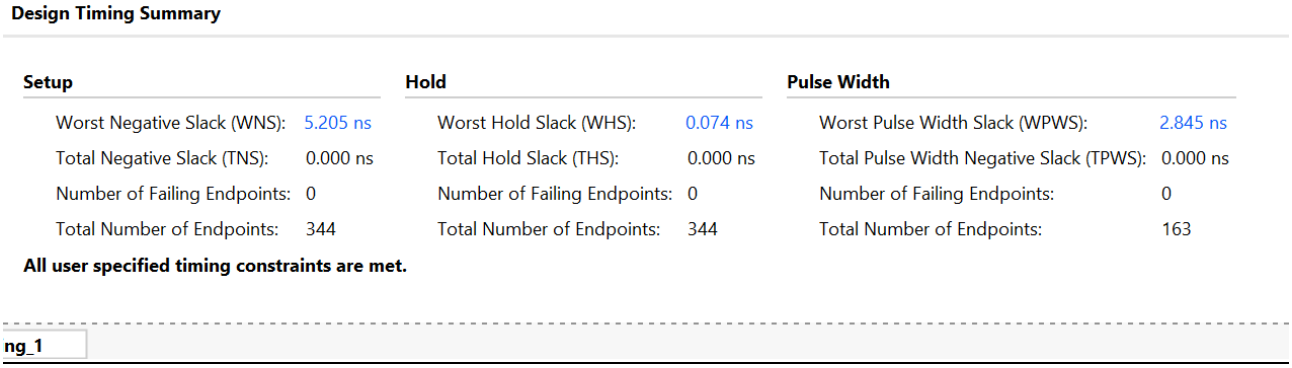


Figure 2, Design Timing Summary

Challenge 4.4

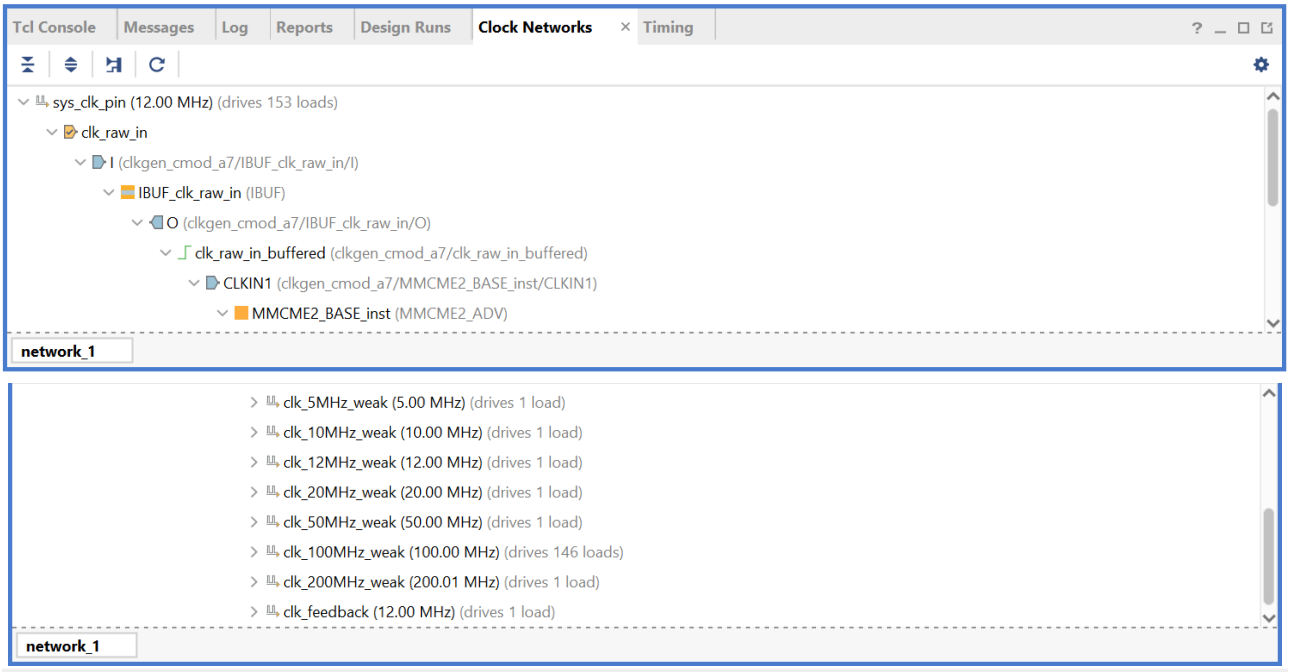


Figure 3, Synthesis timing report, Clock Networks

clk_100MHz shows to be driving 146 loads here as the rt2 design is only making use of 100MHz signal as its main clock routed to input port clk of the main module rt2, and from there passed on to all lower-level building blocks of the design.

Challenge 4.5

The Slice LUTS module has the most (239) registers consumed.

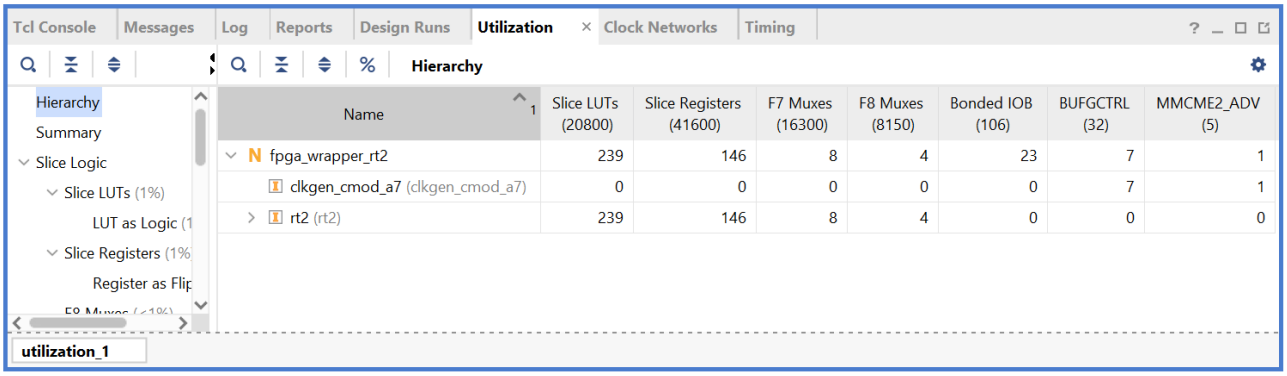


Figure 4, Utilization report

Challenge 4.6

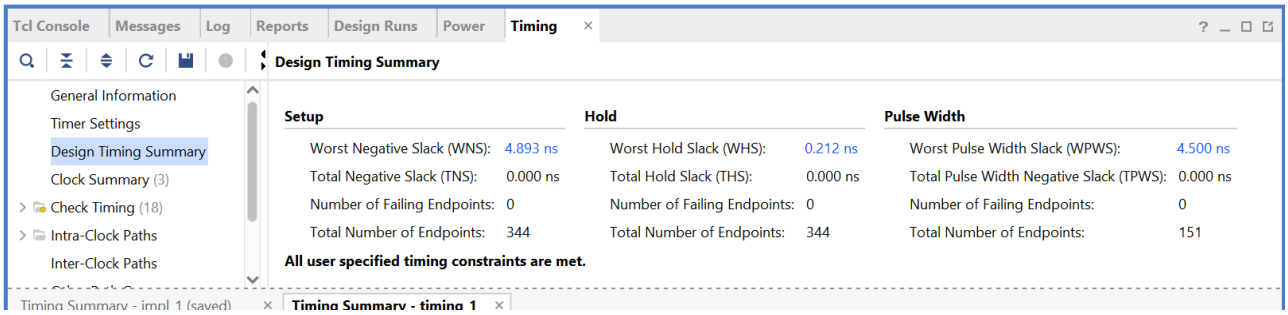


Figure 5, Design Implementation Timing Summary

Challenge 4.7

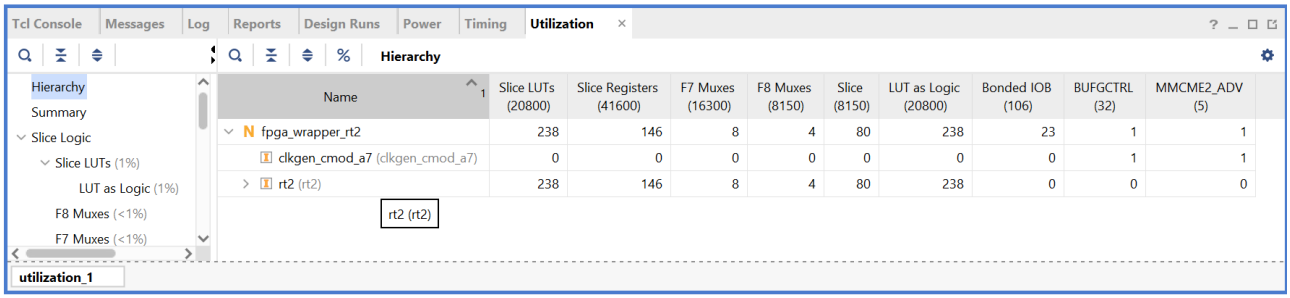


Figure 6, Design Implementation Utilization Report

Challenge 4.8

Report I/O

IO Assignments by Package Pin

Pin Number	Signal ...	Bank Type	Pin Name	Use	IO Standard	IO Bank	Drive (mA)	Slew
P1	pio23	High Range	IO_L19N_T3_VREF_35	OUTPUT	LVCMOS33	35	12	SLOW
N2	pio22	High Range	IO_L10P_T1_AD15P_35	INPUT	LVCMOS33	35		
L2	pio14	High Range	IO_L5N_T0_AD13N_35	OUTPUT	LVCMOS33	35	12	SLOW
L1	pio13	High Range	IO_L6N_T0_VREF_35	OUTPUT	LVCMOS33	35	12	SLOW
K2	pio12	High Range	IO_L5P_T0_AD13P_35	OUTPUT	LVCMOS33	35	12	SLOW
J1	pio11	High Range	IO_L3N_T0_DQS_AD5N_35	OUTPUT	LVCMOS33	35	12	SLOW
J3	pio10	High Range	IO_L7P_T1_AD6P_35	OUTPUT	LVCMOS33	35	12	SLOW
A14	pio9	High Range	IO_L6P_T0_16	OUTPUT	LVCMOS33	16	12	SLOW
B15	pio8	High Range	IO_L11N_T1_SRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
A15	pio7	High Range	IO_L6N_T0_VREF_16	OUTPUT	LVCMOS33	16	12	SLOW
H1	pio6	High Range	IO_L3P_T0_DQS_AD5P_35	OUTPUT	LVCMOS33	35	12	SLOW
C15	pio5	High Range	IO_L11P_T1_SRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
K3	pio4	High Range	IO_L7N_T1_AD6N_35	OUTPUT	LVCMOS33	35	12	SLOW
A16	pio3	High Range	IO_L12P_T1_MRCC_16	OUTPUT	LVCMOS33	16	12	SLOW

IO Assignments by Package Pin

Pin Number	Signal ...	Bank Type	Pin Name	Use	IO Standard	IO Bank	Drive (mA)	Slew
L3	pio2	High Range	IO_L8P_T1_AD14P_35	OUTPUT	LVCMOS33	35	12	SLOW
M3	pio1	High Range	IO_L8N_T1_AD14N_35	OUTPUT	LVCMOS33	35	12	SLOW
C16	led[1]	High Range	IO_L13P_T2_MRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
A17	led[0]	High Range	IO_L12N_T1_MRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
C17	led0_r	High Range	IO_L14P_T2_SRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
B16	led0_g	High Range	IO_L13N_T2_MRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
B17	led0_b	High Range	IO_L14N_T2_SRCC_16	OUTPUT	LVCMOS33	16	12	SLOW
L17	clk_raw_in	High Range	IO_L12P_T1_MRCC_14	INPUT	LVCMOS33	14		
B18	btn[1]	High Range	IO_L19P_T3_16	INPUT	LVCMOS33	16		
A18	btn[0]	High Range	IO_L19N_T3_VREF_16	INPUT	LVCMOS33	16		
A1			GND	GND				
A2			MGTPTXN1_216	Gigabit				
A3			GND	GND				
A4			MGTPRXN0_216	Gigabit				

Figure 7, I/O relevant to the rt2 design

Challenge 4.9

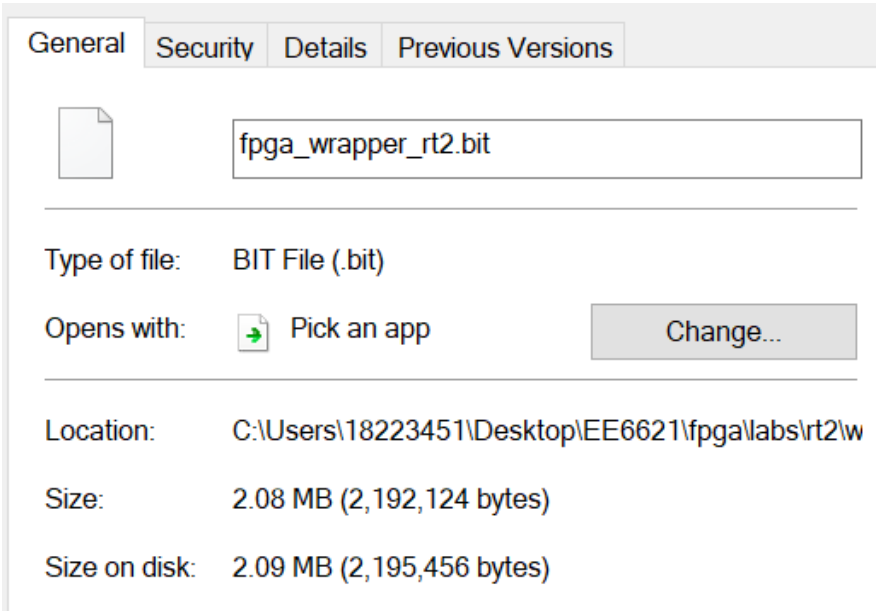


Figure 8, Generated Bitstream file properties

Challenge 4.10

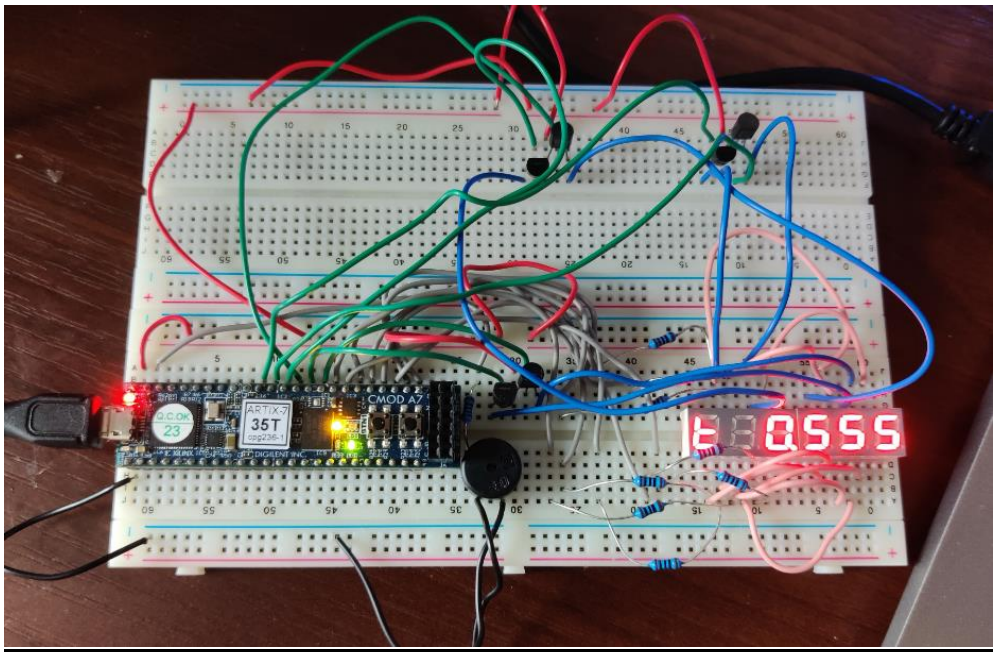


Figure 9, Test Bench Verification

Test	**Pass/Fail**
Display shows UL	Pass
Display shows UL ECE	Pass
Display shows EE6621	Pass
Display shows rt2	Pass
Display enters ready state on PB press at rt2 display	Pass
Display enters steady mode before entering measurement mode	Pass
Display enters cheat mode if PB is pressed before steady mode has ended	Pass
Display timer stops after a press of PB	Pass

Figure 10, Table Of Tests for rt2 based on functional descriptive specification

Challenge 4.11

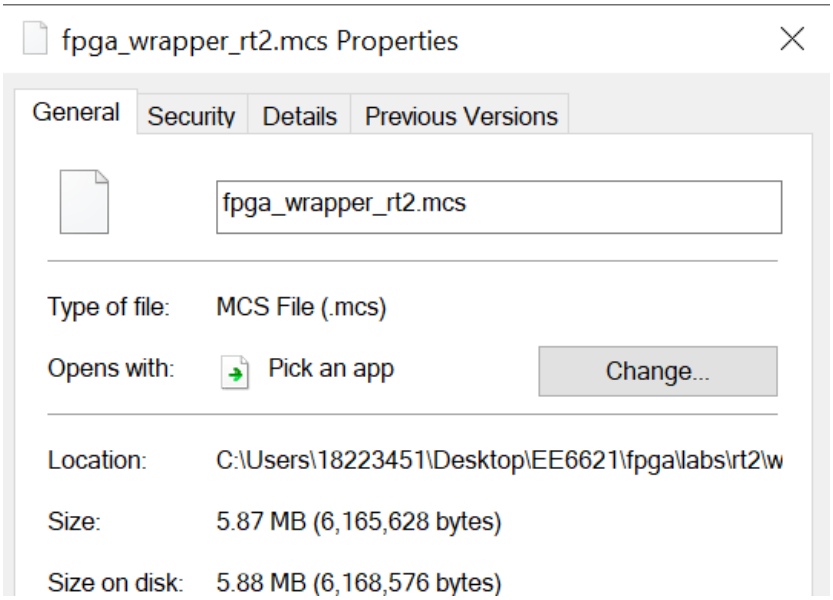


Figure 11, Memory config MCS file properties

Challenge 4.12

Figure 12, Second Table Of Tests for rt2 based on functional descriptive specification after flashing fpga module

Test	**Pass/Fail**
Display shows UL	Pass
Display shows UL ECE	Pass
Display shows EE6621	Pass
Display shows rt2	Pass
Display enters ready state on PB press at rt2 display	Pass
Display enters steady mode before entering measurement mode	Pass
Display enters cheat mode if PB is pressed before steady mode has ended	Pass
Display timer stops after a press of PB	Pass

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.