

=Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	3
Author / Student Name:	Fionn Murray
Student ID:	18223451

## 1 References

- [1] Digilent Inc. (2020, June, 27), Cmod A7 Reference Manual: <https://reference.digilentinc.com/reference/programmablelogic/cmod-a7/reference-manual>.
- [2] 7 Series FPGAs Datasheet: Overview, DS180 (v2.6), Xilinx Inc., 2018
- [3] Artix-7 FPGAs Datasheet: DC and AC Switching Characteristics, DS181 (v1.25), Xilinx Inc., 2018
- [4] 7 Series FPGAs Clocking Resources User Guide, UG471 (v1.14), Xilinx Inc., 2018
- [5] 7 Series FPGAs Configuration User Guide, UG470 (v1.13.1), Xilinx Inc., 2018
- [6] Vivado Design Suite User Guide – Release Notes, Installation and Licensing, UG973 (v2020.1), Xilinx Inc., 2020
- [7] Vivado Design Suite Overview [Online]. Available: <https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html>
- [8] Geany – The Flyweight IDE [Online]. Available: <https://www.geany.org/>

## 2 Lab Challenges

```

C:\Users\18223451\Desktop\EE6621\FPGA\labs\rt2>git status
On branch master
Your branch is up to date with 'origin/master'.

nothing to commit, working tree clean

C:\Users\18223451\Desktop\EE6621\FPGA\labs\rt2>git log -n 20 --pretty=oneline
668e41a8d2c6b6f1a82ead2f622a5e9bbabab61 (HEAD -> master, origin/master, origin/HEAD) memory configuration file for macronix added (2)
a028161b76e63661ba74174e869d98d879f32ea memory configuration file for macronix added
38a12d1c4c8b1200a068f7e40b10ae16852f1729 minor vivado amendments
d232c052393d924d54ae7cc3f9d8e80b68ff5f96 rt2 hardware mods (ay2021/22)
7493bfa62fe7de6d406b5e63c8b18f919a01740 innovus script bugs removed
23942c1839011e4f4ef6d077c4002c1b9b0ef4 innovus v2 (power plan bug removed)
1326f542f6c9e3ef988045e79abb88e28bea3798 innovus tcl added
a08032887e758f98619f98332f4803f582b2f331 bug in innovus_mmc.tcl resolved
164fbc846d278428d7cfa76de2eab63fb7520f70 typo removed
3ca6f10670f9946c2d4c03370748a859d6ad5ab1 typo in tb01_fpga_wrapper_rt2.v
2b2639aceb64d6ca234ec30f4ab98f03c2cb27e2 innovus scripts updated
7b057f7c7f3f8bad32995a7f6979bf12ce7caa68 gds files added
13bf3b16457c9e0e261cedd9e9a9b5987c2fde55 fan waveform configuration added
3cc02012f4c4ca6100f699ffcc0a0296e920d0e6d merge
a6ab7666ee88653aa8fa32ea257a4169f6c37d5 rename elaborate script
ce22ba3770728a9a7004781bab046e9bf6043 wrapper test bench refined
28399c58af33fac2a149cc48dd159331133400 wrapper test bench added
68bb6aa7d47f1710b65fa980d64d9ef96509d8b2 1st and 3st support added
44ee992c2c8bcd587c7fd4166162af3b3e7f8a8d gds3d tech definition added
fdd13d10a4bbaebd33d72c85a7987a6593cccd updates

```

Figure 1, Challenge 3.1 Design's commit log to date of run command

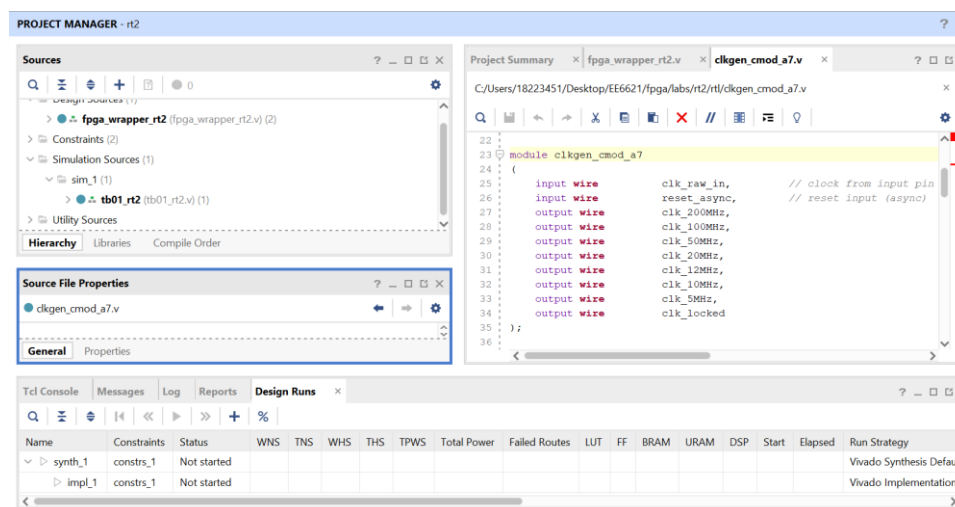


Figure 2, Challenge 3.2 Vivado Project and Sources window

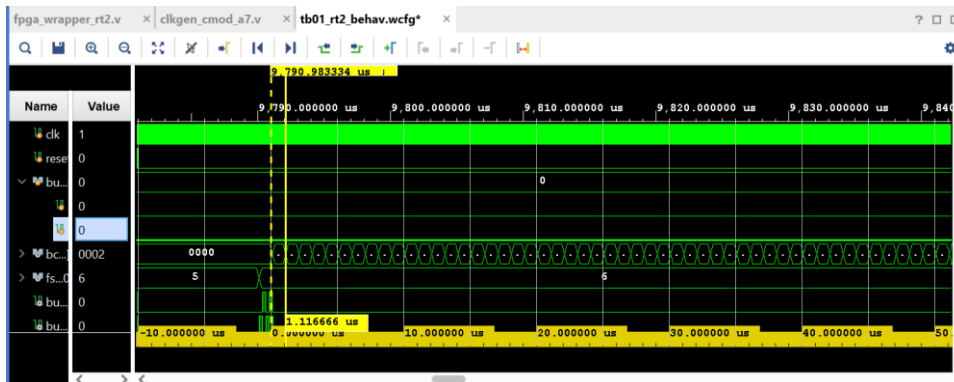


Figure 3, Challenge 3.3

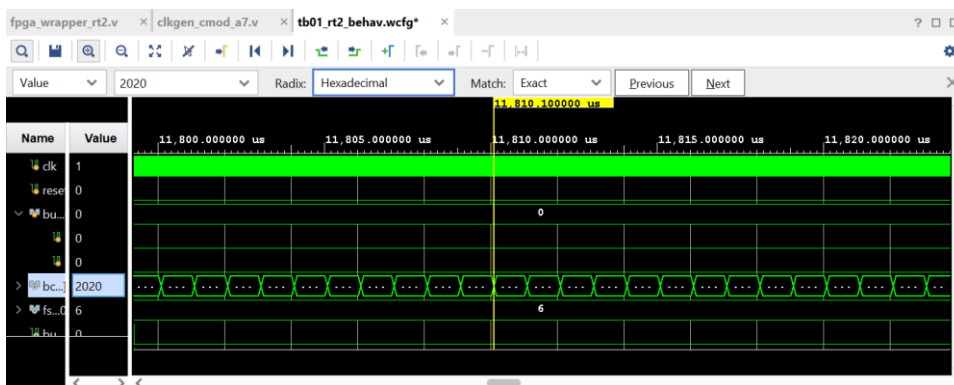


Figure 4, Challenge 3.4

The hexadecimal radix is most meaningful to this HDL object as it simplifies how the binary data is represented – ie an 8bit binary digit vs a 2 digit hex value.

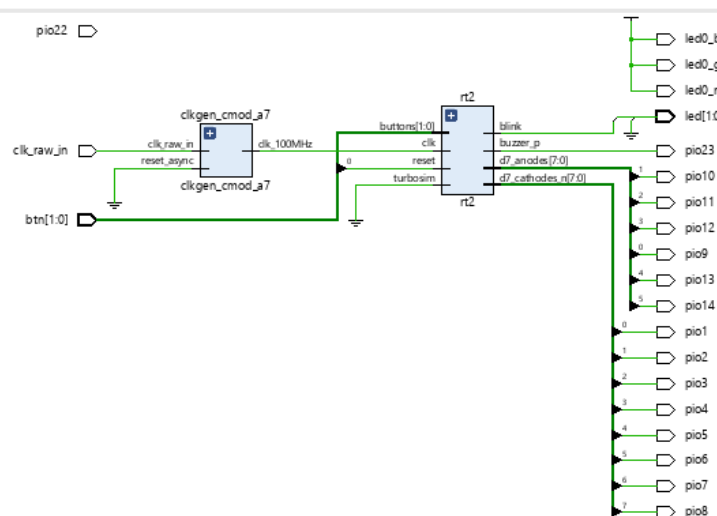


Figure 5, Hierarchical Schematic

---

### 3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.