=Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	2
Author / Student Name:	Fionn Murray
Student ID:	18223451

1 References

[1] Digilent Inc. (2020, June, 27), Cmod A7 Reference Manual: https://reference.digilentinc.com/reference/programmablelogic/cmod-a7/reference-manual.

[2] 7 Series FPGAs Datasheet: Overview, DS180 (v2.6), Xilinx Inc., 2018

[3] Artix-7 FPGAs Datasheet: DC and AC Switching Characteristics, DS181 (v1.25), Xilinx Inc., 2018

[4] 7 Series FPGAs Clocking Resources User Guide, UG471 (v1.14), Xilinx Inc., 2018

[5] 7 Series FPGAs Configuration User Guide, UG470 (v1.13.1), Xilinx Inc., 2018

[6] Vivado Design Suite User Guide – Release Notes, Installation and Licensing, UG973 (v2020.1), Xilinx Inc., 2020

[7] Vivado Design Suite Overview [Online]. Available: https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html

[8] Geany – The Flyweight IDE [Online]. Available: https://www.geany.org/

2 Lab Challenges

The purpose of this lab is to install Xilinx Vivado Design Suite, test vivado: Setting Up a New FPGA Project, FPGA programming, Flashing the FPGA module and installation of multi-tab editor (geany).

Throughout this lab I had no problems installing media on my windows operating software, however I struggled with issues completing the installation on Linux.
The Vivado software worked on windows to flash onto the FPGA module and I have so far seen no issues with windows.

debounce.v | display_7s.v | fpga_wrapper_test01.v | synchroniser_3s.v | test01.v

```
1  //////////////////////////////////////////////////////////////////////////////////
2  // University of Limerick
3  // Design: EE6621 rt2. Test bench focusing on the FSM.
4  // Author: Karl Rinne
5  // Create Date: 23/06/2020
6  // Design Name: generic
7  // Revision: 1.0
8  //////////////////////////////////////////////////////////////////////////////////
9
10 // References
11 // [1] IEEE Standard Verilog Hardware Description Language, IEEE Std 1364-2001
12 // [2] Verilog Quickstart, 3rd edition, James M. Lee, ISBN 0-7923-7672-2
13 // [3] S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition
14
15 // [10] Digilent "Nexys4 DDR FPGA Board Reference Manual", 11/04/2016, Rev C
16 // [11] Digilent "Nexys4 DDR Schematic", 06/10/2014, Rev C.1
17
18 `include "timing.v"
19
20 module tb01_test01;
21
22     reg         clk;
23     reg         reset;
24     reg [1:0]   buttons;            // {L,R}
25
26     // 7-segment display
27     wire [7:0]  d7_cathodes_n;
28     wire [7:0]  d7_anodes;
29     wire        blink;
30     wire        buzzer_p;
31     wire        buzzer_n;
32
33     // tb general purpose integer variables
34     integer     i0, i1;
35     integer     error counter;
```

Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.

