Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	09/11/2021
Lab Number:	9
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Student ID:	18223451

1. References

[1] Cadence: Overview of Running the Incisive Enterprise Simulator [Online]. Available: Through the Cadence Incisive help system.
[2] Cadence: Compiling Verilog Source Files [Online]. Available: Through the Cadence Incisive help system.
[3] Cadence: Elaborating Your Design [Online]. Available: Through the Cadence Incisive help system.
[4] Cadence: Simulating Your Design [Online]. Available: Through the Cadence Incisive help system.
[5] Cadence: Using the Incisive Simulator Utilities [Online]. Available: Through the Cadence Incisive help system.
[6] Cadence: SimVision Introduction [Online]. Available: Through the Cadence Incisive help system.
[7] Cadence: SimVision: Using the FSM Window [Online]. Available: Through the Cadence Incisive help system.

2. Lab Challenges

```
@(#)CDS: Innovus v17.11-s080_1 (64bit) 08/04/2017 11:13 (Linux 2.6.18-194.el5)
@(#)CDS: NanoRoute 17.11-s080_1 NR170721-2155/17_11-UB (database version 2.30, 390.7.1) {superthreading v1.44}
@(#)CDS: AAE 17.11-s034 (64bit) 08/04/2017 (Linux 2.6.18-194.el5)
@(#)CDS: CTE 17.11-s053_1 () Aug  1 2017 23:31:41 ( )
@(#)CDS: SYNTECH 17.11-s012_1 () Jul 21 2017 02:29:12 ( )
@(#)CDS: CPE v17.11-s095
@(#)CDS: IQRC/TQRC 16.1.1-s215 (64bit) Thu Jul  6 20:18:10 PDT 2017 (Linux 2.6.18-194.el5)
@(#)CDS: OA 22.50-p063 Fri Feb  3 19:45:13 2017
@(#)CDS: SGN 10.10-p124 (19-Aug-2014) (64 bit executable)
@(#)CDS: RCDB 11.10
```

Figure 1, Innovus version command output

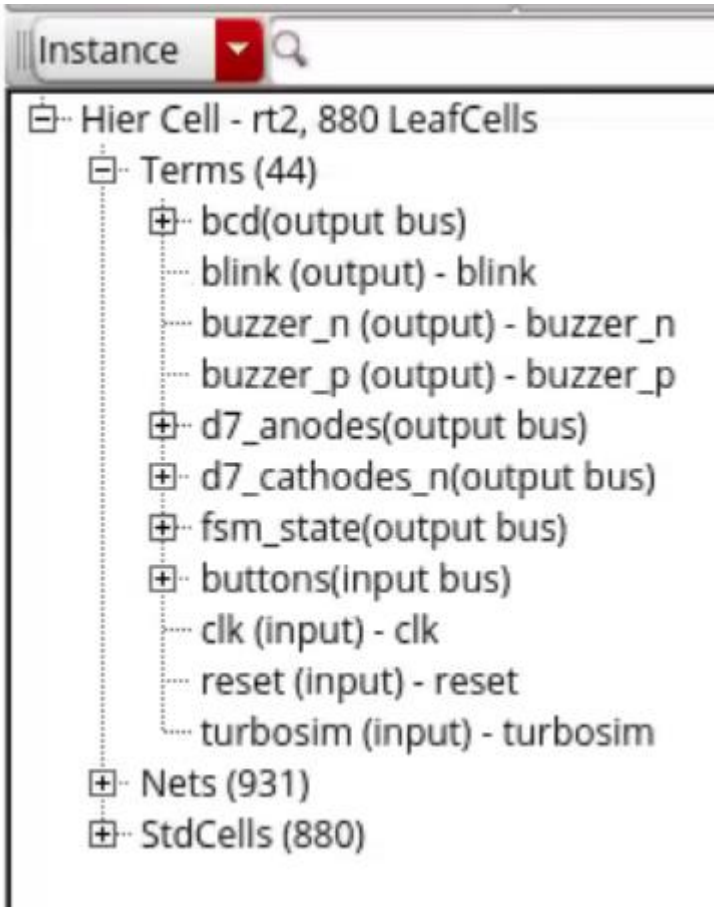

Figure 2, Design browser terms

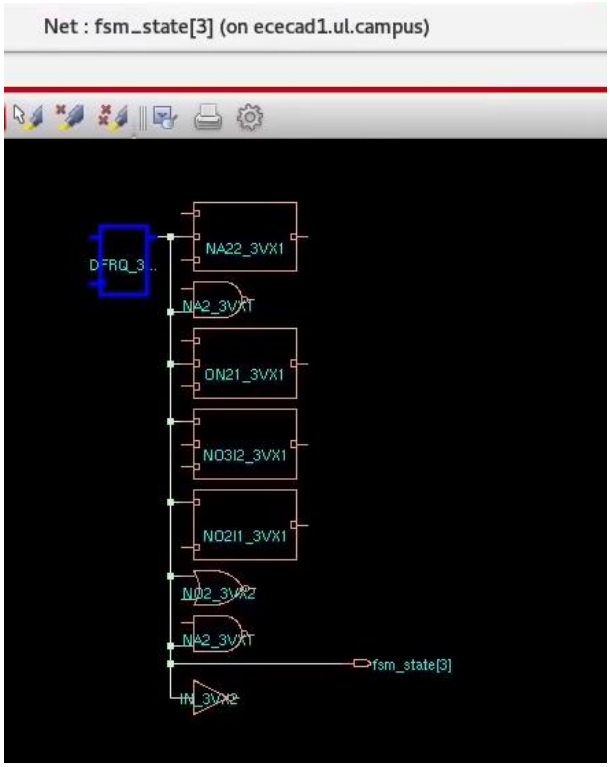

Figure 3, Crtitical path schematic

9 inputs are driven by the output controlling the net in figure 3.

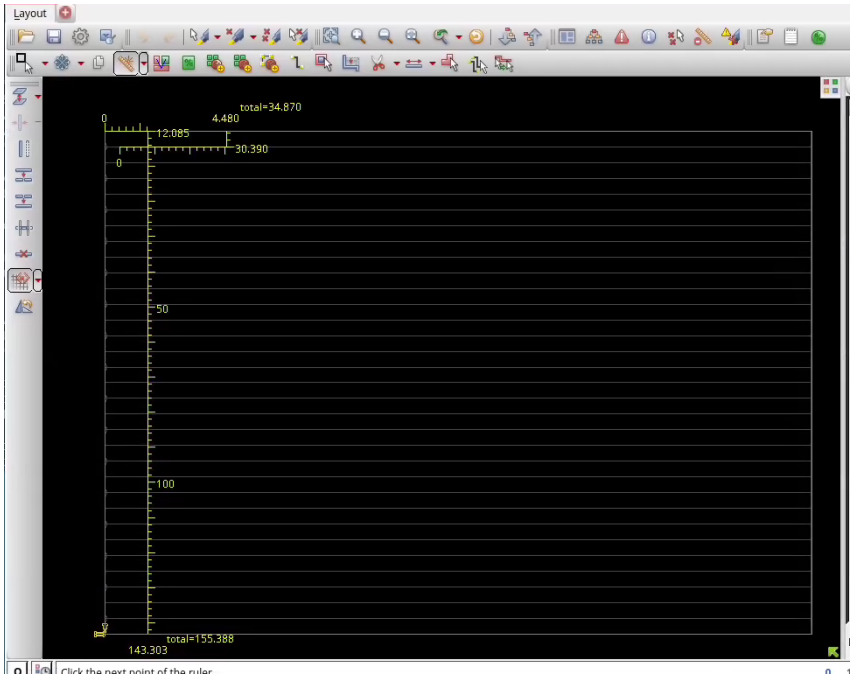

Figure 4, Measuring the common height of each cell: 4.48um

Figure 5, Overall core area measured

$$Estimated\ area: 30150um^2$$
$$Total\ actual\ area:$$
$$201.040 * 143.360 = 28821.0944um^2$$

Knowing the number of standard cells per row is important to design as you can predict the end design when you can measure the area and space allotted for standard cells in each row.

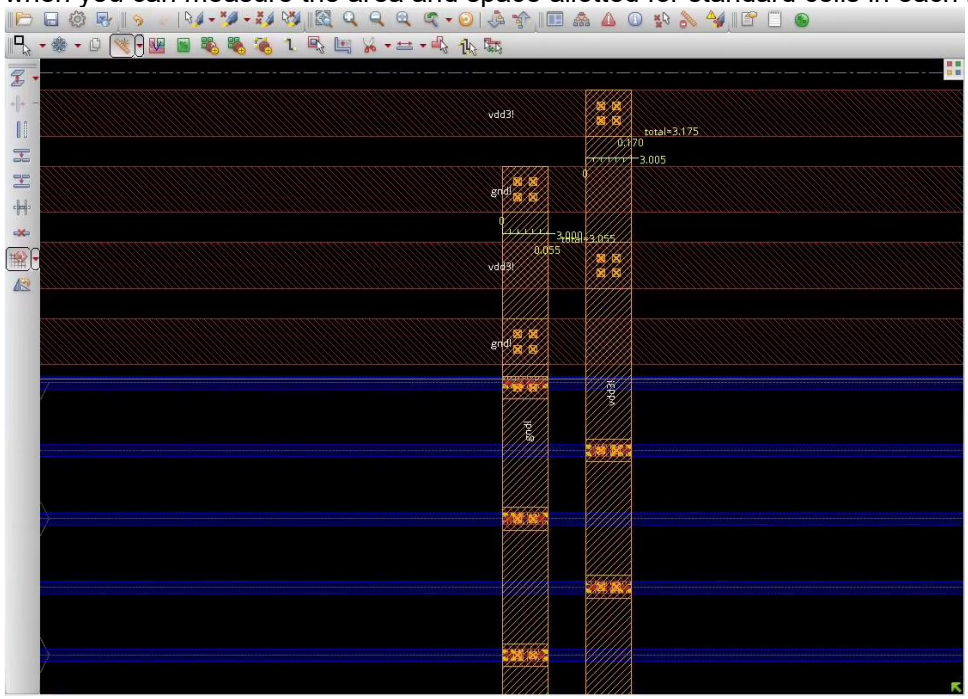

Figure 6, Horizontal supply strips

In figure 6 we see red supply strips labelled METTP5 metal as an outer layer to the core of the design. These metal layers acta as a ground and supply to the design and must have higher integrity than the metal used inside the core

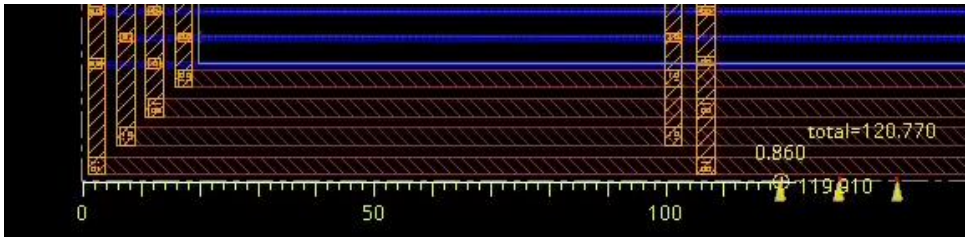

Figure 7, Measure of distance between left edge and clock pin

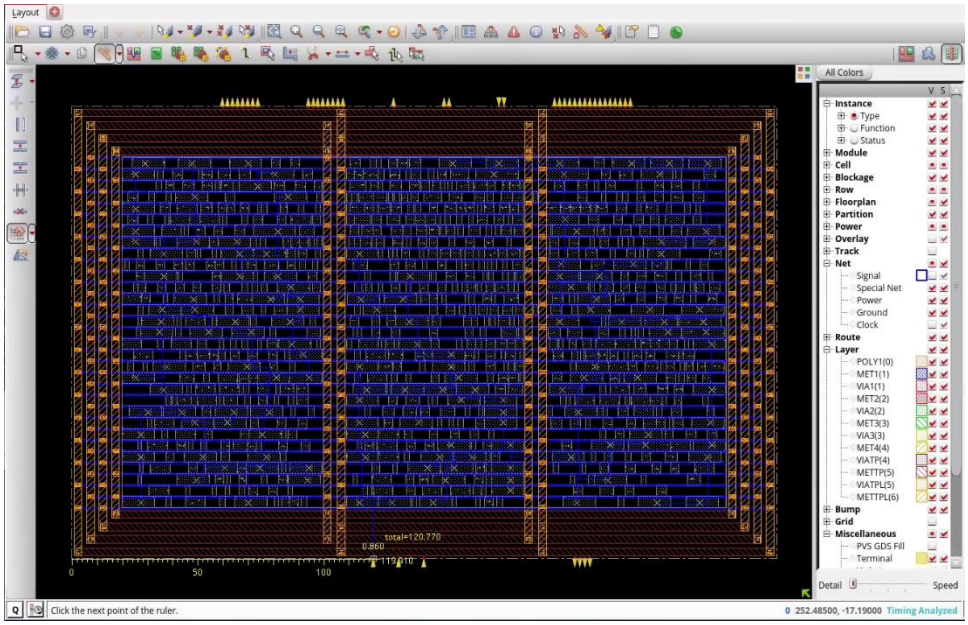

Figure 8, Clear image of how the cells were placed by the script with metal layers and cell text hidden

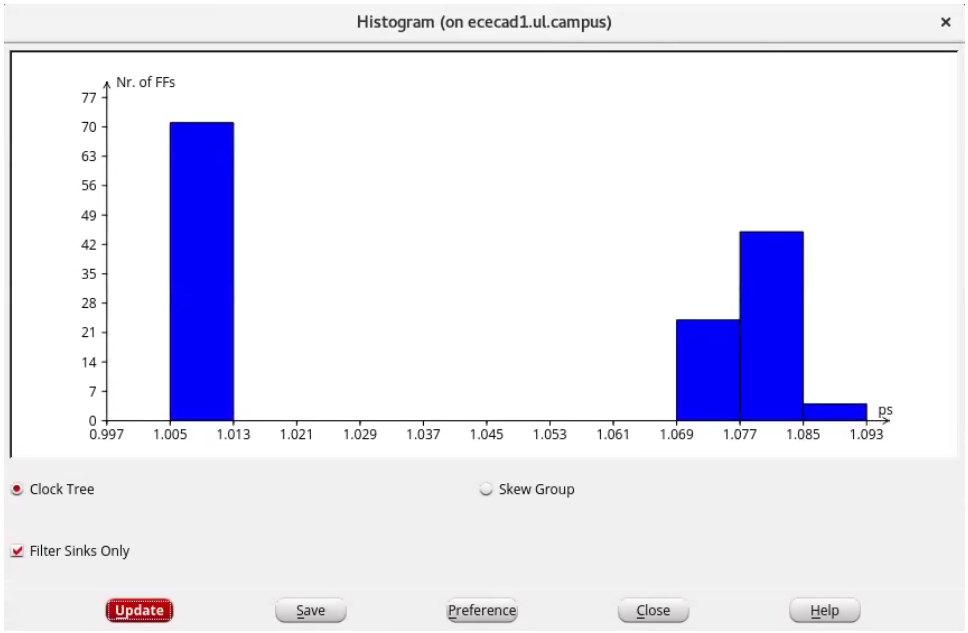

Figure 9, Clock skew histogram

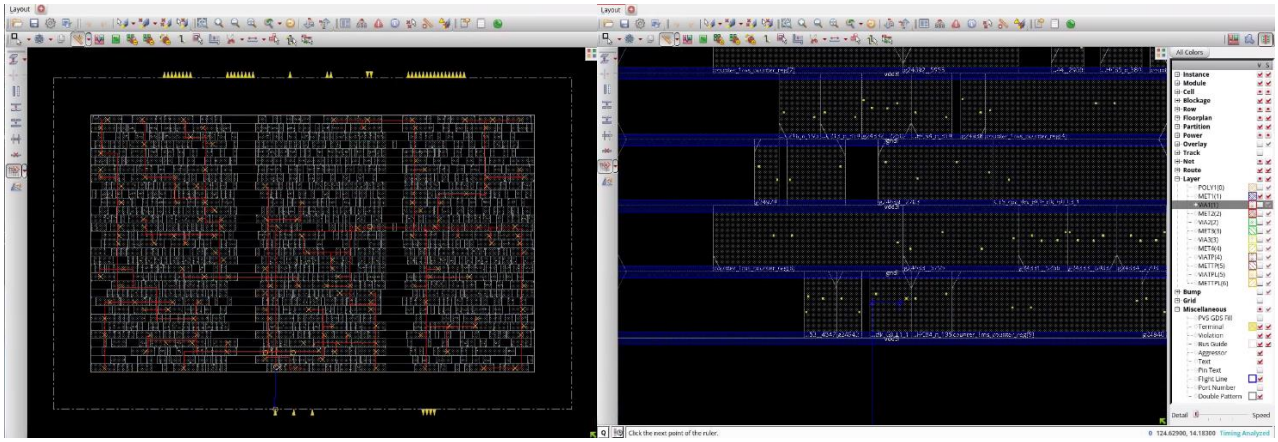

Figure 10, Physical design view showing NanoRoute utilising MET1 for signal routing

```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

Setup views included:
 view_slow
Hold  views included:
 view_fast

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.013  |  0.013  |  0.083  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   202   |   163   |   81    |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.001  | -0.001  |  0.001  |
|           TNS (ns):| -0.001  | -0.001  |  0.000  |
|    Violating Paths:|    1    |    1    |    0    |
|          All Paths:|   202   |   163   |   81    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 73.799%
      (106.733% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
**optDesign ... cpu = 0:00:12, real = 0:00:13, mem = 1175.3M, totSessionCpu=0:15:22 **
 ReSet Options after AAE Based Opt flow
*** Finished optDesign ***
Info: Destroy the CCOpt slew target map.
Removing temporary dont_use automatically set for cells with technology sites with no row.
```

Figure 11, Numbers and types of filler cells placed

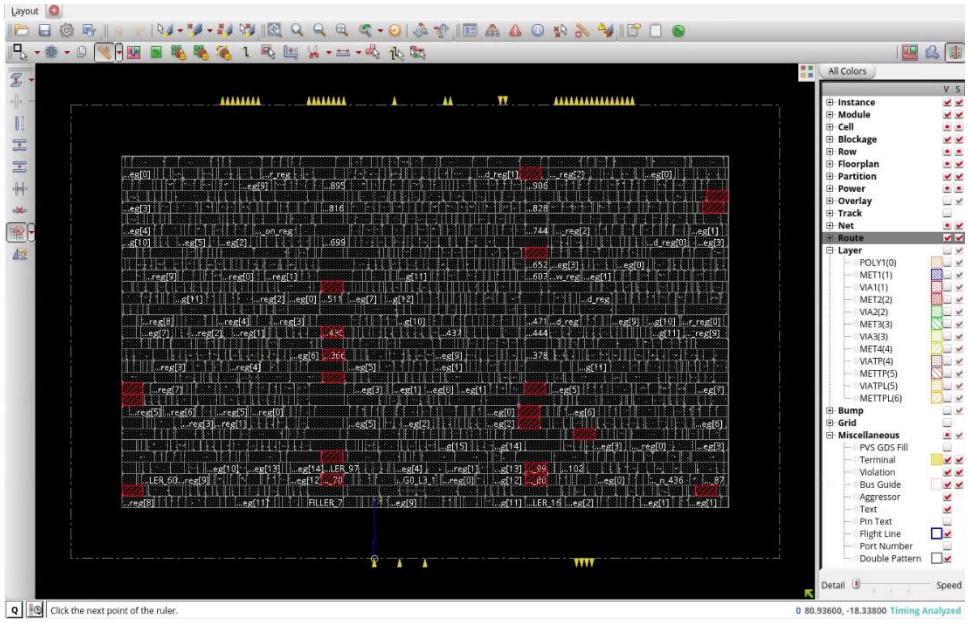

Figure 12, DECAP15 filler cells highlighted*

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 view_slow

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.013  |  0.013  |  0.083  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   202   |   163   |   81    |
+--------------------+---------+---------+---------+

+---------------+-------------------------------+-----------------+
|               |             Real              |       Total     |
|    DRVs       +------------------+------------+-----------------|
|               |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms) |
+---------------+------------------+------------+-----------------+
|   max_cap     |      0 (0)       |   0.000    |      0 (0)      |
|   max_tran    |      0 (0)       |   0.000    |      0 (0)      |
|   max_fanout  |      0 (0)       |     0      |      0 (0)      |
|   max_length  |      0 (0)       |     0      |      0 (0)      |
+---------------+------------------+------------+-----------------+

Density: 73.799%
       (106.733% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 2.0 sec
Total Real time: 2.0 sec
Total Memory Usage: 1228.550781 Mbytes
Reset AAE Options
```

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Hold  views included:
 view_fast

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.529  |  0.004  | -0.529  |
|           TNS (ns):| -5.978  |  0.000  | -5.978  |
|    Violating Paths:|   39    |    0    |   39    |
|          All Paths:|   202   |   163   |   81    |
+--------------------+---------+---------+---------+

Density: 73.799%
       (106.733% with Fillers)
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 1.74 sec
Total Real time: 1.0 sec
Total Memory Usage: 1198.574219 Mbytes
Reset AAE Options
```

Figure 13, view_slow and view_fast timeDesign Summaries

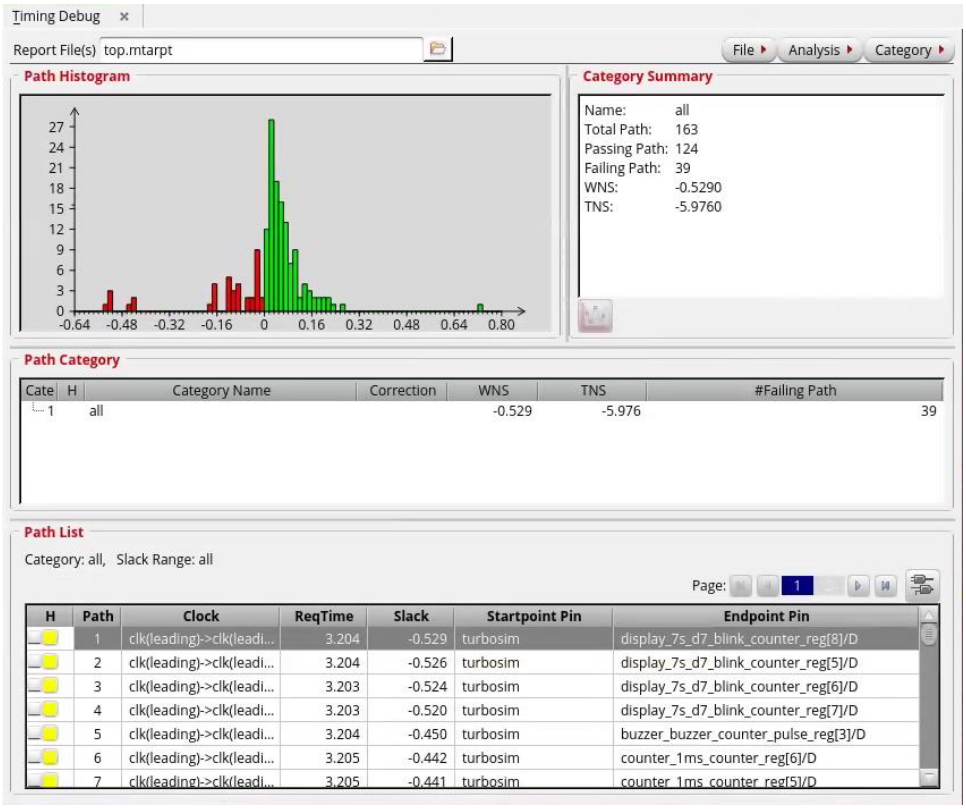

Figure 14, Designs hold slack with check type Hold

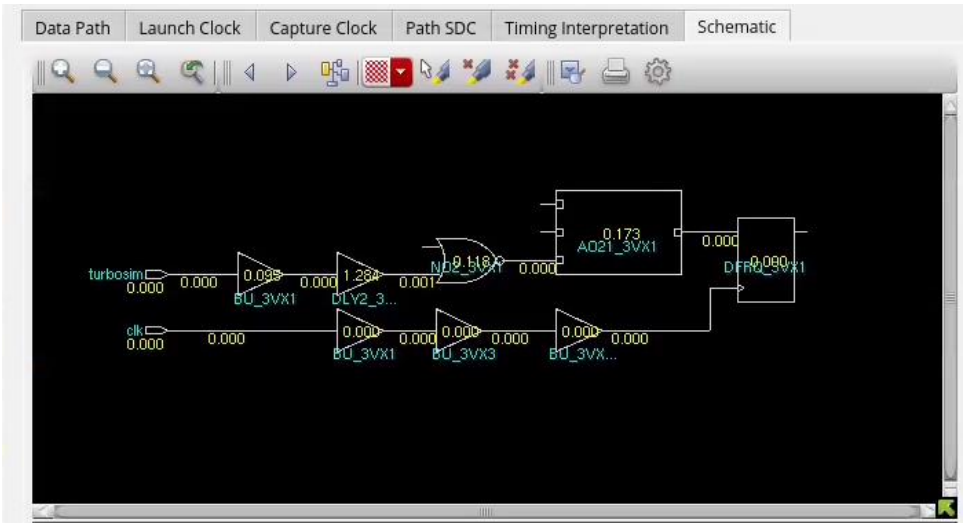

Figure 15, Critical path schematic view

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.