Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	7
Author / Student Name:	Fionn Murray
Student ID:	18223451

1 References

[1] Cadence: Overview of Running the Incisive Enterprise Simulator [Online]. Available: Through the Cadence Incisive help system.

[2] Cadence: Compiling Verilog Source Files [Online]. Available: Through the Cadence Incisive help system.

[3] Cadence: Elaborating Your Design [Online]. Available: Through the Cadence Incisive help system.

[4] Cadence: Simulating Your Design [Online]. Available: Through the Cadence Incisive help system.

[5] Cadence: Using the Incisive Simulator Utilities [Online]. Available: Through the Cadence Incisive help system. [6] Cadence: SimVision Introduction [Online]. Available: Through the Cadence Incisive help system.

[7] Cadence: SimVision: Using the FSM Window [Online]. Available: Through the Cadence Incisive help system.

2 Lab Challenges

```
[s18223451@ececad1: /home/s18223451/ee6621/cadence/labs/rt2] cws$ tree ./INCA_libs/
./INCA_libs/
└── worklib
    └── inca.lnx8664.150.pak

1 directory, 1 file
```

Figure 1, ./INCA_libs/ tree command output

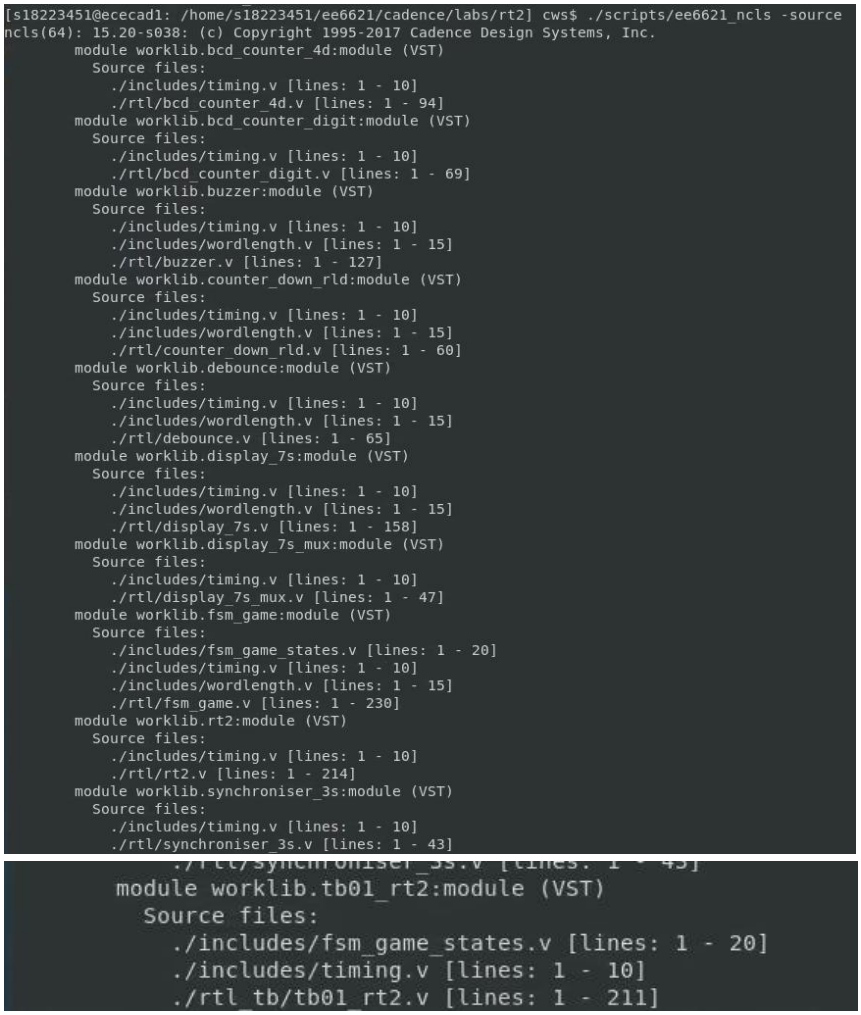

Figure 2, NCLS -source command output

We can see here with that after running the second compilation, including tb01_rt2.f files there is a massive increase in the number of source files in the ee6621_ncls file directory.

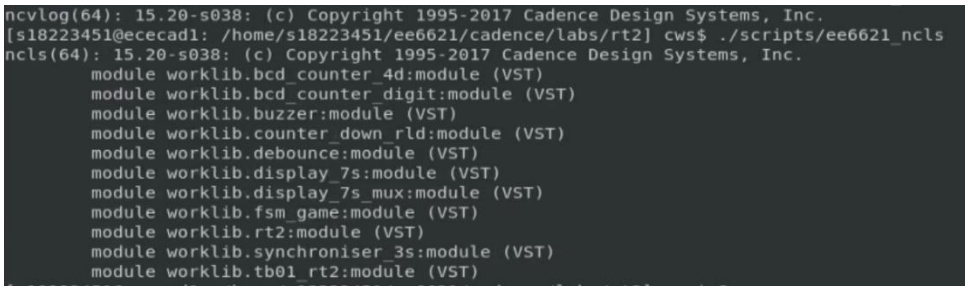

Figure 3, List of all compiled verilog source files

```
[s18223451@ececad1: /home/s18223451/ee6621/cadence/labs/rt2] cws$ ./scripts/ee6621_ncls
ncls(64): 15.20-s038: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
        module worklib.bcd_counter_4d:module (VST)
        module worklib.bcd_counter_4d:module (SIG) <0x7769002d>
        module worklib.bcd_counter_4d:module (COD) <0x7769002d>
        module worklib.bcd_counter_digit:module (VST)
        module worklib.bcd_counter_digit:module (SIG) <0x78e11d5e>
        module worklib.bcd_counter_digit:module (COD) <0x78e11d5e>
        module worklib.buzzer:module (VST)
        module worklib.buzzer:module (SIG) <0x74f9cae2>
        module worklib.buzzer:module (COD) <0x74f9cae2>
        module worklib.counter_down_rld:module (VST)
        module worklib.counter_down_rld:module (SIG) <0x4ca678b9>
        module worklib.counter_down_rld:module (SIG) <0x5ec8e5e5>
        module worklib.counter_down_rld:module (COD) <0x4ca678b9>
        module worklib.counter_down_rld:module (COD) <0x5ec8e5e5>
        module worklib.debounce:module (VST)
        module worklib.debounce:module (SIG) <0x2e7abde8>
        module worklib.debounce:module (COD) <0x2e7abde8>
        module worklib.display_7s:module (VST)
        module worklib.display_7s:module (SIG) <0x1a0a56f7>
        module worklib.display_7s:module (COD) <0x1a0a56f7>
        module worklib.display_7s_mux:module (VST)
        module worklib.display_7s_mux:module (SIG) <0x4c10cc3f>
        module worklib.display_7s_mux:module (COD) <0x4c10cc3f>
        module worklib.fsm_game:module (VST)
        module worklib.fsm_game:module (SIG) <0x0dae69b6>
        module worklib.fsm_game:module (COD) <0x0dae69b6>
        module worklib.rt2:module (VST)
        module worklib.rt2:module (SIG) <0x24c42083>
        module worklib.rt2:module (COD) <0x24c42083>
        module worklib.synchroniser_3s:module (VST)
        module worklib.synchroniser_3s:module (SIG) <0x15bf55d8>
        module worklib.synchroniser_3s:module (COD) <0x15bf55d8>
        module worklib.tb01_rt2:module (VST)
        module worklib.tb01_rt2:module (SIG) <0x17e66954>
        module worklib.tb01_rt2:module (COD) <0x17e66954>
        snapshot worklib.tb01_rt2:module (SSS)
```

Figure 4, Challenge 7.1 Summary produced by ncls script

Challenge 7.2

```
        $strobe();
        $strobe("=====================================================");
        $strobe("Launch TEST 3 (Normal use case with reaction time of 1000ms (1000us sim time))");
        #5
        buttons=2'b10;  // L: Gameplay. R: Reset
        $strobe("Sim Info: Button pressed at %0t.",$time);
        wait (fsm_state==S_READY)
        #5
        buttons=2'b00;  // L: Gameplay. R: Reset
        $strobe("Sim Info: Button released at %0t.",$time);
        wait (fsm_state==S_RUN)
        #1_000_000    // simulated reaction time of 1000ms (measured time may differ by 1 bcd lsb because of debounce)
        buttons=2'b10;  // L: Gameplay. R: Reset
        $strobe("Sim Info: Button pressed at %0t.",$time);
        @ (fsm_state)
        #10
        $strobe("Sim Info: BCD shows \"tr  %04h\"",bcd);
        if (fsm_state==S_STOPPED && (bcd>='h1000) && (bcd<='h1001) ) begin
            $strobe("PASS: TEST 3");
            $strobe("=====================================================");
        end else begin
            $strobe("FAIL: TEST 3");
            $strobe("=====================================================");
            error_counter=error_counter+1;
        end

        $strobe();
        $strobe("=====================================================");
        $strobe("Sim Info: Simulation finished normally with %0d error(s) at time %0t",error_counter,$time);
        $strobe("=====================================================");

        #10 $finish;
    end
```

After each set of $Strobe commands in the script they must be terminated with the $finish after the selected number of iterations. The test bench requires multiple $finish commands because of the separate loops.

Challenge 7.3

```
ncsim> value -verbose rt2.synchroniser_3s_reset.*
clk=1'h0 reset=1'h0 en=1'h1 in=1'h0 out=1'h0 sr=3'h0
```

Figure 5, value -verbose rt2.sunchroniser_3s_reset. output*

The output displays the current value of each variable in the system at the current set time. The same values being currently inspected in simvision

Challenge 7.4

```
WAIT_VLONG=32'h00000f9f
WAIT_LONG=32'h000007cf
WAIT_MEDIUM=32'h000003e7
WAIT_SHORT=32'h000000c7
RND_MIN=32'h000000c8
RND_MAX=32'h00000bb7
clk=1'h0 reset=1'h0 timebase=1'h0 button=1'h1 dis_sel=3'h7 beep=1'h0
reaction_counter_clr=1'h0
reaction_counter_en=1'h0
reaction_counter_fs=1'h0
fsm_state=4'h7
S_NOB=32'h00000004 S_SHOW_UL=32'h00000000 S_SHOW_ECE=32'h00000001
S_SHOW_MODULE=32'h00000002 S_SHOW_DESIGN=32'h00000003 S_READY=32'h00000004
S_STEADY=32'h00000005 S_RUN=32'h00000006 S_STOPPED=32'h00000007 S_CHEAT=32'h00000008
S_RESET=32'h0000000f state=4'h7 next_state=4'h7
D_UL=32'h00000000 D_ECE=32'h00000001 D_MODULE=32'h00000002
D_LAB=32'h00000003 D_READY=32'h00000004 D_STEADY=32'h00000005 D_CHEAT=32'h00000006
D_BCD=32'h00000007
counter=12'h7cf counter_load_value=12'h7cf counter_load=1'h0 counter_zero=1'h0 rnd_counter=12'h6d1 rnd_counter_max=1'h0
Scounter_load_rnd=1'h0 button_prev=1'h1 button_logged=1'h1 button_logged_clr=1'h0
```

Figure 6, Simulation objects of module fsm_game

This current output is displaying the respective values for each current state in the fsm_game module in the simvision software.

Challenge 7.5

```
        Design hierarchy summary:
                                Instances  Unique
                Modules:               16      11
                Registers:             88      49
                Scalar wires:          58       -
                Expanded wires:        18       5
                Vectored wires:        27       -
                Always blocks:         24      19
                Initial blocks:         5       5
                Cont. assignments:     27      38
                Pseudo assignments:    12      12
                Simulation timescale:  1ps
        Writing initial simulation snapshot: worklib.tb01_rt2:v
Loading snapshot worklib.tb01_rt2:v ..................... Done
```

Figure 7, Design hierarchy summary produced by irun

Challenge 7.6

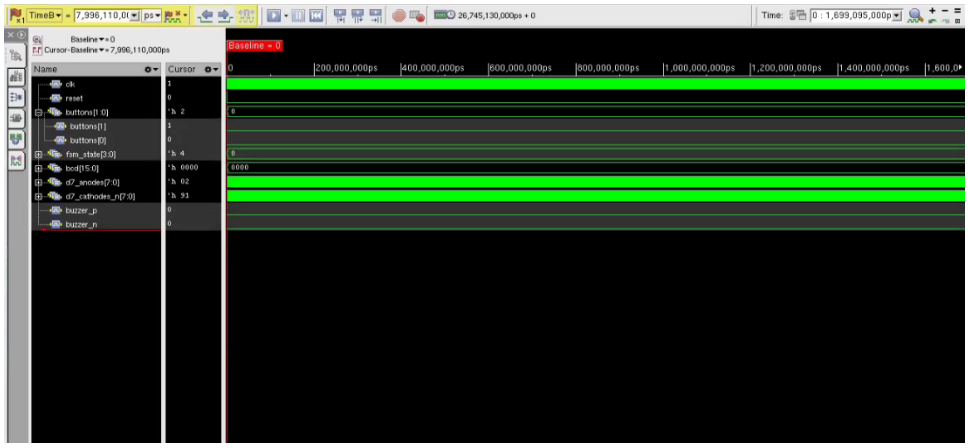

Figure 8, Signals at full-x zoom

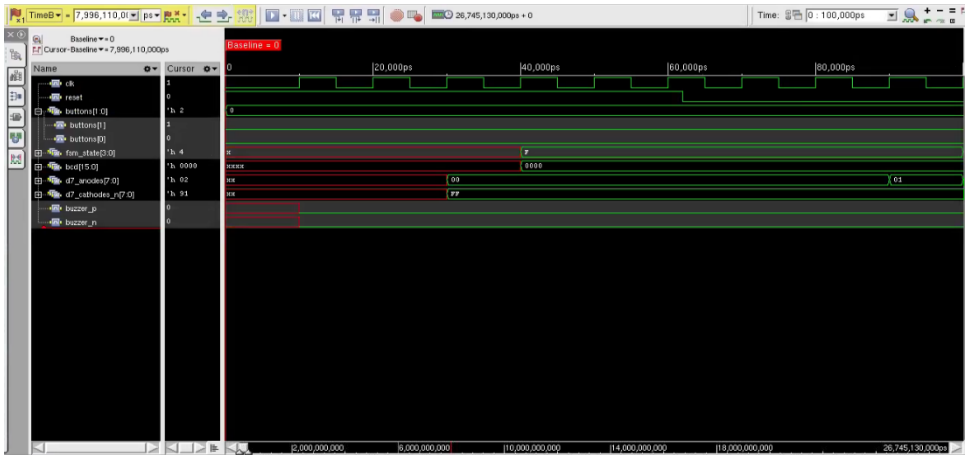

Figure 9, Signals during trange_reset interval

Challenge 7.7

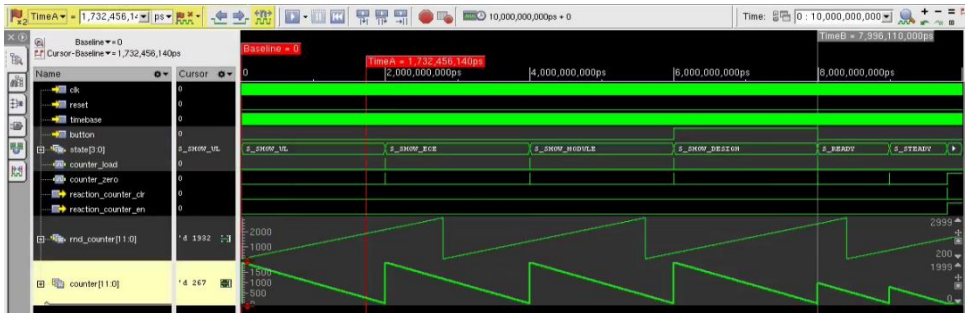

Figure 10, SimVision Waveform window for FSM debug

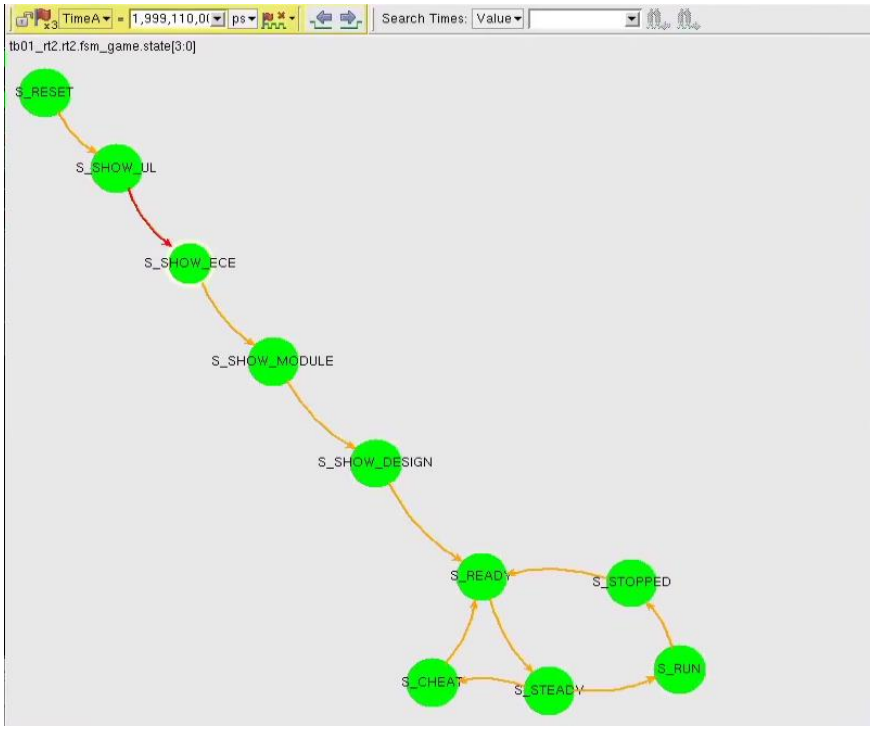

Figure 11, SimVision FSM window

Challenge 7.8

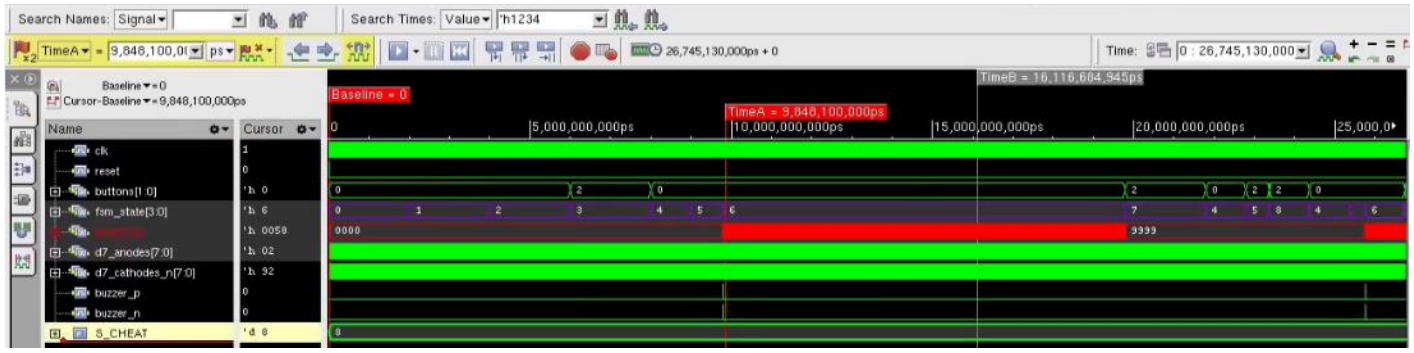

Figure 12, Counter bcd[15:0] at value h1234

Challenge 7.9

Figure 13, Time spent in FSM state S_CHEAT between TimeA and TimeB

Challenge 7.10

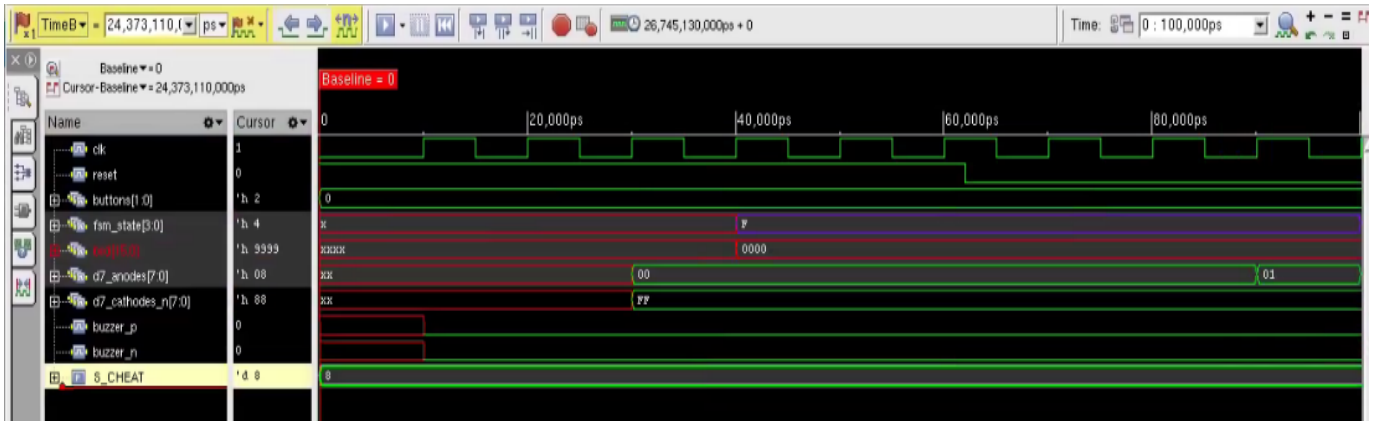

Figure 14, Design states immediately after reset. Range 0ns:100ns

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.