



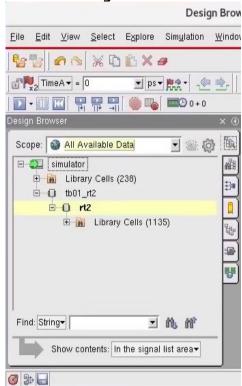
Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	09/11/2021
Lab Number:	10
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Student ID:	18223451

## 1. References

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- [2] Cadence: Compiling Verilog Source Files [Online]. Available: Through the Cadence Incisive help system.
- [3] Cadence: Elaborating Your Design [Online]. Available: Through the Cadence Incisive help system.
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- [5] Cadence: Using the Incisive Simulator Utilities [Online]. Available: Through the Cadence Incisive help system.
- [6] Cadence: SimVision Introduction [Online]. Available: Through the Cadence Incisive help system.
- [7] Cadence: SimVision: Using the FSM Window [Online]. Available: Through the Cadence Incisive help system.
  - [8] Cadence: Innovus User Guide [Online]. Available: Through the Cadence Genus help system.
- [9] Cadence: Innovus Text Command Reference [Online]. Available: Through the Cadence Genus help system.

## 2. Lab Challenges

tb01\_rt2.fsm\_state[3:0]



<u>Fiaure 1. Challenae 10.1: rt2 standard cell count</u> 🗳 - 🖐 Send To: 🗽 🚓 🚉 🚉 🔟 🔲 🔳 Search Names: Signal ▼ Search Times: Value ▼ **→** M<sub>0</sub> M<sup>0</sup> TimeA = 26.74513276 ms = 26.74513276 Time: 3- 26.445822781ms: 🗹 🔍 + - = 🔭 🚉 🦸 **⇔**▼ Cursor •▼ 26.45ms 126.55ms 488 <u>tb</u>
tb01\_rt2.reset

■ tb01 in table

■ tb01 in table

■ tb01 in table

■ tb01 in table

■ table 4 tb01 rt2.buttons[1]





Figure 2, Post implementation timing simulation signal response

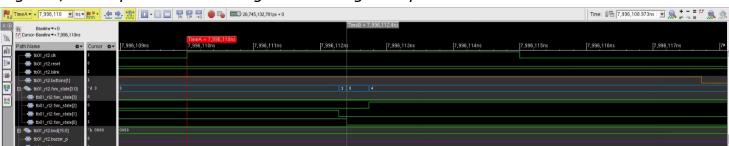


Figure 3, Challenge 10.2 rt2 fsm state and cathodes signal and timing interval

```
Product : 'Virtuos(s) Sixtrem Out
Program : If (2005): virtuose wersion 5.1.7-64b 18/86/2017 28:26 (s)ffw865) $

Sterred at: 15-86w-2021 15:46:11
User Name : siz22451
Blost Name : cecedit ul. campus
User Laws : 18/22451
Blost Name : cecedit ul. campus
User Laws : 18/22451
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Figure 5, Challenge 10.3 rt2.gds file view in terminal

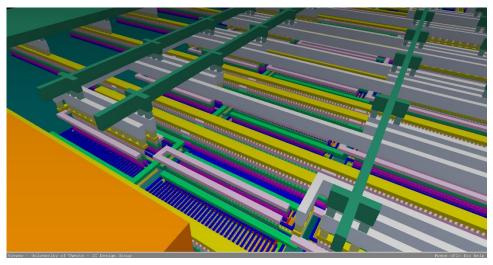


Figure 6, GDS3D 3D view of rt2.gds top metal METTPL not shown

## 3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.