Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	5
Author / Student Name:	Fionn Murray
Student ID:	18223451

1 References

[1] 7 Series FPGAs Datasheet: Overview, DS180 (v2.6), Xilinx Inc., 2018

[2] Artix-7 FPGAs Datasheet: DC and AC Switching Characteristics, DS181 (v1.25), Xilinx Inc., 2018

[3] 7 Series FPGAs Clocking Resources User Guide, UG471 (v1.14), Xilinx Inc., 2018

[4] 7 Series FPGAs Configuration User Guide, UG470 (v1.13.1), Xilinx Inc., 2018 [5] Vivado Design Suite User Guide – Release Notes, Installation and Licensing, UG973 (v2020.1), Xilinx Inc., 2020

[6] Vivado Design Suite User Guide – Using the Vivado ISE, UG893 (v2019.2), Xilinx Inc., 2019

[7] Vivado Design Suite User Guide – System Level Design Entry, UG895 (v2019.2), Xilinx Inc., 2019

[8] Vivado Design Suite User Guide – Using TCL Scripting, UG894 (v2019.2), Xilinx Inc., 2019

[9] Vivado Design Suite User Guide – Logic Simulation, UG900 (v2019.2), Xilinx Inc., 2019

[10] Vivado Design Suite User Guide – Synthesis, UG901 (v2019.2), Xilinx Inc., 2019

[11] Vivado Design Suite User Guide – Implementation, UG904 (v2019.2), Xilinx Inc., 2019

[12] Vivado Design Suite User Guide – Using Constraints, UG903 (v2019.2), Xilinx Inc., 2019

[13] Vivado Design Suite Overview [Online]. Available: https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html

[14] Revision control system git [Online]. Available: https://git-scm.com/

[15] Digilent Inc. (2020, June, 27), Cmod A7 Reference Manual: https://reference.digilentinc.com/reference/programmablelogic/cmod-a7/reference-manual.Lab Challenges

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2 Lab Challenges

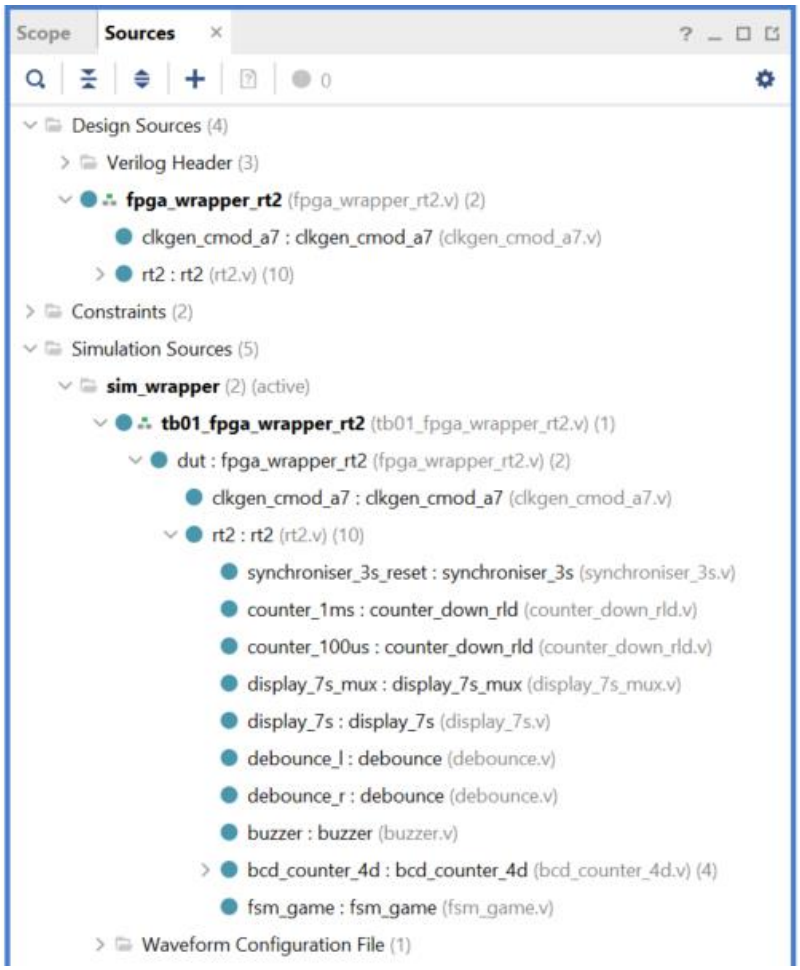

Figure 1, Challenge 5.1 sim_wrapper sources window

```
45      // Generate FPGA clock oscillator signal
46      initial begin
47          clk = 0;                    // Signal clk starts at 0.
48          #41.666;
49          forever #41.666 clk=~clk;
50      end
```

Figure 2, Challenge 5.2 fpga_wrapper_rt2.v module clock frequency

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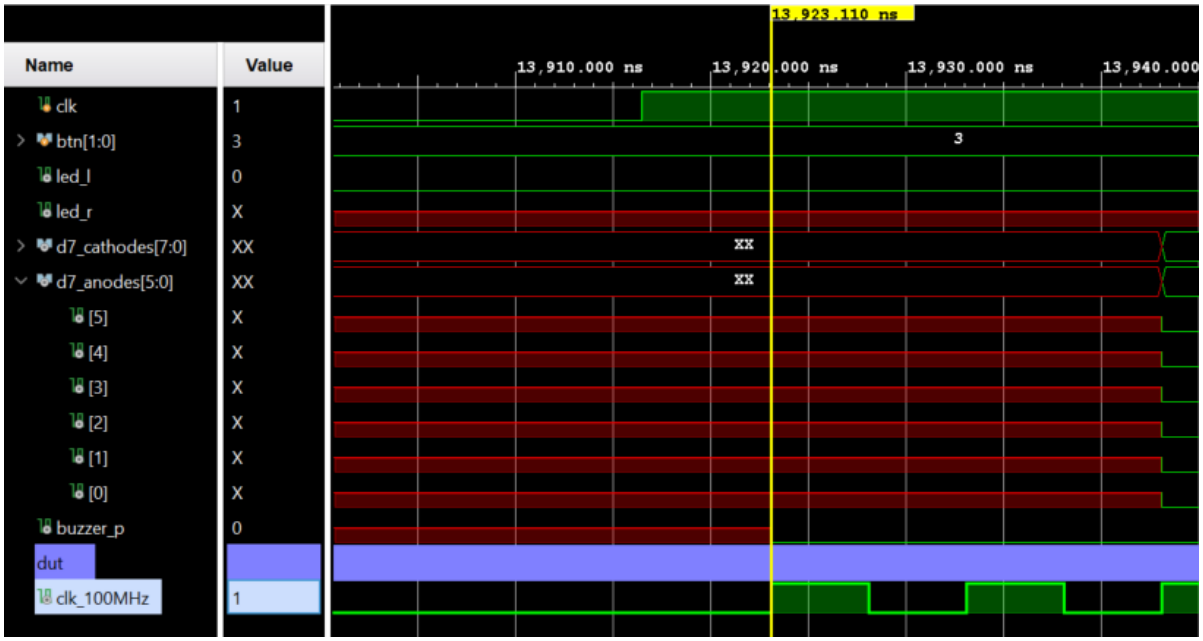

Figure 3, Challenge 5.3 clk_100MHz start-up behavior showing delay before available

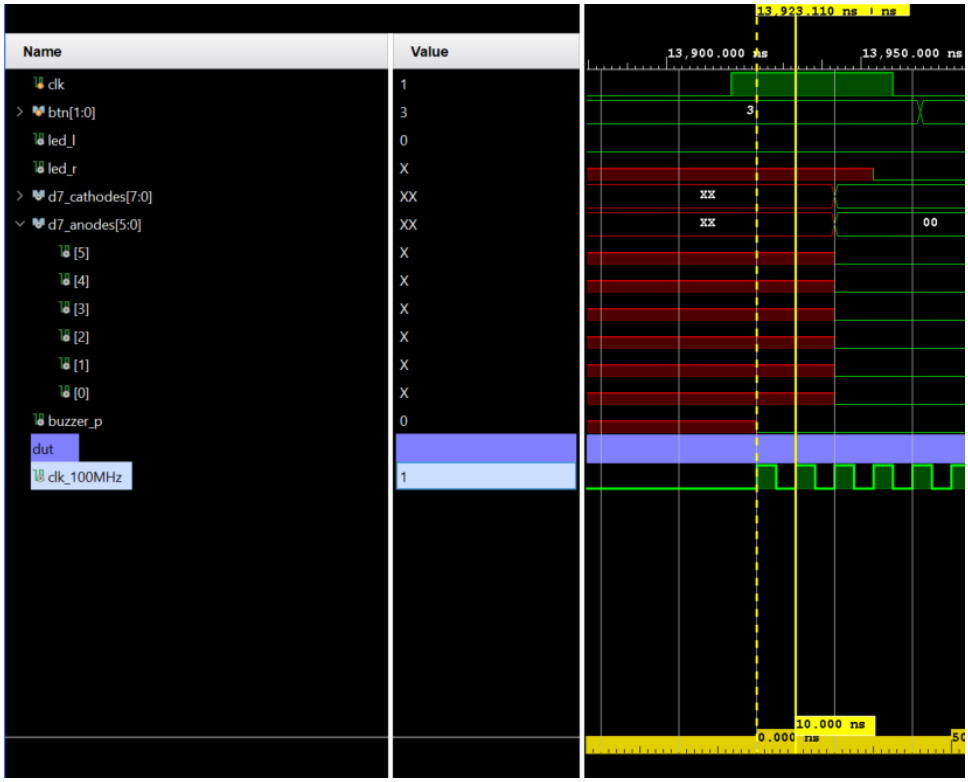

Figure 4, Challenge 5.4 clk_100MHz frequency

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Figure 5 Challenge 5.4 d7_anodes asserting deviating slightly due to clk_100MHz delay

```
$strobe("Sim Info: Test 1. Run one complete display cycle, check for string 'UL    '");

wait ( d7_anodes==6'b0001_0000 )
#10
if ( d7_cathodes==8'b1100_0111 ) begin
end else begin
    $strobe("FAIL: wrong character in display position 4, expected 'L'");
    $strobe("=============================================================");
    error_counter=error_counter+1;
end

wait ( d7_anodes==6'b0010_0000 )
#10
if ( d7_cathodes==8'b1100_0001 ) begin
    $strobe("Sim Info: Test 1. *** PASS ***");

end else begin
    $strobe("FAIL: wrong character in display position 5, expected 'U'");
    $strobe("=============================================================");
    error_counter=error_counter+1;
end
```

Figure 6, Challenge 5.5 Fail checks for character string UL

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```
source tb01_fpga_wrapper_rt2.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0} {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#      send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform
#   }
# }
INFO: [USF-XSim-96] XSim completed. Design snapshot 'tb01_fpga_wrapper_rt2_behav' loaded.
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:15 . Memory (MB): peak = 1209.320 ; gain = 0.000
save_wave_config {C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/work_vivado_35t/rt2/tb01_fpga_wrapper_rt2_behav.wcfg}
add_files -fileset sim_wrapper -norecurse C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/work_vivado_35t/rt2/tb01_fpga_wrapper_rt2_behav.wcfg
set_property xsim.view C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/work_vivado_35t/rt2/tb01_fpga_wrapper_rt2_behav.wcfg [get_filesets sim_wrapper]
run all
Sim Info: Welcome to EE6621 wrapper test. Module tb01_fpga_wrapper_rt2. Starting simulation at time 0.000 ms.
=======================================================
Sim Info: Request reset, and wait for MMCM clocks to arrive
          MMCM clock is running. Released from reset...
Sim Info: Test 1. Run one complete display cycle, check for string 'UL    '
Sim Info: Test 1. *** PASS ***

=======================================================
Sim Info: Simulation finished normally with 0 error(s) at time 4.015 ms
=======================================================
$finish called at time : 4014959109 ps : File "C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/rtl_tb/tb01_fpga_wrapper_rt2.v" Line 105
run: Time (s): cpu = 00:00:03 ; elapsed = 00:00:15 . Memory (MB): peak = 1209.320 ; gain = 0.000
add_bp {C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/rtl_tb/tb01_fpga_wrapper_rt2.v} 93
remove_bps -file {C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/rtl_tb/tb01_fpga_wrapper_rt2.v} -line 93
```

Figure 7, Console simulation message

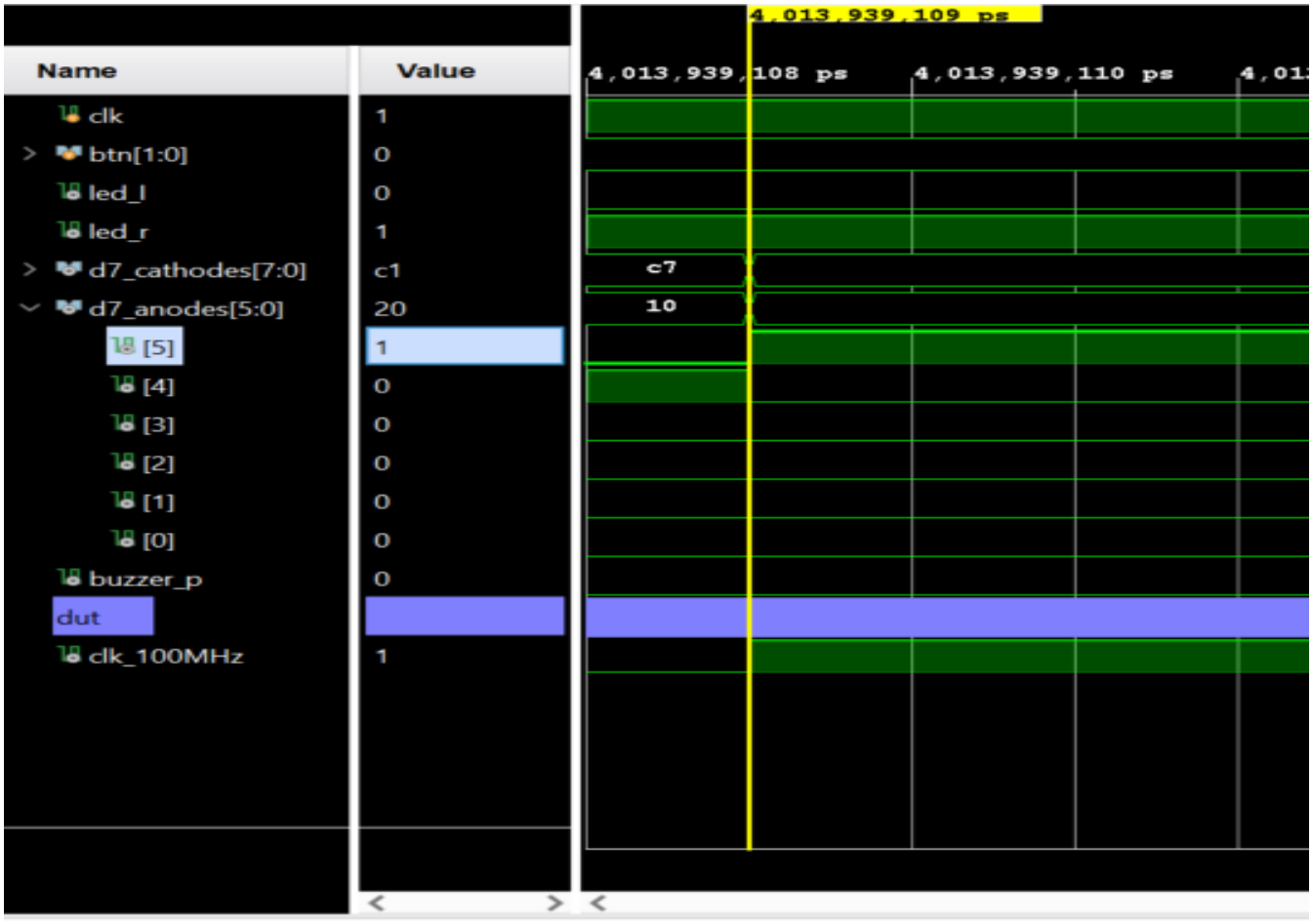

Figure 8, Challenge 5.6 d7_anode[5] asserting

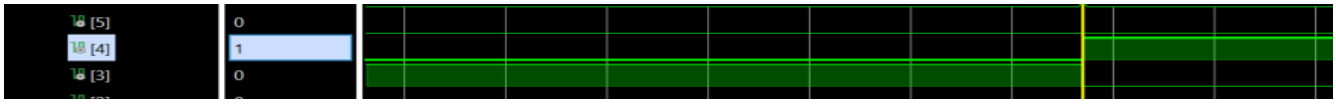

Figure 9, Challenge 5.6 D7_anode[5] and D7_anode[4] alternating near the end of the clock cycle

```
run all
Sim Info: Welcome to EE6621 wrapper test. Module tb01_fpga_wrapper_rt2. Starting simulation at time 0.000 ms.
=======================================================
Sim Info: Request reset, and wait for MMCM clocks to arrive
          MMCM clock is running. Released from reset...
Sim Info: Test 1. Run one complete display cycle, check for string 'UL    '
Sim Info: Test 1. *** PASS ***

=======================================================
Sim Info: Simulation finished normally with 0 error(s) at time 4.015 ms
=======================================================
$finish called at time : 4014949209 ps : File "C:/Users/18223451/Desktop/EE6621/fpga/labs/rt2/rtl_tb/tb01_fpga_wrapper_rt2.v" Line 105
run: Time (s): cpu = 00:00:04 ; elapsed = 00:00:22 . Memory (MB): peak = 2283.961 ; gain = 0.000
```

Figure 10, Console simulation confirmation

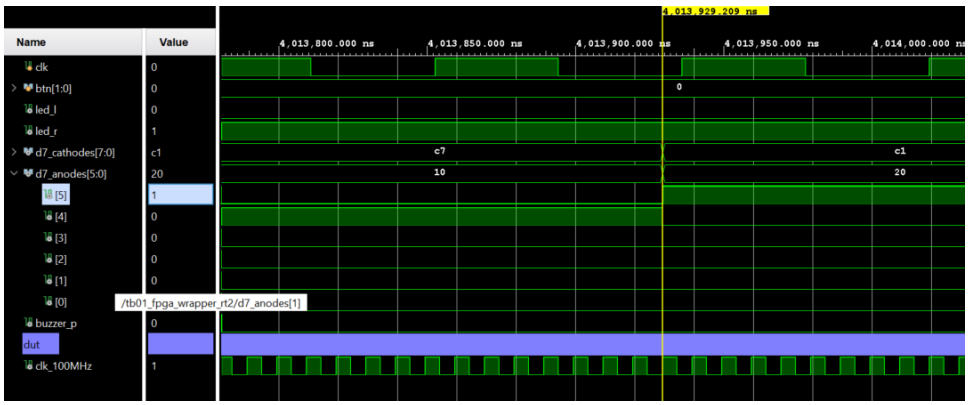

Figure 11, Challenge 5.7 d7_anode[5] asserting

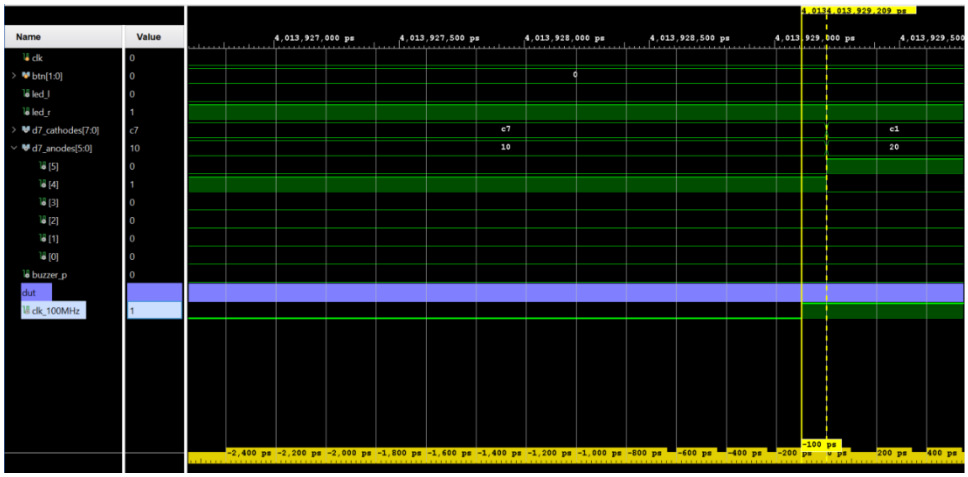

Figure 12, Challenge 5.8 clk_100MHz d7_anode[4] delay

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```
run all
Sim Info: Welcome to EE6621 wrapper test. Module tb01_fpga_wrapper_rt2. Starting simulation at time 0.000 ms.
============================================================
Sim Info: Request reset, and wait for MMCM clocks to arrive
          MMCM clock is running. Released from reset...
Sim Info: Test 1. Run one complete display cycle, check for string 'UL    '
```

Figure 13, Console implementation confirmation

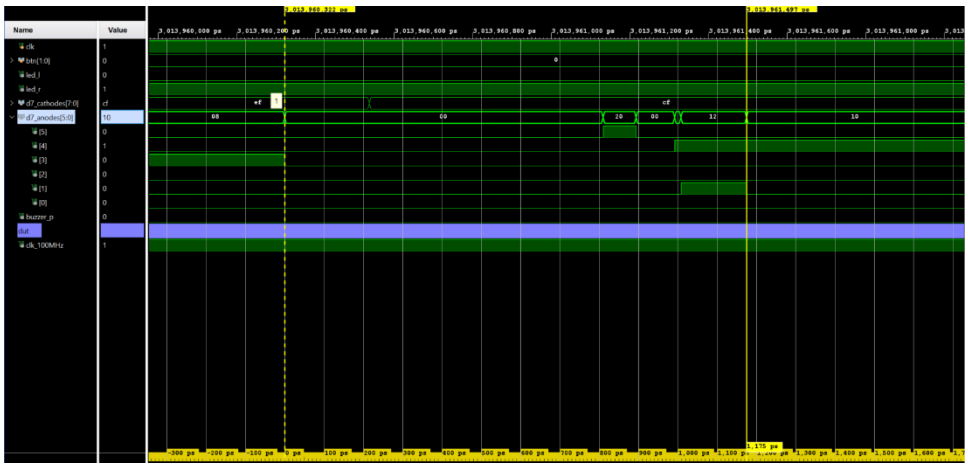

Figure 14, d7_anodes[5:0] glitched shown with cursors

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.

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