Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	01/11/2021
Lab Number:	8
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Student ID:	18223451

1 References

[1] Cadence: Genus Synthesis Flows Guide for Legacy UI [Online]. Available: Through the Cadence Genus help system.

[2] Cadence: Genus User Guide for Legacy UI [Online]. Available: Through the Cadence Genus help system.

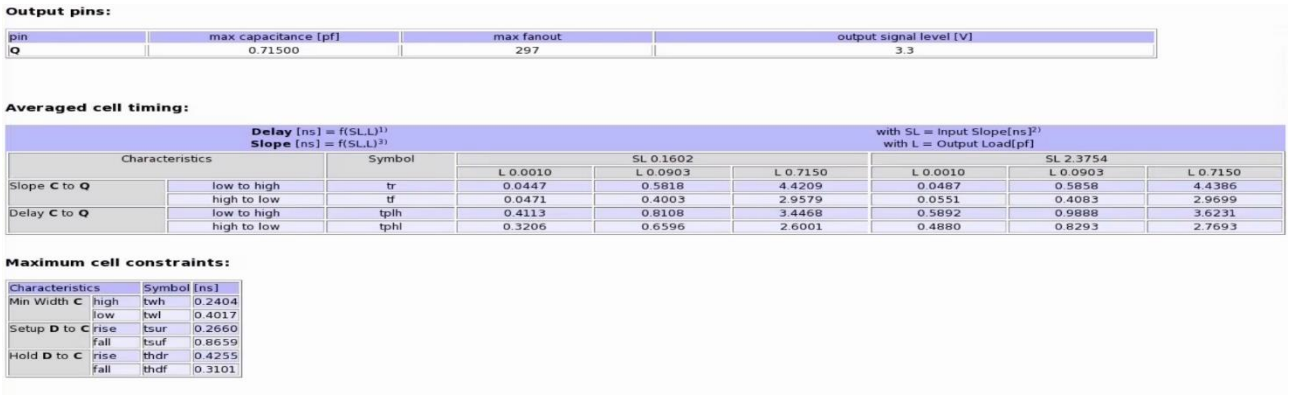
[3] Cadence: Genus Timing Analysis Guide for Legacy UI [Online]. Available: Through the Cadence Genus help system.

[4] Cadence: Genus HDL Modeling for Legacy UI [Online]. Available: Through the Cadence Genus help system.

2 Lab Challenges

```
[s18223451@ececad1: /home/s18223451/ee6621/cadence/labs] cws$ genus -64bit -version
TMPDIR is being set to /home/s18223451/temp/genus_temp_48945_ececad1.ul.campus_s18223451_iFphXu
Program Name: Genus(TM) Synthesis Solution, Version: 17.11-s014_1
@(#)CDS: SYNTECH 17.11-s012_1 () Jul 21 2017 02:29:12 ( )
@(#)CDS: SGN 10.10-p122 (22-Jan-2016) (64 bit executable)
Normal exit.
```

Figure 1, Cadence Genus Version



Output pins:

pin	max capacitance [pf]	max fanout	output signal level [V]
Q	0.71500	297	3.3

Averaged cell timing:

Delay [ns] = f(SL,L)[1]
Slope [ns] = f(SL,L)[2]
with SL = Input Slope[ns][2]
with L = Output Load[pf]

Characteristics		Symbol	SL 0.1602			SL 2.3754		
			L 0.0010	L 0.0903	L 0.7150	L 0.0010	L 0.0903	L 0.7150
Slope C to Q	low to high	tr	0.0447	0.5818	4.4209	0.0487	0.5858	4.4386
	high to low	tf	0.0471	0.4003	2.9579	0.0551	0.4083	2.9699
Delay C to Q	low to high	tplh	0.4113	0.8108	3.4468	0.5892	0.9888	3.6231
	high to low	tphl	0.3206	0.6596	2.6001	0.4880	0.8293	2.7693

Maximum cell constraints:

Characteristics		Symbol	[ns]
Min Width C	high	twh	0.2404
	low	twl	0.4017
Setup D to C	rise	tsur	0.2660
	fall	tsuf	0.8659
Hold D to C	rise	thdr	0.4255
	fall	thdf	0.3101

Figure 2, Challenge 8.1 DFRQ_3VX1 information

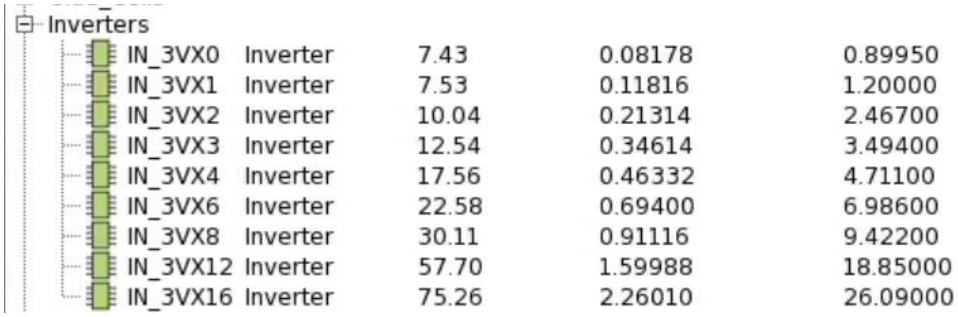
Clock-to-output propagation delay = 0.4113, for lowest slew rate and = 0.3206 lowest loading case.

Challenge 8.2:

DFRQ_3VX1=57.7 um^2, height=4.48um

=>width of standard cell= 57.7/4.48= 12.88um

Challenge 8.3:



Inverters				
IN_3VX0	Inverter	7.43	0.08178	0.89950
IN_3VX1	Inverter	7.53	0.11816	1.20000
IN_3VX2	Inverter	10.04	0.21314	2.46700
IN_3VX3	Inverter	12.54	0.34614	3.49400
IN_3VX4	Inverter	17.56	0.46332	4.71100
IN_3VX6	Inverter	22.58	0.69400	6.98600
IN_3VX8	Inverter	30.11	0.91116	9.42200
IN_3VX12	Inverter	57.70	1.59988	18.85000
IN_3VX16	Inverter	75.26	2.26010	26.09000

Figure 3, List of inverters in the library

Smallest area = 7.42um^2, estimated width of cell = $\sqrt{7.42}$ =2.72um

Challenge 8.4:

```
legacy_genus:/> find ./libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/ -libcell DFR*
/libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRQ_3VX1 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRQ_3VX2
 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRQ_3VX4 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRRQ_3V
X1 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRRQ_3VX2 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRRQ
_3VX4 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRRS_3VX1 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DF
RRS_3VX2 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRRS_3VX4 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells
/DFRSQ_3VX1 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libcells/DFRSQ_3VX2 /libraries/D_CELLS_3V_LPMOS_slow_3_00V_125C/libce
lls/DFRSQ_3VX4
```

Figure 4, Output of libcell DFR in D_CELLS directory

This lists each of the DFF files shown in figure 3, the xlibd screenshot of the lab brief.

Challenge 8.6:

```
legacy_genus:/> report_clocks
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 17.11-s014_1
  Generated on:           Nov 02 2021  02:08:20 pm
  Module:                 rt2
  Technology libraries:   D_CELLS_3V_LPMOS_slow_3_00V_125C 2.1.1
                          D_CELLS_3V_LPMOS_typ_3_30V_25C 2.1.1
                          D_CELLS_3V_LPMOS_fast_3_60V_m40C 2.1.1
  Operating conditions:   slow_3_00V_125C
  Interconnect mode:      global
  Area mode:              physical library
=============================================================


 Clock Description
 -----------------

 Clock                              Clock    Source     No of
 Name     Period   Rise    Fall     Domain  Pin/Port  Registers
-------------------------------------------------------------------
 clk      10000.0   0.0   5000.0   domain_1   clk          151

 Clock Network Latency / Setup Uncertainty
 -----------------------------------------

        Network   Network   Source   Source     Setup        Setup
Clock   Latency   Latency  Latency  Latency  Uncertainty  Uncertainty
 Name     Rise      Fall     Rise     Fall       Rise         Fall
-----------------------------------------------------------------------
clk      1000.0    1000.0   1000.0   1000.0       500.0        500.0

 Clock Relationship (with uncertainty & latency)
 -----------------------------------------------

  From    To    R->R     R->F     F->R     F->F
-----------------------------------------------
  clk    clk   9500.0   4500.0   4500.0   9500.0
```

Figure 5, report_clocks output showing 100MHz clock frequency

Challenge 8.7:

```
SDFRQ_3VX1            6    451.584    D_CELLS_3V_LPMOS_slow_3_00V_125C
SDFRQ_3VX2            4    321.126    D_CELLS_3V_LPMOS_slow_3_00V_125C
-----------------------------------------------------------------------
total               880  20175.770


     Type      Instances     Area   Area %
-----------------------------------------
sequential            144  8630.272   42.8
inverter              143  1133.978    5.6
buffer                  8   100.352    0.5
logic                 585 10311.168   51.1
physical_cells          0     0.000    0.0
-----------------------------------------
total                 880 20175.770  100.0
```

Figure 6, report gates output

```
[s18223451@ececad1: /home/s18223451/ee6621/cadence/labs/rt2/genus_to_innovus] cws$ ls
rt2._default_constraint_mode_.sdc  rt2.g                rt2.invs_setup.tcl  rt2.mode
rt2._default_view_latency.sdc      rt2.genus_setup.tcl  rt2.metrics.json    rt2.v
rt2.flowkit_settings.tcl           rt2.globals          rt2.mmode.tcl       rt2.wnm_attrs.tcl
```

Figure 7, files in ./genus_to_innovus

Challenge 8.8

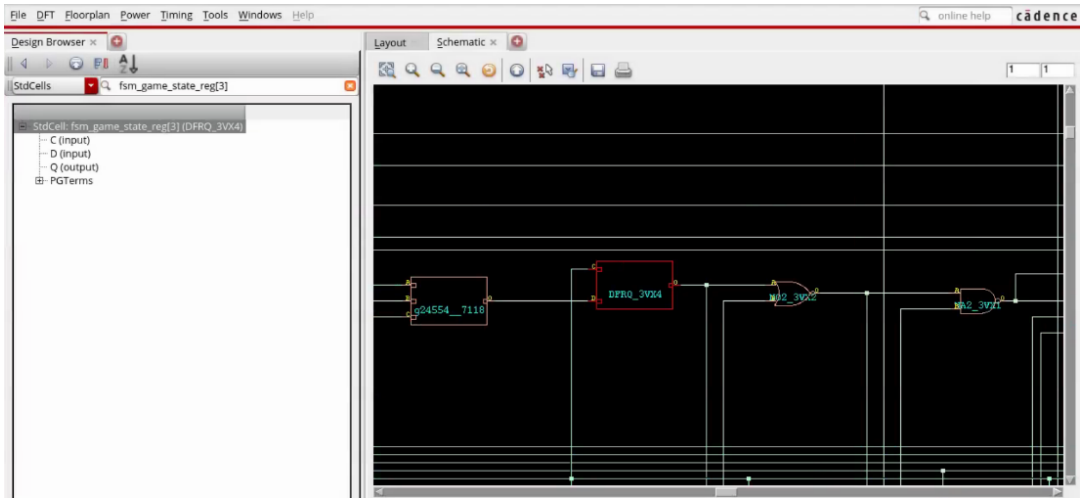


Figure 8, fsm_game_state_reg[3]

Challenge 8.9

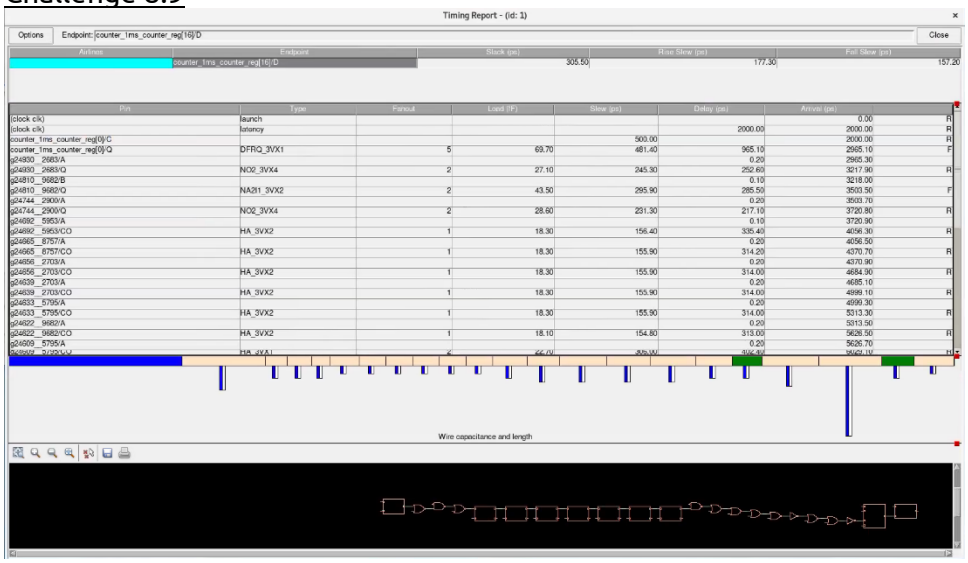


Figure 9, Timing Report Tool

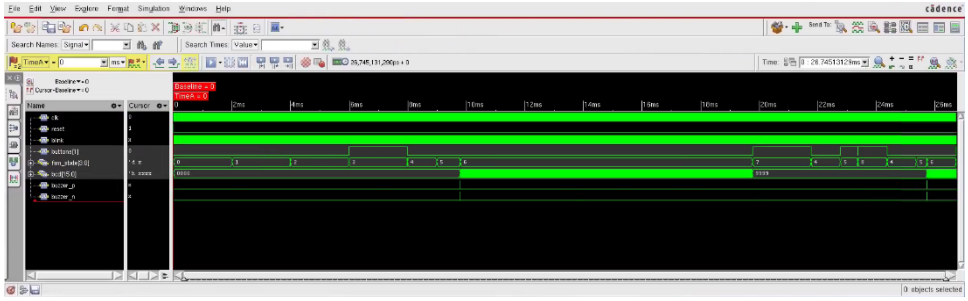


Figure 10, Simvision waveform window

Challenge 8.10

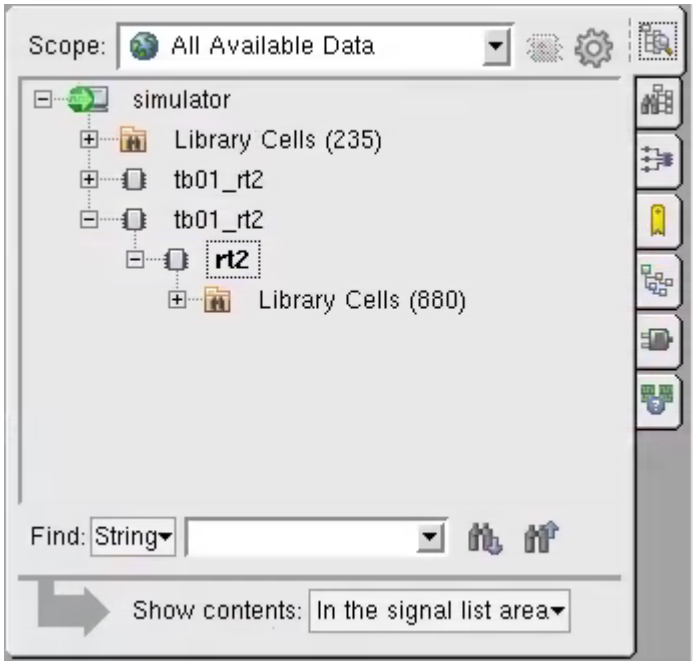


Figure 11, Simvision rt2 library cell count

The cell should show 892 standard cells in the rt2 directory, however I exited the simvision and genus before screenshotting upon running it the first time. I could not get it to display the correct 892 cells again the second time. Apologies for the troubles here.

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.

