=Module:	EE6621 ASICs 1 (Digital ASICs)
Date:	29/12/2019
Lab Number:	3
Author / Student Name:	Fionn Murray
Student ID:	18223451

1 References

[1] Digilent Inc. (2020, June, 27), Cmod A7 Reference Manual: https://reference.digilentinc.com/reference/programmablelogic/cmod-a7/reference-manual.

[2] 7 Series FPGAs Datasheet: Overview, DS180 (v2.6), Xilinx Inc., 2018

[3] Artix-7 FPGAs Datasheet: DC and AC Switching Characteristics, DS181 (v1.25), Xilinx Inc., 2018

[4] 7 Series FPGAs Clocking Resources User Guide, UG471 (v1.14), Xilinx Inc., 2018

[5] 7 Series FPGAs Configuration User Guide, UG470 (v1.13.1), Xilinx Inc., 2018

[6] Vivado Design Suite User Guide – Release Notes, Installation and Licensing, UG973 (v2020.1), Xilinx Inc., 2020

[7] Vivado Design Suite Overview [Online]. Available: https://www.xilinx.com/products/design-tools/vivado/vivado-ml.html

[8] Geany – The Flyweight IDE [Online]. Available: https://www.geany.org/

2 Lab Challenges

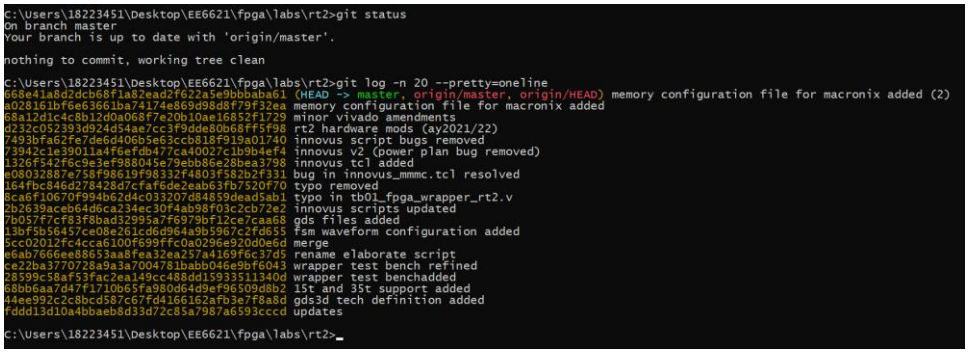

Figure 1, Challenge 3.1 Design's commit log to date of run command

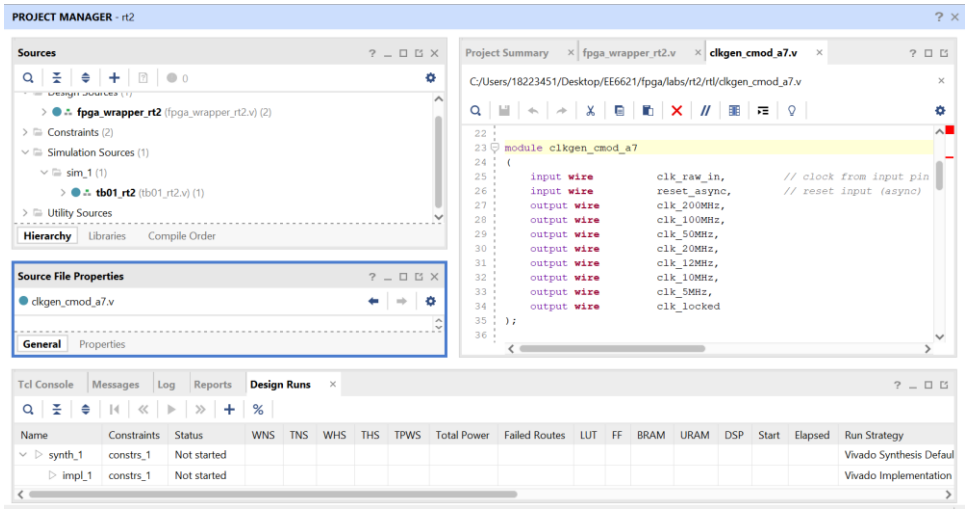

Figure 2, Challenge 3.2 Vivado Project and Sources window

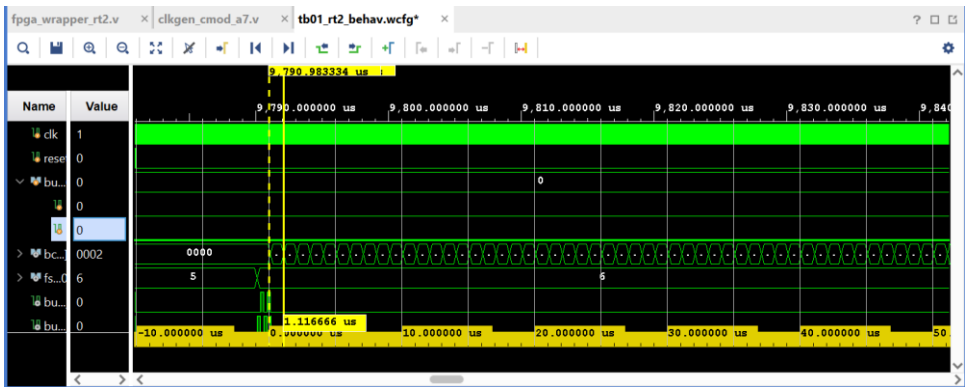

Figure 3, Challenge 3.3

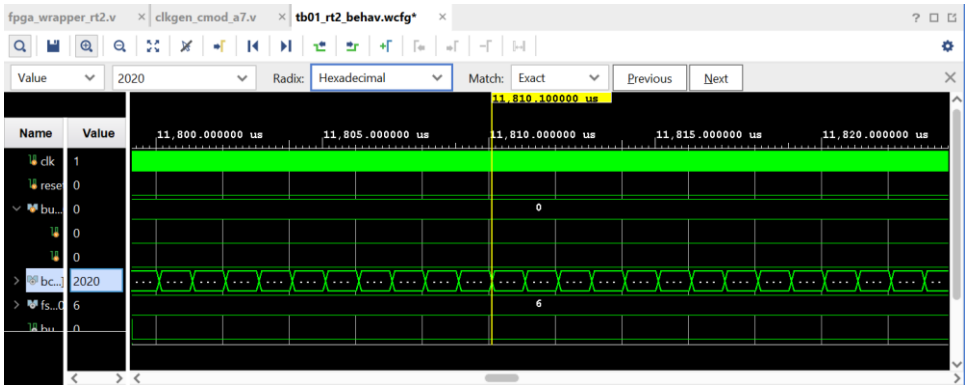

Figure 4, Challenge 3.4

The hexadecimal radix is most meaningful to this HDL object as it simplifies how the binary data is represented – ie an 8bit binary digit vs a 2 digit hex value.

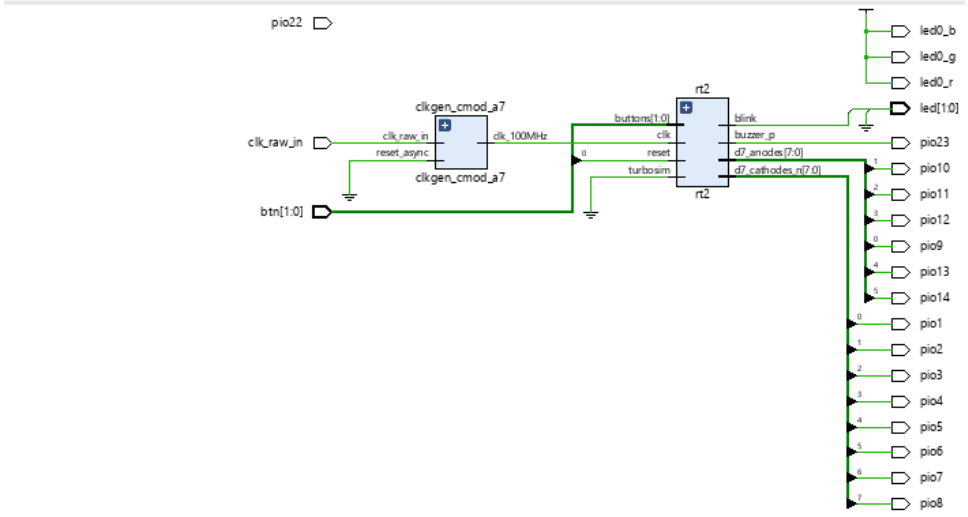

Figure 5, Hierarchical Schematic

3. Declaration of Authorship

I confirm that this lab report, submitted for assessment, is my own original work.