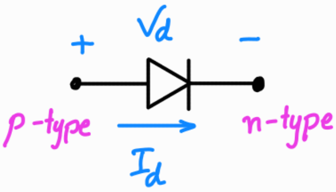
Diode —

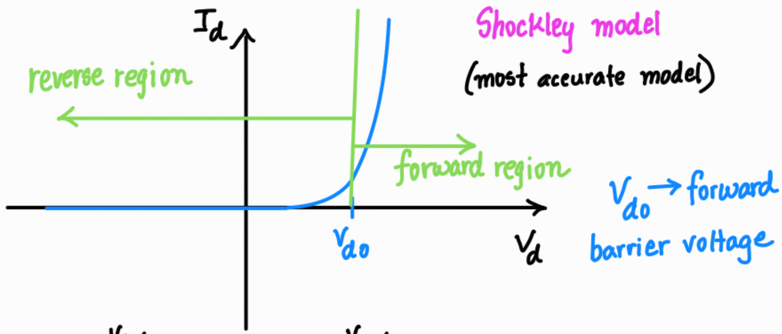
Diode is a 2 terminal passive device like a resistor. However, unlike a resistor, a diode is an electronic device with a non-linear IV relationship.

Schematic —



The polarity of the diode voltage & the direction of the current must be maintained for all cases.

IV —



$$I_d = I_s(e^{qV_d/nkT} - 1) = I_s(e^{V_D/nV_T} - 1) \quad \text{where,}$$

$I_s = 10^{-12}A$ (reverse saturation current)

$q = 1.6 \times 10^{-19} C$ (magnitude of electrical charge of an electron)

n = ranges from 1 to 2 (ideality factor, $n = 1$ for ideal diodes)

$k = 1.38 \times 10^{-23}$ J/K (Boltzmann's constant)

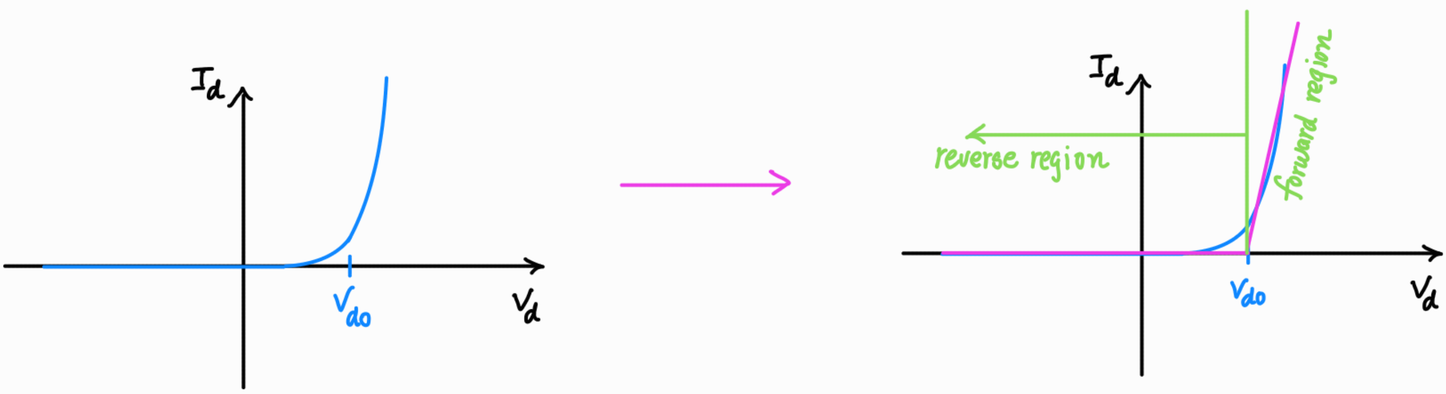
T = temperature (in Kelvin)

V_T = thermal voltage = $\frac{kT}{q} \approx 26mV$ @ room temp (300K)

Piecewise linear models —

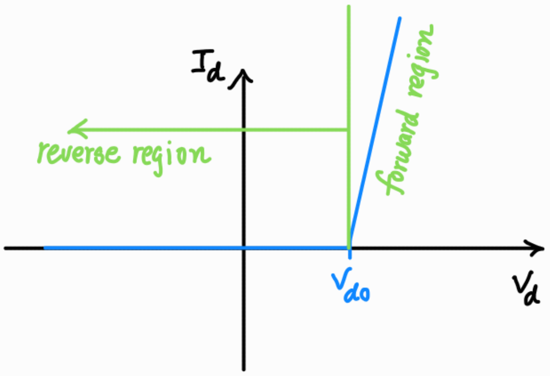
The Shockley diode model is infeasible for most applications. Equations containing the exponential IV, in most cases, do not have any closed form solution & as such cannot be solved. So instead, we give up some accuracy (negligible in most cases) to approximate the Shockley model with piecewise linear models.

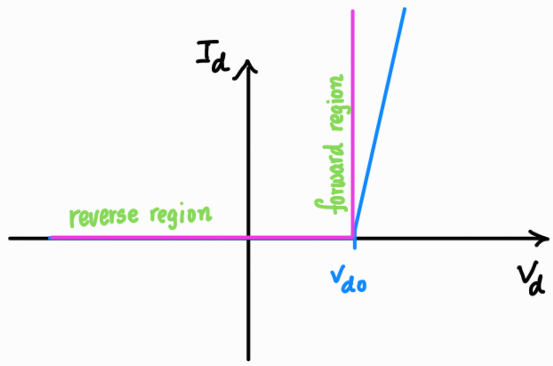
1st level of approximation —



This approximate model is called the Constant Voltage Drop + Resistance (CVD+R) model

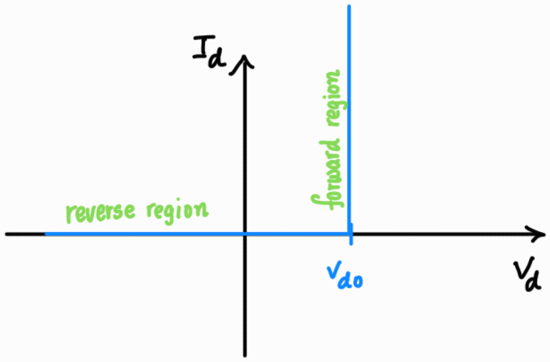
2nd level of approximation —

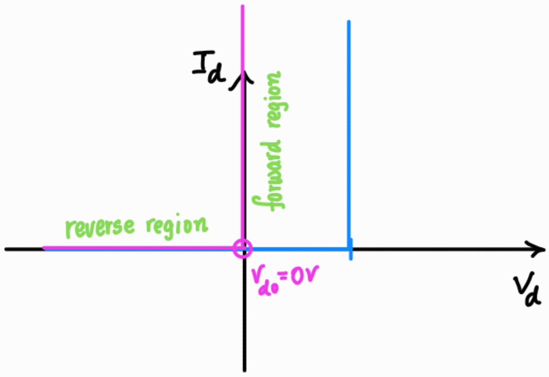




This approximate model is called the CVD model.

3rd level of approximation —

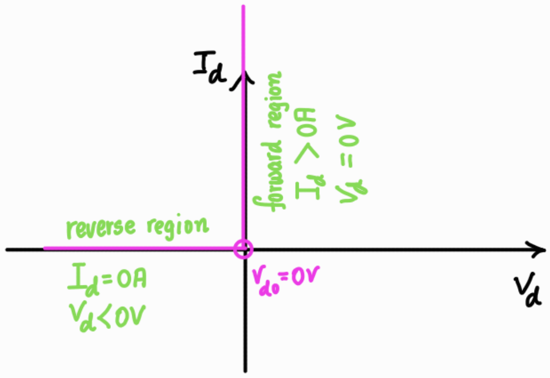
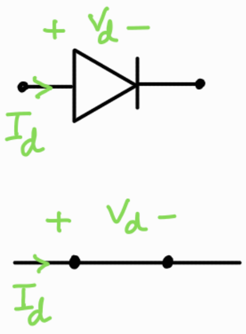
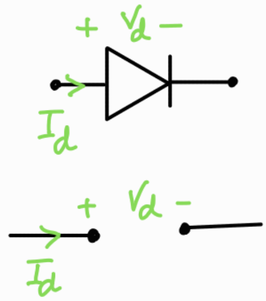
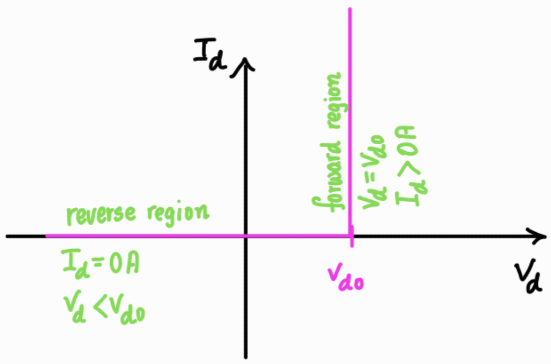
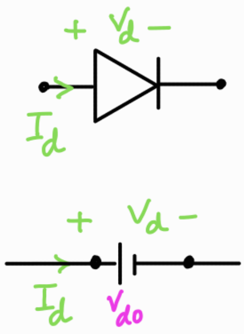
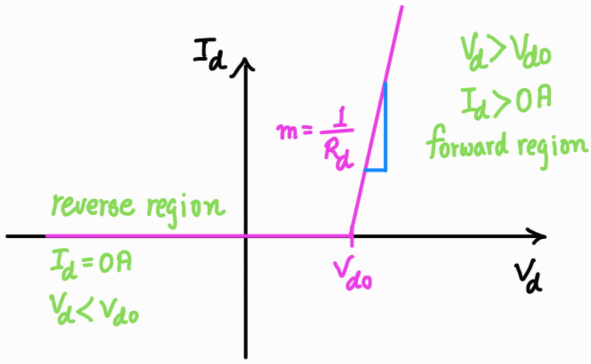
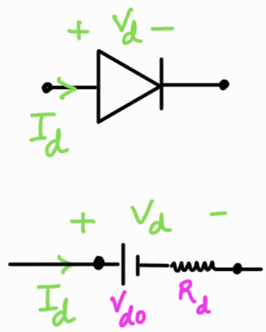




This is the ideal diode model. Its basically the CVD model with $V_{do} = 0V$

Non linear devices operate like different basic devices @ different operating regions. The mode of operation is determined by the value of I & V. For diode, we have 2 modes of operation — (i) forward region & (ii) reverse region. The I & V ranges for these regions of operation depend on the diode model being used.

For this course, at least for most parts, we will limit ourselves to ideal diode, CVD & CVD +R models. Operating regions and associated I & V ranges are compiled below —

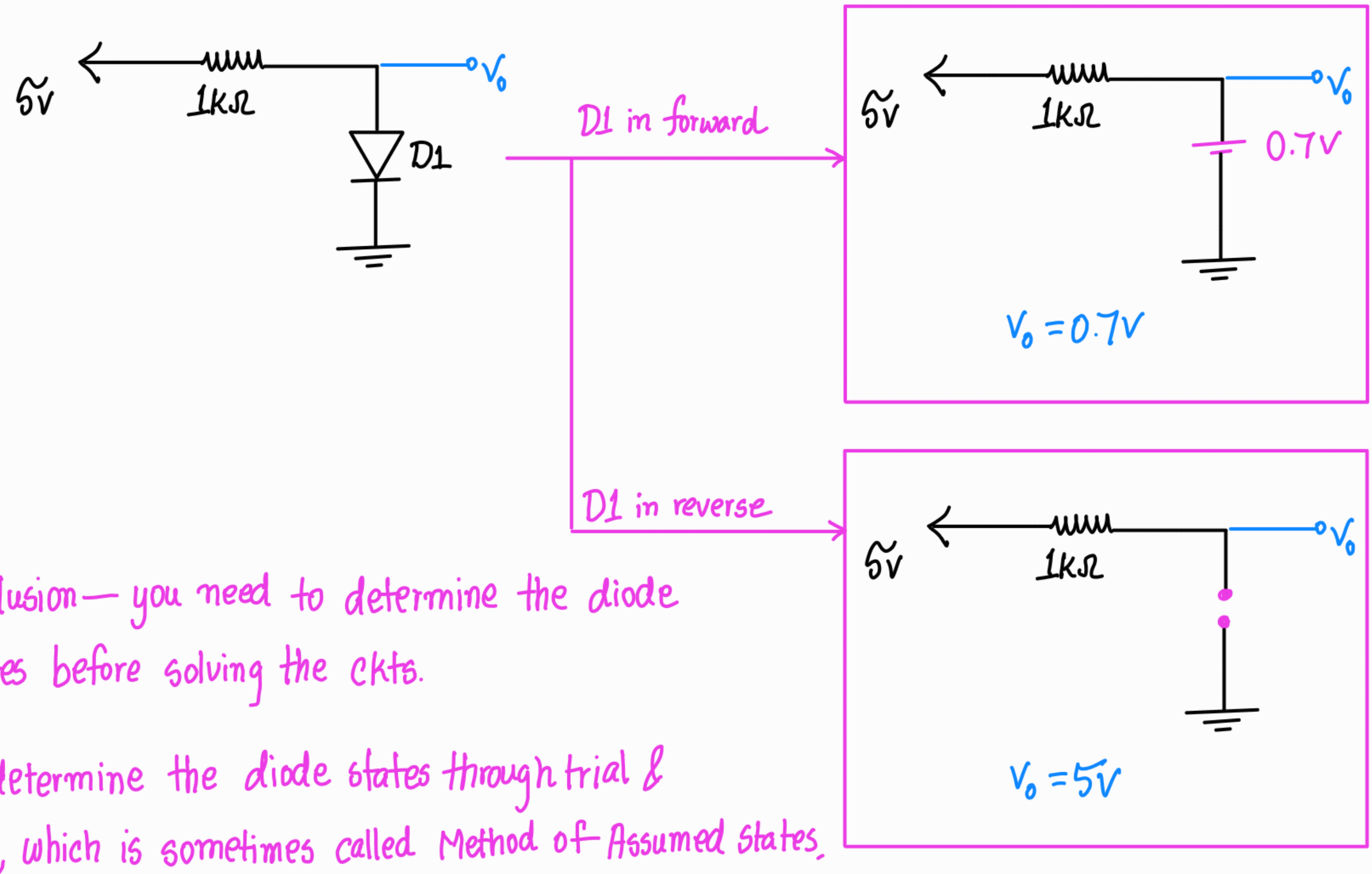
Diode model	IV ranges for different operating regions	Forward region equivalent ckt	Reverse region equivalent ckt
Ideal parameters – N/A		 $V_d = 0V$ always	 $I_d = 0A$ always
CVD parameters – V_{do}		 $V_d = V_{do}$ always	Same as ideal
CVD+R parameters – V_{do}, R_d		 $V_d = V_{do} + I_d R_d$ $\because I_d > 0A \rightarrow V_d > V_{do}$	Same as ideal

For all diode problems, diode model along with parameters will be provided. If parameters are not provided in the question, you are free to assume values. Most commonly $V_{do} = 0.7\ V$ & $R_d = 50\Omega$.

Solving ckts with diodes —

The first step of solving ckts with diodes is to first identify the operating region for each diode. Different operating states can drastically change ckt parameters.

for example, take the following ckt [assume CVD (0.7V)] —



Conclusion — you need to determine the diode states before solving the ckts.

We determine the diode states through trial & error, which is sometimes called Method of Assumed States, or MAS in short.

MAS steps —

(i) Assume the states of the diodes present in the ckt. If you have 1 diode, it can either be forward or reverse. If you have 2 diodes, they together can be (forward, forward), (forward, reverse), (reverse, forward) or (reverse, reverse). The correct combination can be any 1 of the 4. For n diodes, you will have 1 correct combination from 2^n possibilities.

(ii) Replace the diodes with their state equivalent ckts. Remember to account the diode model for this step as different diode models have different equivalent ckts (refer to the earlier table).

(iii) Solve for V_d & I_d for all the diodes.

(iv) Check the V_d & I_d for each diode against the assumed operating region IV ranges. If the calculated V_d & I_d satisfies the operating ranges for all the diodes under the assumed states, you have found the correct states. If your calculated V_d & I_d falls outside the required IV range, your assumption is wrong and you have to assume a new combination of states and repeat all the steps again. If you check the table listing the operating ranges, you will see that the state equivalent ckts will always force V_d (for forward region) & I_d (for reverse region) to match the required IV range for the corresponding operating regions. As such, it is enough to prove that $V_d < V_{do}$ for reverse region & $I_d > 0A$ for forward region, for all models.

NB — Even though there can be 2^n choices, practicing the problems will allow you to make educated guesses, which effectively brings the number of trials down to 2/3.

Whole pipeline to solve ckts with diodes —

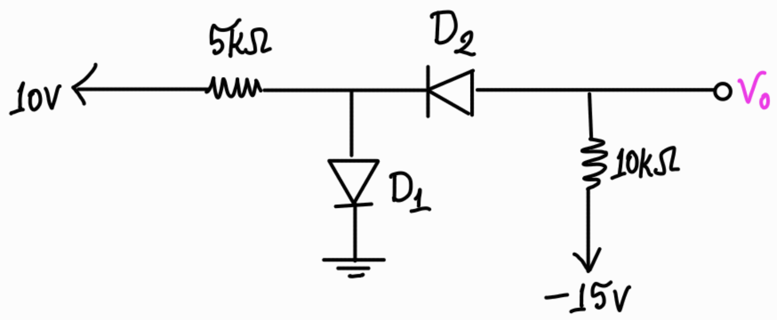
(i) Determine the correct ckt state using MAS.

(ii) Replace the ckt with equivalent state form.

(iii) Solve for the required variables.

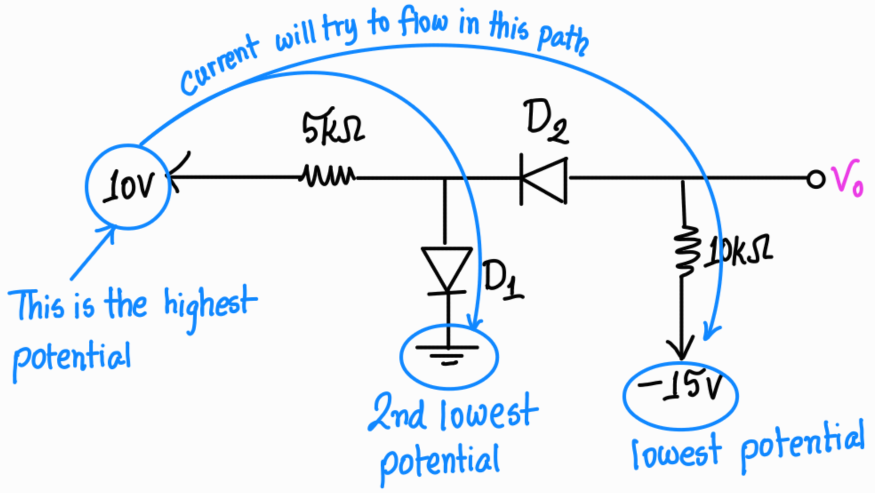
Examples —

① Determine V_o. Assume CVD (0.7V) for the diodes



Answer

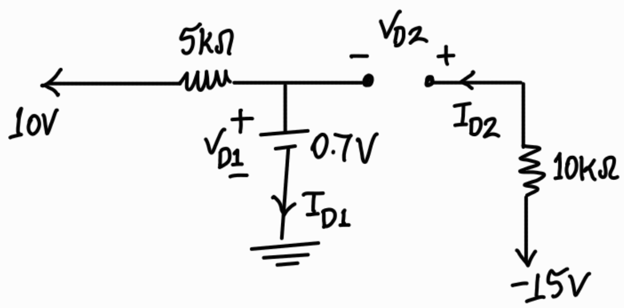
Lets make an educated guess here —



following the current flow path D1 should be forward while D2 should be reverse.

There is no way to be sure without verifying through calculation. However this is a good starting place.

Assuming D1 to be forward & D2 to be reverse, the state equivalent ckt —

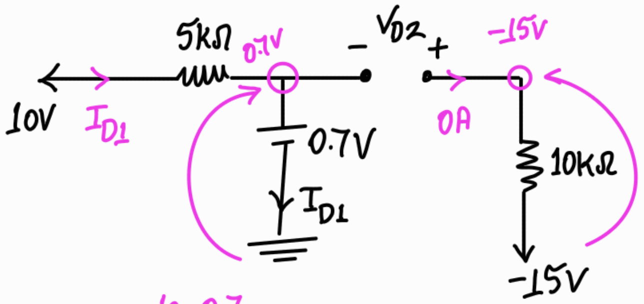


We have to prove,

$I_{D1} > 0A$ for D1 to be forward

$V_{D2} < 0.7V$ for D2 to be reverse

Remember to place the polarity & current direction properly. The terminal @ the base of the triangle gets +ve polarity & also the current enters this terminal.



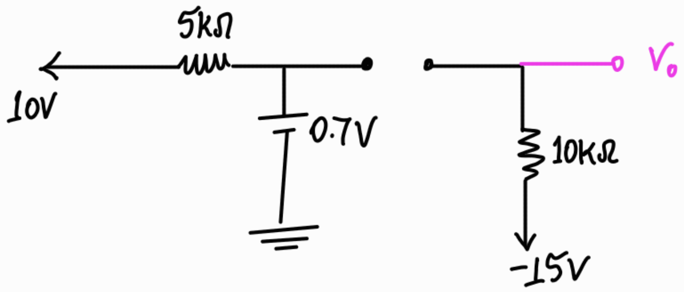
$$I_{D1} = \frac{10-0.7}{5} = 1.86mA$$

$$V_{D2} = -15-0.7 = -15.7V$$

So, $I_{D1} = 1.86mA > 0A$

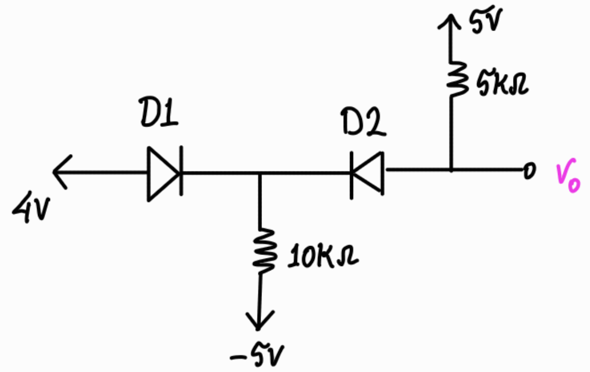
$V_{D2} = -15.7V < 0.7V$ → State verified.

So the equivalent ckt (redrawing) — You can skip this step



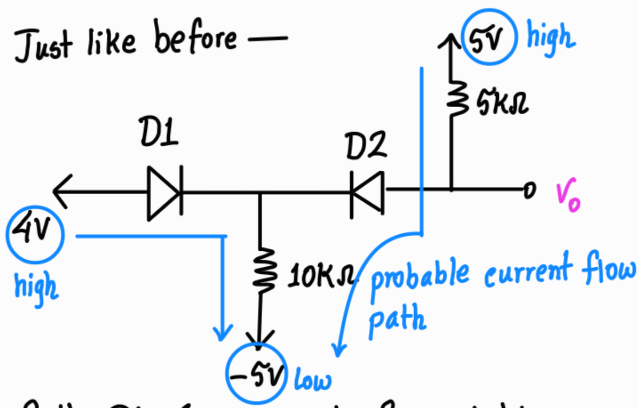
$\therefore V_o = -15V$ ← You can directly write this

② Determine V_o using CVD (0.7V) —



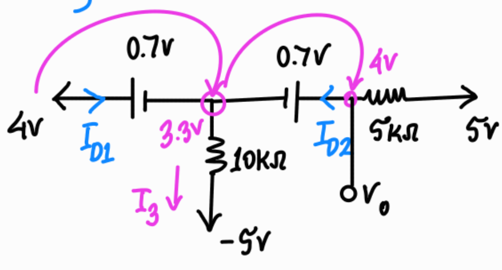
Answer —

Just like before —



Both D1 & D2 can be forward bias.

Assuming D1 & D2 to be forward bias —



$$I_3 = \frac{3.3-(-5)}{10} = 0.83mA$$

$$I_{D2} = \frac{5-4}{5} = 0.2mA > 0A$$

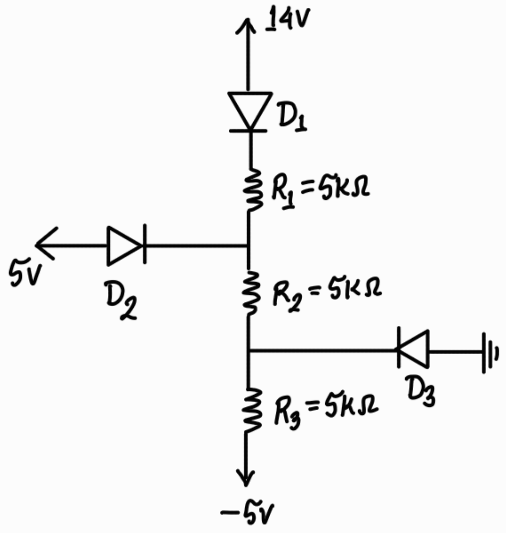
$$\therefore I_{D1} = 0.83 - 0.2 = 0.63\ mA > 0A$$

} Verified

$\therefore V_o = 4V$

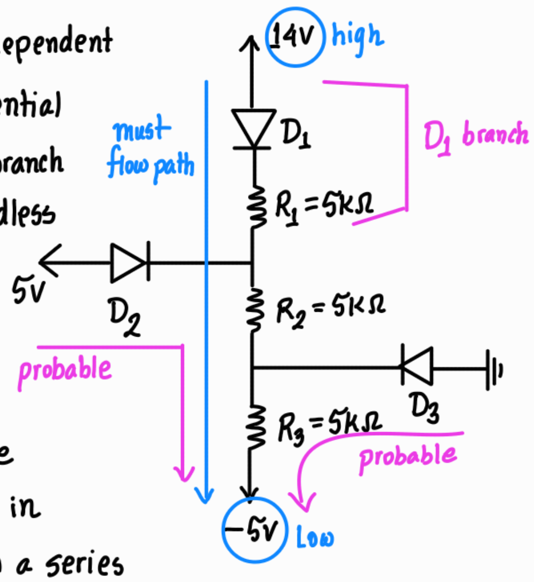
③ Determine V_{R2} assuming CVD (0.7V)

often used $\begin{cases} \text{ON} \leftarrow \text{forward} \\ \text{OFF} \leftarrow \text{reverse} \end{cases}$

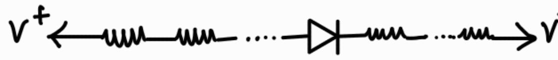


Answer —

Here, D_1 will be ON independent of D_2 and D_3. The potential difference in the D_1 branch remains adequate regardless of the states of D_2 & D_3 to turn on D_1.

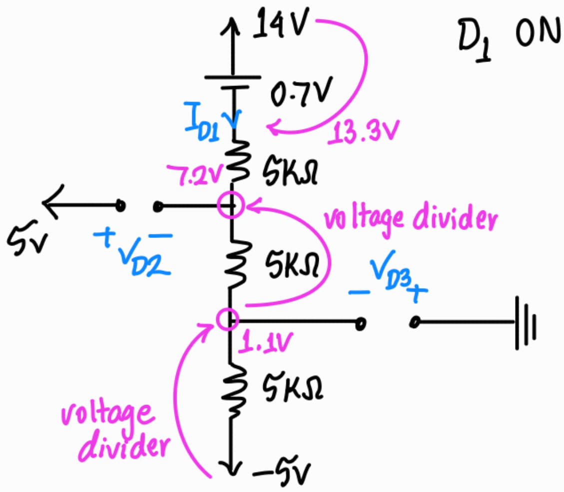


You can try out yourself. Remember that the diode gets the highest priority in terms of voltage drop in a series connection. So in a series string —



, if $v^+ - v^- > V_{do}$, the diode will be ON.

However, there is no easy way to predict the state of D_2 & D_3. You have to manually assume the states & test them. Start from the combination that is the easiest to handle, both reverse —

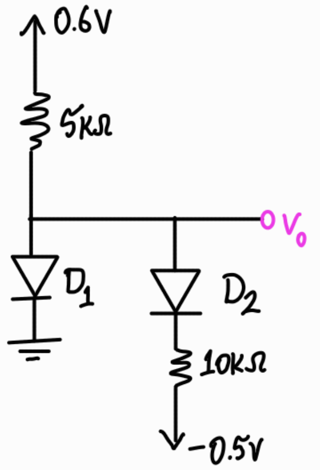


D_1 ON, D_2, D_3 OFF

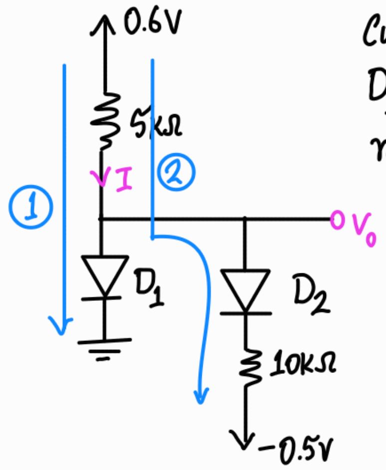
$$\left.\begin{aligned} I_{D_1} &= 1.22\text{mA} > 0\text{A} \\ V_{D2} &= 5 - 7.2 = -2.2\text{V} < 0.7\text{V} \\ V_{D3} &= 0 - 1.1 = -1.1\text{V} < 0.7\text{V} \end{aligned}\right\} \text{Correct assumption}$$

$\therefore V_{R_2} = 7.2 - 1.1 = 6.1\text{V}$

④ Determine V_o using CVD+R ($V_{do}=0.6V, R_d=50\Omega$)



Answer —



Current flowing paths. However, in path ①, D_1 shouldn't conduct. For CVD+R model, $V_d > V_{do}$ for conduction, but in line ① —

$$5I + V_{D_1} = 0.6$$

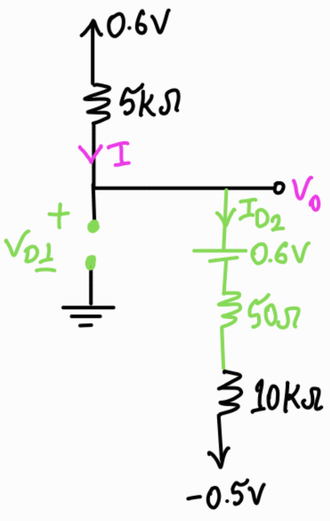
diodes block −ve current

$$\Rightarrow V_{D_1} = 0.6 - 5I \;(I \nless 0A)$$

So, D_1 will not conduct.

If D_1 doesn't conduct, everything in line ② becomes a series ckt. Since, diodes get the most priority D_2 must conduct as $V^+ - V^-$ in the string is $1.1V > 0.6V$.

So the ckt becomes —



$$I = \frac{1.1}{15000+50} = 0.073\,mA = I_{D2} > 0A$$

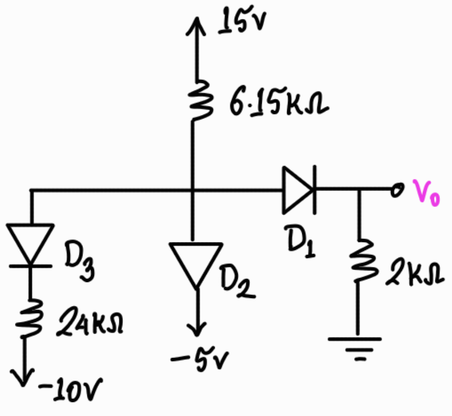
$$V_o = 0.6 - 0.073 \times 5 = 0.23455V = V_{D1} < 0.6V$$

verified

$V_o = 0.23455\ V \leftarrow$ answer

#So, sometimes you can reach solid conclusions without even using MAS.

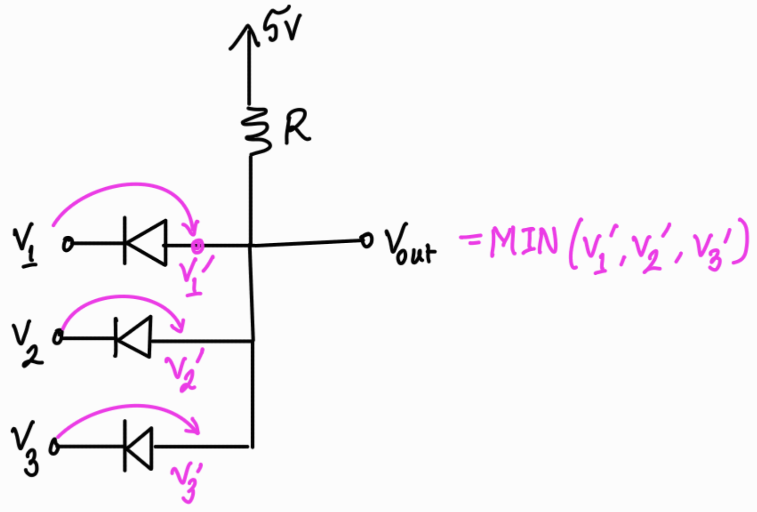
5) Determine V_0 assuming CVD (0.7V)



Answer —

This is a cool question. In the next segment, when you will learn about gates, specifically AND gate, you will find resemblence of this problem with a diode AND gate. AND gate is also called a MIN gate as in only the lowest effective input is passed on.

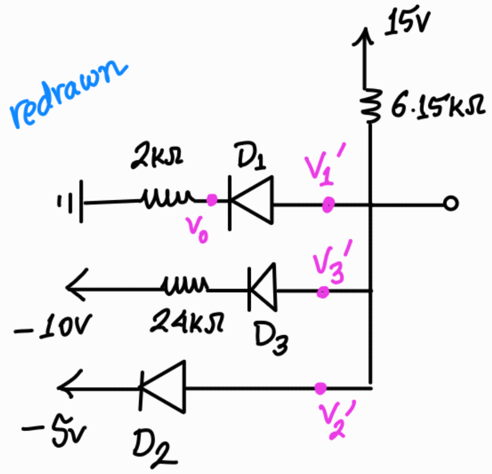
AND gate —



V_1', V_2' & V_3' are the effective voltages.

In this config only one branch conduct generally, unless multiple branches have the lowest effective voltages.

Now compare this to the given ckt—



$V_1' = 0 + 0.7 + 2i_1 = 2i_1 + 0.7$

$V_2' = -5 + 0.7 = -4.3V$

$V_3' = -10 + 0.7 + 24i_3 = -9.3 + 24i_3$

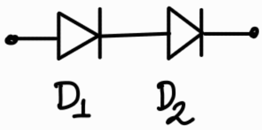
$\because i_1, i_3 > 0A$

$V_1' > V_2'$ & $V_1' > V_3'$

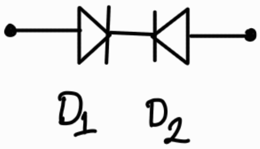
D_1 will never conduct

$\therefore V_0 = 0V$

2 special cases —

① 

If two diodes are connected in series following the same alignment, they must be in the same state — both forward or both reverse

② 

If two diodes are connected in series in the opposite alignment, both diodes must be OFF.