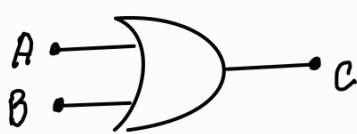
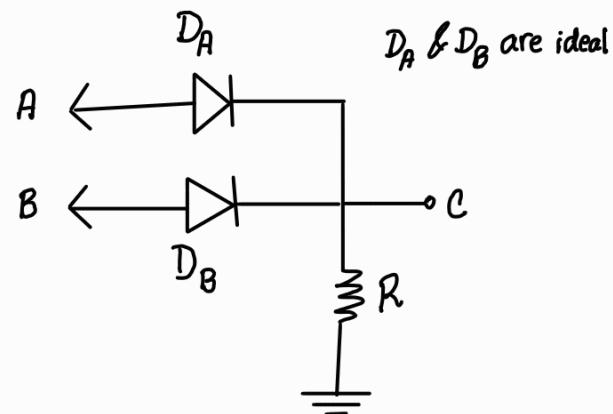


# Diode logic (DL gates) —

## OR gate (ideal diodes)



→ implemented as



Truth table —

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

→ in terms of voltages →

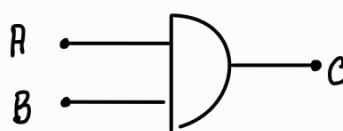
0 → 0V (low)  
1 → 5V (high)

A	B	C
0V	0V	0V
0V	5V	5V
5V	0V	5V
5V	5V	5V

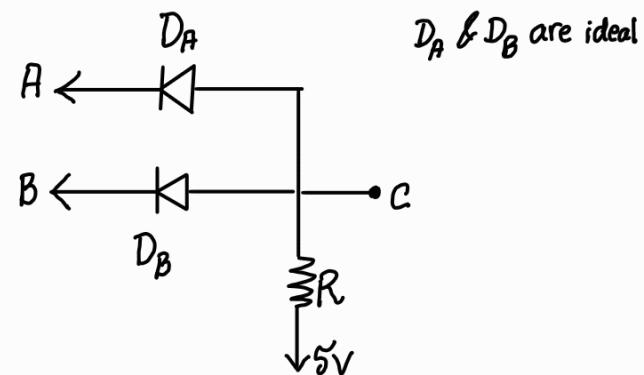
→ diode states

A	B	$D_A$	$D_B$
0V	0V	OFF	OFF
0V	5V	OFF	ON
5V	0V	ON	OFF
5V	5V	ON	ON

## AND gate (ideal diodes)



→ implemented as



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

→ in terms of voltages →

0 → 0V (low)  
1 → 5V (high)

A	B	C
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

→ diode states

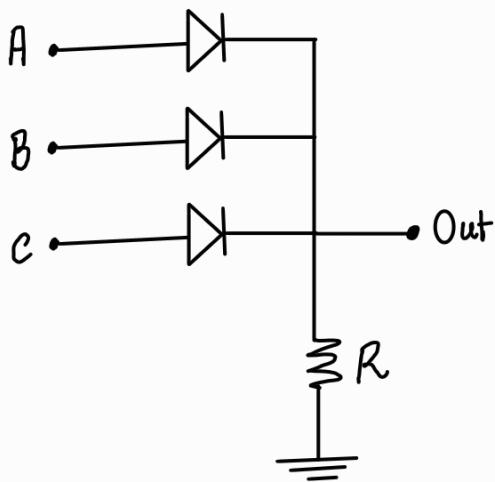
A	B	$D_A$	$D_B$
0V	0V	ON	ON
0V	5V	ON	OFF
5V	0V	OFF	ON
5V	5V	OFF	OFF

## NOT gate —

NOT gates cannot be implemented with diode logic.

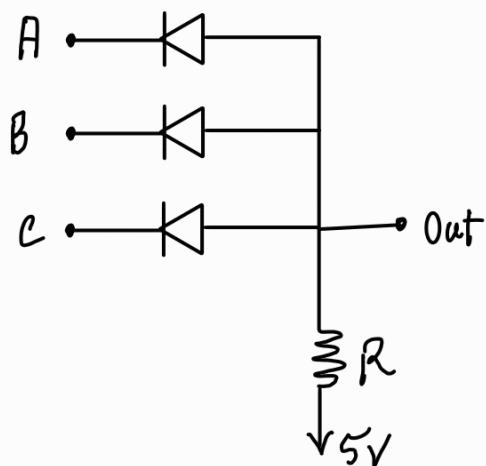
## Example—

Implement the logic function —  $A + B + C$  (+ indicates OR)



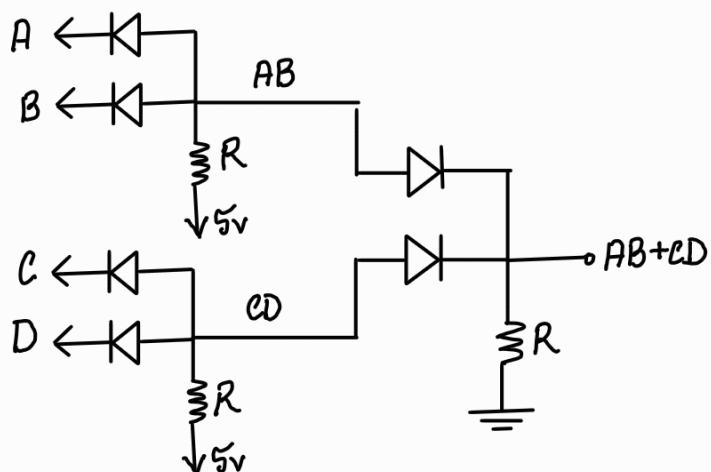
for implementing logic functions, always assume ideal diodes

Implement the logic function —  $ABC$  (multiplication indicates AND)



You can choose any R value or just keep R as placeholder, and that's perfectly fine for 251.

Implement the logic function —  $AB + CD$

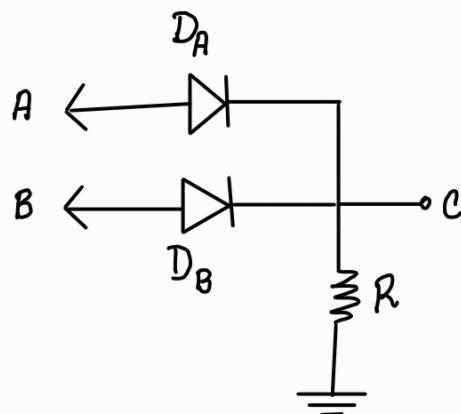


Implement the function —  $\overline{AB} + \overline{CD}$  (the bar,  $\overline{-}$ , over any variable indicates NOT)

We cannot implement NOT using DL and so this function cannot be implemented.

Diode logic (CVD model, uniform  $V_{do}$ ) —

OR gate —



assume same forward barrier voltage for  $D_A$  &  $D_B$

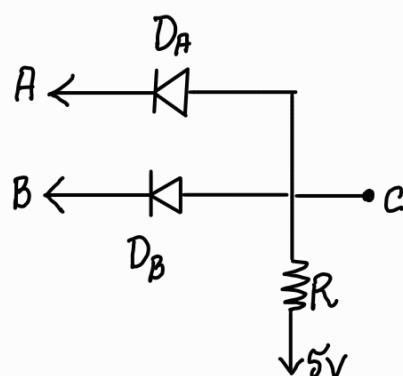
A	B	$D_A$	$D_B$	Expected C	C
0V	0V	OFF	OFF	0V	0V
0V	5V	OFF	ON	5V	$5 - V_{do}$ V
5V	0V	ON	OFF	5V	$5 - V_{do}$ V
5V	5V	ON	ON	5V	$5 - V_{do}$ V

try using MAS

High state gets degraded

The config still acts like an OR gate, however this type of CVD models will be given as analysis problems & not as design problems.

AND gate —

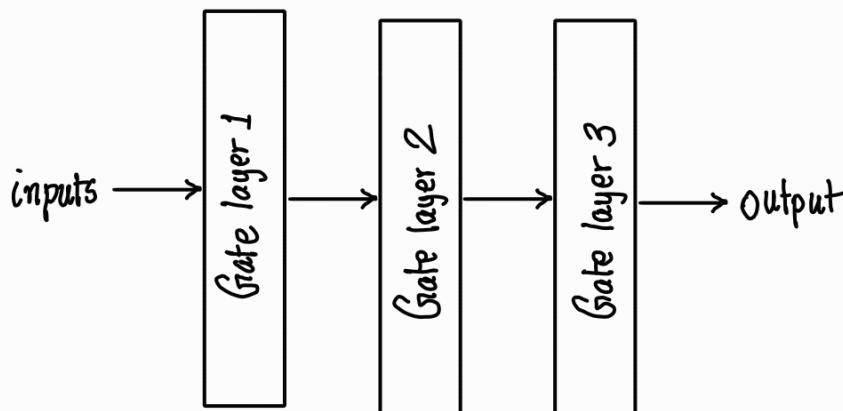


A	B	$D_A$	$D_B$	Expected C	C
0V	0V	ON	ON	0V	$V_{do}$ V
0V	5V	ON	OFF	0V	$V_{do}$ V
5V	0V	OFF	ON	0V	$V_{do}$ V
5V	5V	OFF	OFF	5V	5V

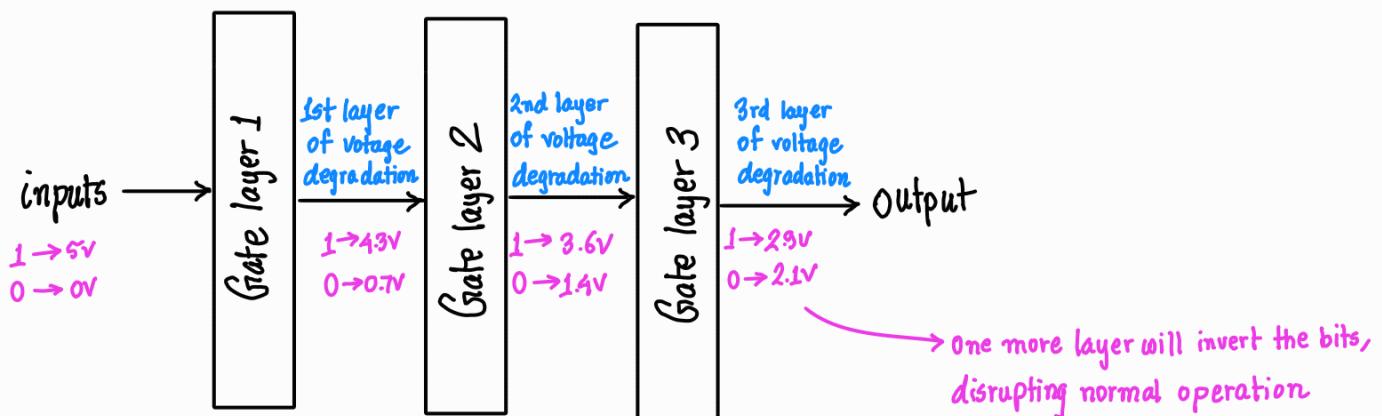
Low state gets degraded

## DL gates & their practicality — (skippable)

Since diode logic gate degrades the outputs, something unwanted happens when you use DL gates in practical applications. Practical applications require multiple gates cascaded one after another. Let's consider a simpler version of gates connected in layers —



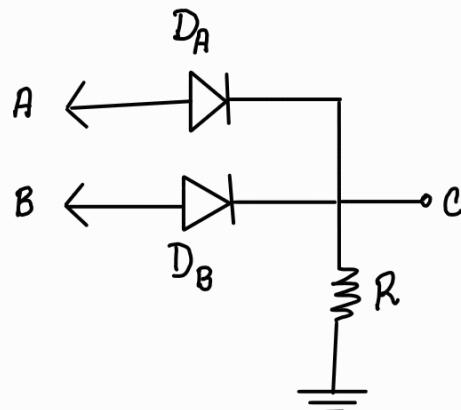
Assume that each layer is composed of AND & OR gates without any cascading. However the next layer is cascaded to the previous one, as in the next layer uses the outputs of the previous layer as inputs. For example, in the given figure, layer 2 is cascaded upon layer 1 and uses the outputs of layer 1 as inputs. Consider all the gates belong to DL family with CVD diodes ( $V_{d0} = 0.7V$ ). For the inputs logic 1 is represented by 5V and logic 0 is represented by 0V. Let's see what happens to the voltage levels after 3 layers of gates —



So in practical operations, we never use DL gates.

# Diode logic (Ideal model, unequal state voltages @ input) —

OR gate (acts as a MAX gate) —



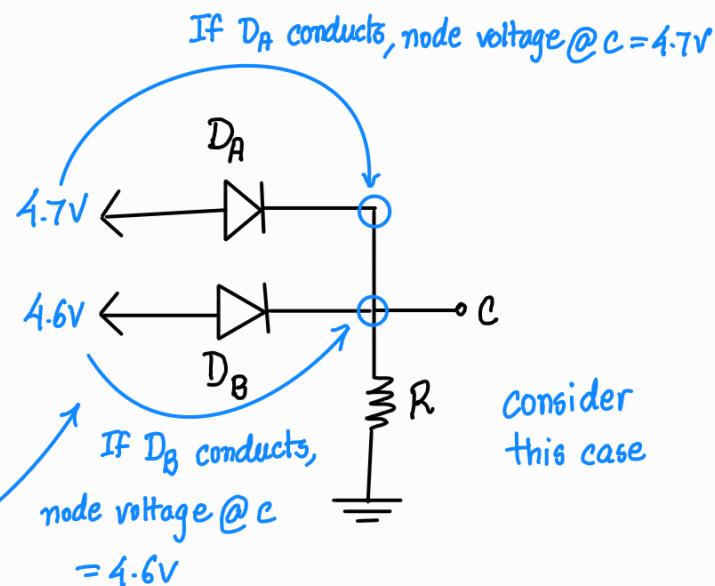
	Expected	A	B
Low	0V	0.5V	0.6V
High	5V	4.7V	4.6V

This type of degradation can happen after one layer of DL gates as seen in the prev. segment

A	B	D <sub>A</sub>	D <sub>B</sub>	C = MAX(A, B)
0.5V	0.6V	OFF	ON	0.6V
0.5V	4.6V	OFF	ON	4.6V
4.7V	0.6V	ON	OFF	4.7V
4.7V	4.6V	ON	OFF	4.7V

try using MAS

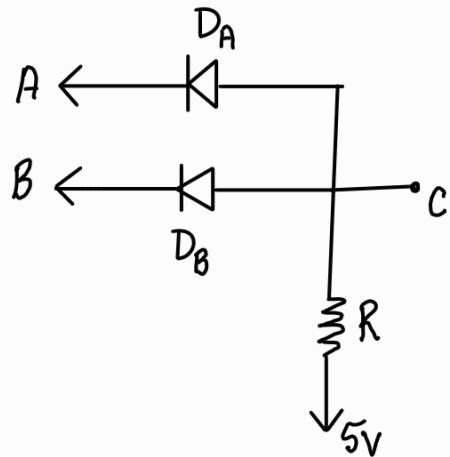
The ON OFF schedule changes as well.  
For this case generally one diode will stay ON unless multiple diode branches are connected to the same input voltage values.



consider this case

2 different node voltages cannot exist @ the same node. Hence both D<sub>1</sub> & D<sub>2</sub> cannot conduct at the same time.

AND gate (acts as a MIN gate)



	Expected	A	B
Low	0V	0.5V	0.6V
High	5V	4.7V	4.6V

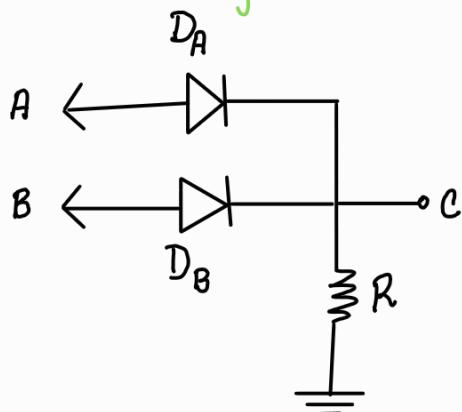
A	B	D <sub>A</sub>	D <sub>B</sub>	C = MIN(A,B)
0.5V	0.6V	ON	OFF	0.5V
0.5V	4.6V	ON	OFF	0.5V
4.7V	0.6V	OFF	ON	0.6V
4.7V	4.6V	OFF	ON	4.6V

Same pattern as before.

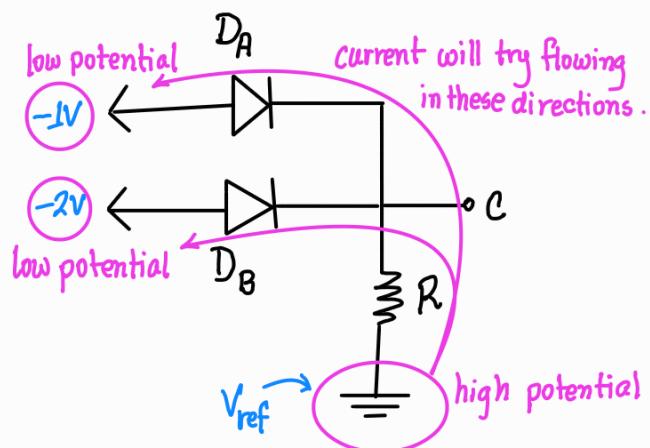
MAX gate is a more generalized version of an OR gate & MIN gate is a more generalized version of an AND gate. So for analysis problems (examples coming up soon) you can start by using the concepts of MAX & MIN gates directly instead of trying OR or AND gates.

Working range for MIN MAX gates for ideal diode construction —

Consider the MAX gate —



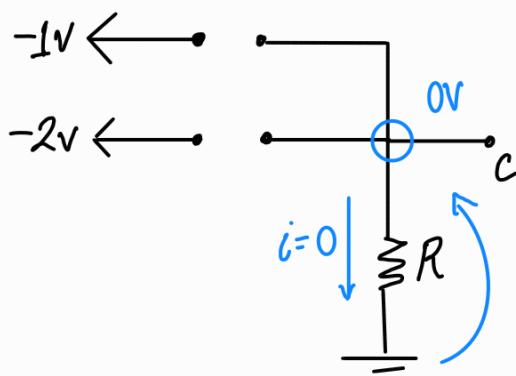
Assume  $A = -1V$  &  $B = -2V$ . Then the ckt —



So,  $D_A$  &  $D_B$  will both be OFF. Basically when inputs are lower than the  $V_{ref}$ , 0V here, none of the diodes will conduct. What will be the value of  $C$  then?

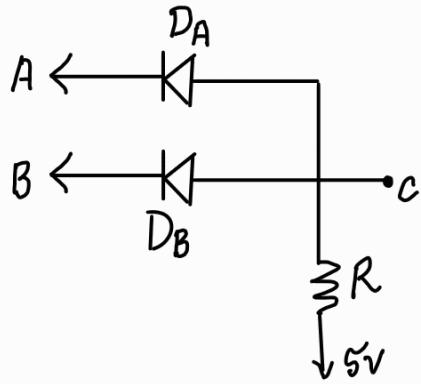
For such cases the value of  $C$  will be determined by the rest of the ckt.

for this case the ckt becomes —

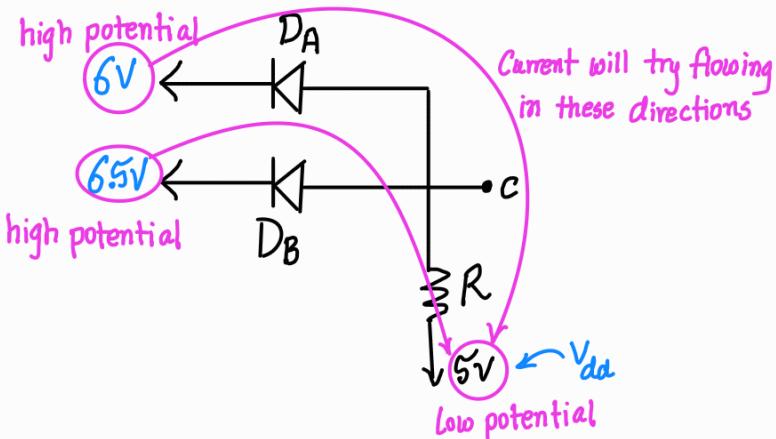


$\therefore C = 0V$  ← the mathematical problems will not always be this simple. Check the last example. Also check the ps @ the end.

Consider the MIN gate —



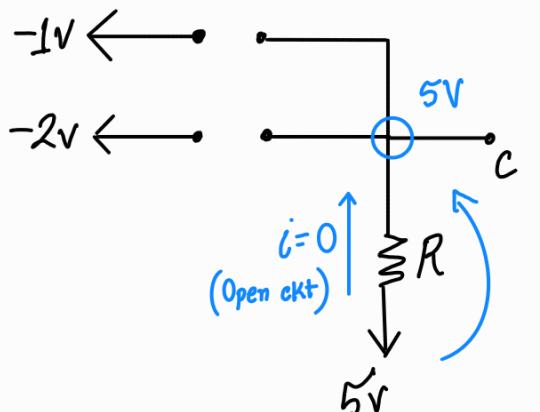
Assume  $A = 6V$  &  $B = 6.5V$  —



So both  $D_A$  &  $D_B$  will remain OFF. This scenario occurs when input voltages are higher than  $V_{dd}$ , 5V here. What will be the value of C here?

Just like before, the value of C will depend on the rest of the ckt

for this case the ckt becomes —

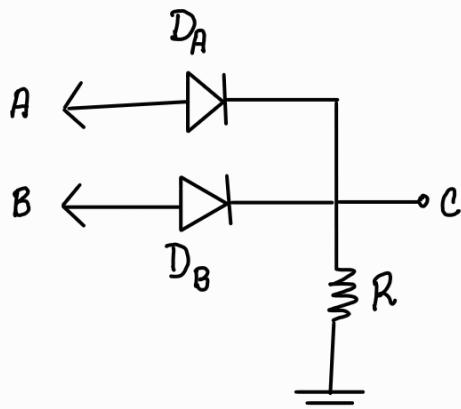


$\therefore C = 5V$  ← same caveat applies here.

Before going to the examples, we need to see 2 more cases for MIN MAX gates.

## MIN MAX gates for CVD diodes, uniform $V_{do}$

Now just doing MIN, MAX on input voltages will not be enough. The input voltages will degrade a bit owing to the CVD model. The output for MAX gate will become  $\text{MAX}(\text{inputs}) - V_{do}$  & for the MIN gate will become  $\text{MIN}(\text{inputs}) + V_{do}$ . For example take the previous MAX gate example —

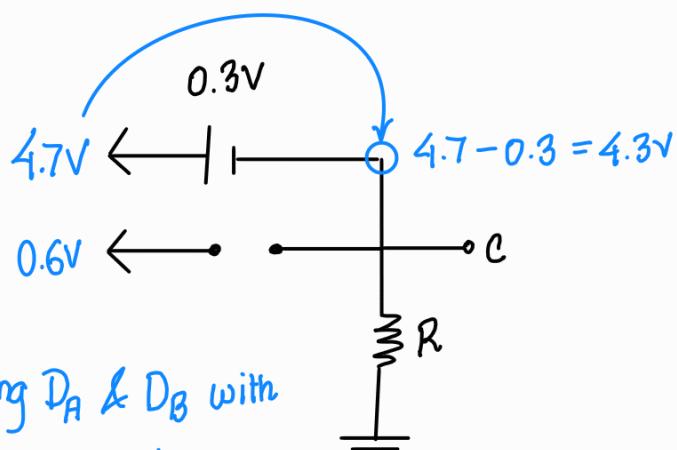


	Expected	A	B
Low	0V	0.5V	0.6V
High	5V	4.7V	4.6V

Assume CVD (0.3V)

A	B	$D_A$	$D_B$	$C = \text{MAX}(A, B) - V_{do}$
0.5V	0.6V	OFF	ON	$0.6V - V_{do} = 0.3V$
0.5V	4.6V	OFF	ON	$4.6V - V_{do} = 4.3V$
4.7V	0.6V	ON	OFF	$4.7V - V_{do} = 4.4V$
4.7V	4.6V	ON	OFF	$4.7V - V_{do} = 4.4V$

→ Let's see this particular case & understand how we get the output value



replacing  $D_A$  &  $D_B$  with state equivalent ckt

Well this feels a bit roundabout. In fact this method of figuring out the output value will not work for the next case where every diode have different forward barrier voltages. Well you can always solve using MAS but there is an easier way when you work within a certain boundary.

Let's skip the MIN gate. You can try it out yourself and instead learn the most general case.

## MIN MAX gates for CVD diodes, non uniform $V_{do}$

This is the most general case and we deal it with by updating our formulas—

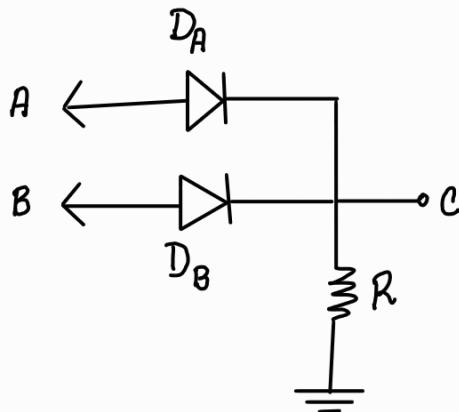
MAX (inputs) become MAX (effective inputs) for MAX gate.

MIN (inputs) become MIN (effective inputs) for MIN gate.

So what are the effective inputs?

Effective input is the voltage reflected at the output node for a certain input voltage assuming the input branch to be in forward region while keeping all the rest in reverse.

Lets understand this with an example—

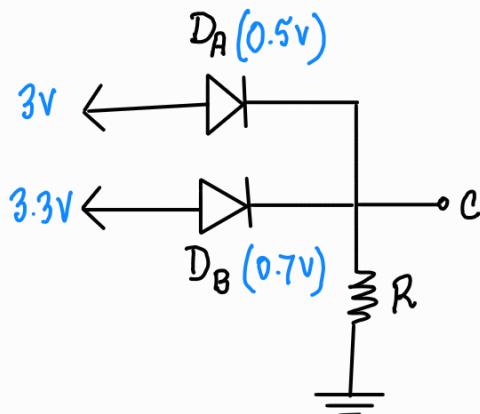


for this MAX gate,  $A = 3V$  &  $B = 3.3V$

$$V_{D_A} = 0.5V \quad \& \quad V_{D_B} = 0.7V$$

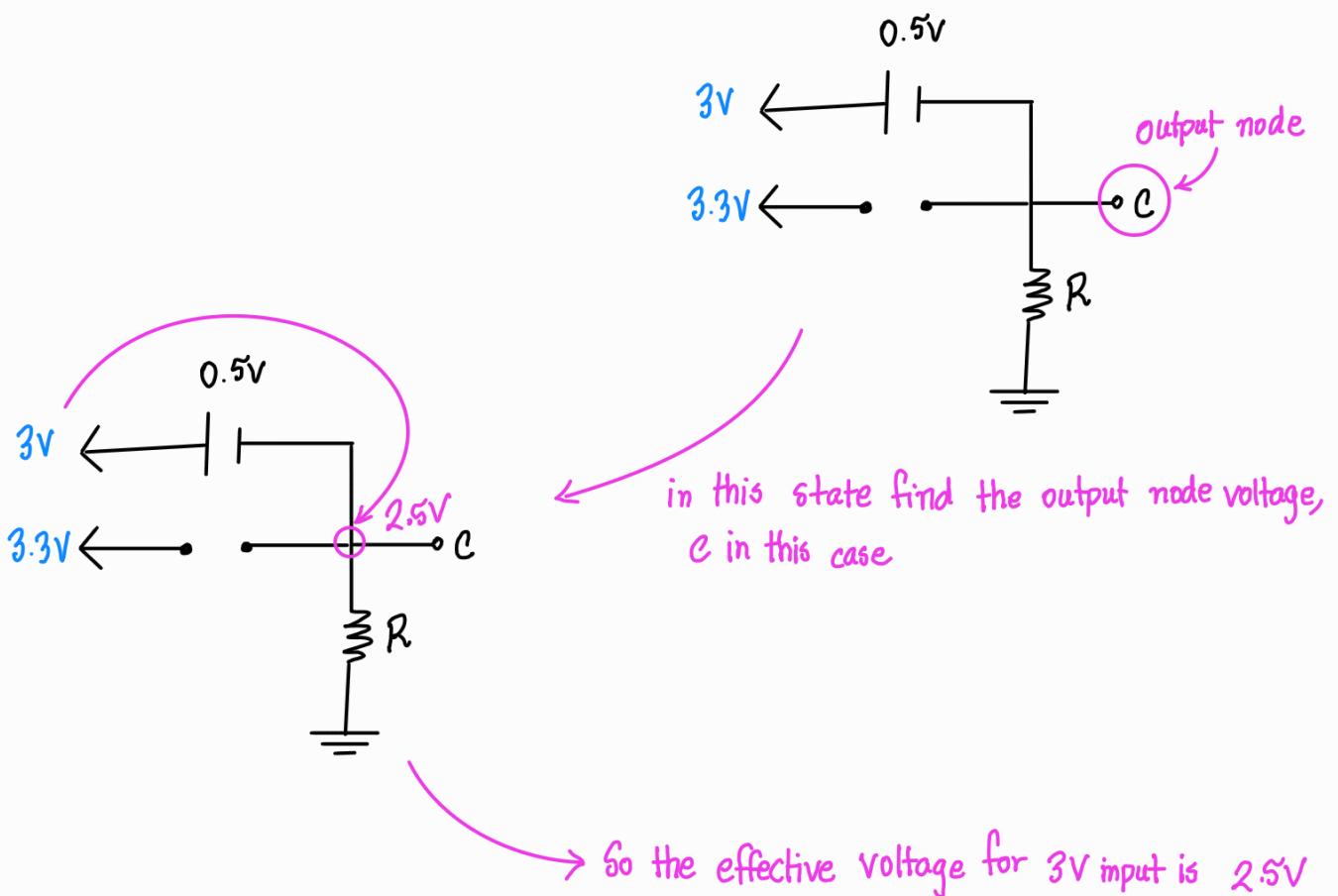
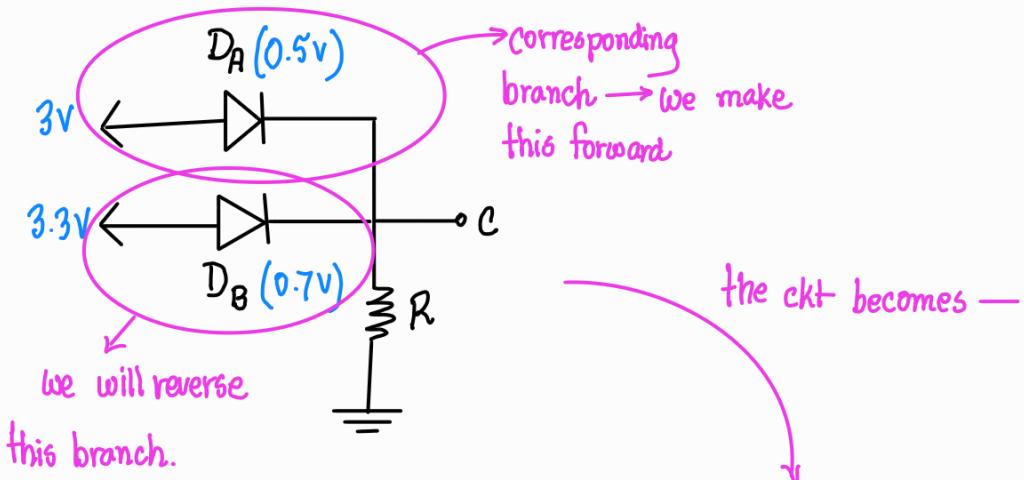
what are the effective voltages for A & B? What will be the output voltage @ C?

Lets rewrite the Ckt with the given values—



Now lets find the effective input voltage for 3V—

To find the effective value of 3V input, we make the corresponding branch forward & reverse every other input branches —

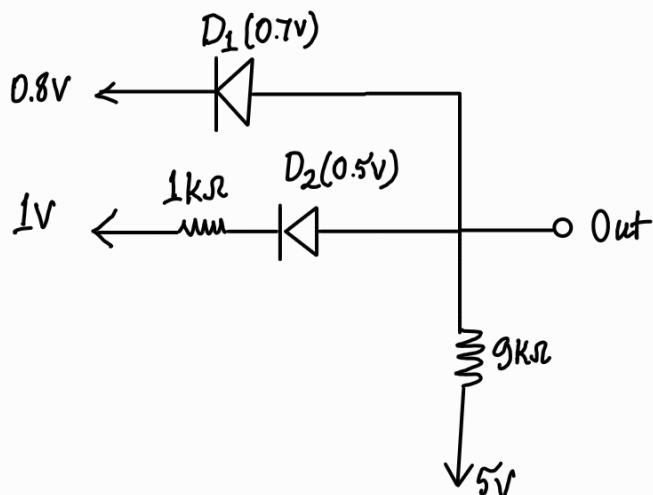


If you proceed in the same way for 3.3V input, you will get an effective input of 2.6V

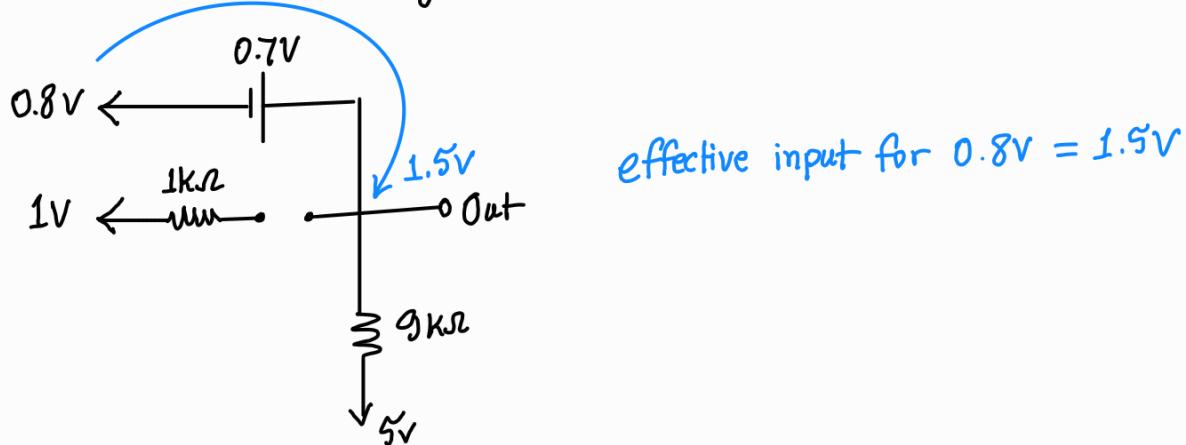
So the final output voltage =  $\text{MAX}(2.5, 2.6) = 2.6V$

Another example — a little harder this time —

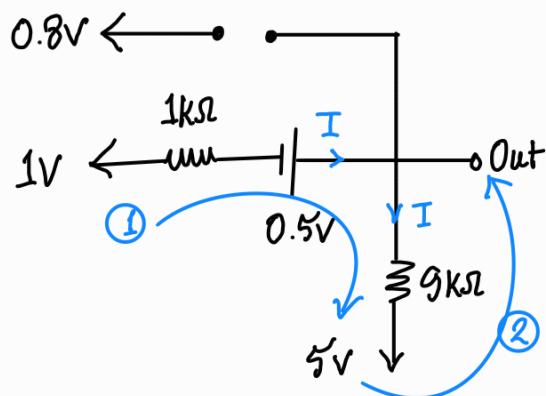
Find the output voltage for the given MIN gate —



to find the effective input voltage for 0.8V, the ckt becomes —



to find the effective voltage for 1V input, the ckt becomes —



KVL in line 1 —

$$I - 0.5 + 9I = 1 - 5$$

$$\Rightarrow I = -0.35 \text{ mA}$$

KVL in line 2 —

$$-9 \times (-0.35) = 5 - \text{out}$$

$$\Rightarrow \text{out} = 5 - 3.15 = 1.85 \text{ V}$$

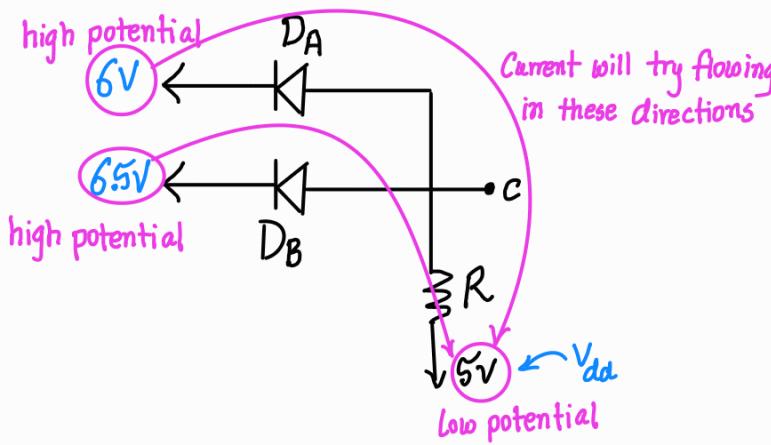
∴ effective input voltage for 1V = 1.85V

$$\therefore \text{out} = \text{MIN}(1.5, 1.85) = 1.5 \text{ V}$$

Working range for MIN MAX gates for non-uniform CVD diode construction —

Unlike before where we only accounted for input voltages, we have to account for effective inputs now —

Assume  $A = 6V$  &  $B = 6.5V$  —



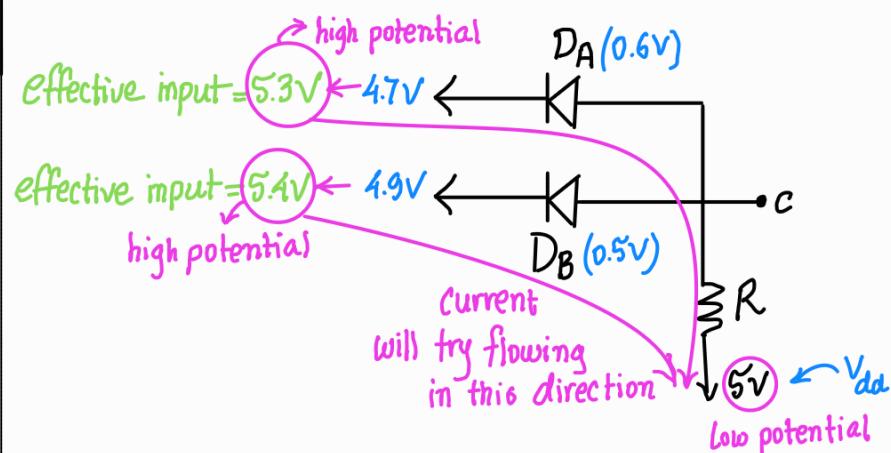
Recap for MIN gate

So both  $D_A$  &  $D_B$  will remain OFF. This scenario occurs when input voltages are higher than  $V_{dd}, 5V$  here.

update

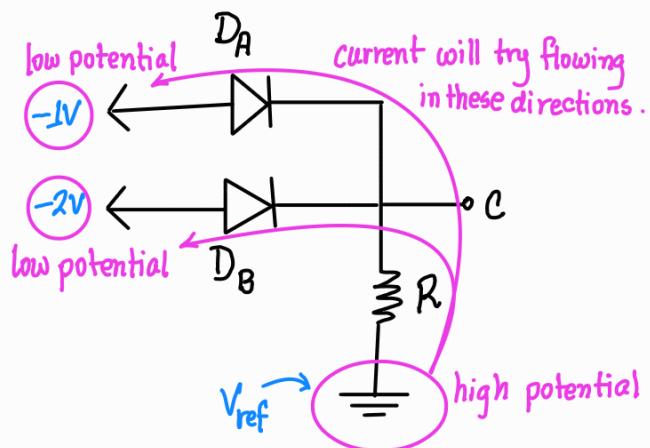
Try using MAS

Assume  $A = 4.7V$  &  $B = 4.9V$ ;  $V_{D_A} = 0.6V$  &  $V_{D_B} = 0.5V$



So both  $D_A$  &  $D_B$  will remain OFF. This scenario will now occur when effective input voltages are higher than  $V_{dd}, 5V$  here.

Assume  $A = -1V$  &  $B = -2V$ . Then the ckt —



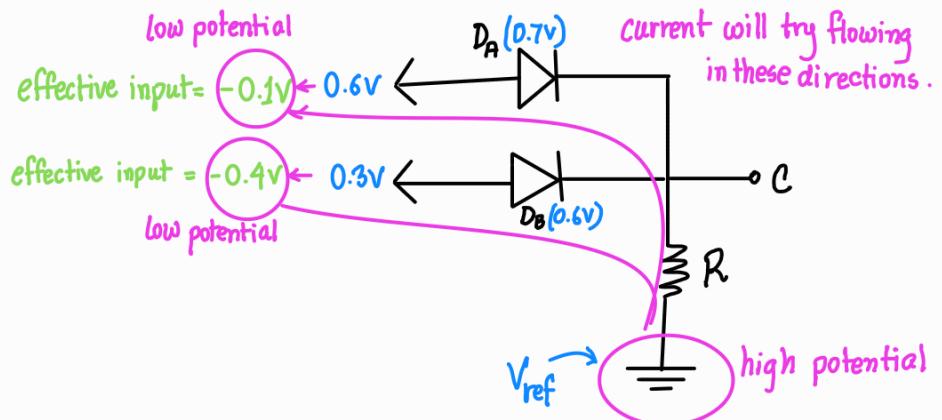
Recap for MAX gate

So,  $D_A$  &  $D_B$  will both be OFF. Basically when inputs are lower the  $V_{ref}$ , OV here, none of the diodes will conduct.

updating

Try using MAS.

Assume  $A = 0.6V$  &  $B = 0.3V$ ;  $V_{D_A} = 0.7V$  &  $V_{D_B} = 0.6V$  —

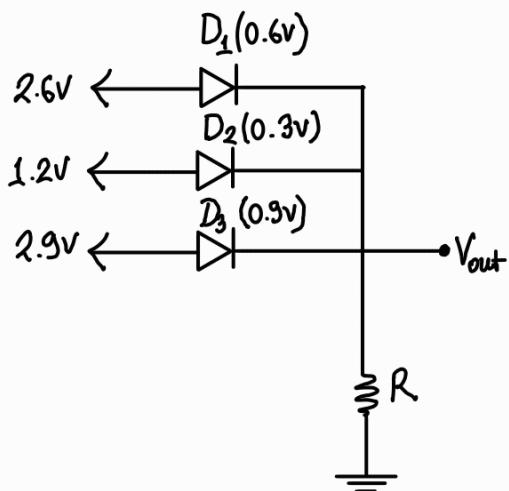


So,  $D_A$  &  $D_B$  will both be OFF. The updated criteria now is that effective input must be less than  $V_{ref}$ , OV in this case for both the input diodes to be off.

final note — to find the value of  $C$ , reverse the two diodes and find  $C$  from the rest of the ckt.

## Examples —

(i) Find  $V_{out}$ . Which of the diodes will conduct?



Answer —

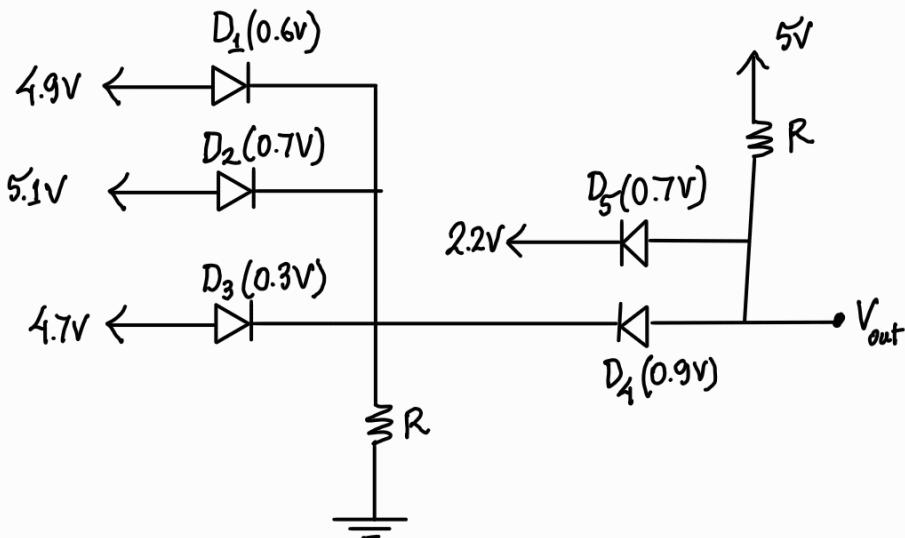
effective voltages —

$$\begin{aligned} 2.6V &\rightarrow 2V \\ 1.2V &\rightarrow 0.9V \\ 2.9V &\rightarrow 2V \end{aligned}$$

$$\therefore V_{out} = \text{MAX}(2, 0.9, 2) = 2V$$

2V is the effective voltage for the 2.6V & 2.9V inputs.  
So,  $D_1$  &  $D_2$  will conduct.

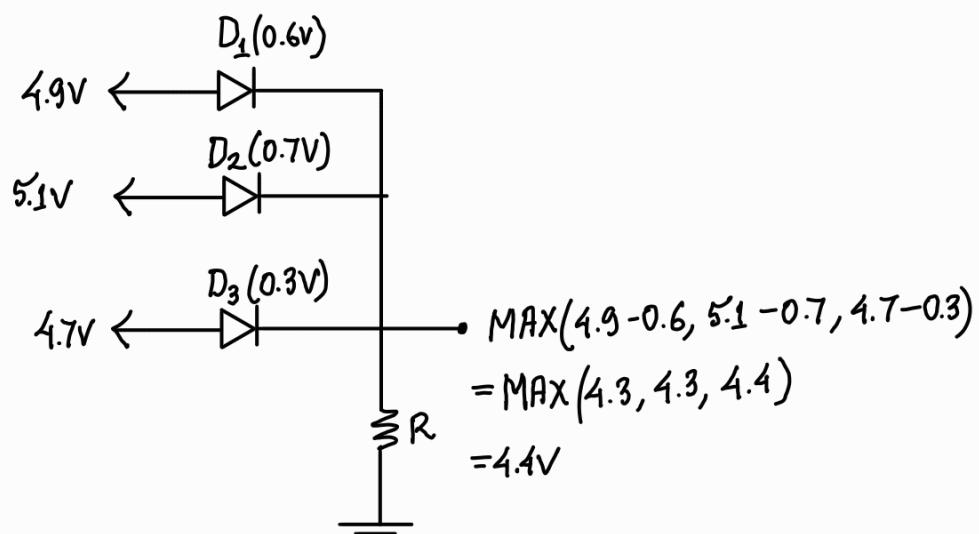
(ii) Find  $V_{out}$ .



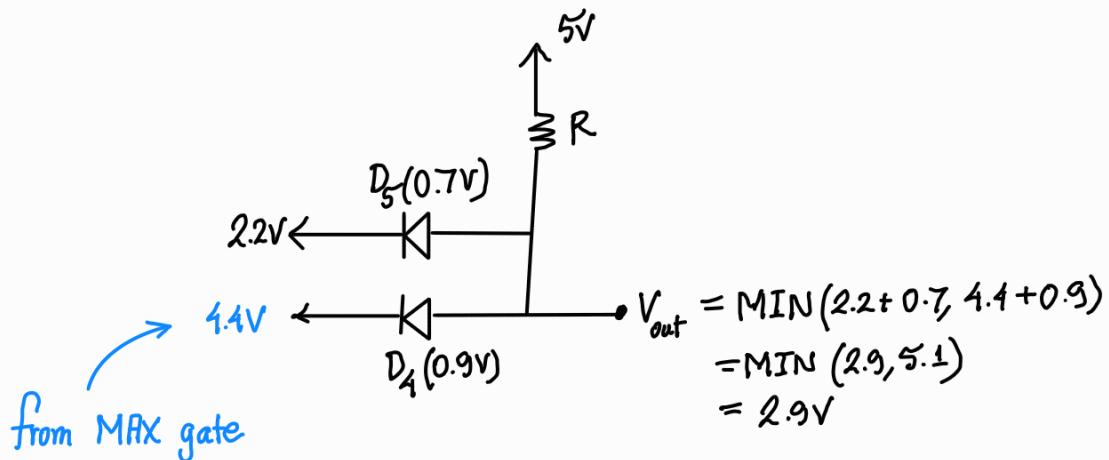
Answer —

Always start from the original inputs for cascades such as this —

For the left MAX gate —



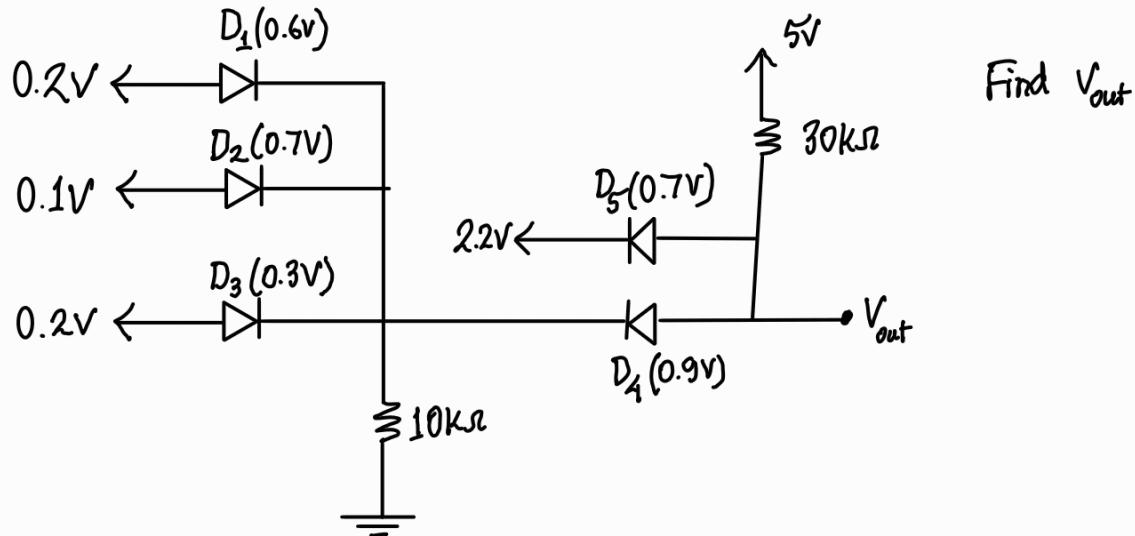
Now for the right MIN gate —



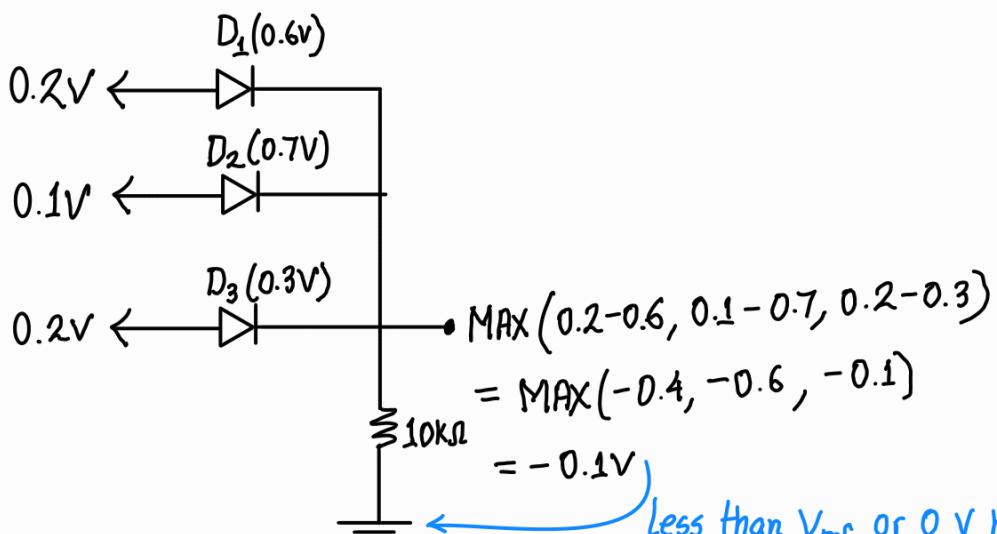
When a gate has conducting input paths, you can just drop the ckt with its output voltage

But the math becomes harder when the earlier gates do not conduct. Consider —

iii



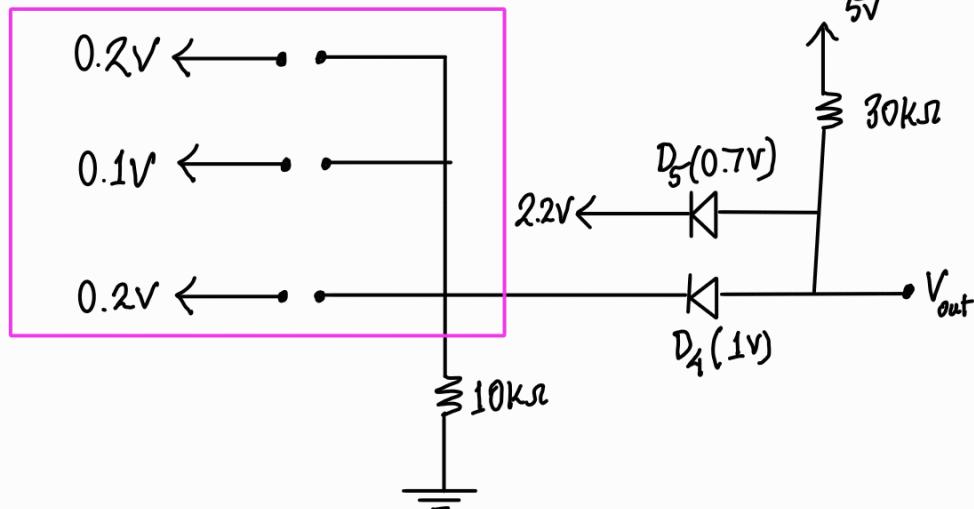
for the left MAX gate —



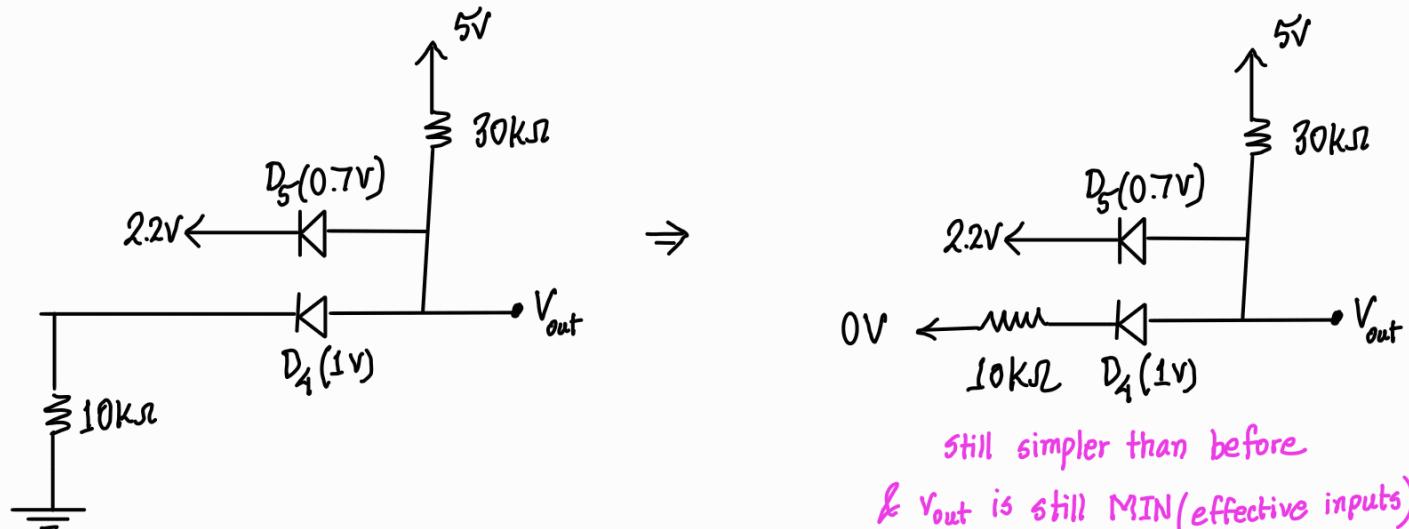
Less than  $V_{ref}$  or 0V here. So, none of the diodes will conduct. The output will depend on the rest of the ckt.

Reversing  $D_1$ ,  $D_2$  &  $D_3$ , the ckt becomes —

(we can just omit this part)

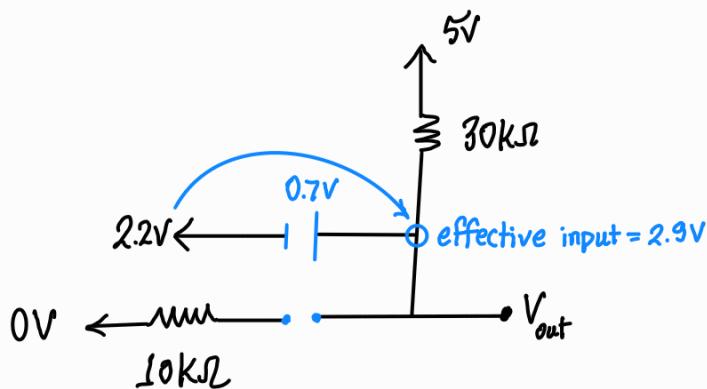


then the ckt becomes —



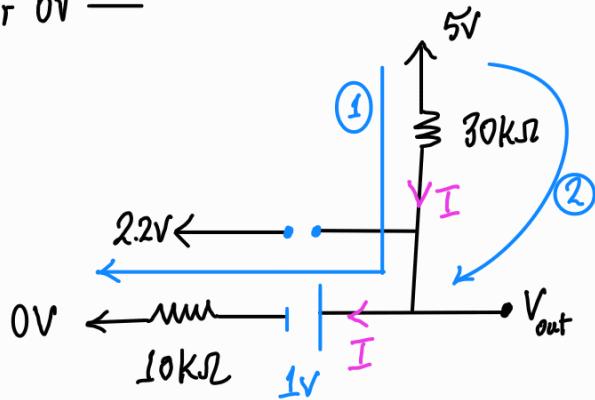
effective inputs —

for 2.2V —



If you do not understand what is going on here, I would suggest you to go through the MIN MAX gates for CVD diodes, non uniform  $V_{do}$  section.

for OV —



KVL in line 1 —

$$30I + 1 + 10I = 5 - 0$$

$$\Rightarrow I = 0.1 \text{ mA}$$

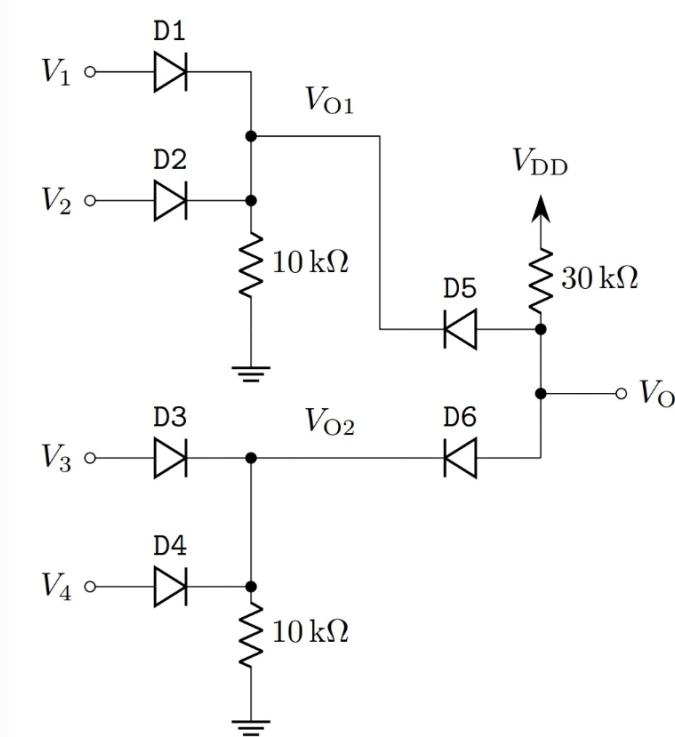
$$\therefore V_{out} = 5 - 30 \times 0.1 \quad [\text{KVL in line 2}] \\ = 2V$$

$\therefore$  effective input = 2V

So finally,  $V_{out} = \text{MIN}(2.2, 2) = 2V$

Now lets look at the mid problem —

iv) Find  $V_o$



Input voltages

$$V_1 = 2V$$

$$V_2 = 2.2V$$

$$V_3 = -2V$$

$$V_4 = -3V$$

$$V_{D1} = 0.3V$$

$$V_{D2} = 0.7V$$

$$V_{D3} = 0.5V$$

$$V_{D4} = 0.9V$$

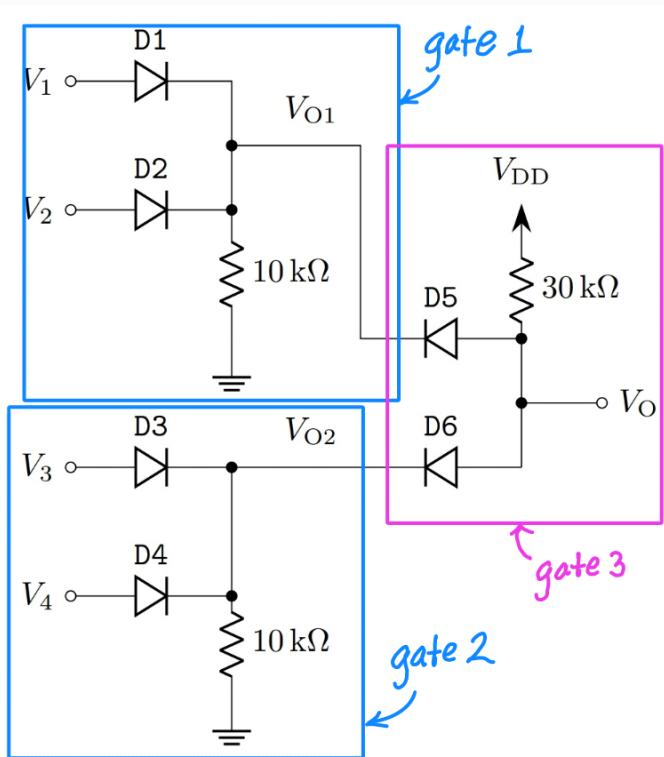
$$V_{D5} = 1V$$

$$V_{D6} = 1V$$

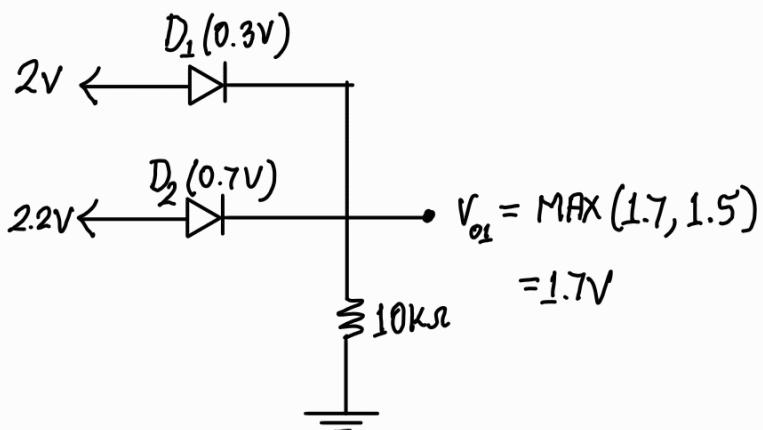
Barrier voltages

Answer —

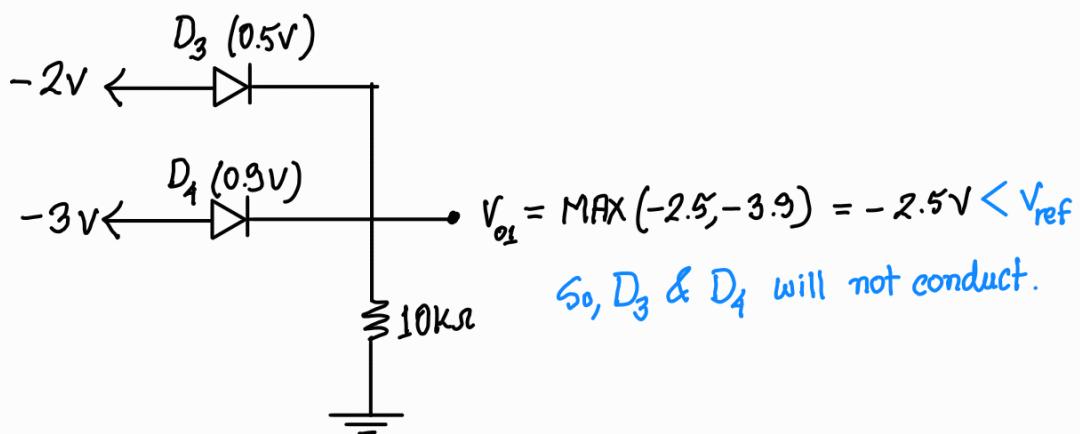
Let's label the gates and deal with them one at a time —



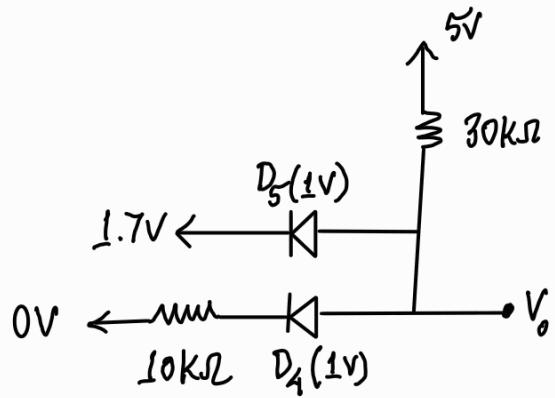
for gate 1 —



for gate 2 —



At this point, the ckt boils down to —



effective value of 1.7V — 2.7V

effective value of 0V — 2V → same as last example

$$\therefore V_o = \text{MIN}(2.7, 2) = 2V$$

PS — this is a hard problem. Chances of such hard problems being set for this mid is very very low.