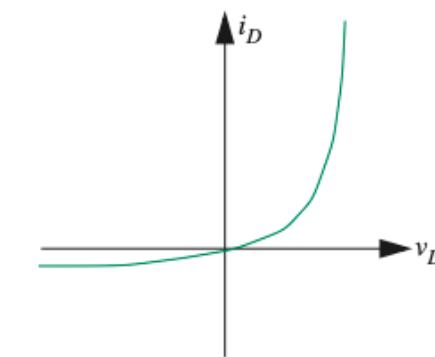
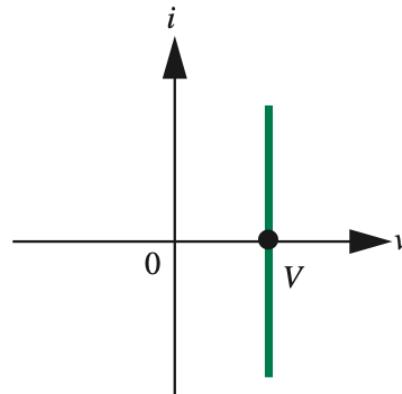
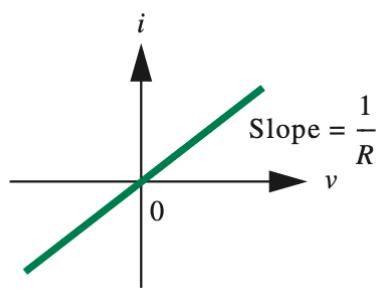
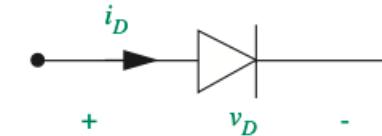
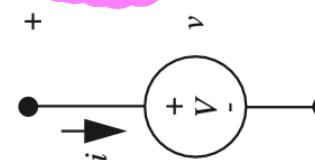
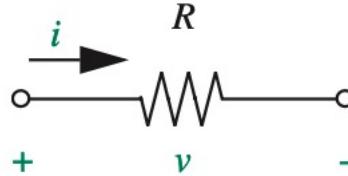


CSE 251 (After Mid)
Electronic Devices and Circuits

Iftekhar Hossain Rahi
22201168

Three terminal devices

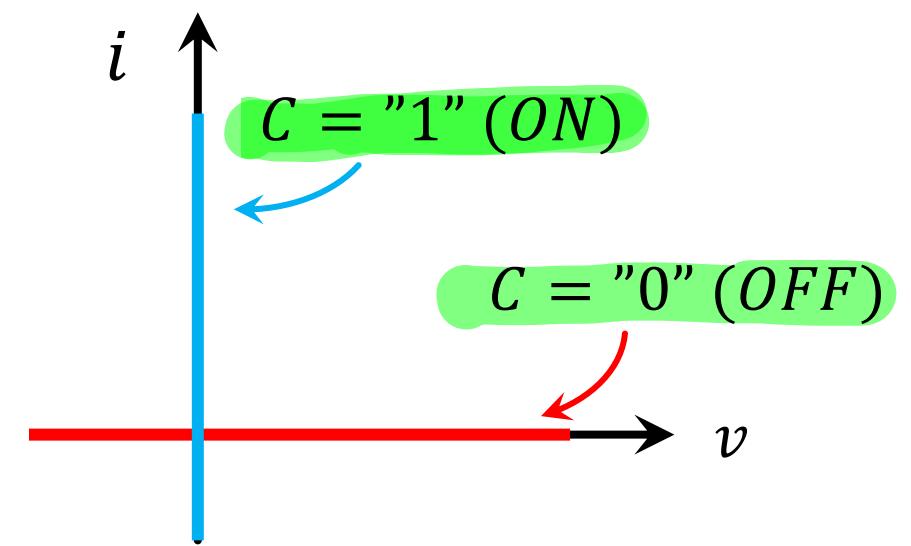
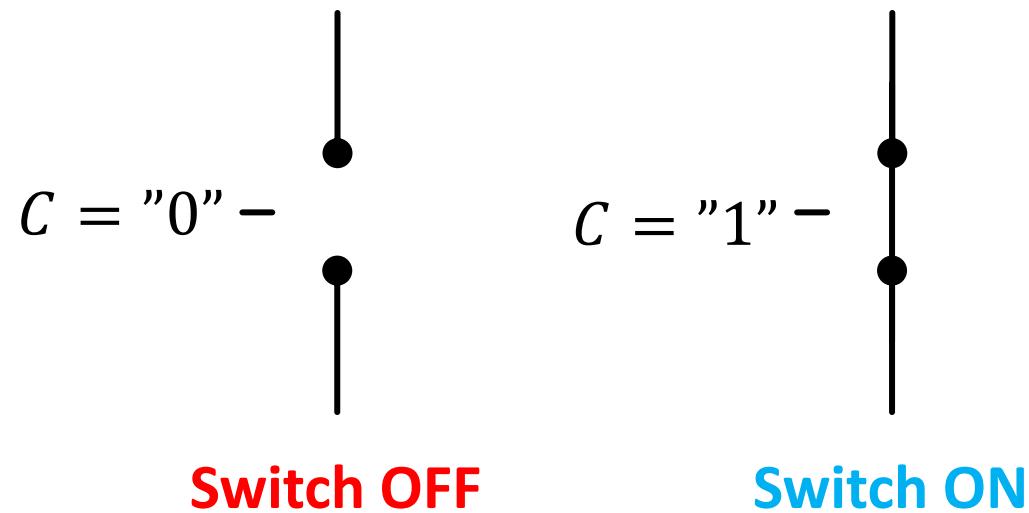
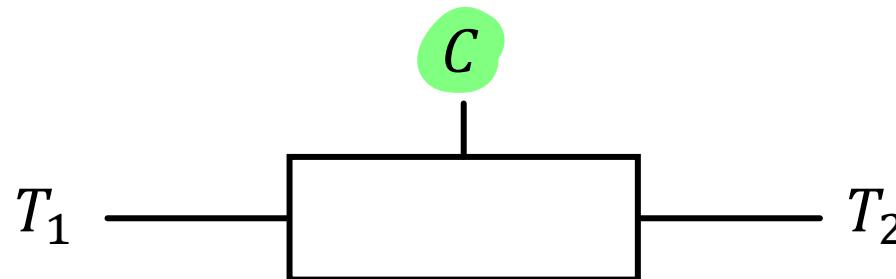
- Two terminal devices have fixed IV characteristics



- Three terminal devices – IV of two terminal can be controlled using the third terminal.
- Examples – Switch (linear), Transistors (non-linear)

Switch – IV Characteristics

- IV characteristics between terminal T_1 and T_2 is controlled by C



Switch – Types

- Depending on the control, the switch can be
 - **Analog:** Controlled using physical toggle/button
 - **Digital:** Controlled using voltage or current. Example – **MOSFET** (voltage controlled), **BJT** (current controlled)



Push button



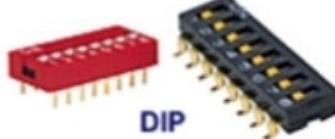
Rotary



Toggle



Slide

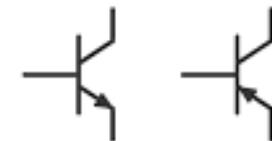


DIP

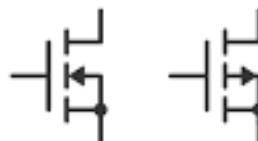


Dynamite Plunger

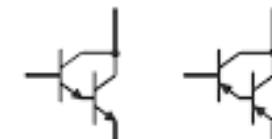
Analog switches



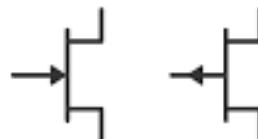
BJT



MOSFET



Darlington

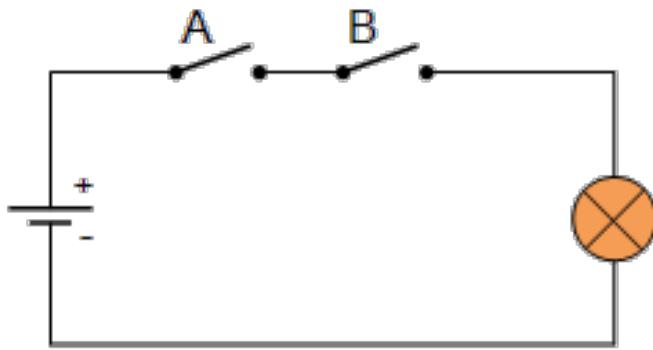


JFET

Digital switches (Transistors)

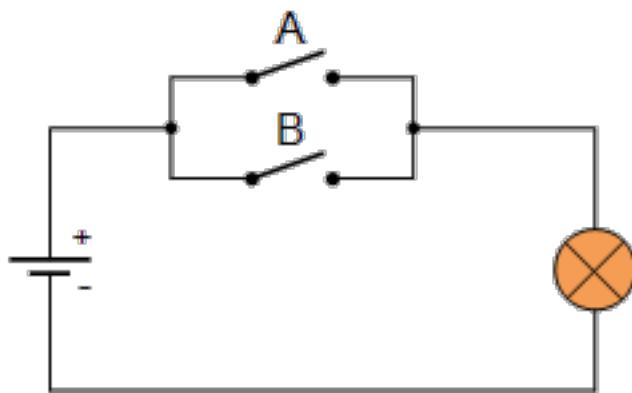
Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

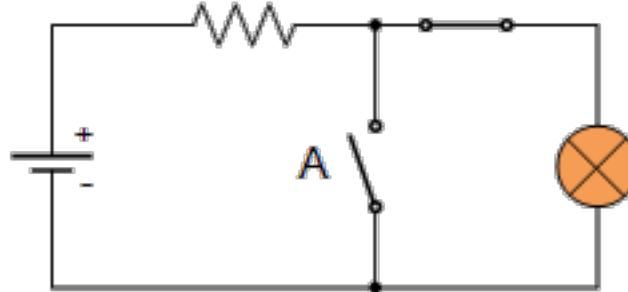
AND operation



A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

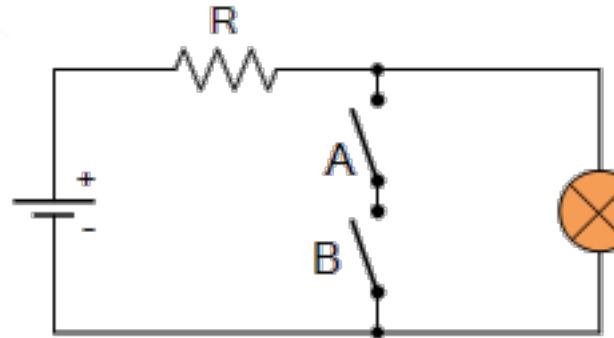
OR operation

Switch Application – Logic Gates



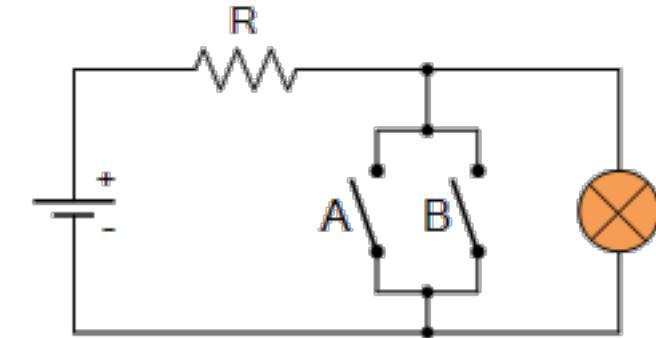
A	Bulb
0	ON
1	OFF

NOT operation



A	B	Bulb
0	0	ON
0	1	ON
1	0	ON
1	1	OFF

NAND operation



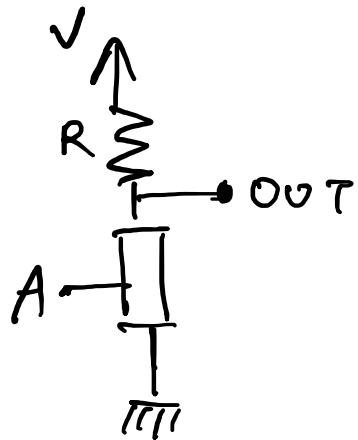
A	B	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

NOR operation

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits
-> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

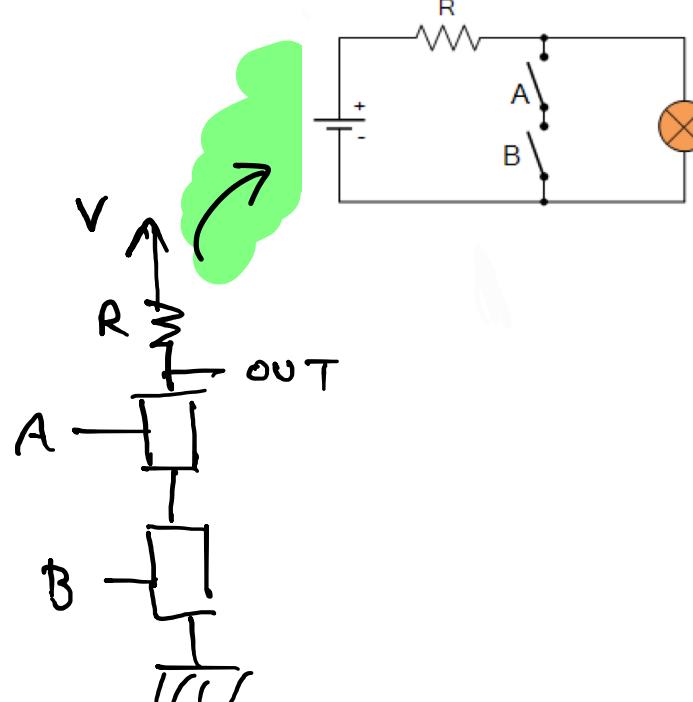
Switch Application – Logic Gates

Alternative representations:



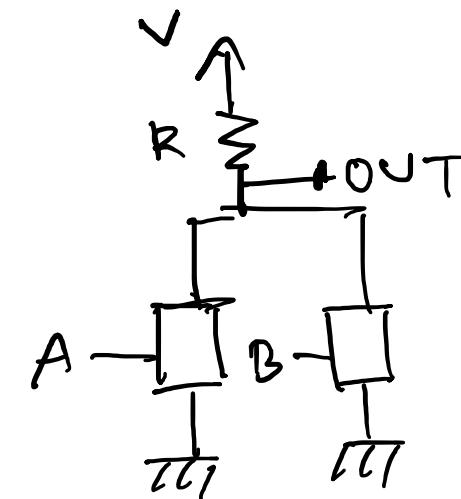
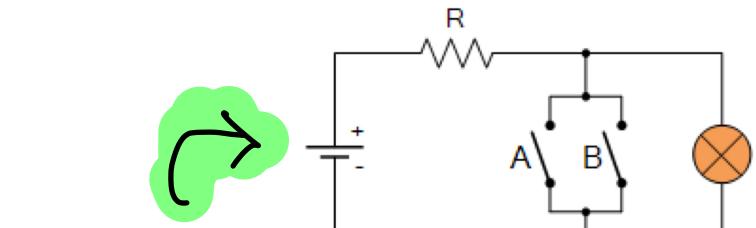
$$OUT = \overline{A}$$

(NOT)



$$OUT = \overline{AB}$$

(NAND)

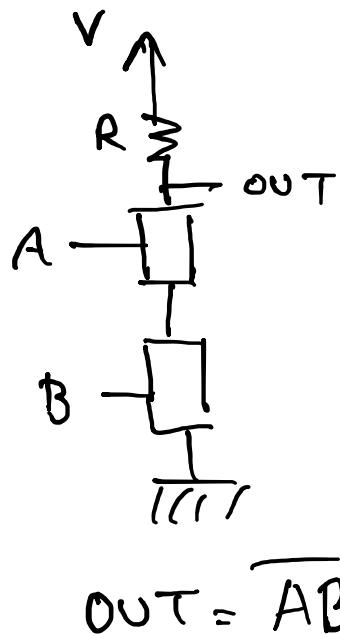


$$OUT = \overline{A+B}$$

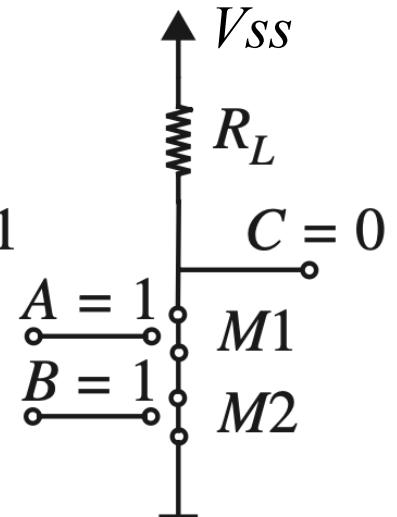
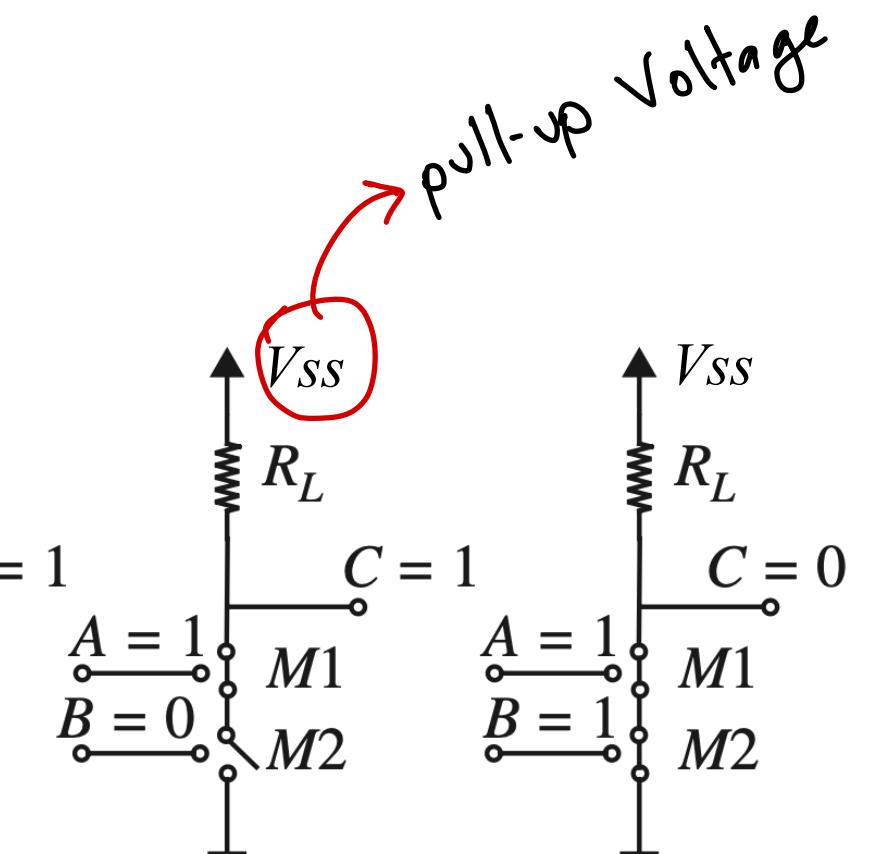
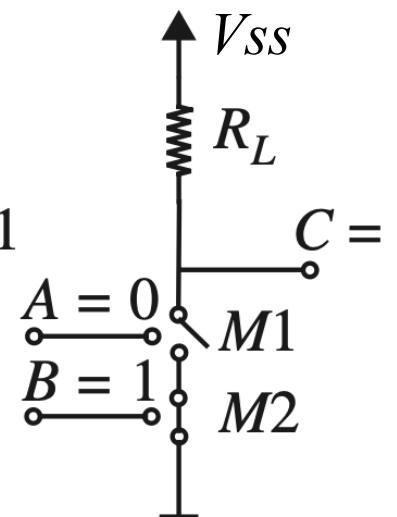
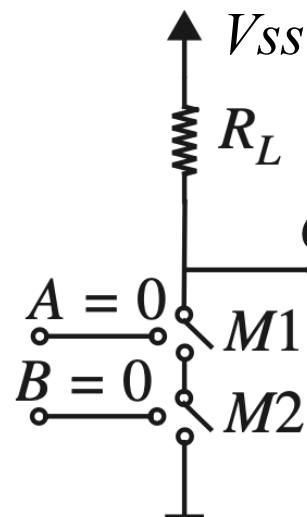
(NOR)

Switch Application – Logic Gates

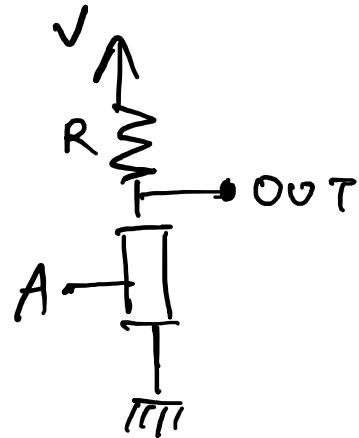
Alternative representations:



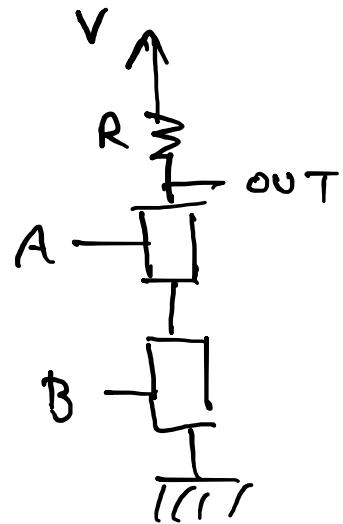
(NAND)



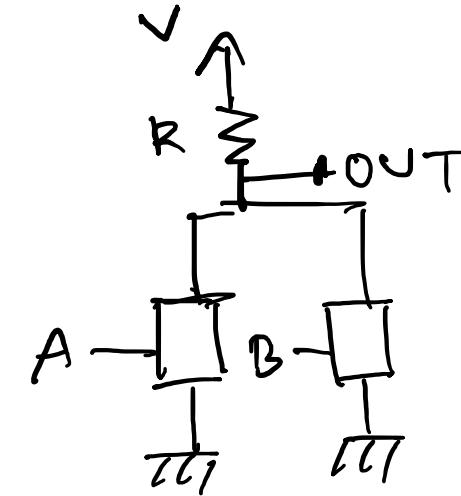
Switch Application – Logic Gates



$$OUT = \overline{A}$$



$$OUT = \overline{AB}$$

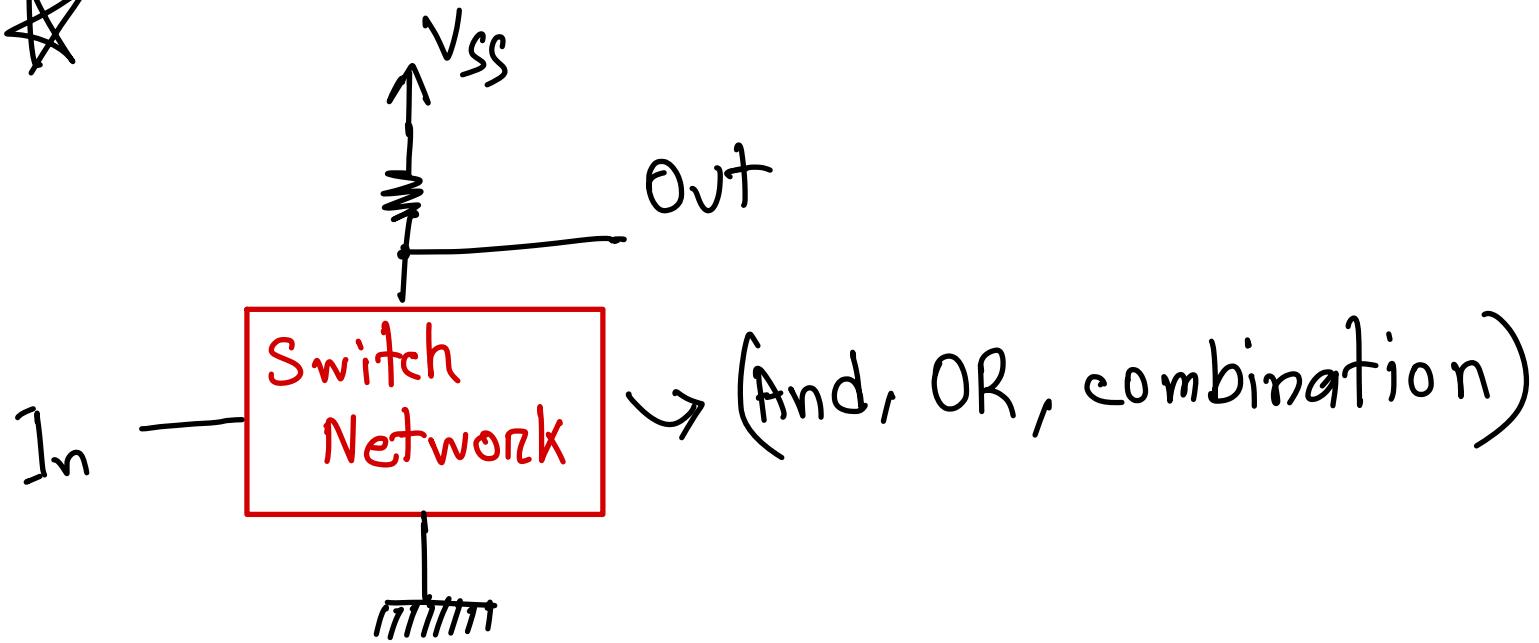


$$OUT = \overline{A+B}$$

A	V_{OUT}
0	5V
1	0V

A	B	V_{OUT}
0	0	5V
0	1	5V
1	0	5V
1	1	0V

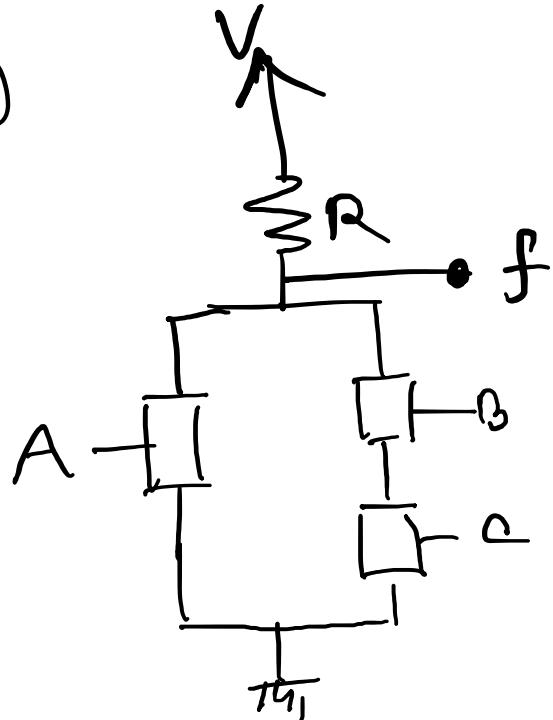
A	B	V_{OUT}
0	0	5V
0	1	0V
1	0	0V
1	1	0V



Switch network হাতে ও V_{SS} , ground, R একে, অবিক্ষু
মিলান্ত সর্কিন সর্কিন একে যাবে। AB একে কথা,
কিন্তু একে মাবে \overline{AB}

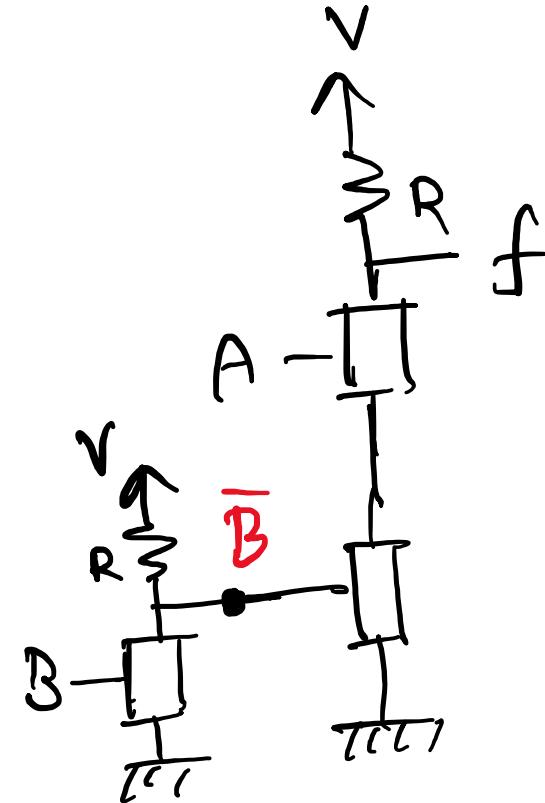
Examples

①



$$f = \overline{A + B \cdot C}$$

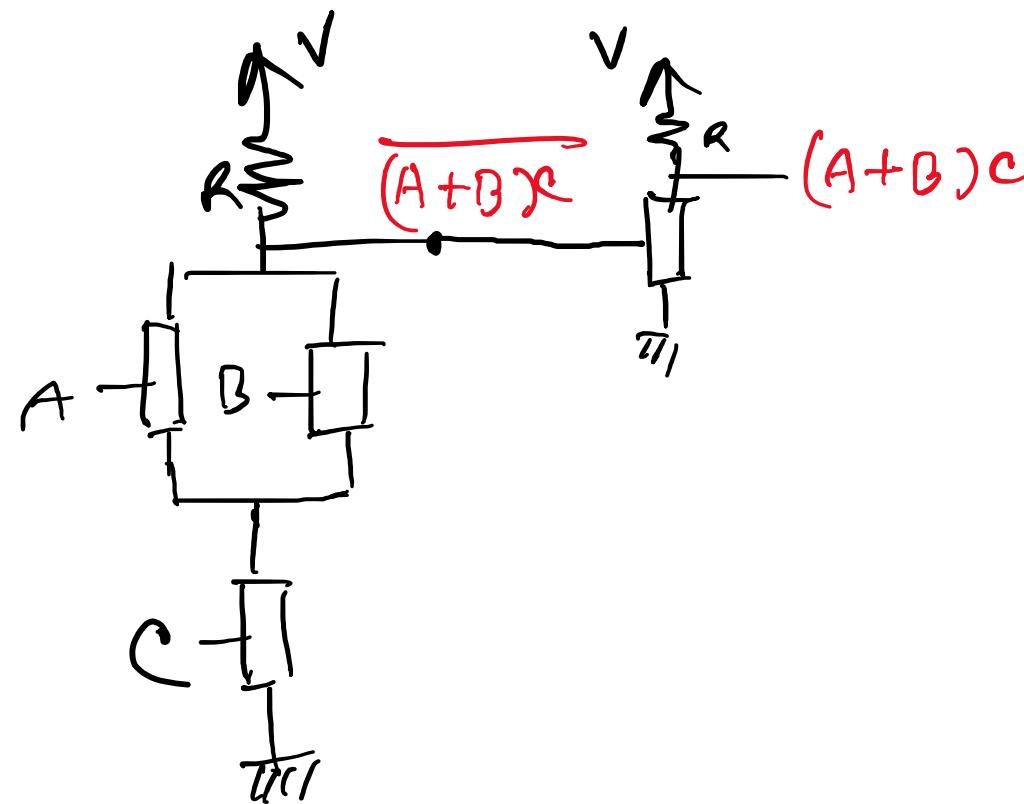
②



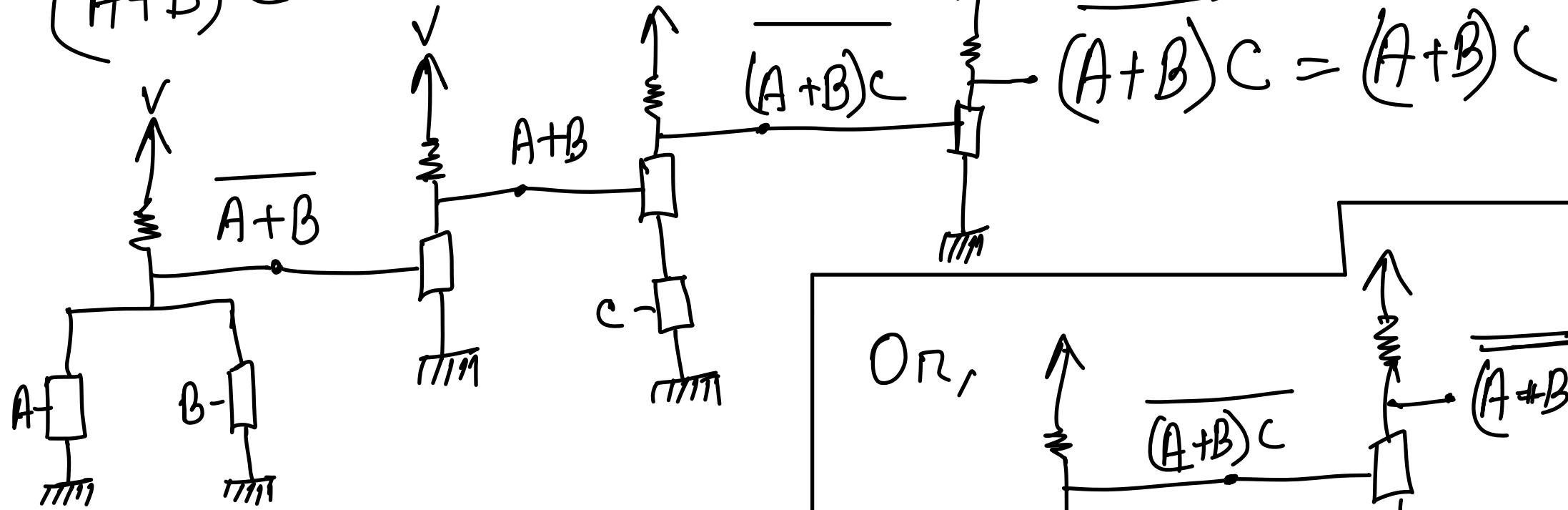
$$f = \overline{A \overline{B}}$$

③ Example

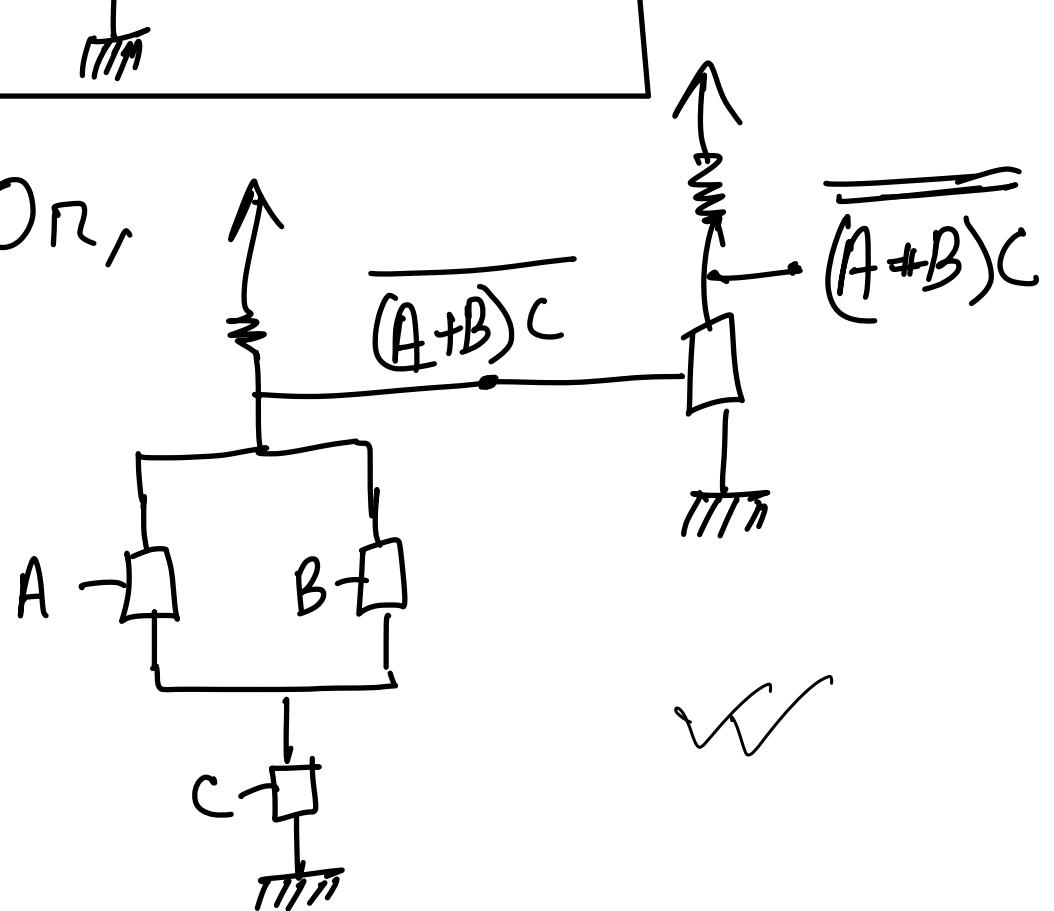
Implement using switches: $f = (A + B)C$



$$③ (A+B)C$$



Or,



Always, there will be various ways to draw the circuit.

try to think and find out the most easy way.

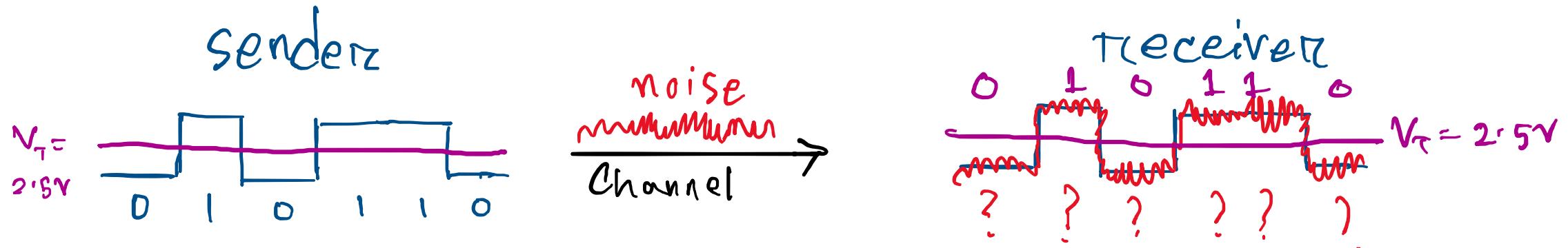
Digital Representation

- Binary → Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

Voltage	Current	State
5V → 1	2mA → 1	ON → 1
0V → 0	3mA → 0	OFF → 0
0V → 1		Low resistance → 1
3.3V → 0		High resistance → 0

Digital Representation

Suppose you want to send 010110



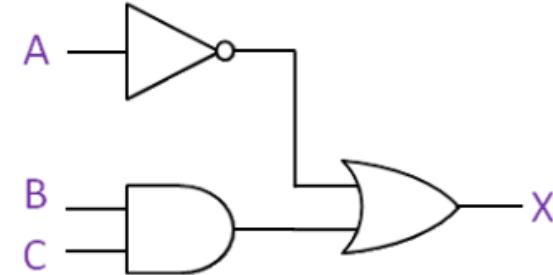
- Single value based representation fails in the presence of noise
- Better approach – threshold-based system
- Simplest: **Logical 0** = $V < V_T$ **Logical 1** = $V > V_T$

Static Discipline

- Specification for digital devices
- Requires devices to adhere to common representation to ensure that **valid input produces valid output**
- This means, if

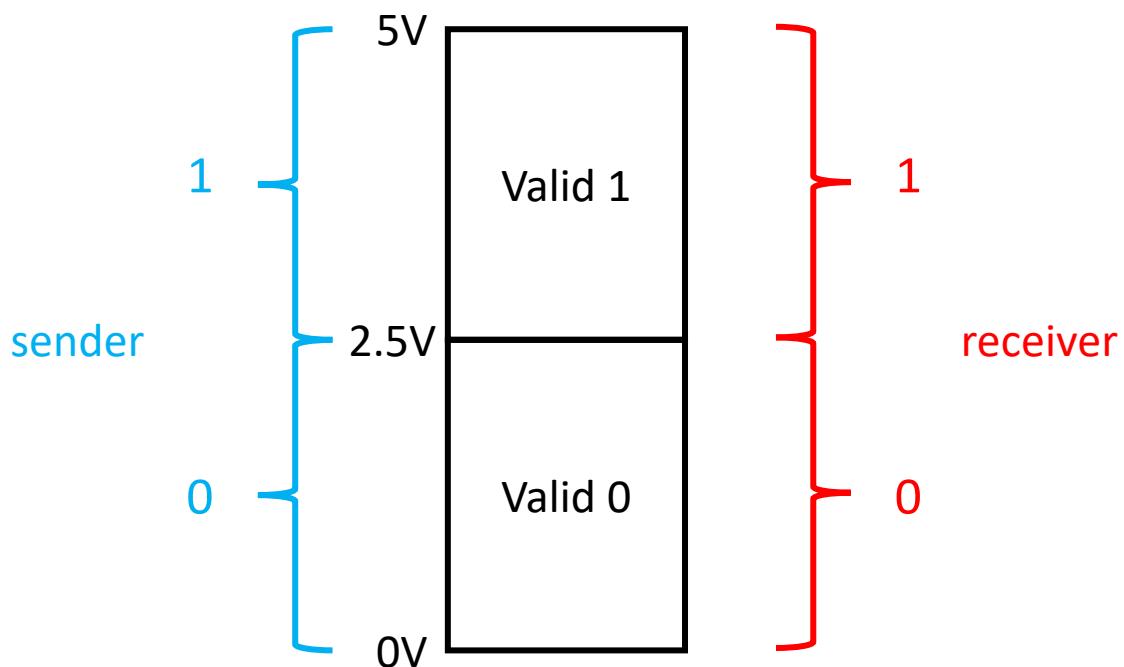
• Sender sends “0” $\xrightarrow[\text{Channel}]{\text{noise}} \text{Receiver interprets as “0”}$

• Sender sends “1” $\xrightarrow[\text{Channel}]{\text{noise}} \text{Receiver interprets as “1”}$

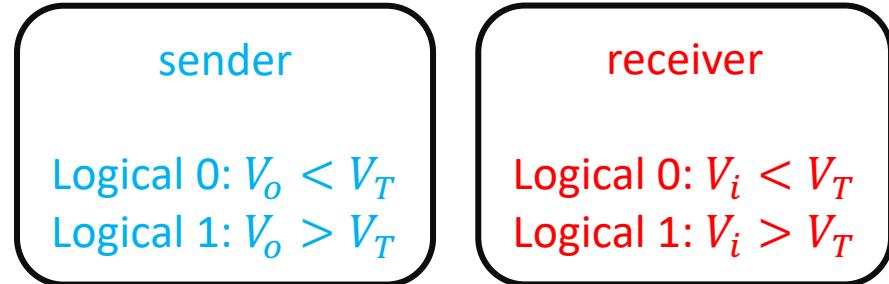


Static Discipline

Naïve approach: Single threshold based system



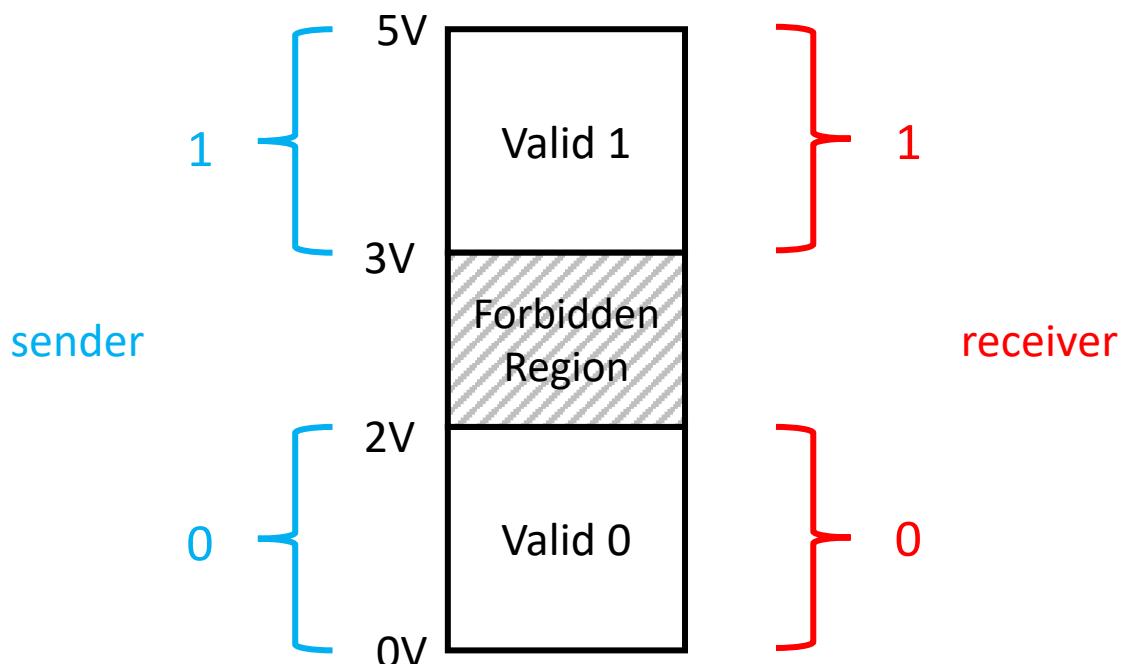
$$V_T = 2.5 V$$



What if $V_i = 2.5V$? Undefined!

Static Discipline

Double threshold based system



V_H = High voltage threshold = 3V

V_L = Low voltage threshold = 2V

sender

Logical 0: $V_o < V_L$
Logical 1: $V_o > V_H$

receiver

Logical 0: $V_i < V_L$
Logical 1: $V_i > V_H$

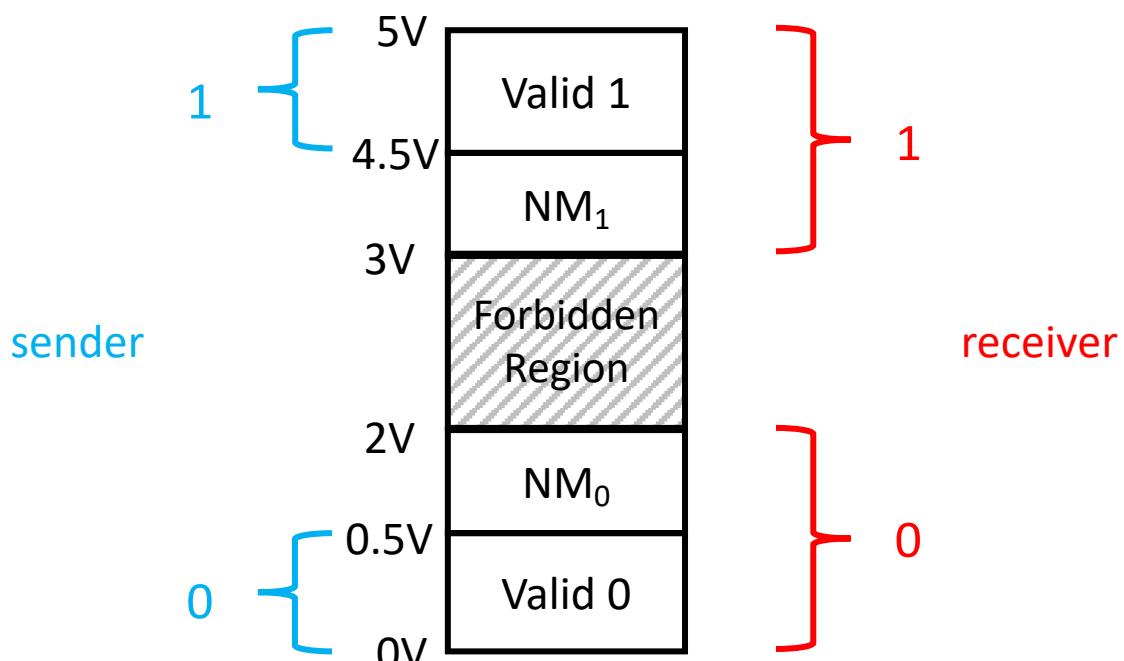
What if $V_o = 1.9V$ and channel noise is $0.5V$?

$V_i = 1.9V + 0.5V = 2.4V$ = invalid

→ valid output producing invalid input,
i.e., no margin for noise

Static Discipline

Four threshold based system → Tighter restriction on sender (**output**)



V_{OH} = Output high voltage threshold = 4.5V

V_{OL} = Output low voltage threshold = 0.5V

V_{IH} = Input high voltage threshold = 3V

V_{IL} = Input low voltage threshold = 2V

sender

Logical 0: $V_o < V_{OL}$
Logical 1: $V_o > V_{OH}$

receiver

Logical 0: $V_i < V_{IL}$
Logical 1: $V_i > V_{IH}$

For static discipline, $V_{OL} < V_{IL} < V_{IH} < V_{OH}$

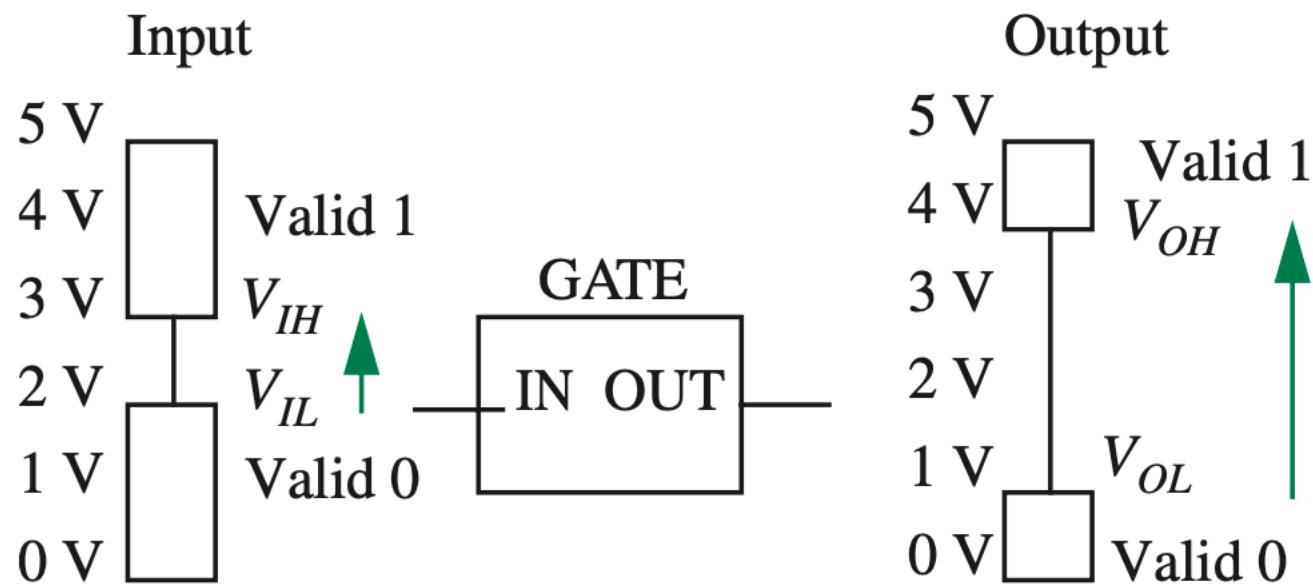
Noise margins (NM):

- $NM_1 = V_{OH} - V_{IH} = 4.5 - 3 = 1.5V$ (significance?)
- $NM_0 = V_{IL} - V_{OL} = 2 - 0.5 = 1.5V$ (significance?)

skipped

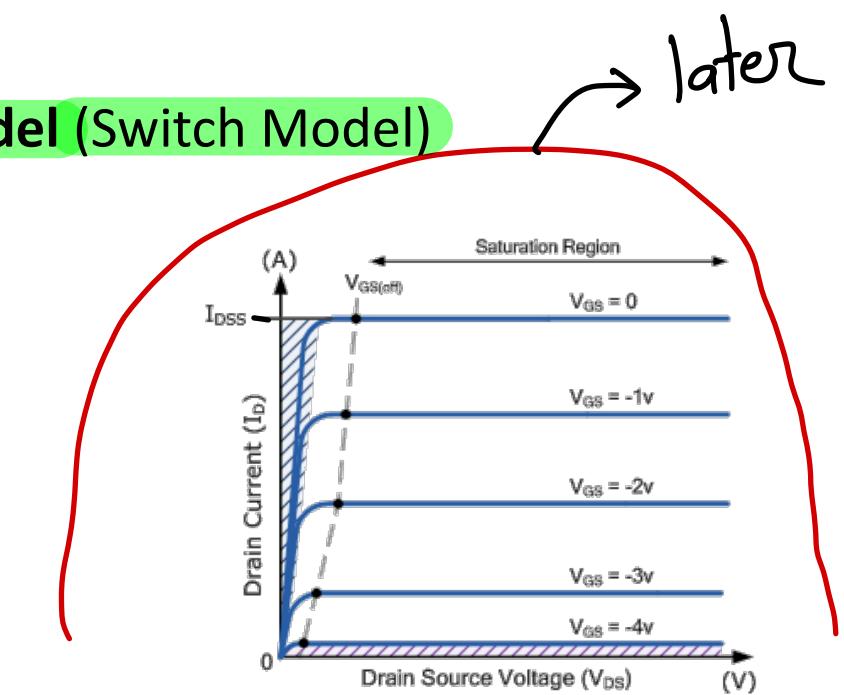
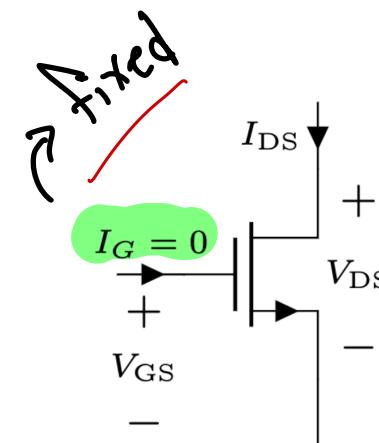
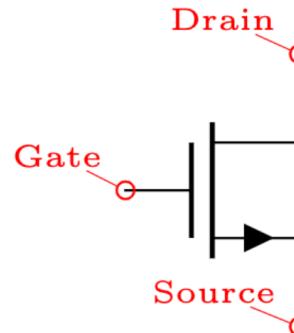
Static Discipline

Four threshold based system → Tighter restriction on sender (**output**)



Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – Voltage Controlled, Current Controlled
- **Metal Oxide Semiconductor Field Effect Transistor (MOSFET)** are voltage controlled
- Control, $C = V_{GS}$. The IV characteristics (I_{DS} vs V_{DS}) depends on V_{GS}
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model (Switch Model)**



MOSFET S Model

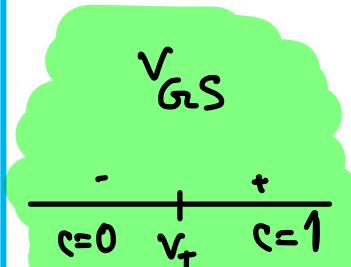
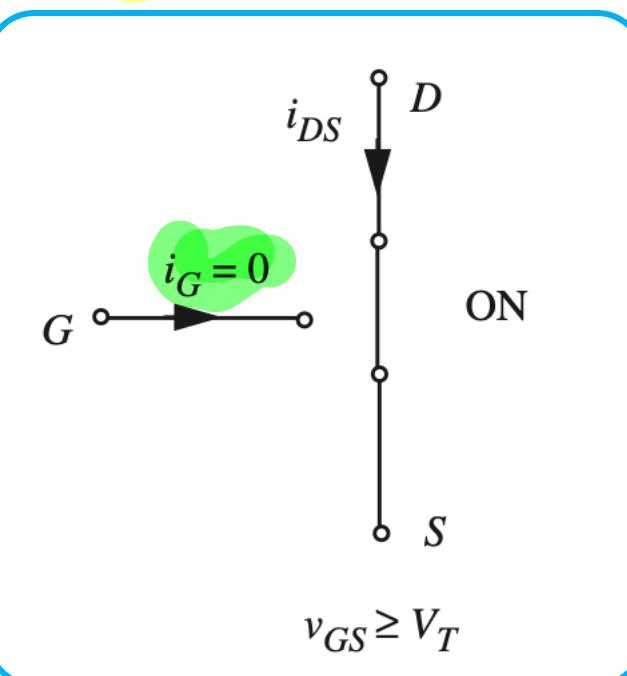
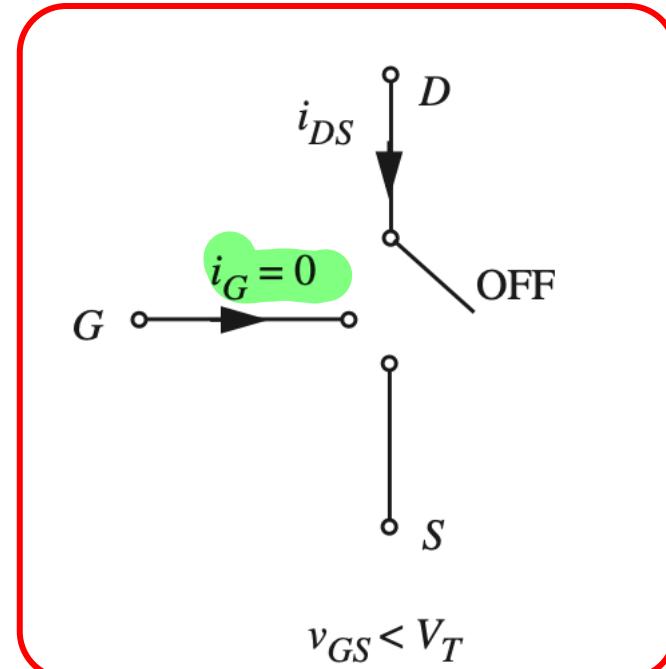
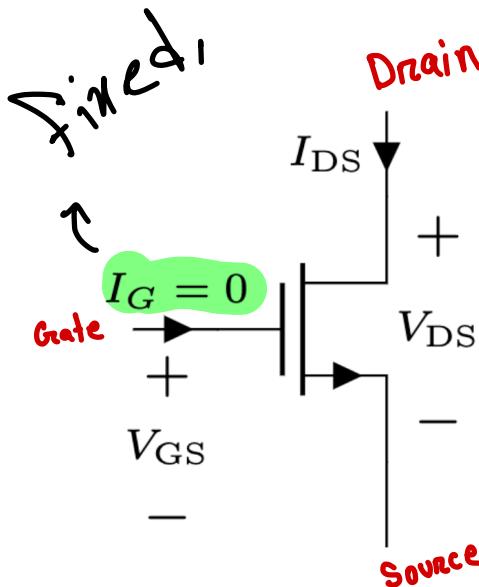
Switch

Control terminal = Gate

V_T = threshold voltage

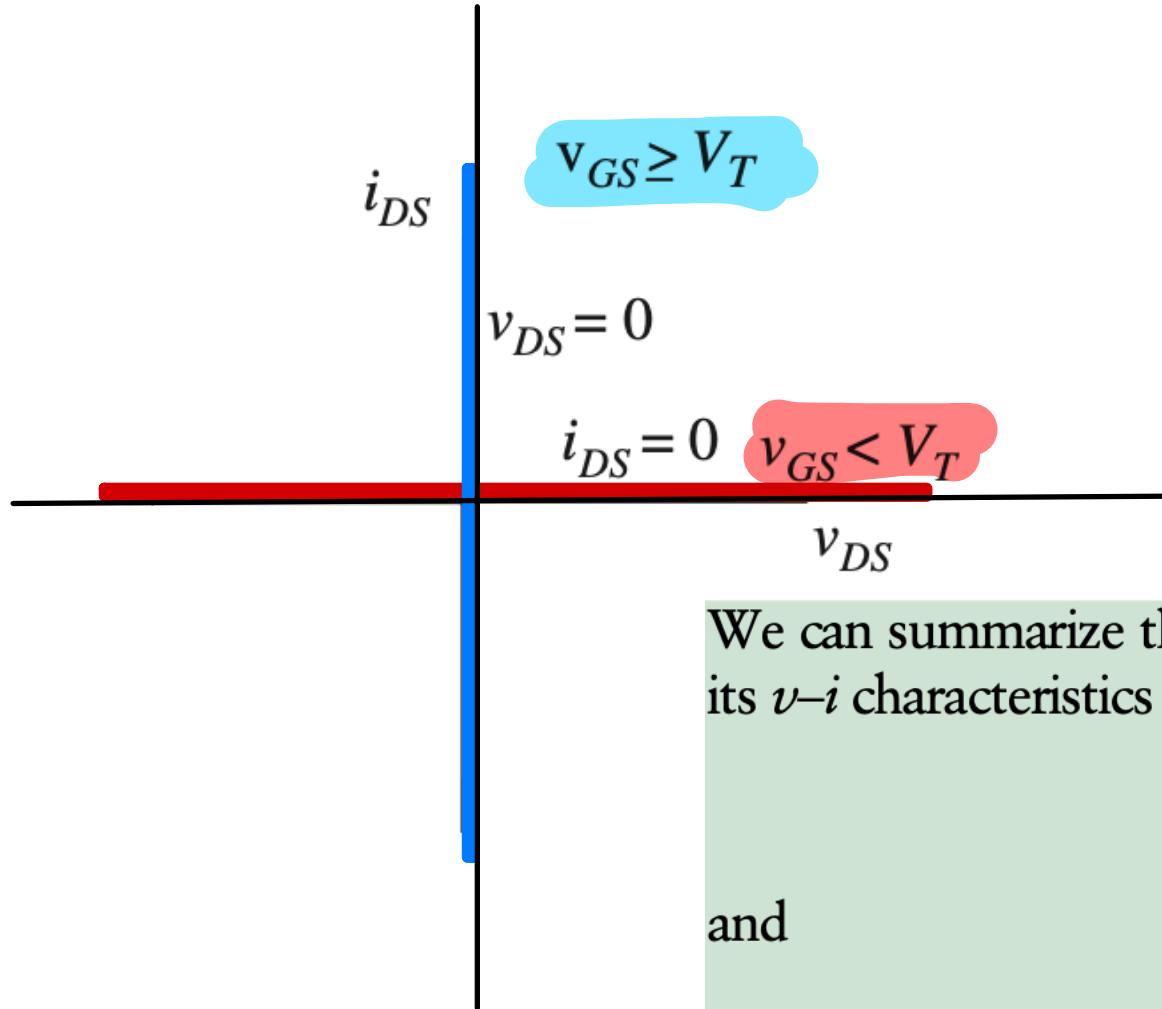
- The MOSFET (approximately) behaves like a switch

- $C = V_{GS}$. Here, $C = "0" \Rightarrow V_{GS} < V_T$, and $C = "1" \Rightarrow V_{GS} \geq V_T$



V_{GS} $c=0$

MOSFET S-Model



We can summarize the S model for the MOSFET in algebraic form by stating its $v-i$ characteristics as follows:

for $v_{GS} < V_T$, $i_{DS} = 0$

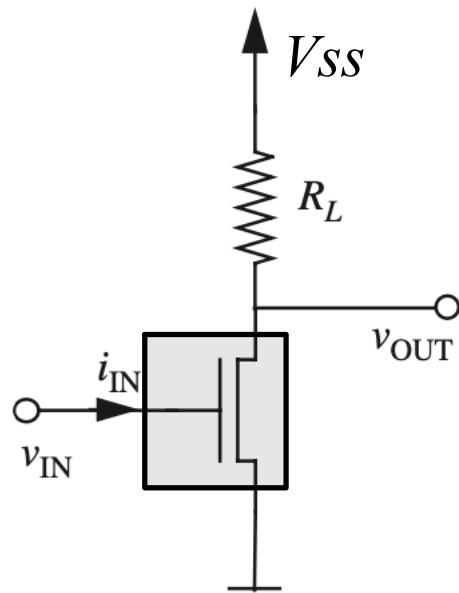
and

for $v_{GS} \geq V_T$, $v_{DS} = 0$

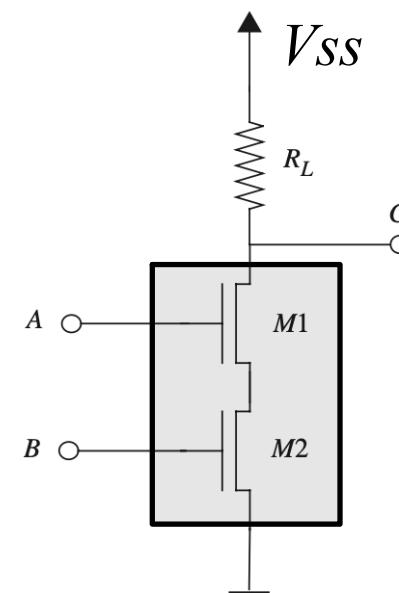
(6.2)

Logic Gates using MOSFET

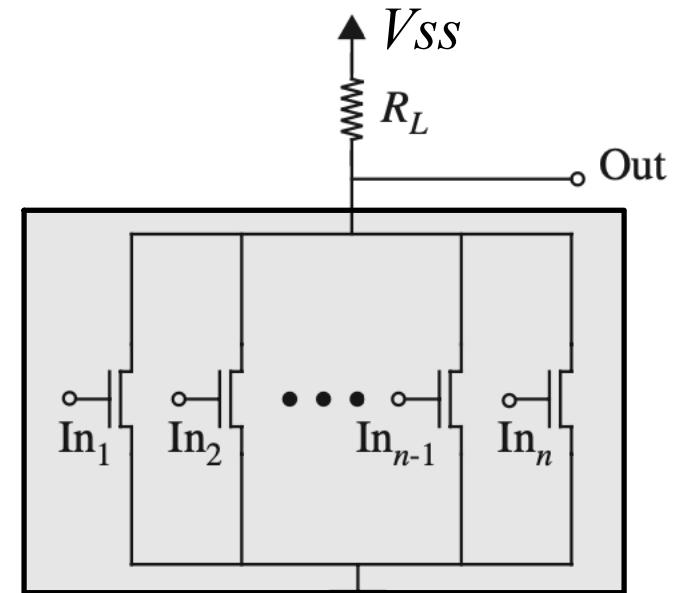
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

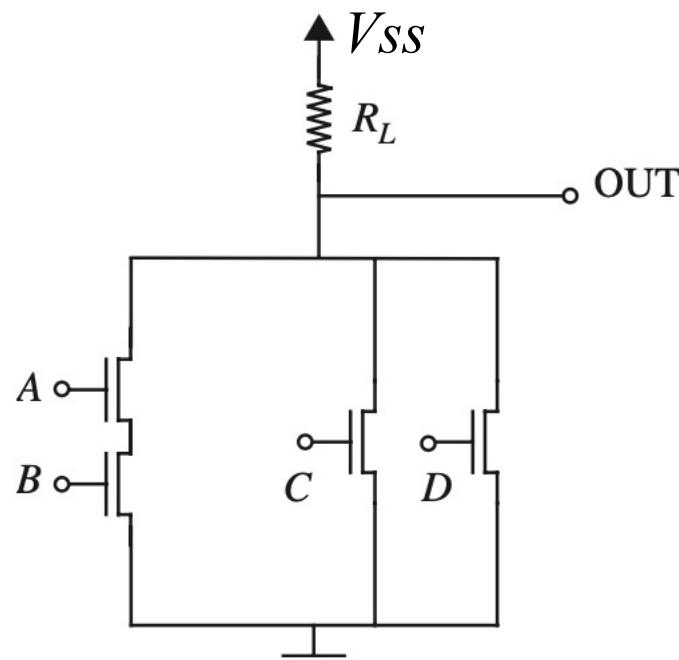


NAND Gate (Inverter)

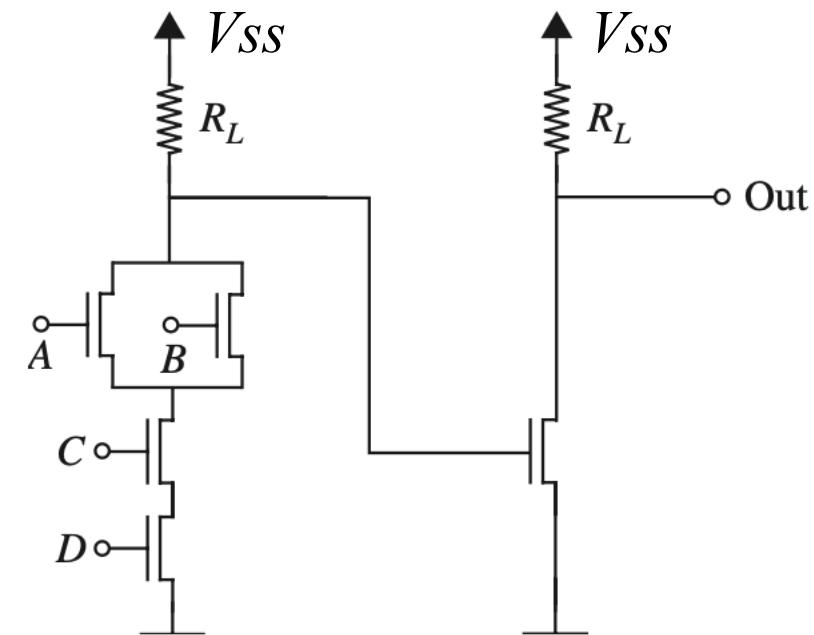


NOR Gate (Inverter)

MOSFET Logic Gates – More Examples



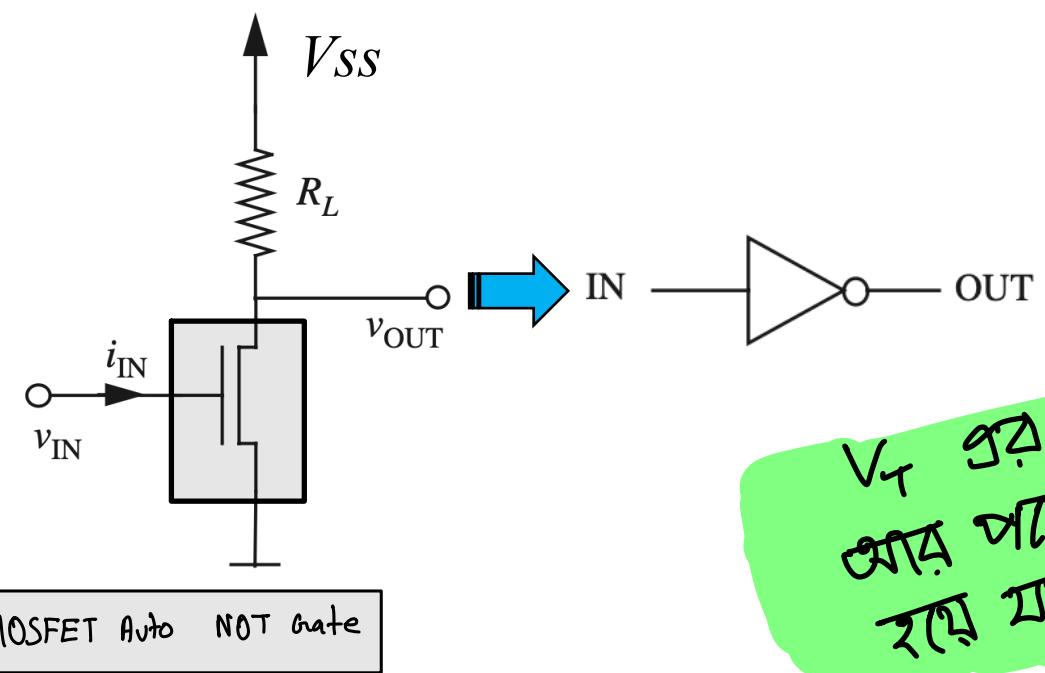
$$OUT = \overline{AB + C + D}$$



$$Out = \overline{(A + B)CD} = (A + B)CD$$

Voltage Transfer Characteristics (VTC) = $(V_{out} \text{ vs } V_{in})$

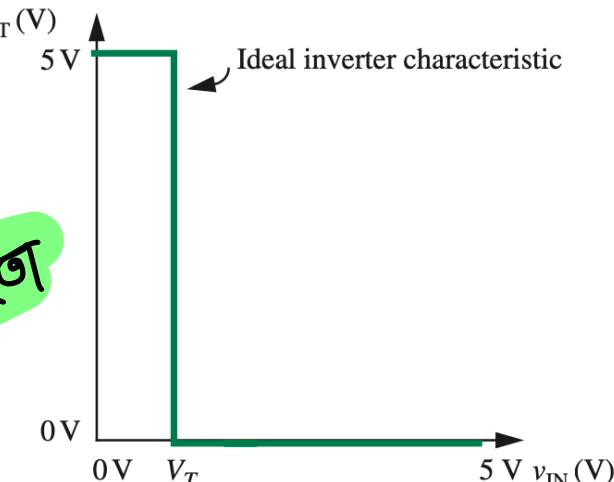
- Reminder: VTC is a graph where x axis = input voltage, y axis = output voltage
- Why? Design logic gates to follow a given static discipline



V_T ৰ জো আবশ্যিক
যোৱা দিতা inverter কৰা
কৰুন প্রতিক্রিয়া

When $v_{IN} < V_T$ (Logical 0), $v_{OUT} = V_s = 5V$ (Logical 1)

When $v_{IN} \geq V_T$ (Logical 1), $v_{OUT} = 0$ (Logical 0)



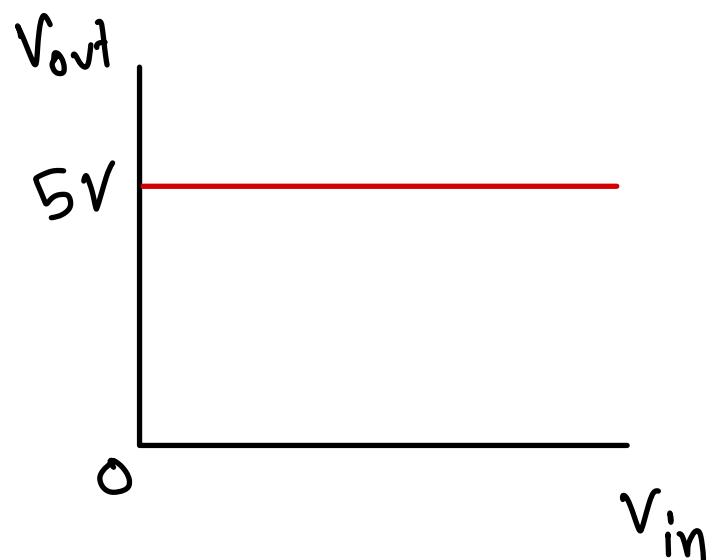
when,

$$V_{in} < V_T$$

$$\Rightarrow A = \text{off} = 0$$

then,

$$\therefore V_{out} = V_{SS} = 1$$

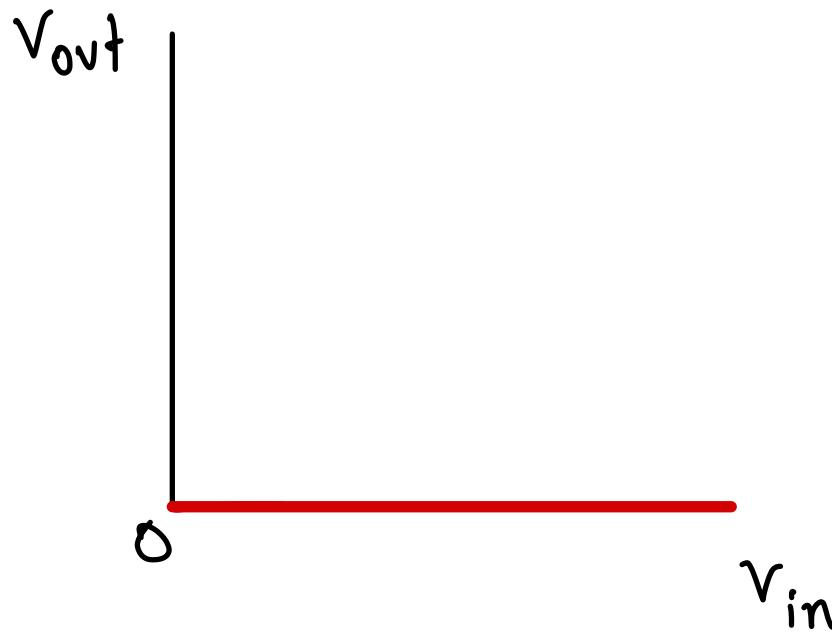


when,

$$V_{in} > V_T$$

$$\Rightarrow A = \text{on} = 1$$

$$\therefore \text{then, } V_{out} = \text{ground} = 0$$



Input 0 $\overline{2}(m)$

output 1 $\overline{2}(th)$

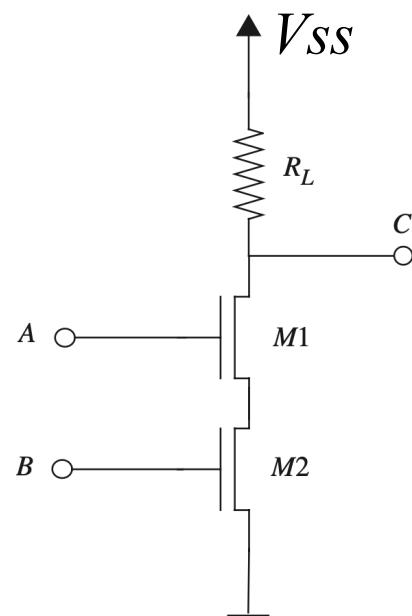
vice versa

It's working
like an inverter

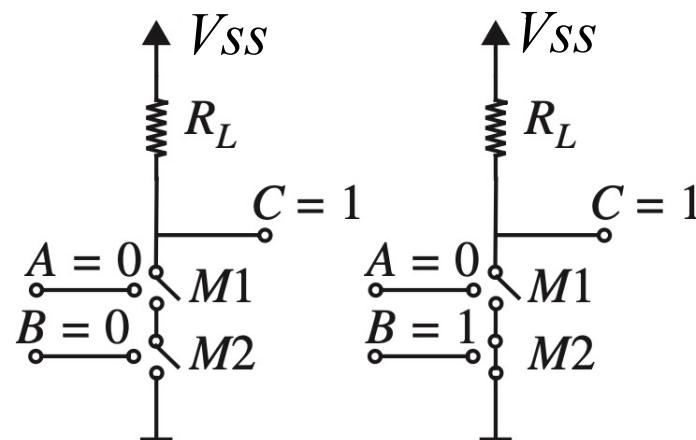
here's the
reference
point is
threshold.

VTC of NAND gate

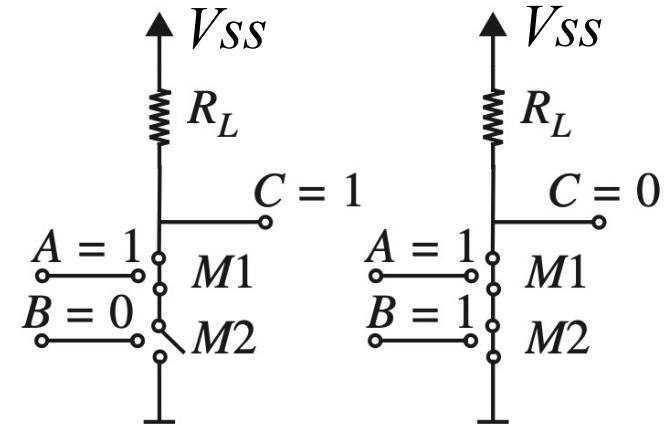
- We only have one x axis, but two **inputs** *variable*
- Solution: Draw two VTC, one considering **$A = "0"$** , one considering **$A = "1"$**



When **$A = "0"$**



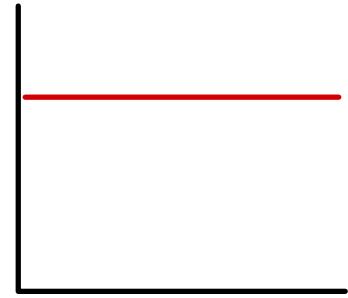
When **$A = "1"$**



$$A = 0$$

$$B = 0$$

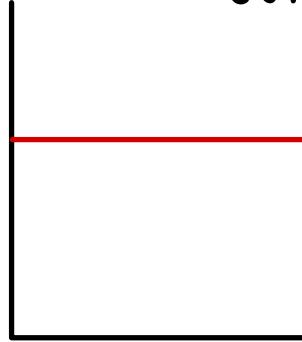
$$V_{out} = 1$$



$$A = 0$$

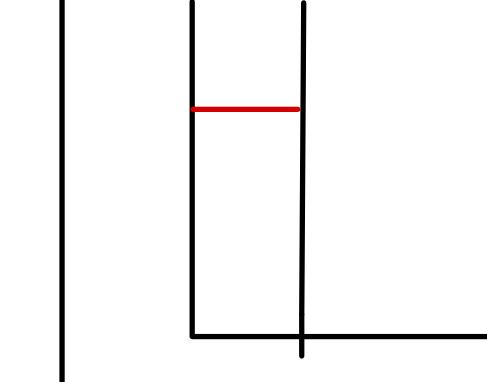
$$B = 1$$

$$V_{out} = 1$$



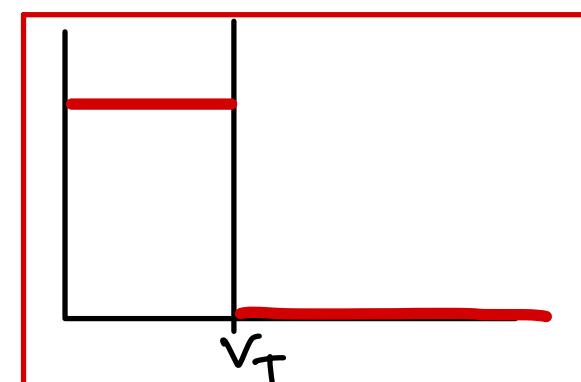
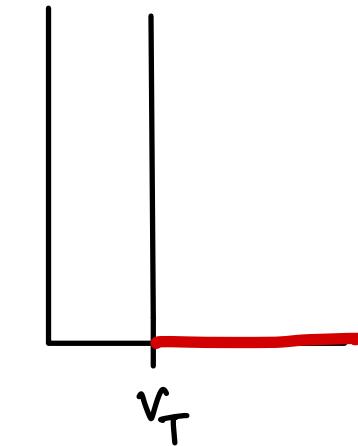
$$A = 1$$

$$B = 0$$



$$A = 1$$

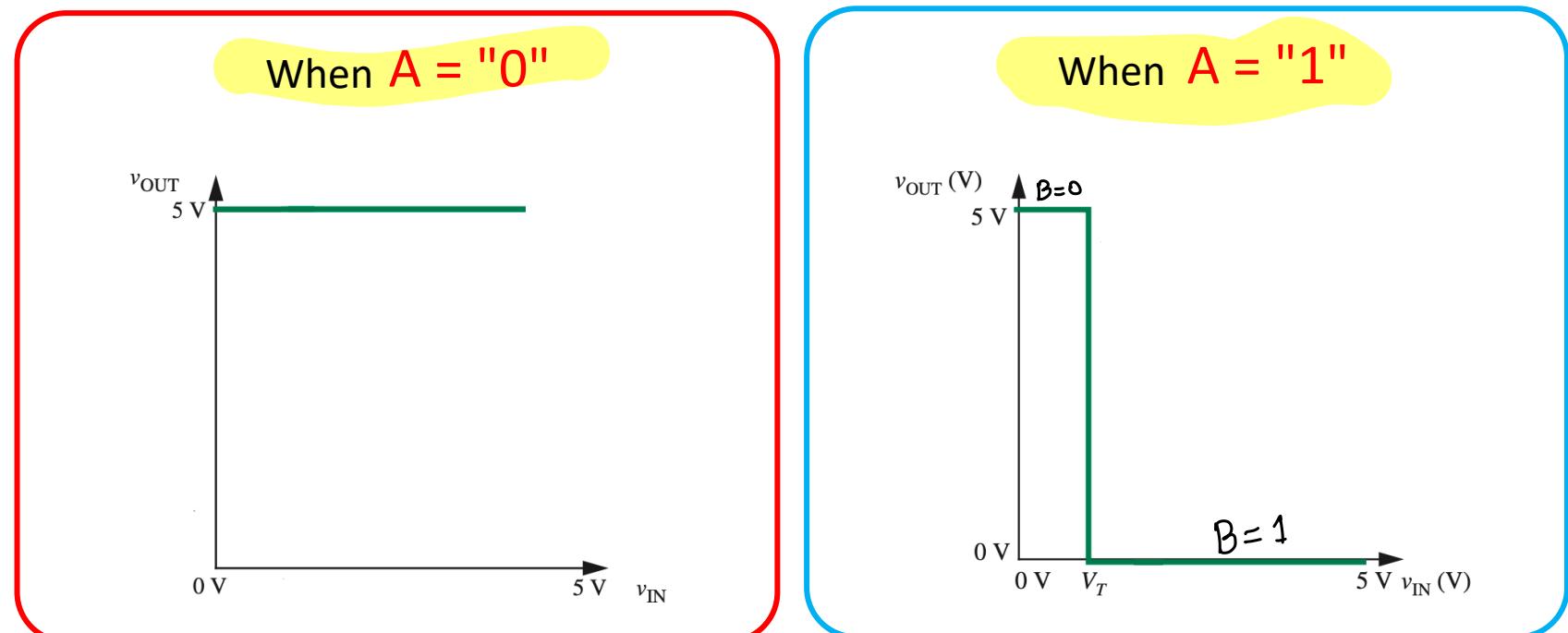
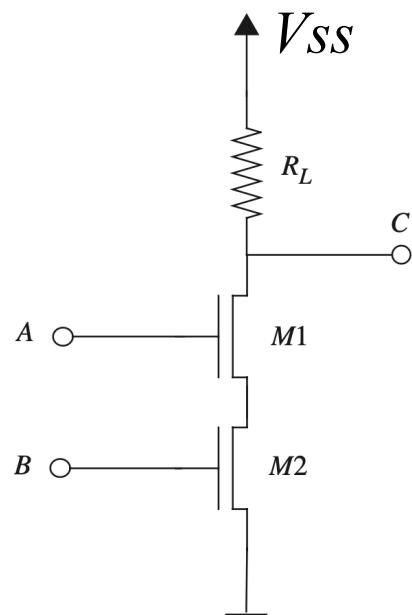
$$B = 1$$



→ direct draw
this

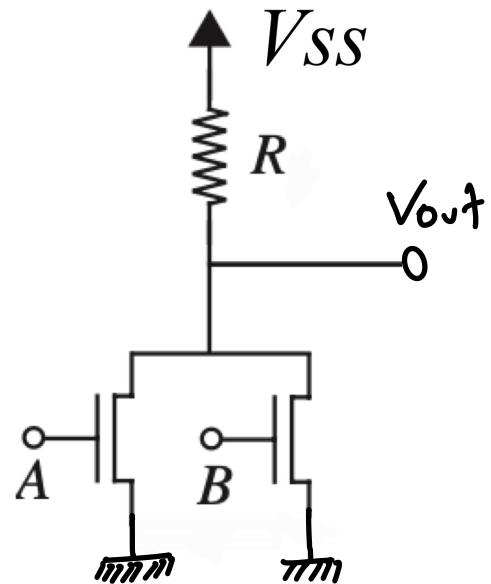
VTC of NAND gate

- We only have one x axis, but two inputs
- Solution: Draw two VTC, one considering $A = "0"$, one considering $A = "1"$

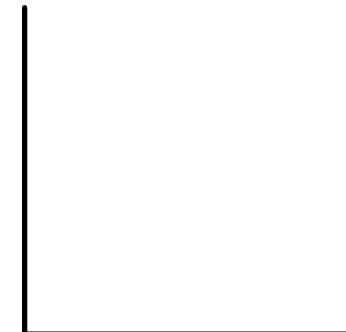


Homework: Find VTC for NOR gate

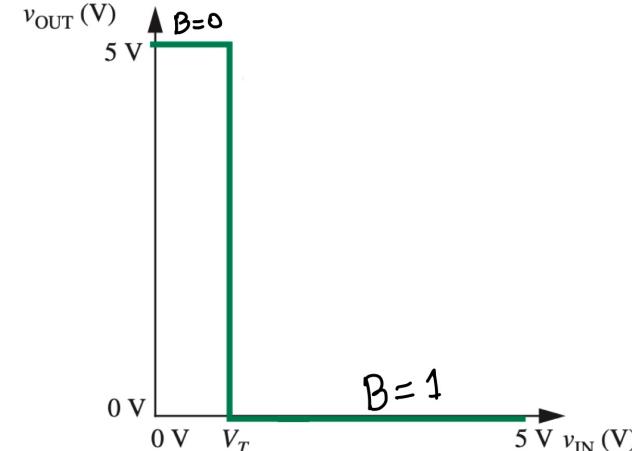
H.W \rightarrow VTC for NOR Gate



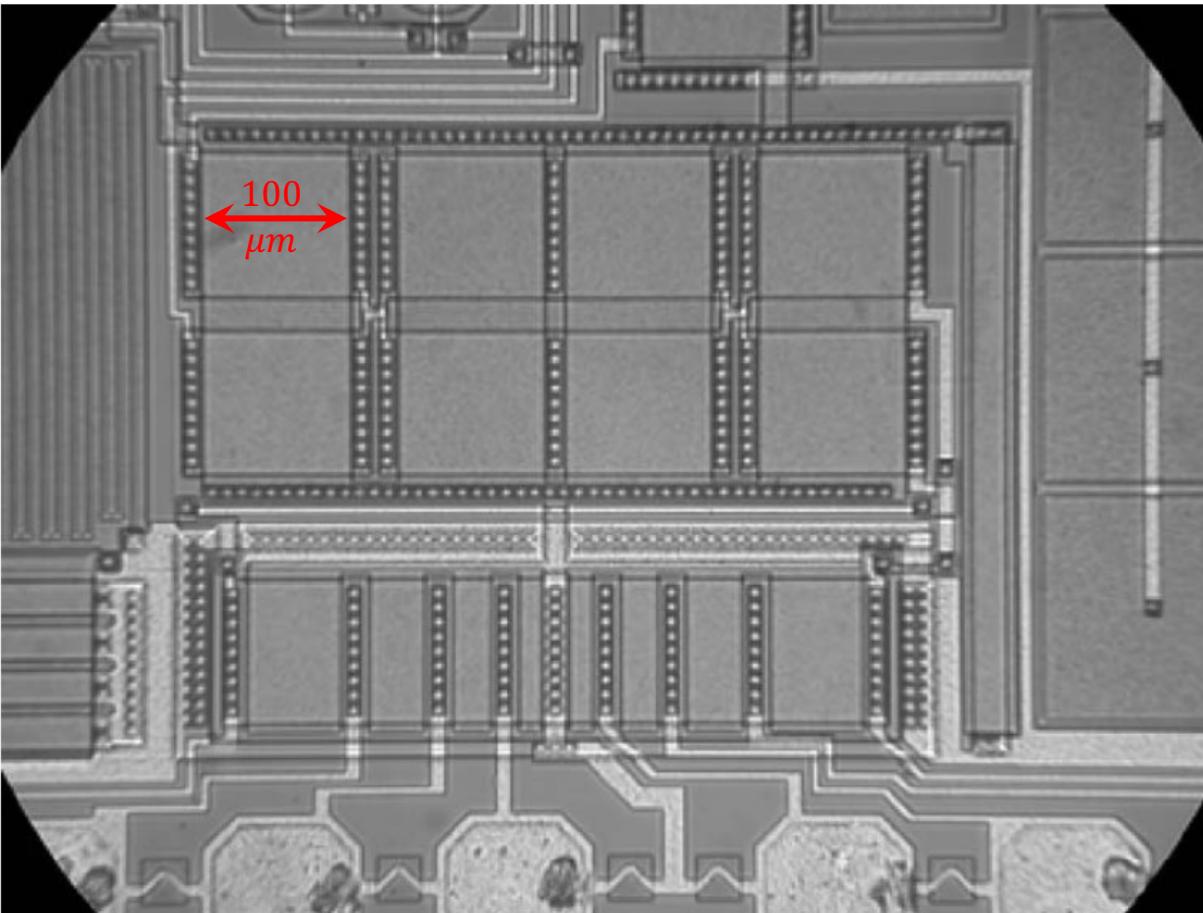
$$\left. \begin{array}{l} A=1 \\ B=0 \\ B=1 \end{array} \right\} V_{out} = 0$$



$$\left. \begin{array}{l} A=0 \\ B=0 \rightarrow V_{out} = V_{SS} \\ B=1 \rightarrow V_{out} = 0 \end{array} \right.$$



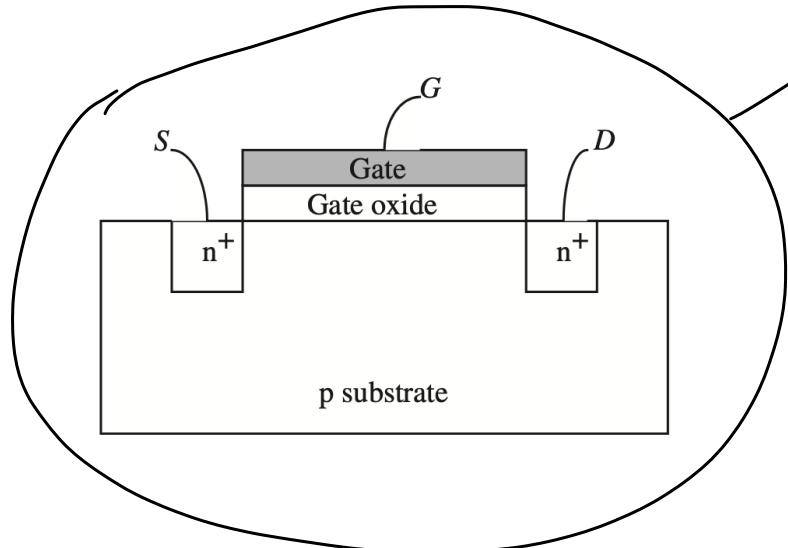
Construction of Real MOSFET



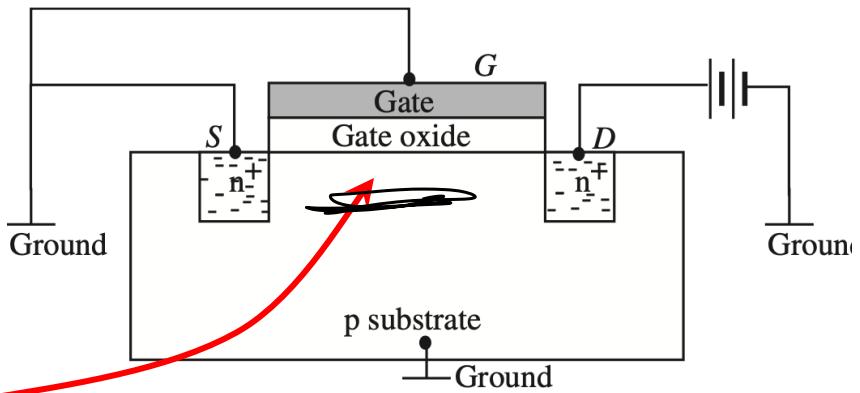
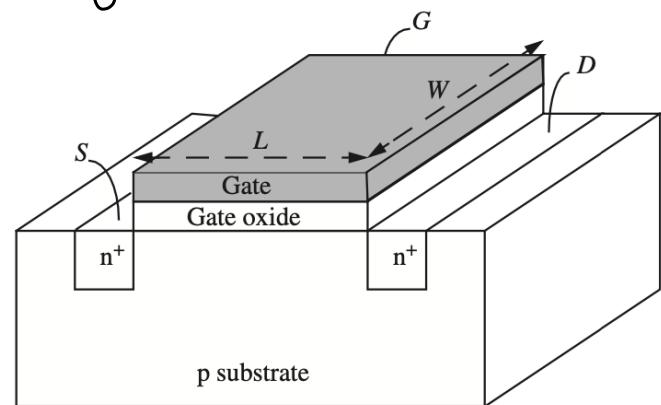
Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100 μm . (Photograph Courtesy of Maxim Integrated Products.)

Construction of Real MOSFET

Simplified cross section
and 3D view

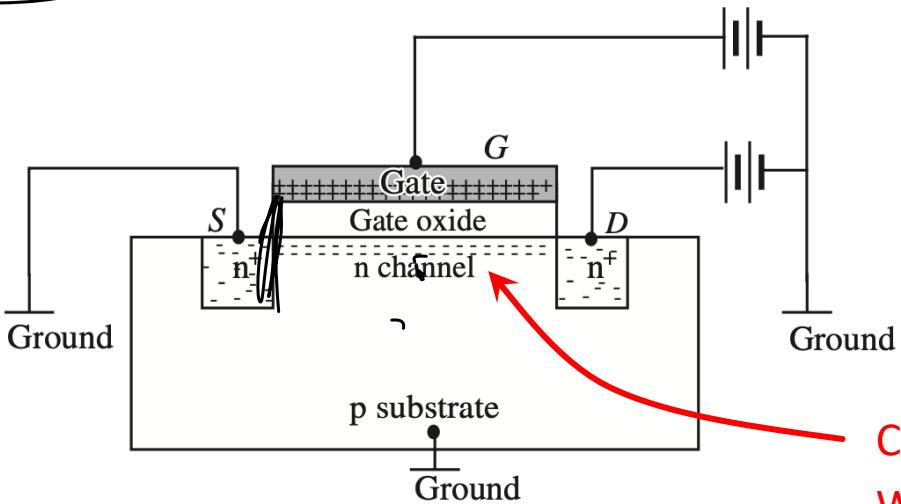


n type MOSFET



No channel, open ckt

$$V_{GS} = 0V$$

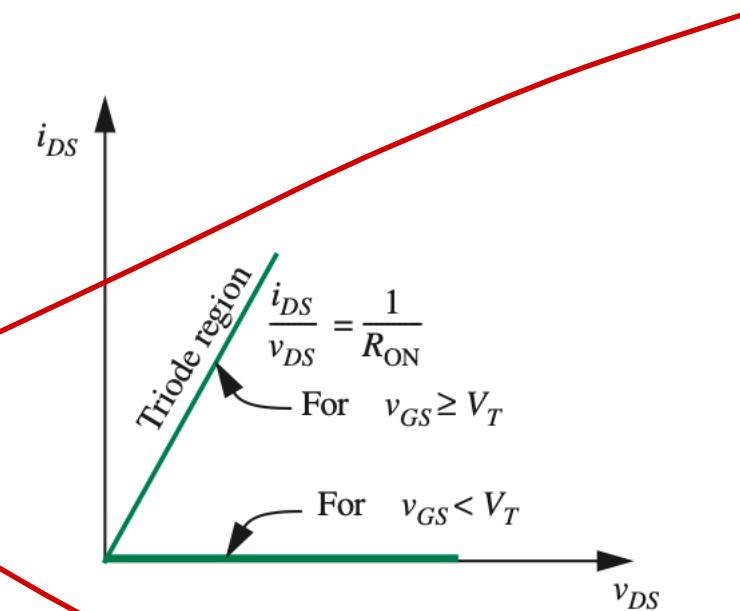
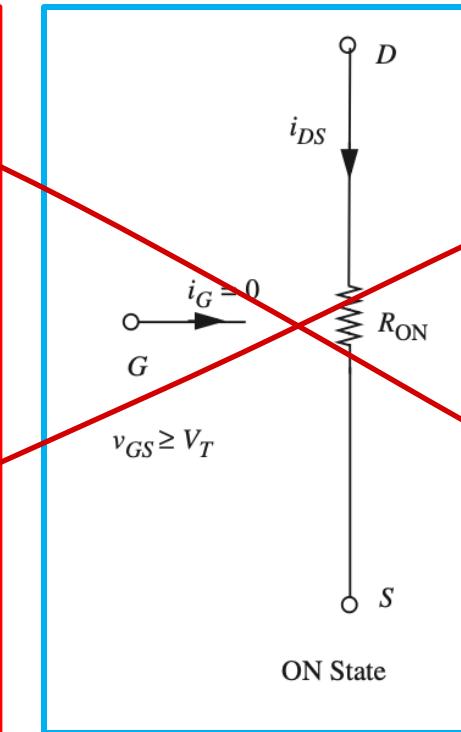
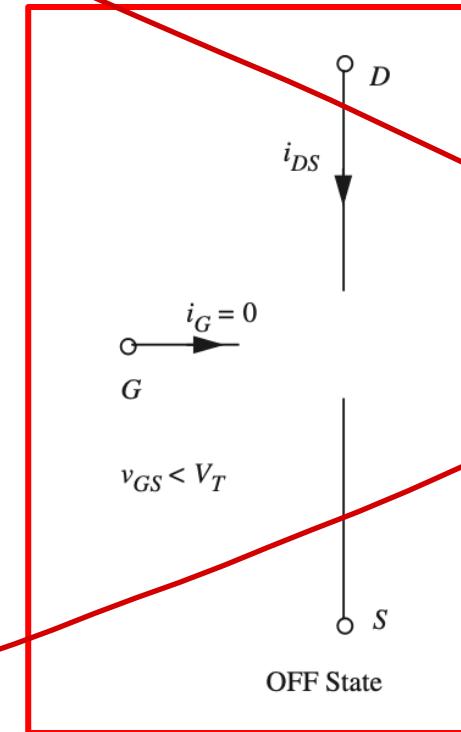
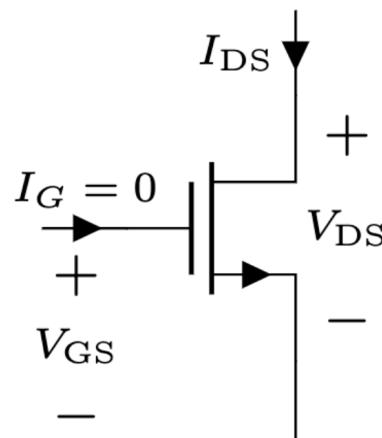


Channel created
Will have some R
-> SR model

SR Model

Excluded in

Summer 24



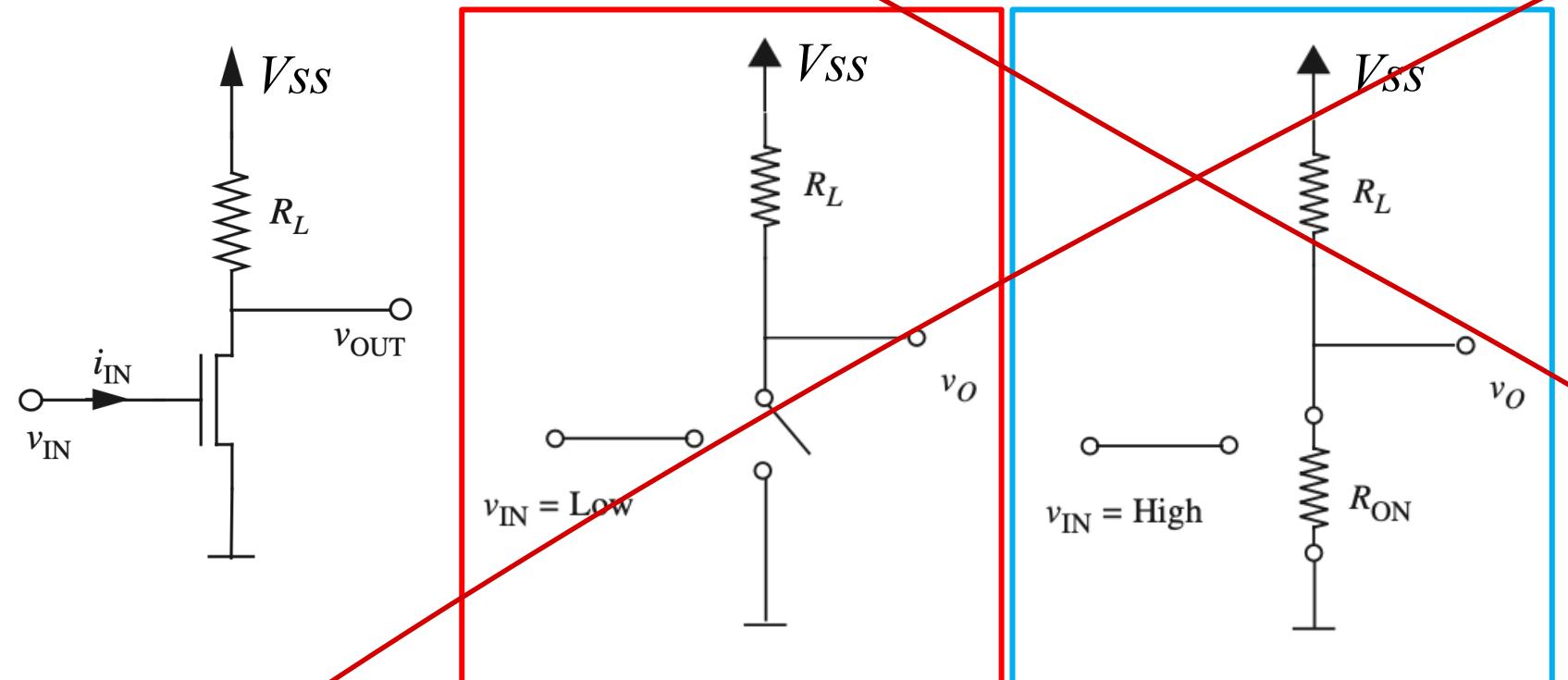
$$R_{ON} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{k V_{OV}}$$

Unit of $k = mA/V^2$

- SR model is a better approximation than S model
- However, still an approximation. This model fails when V_{DS} increases to around $V_{GS} - V_T$

SR Model - Inverter

Excluded

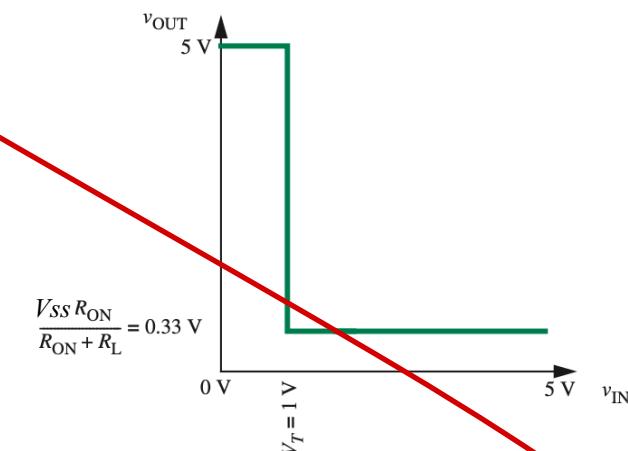


$$v_{OUT,High} = V_{SS}$$

$$v_{OUT,Low} = V_{SS} \frac{R_{ON}}{R_{ON} + R_L} \neq 0$$

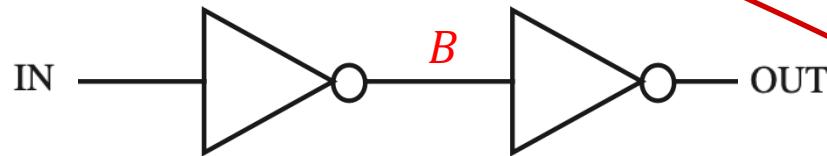
For example, if $V_{SS} = 5V$,
 $R_{ON} = 1 k\Omega$, $R_L = 14 k\Omega$

$$V_{SS} \frac{R_{ON}}{R_{ON} + R_L} = 0.33 \text{ V.}$$



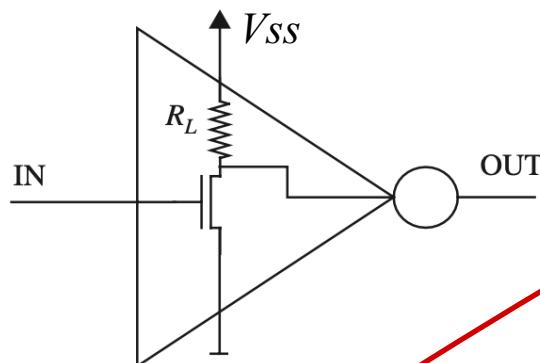
Design of logic gates

Excluded



Expected

IN	B	OUT
Low ($V_{IN} < V_T$)	High (5V)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} < V_T$)	Low ($V_{OUT,Low}$)	High (5V)



Actual

IN	B	OUT
Low ($V_{IN} < V_T$)	High (5V)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} < V_T$)	Low ($V_{OUT,Low} = 0.5 V$)	Low ($V_{OUT} = V_{OUT,Low}$)

$$V_T = 0.4 \text{ V}, V_{SS} = 5 \text{ V}, R_{ON} = 1 \text{ k}\Omega, R_L = 9 \text{ k}\Omega$$

$$V_{OUT,High} = V_{SS} = 5 \text{ V}$$

$$V_{OUT,Low} = V_{SS} \frac{R_{ON}}{R_{ON} + R_L} = 5 \frac{1}{1 + 9} = 0.5 \text{ V}$$

Therefore, need to design logic gates properly such that

$$V_{SS} \frac{R_{ON}}{R_{ON} + R_L} < V_T.$$

Design of logic gates - Example

~~Excluded~~

Assume the following values for the inverter circuit parameters: $V_S = 5 \text{ V}$, $V_T = 1 \text{ V}$, and $R_L = 10 \text{ k}\Omega$. Assume, further, that $\frac{1}{k'_n V_{OV}} = 5$ for the MOSFET. Determine a $\frac{W}{L}$ sizing for the MOSFET so that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter.

Solution:

$$\begin{aligned} V_S \frac{R_{ON}}{R_{ON} + R_L} &< V_T \\ \Rightarrow 5 \frac{R_{ON}}{R_{ON} + 10} &< 1 \\ \Rightarrow 5R_{ON} &< R_{ON} + 10 \\ \Rightarrow R_{ON} &< \frac{10}{4} = 2.5 \end{aligned}$$

Now,

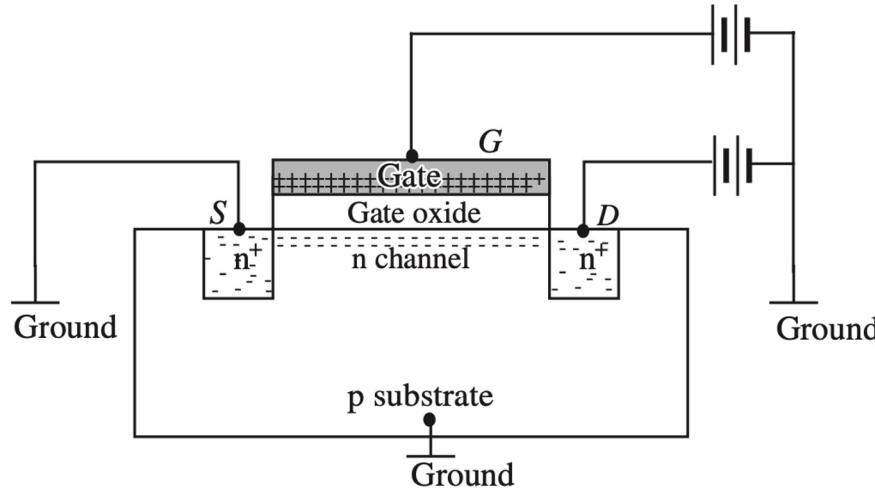
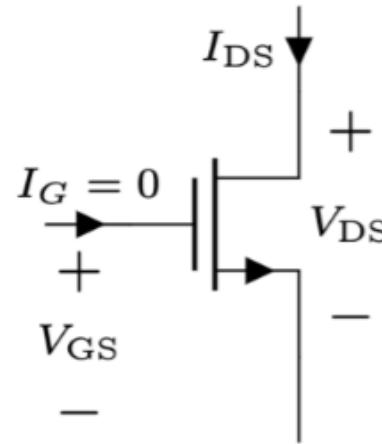
$$R_{ON} = \frac{1}{k'_n \frac{W}{L} V_{OV}} = 5 \times \frac{1}{W/L}$$

Hence

$$\frac{5}{W/L} < 2.5 \Rightarrow \frac{W}{L} > \frac{5}{2.5}$$

$$\Rightarrow \frac{W}{L} > 2$$

Review – MOSFET



Control = $V_{GS} = V_G - V_S$, controls the IV between drain-source (I_{DS} vs V_{DS})

Threshold voltage = V_T , minimum voltage required to create the channel

Models

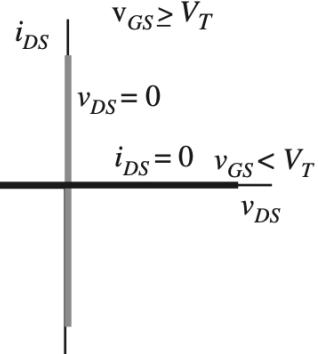
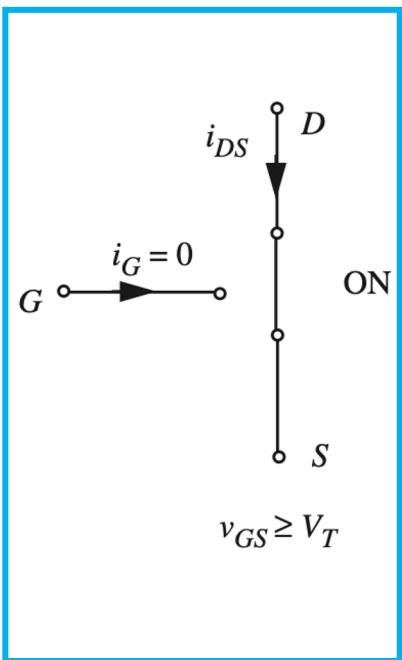
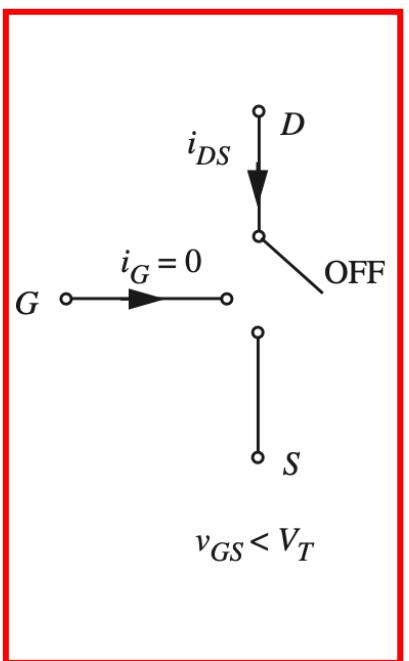
1. **S Mode:** Assumes an ideal channel with zero resistance

2. **SR Model:** Assumes finite channel resistance, R_{ON} , depends on $V_{GS} - V_T = V_{OV}$

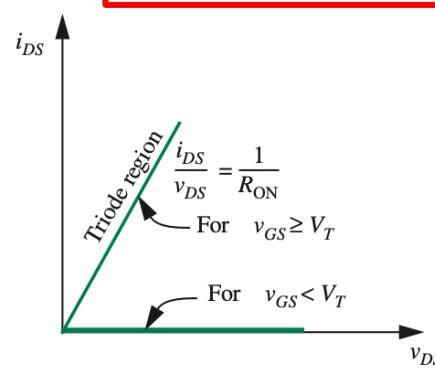
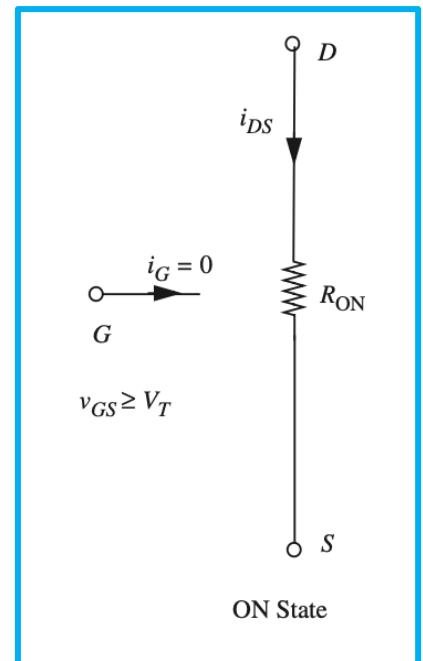
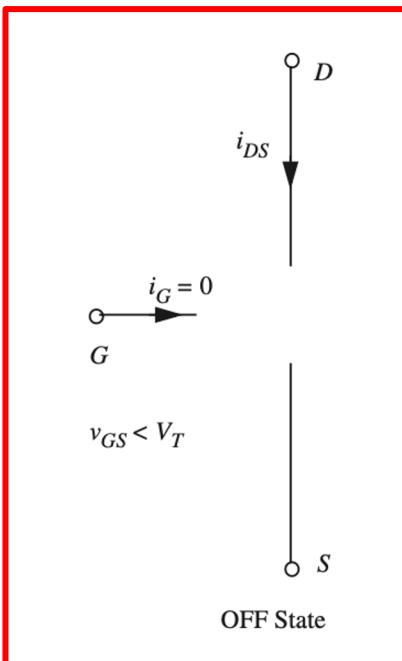
$V_{overdrive}$

MOSFET Linear Models

S Model



SR Model

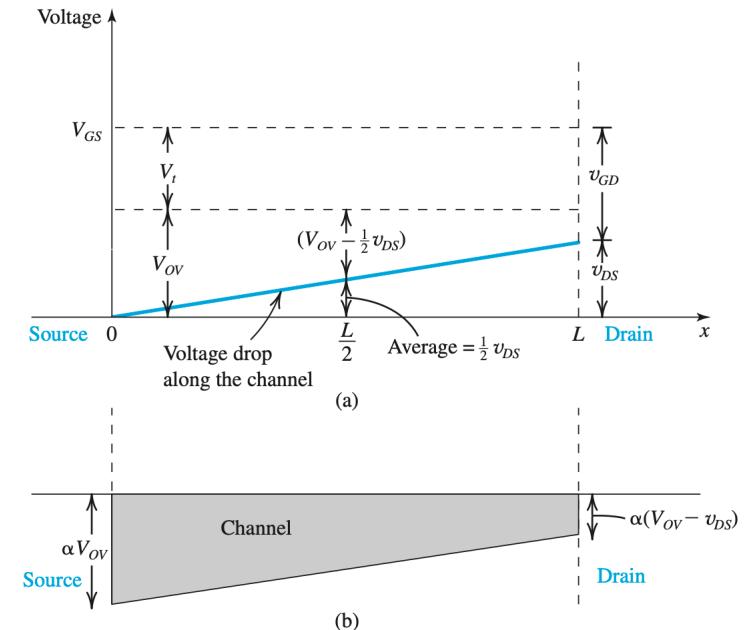
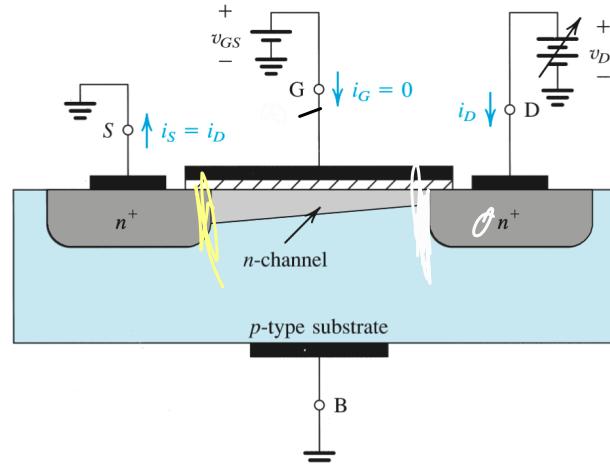
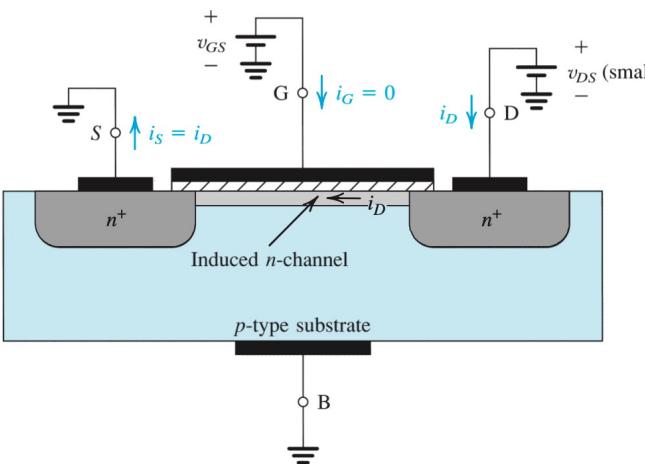


$$R_{ON} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{kV_{OV}}$$

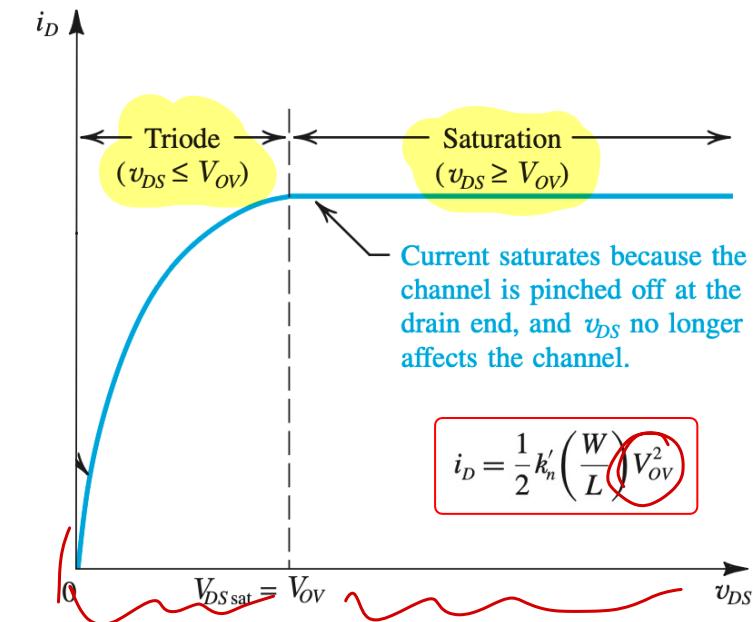
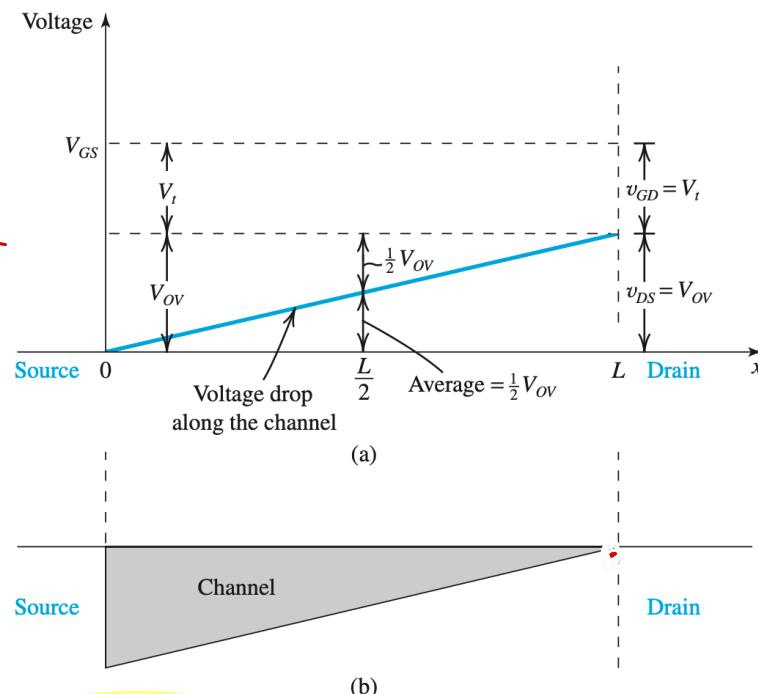
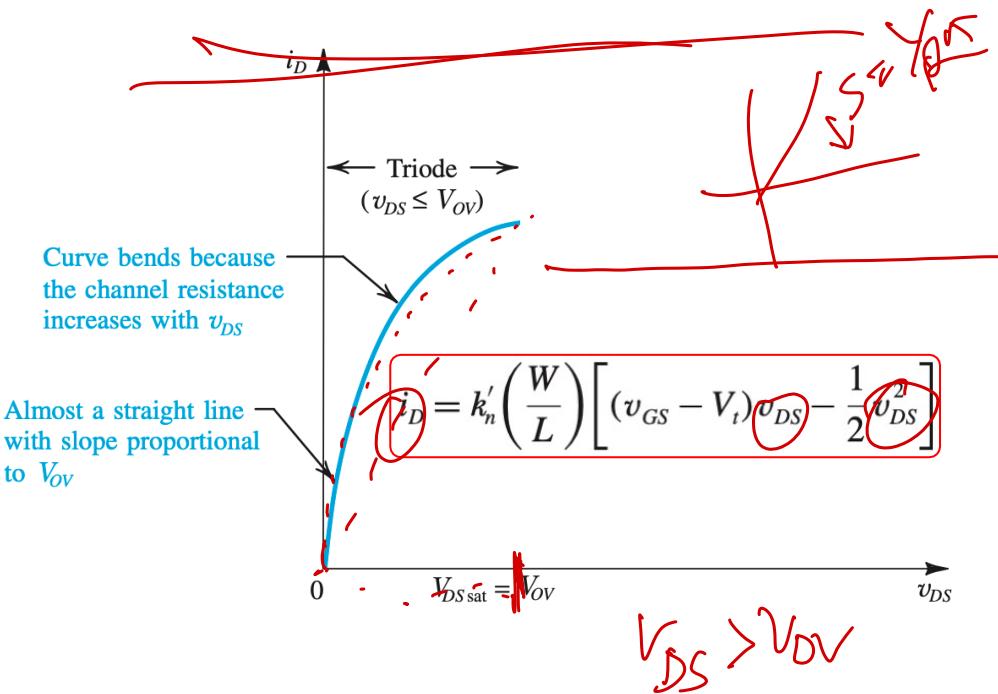
Real MOSFET



- Why $R_{ON} = \frac{1}{k'_n \frac{W}{L} (V_{GS} - V_T)} = \frac{1}{kV_{OV}}$? Because channel width $\propto V_{OV}$, and $R \propto \frac{1}{\text{width}}$
- For small V_{DS} , uniform channel, hence fixed R_{ON} , therefore SR model valid.
- As V_{DS} is increased, channel becomes tapered cause $V_{GD} \downarrow$. Resistance \uparrow , slope \downarrow .
- This mode is called the **triode mode**. Condition: $V_{DS} < V_{OV}$



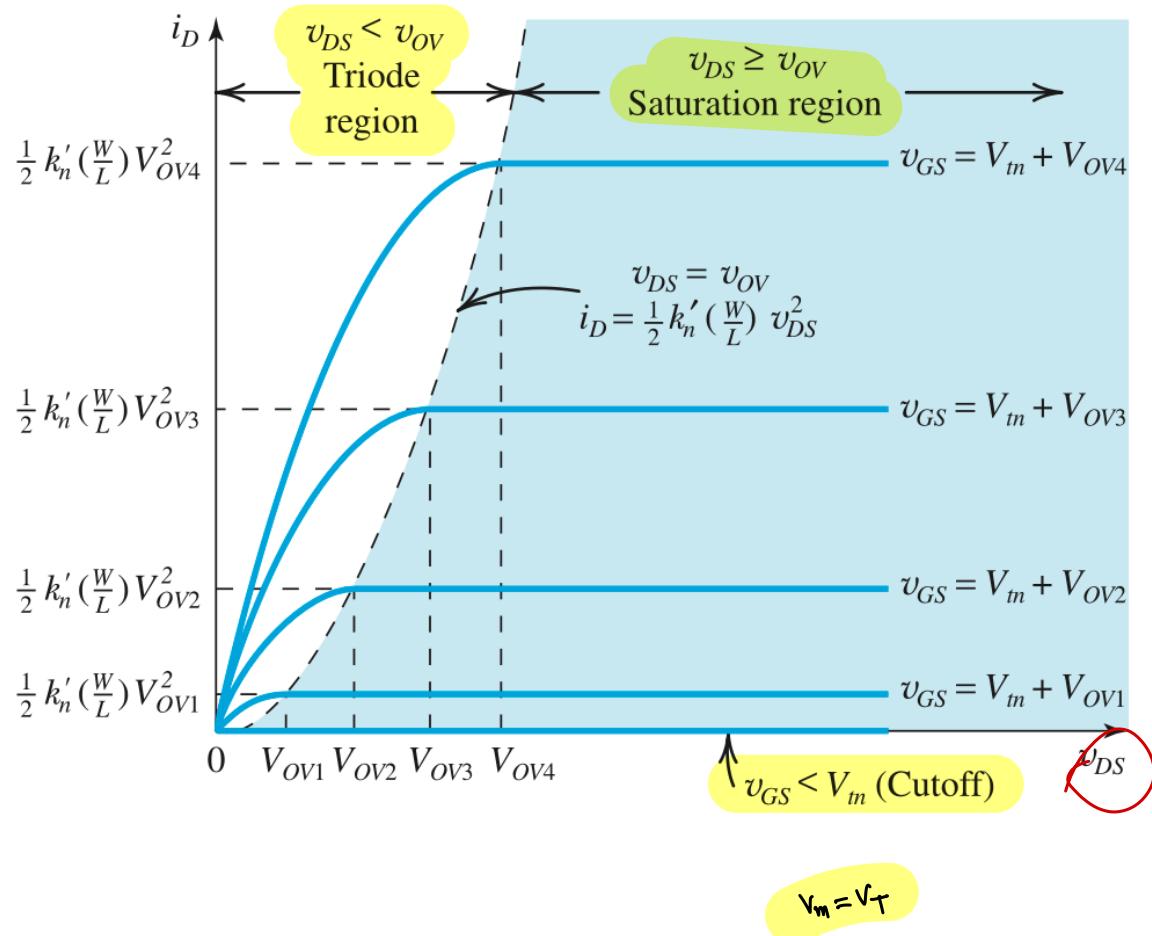
Real MOSFET



$$V_{OV} = V_{GS} - V_t$$

- When $V_{DS} = V_{OV}$, channel pinches off.
- Increasing V_{DS} further have no effect on channel shape. Hence, current saturates
- This mode is called the **saturation mode**. Condition: $V_{DS} \geq V_{OV}$
- Behaves like a current source (constant current) that depends on V_{OV}

IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \geq V_T$ $V_{DS} < V_{OV}$	$I_D = k \left[V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2 \right]$
Saturation	$V_{GS} \geq V_T$ $V_{DS} \geq V_{OV}$	$I_D = \frac{k}{2} V_{OV}^2$

$$V_{OV} = V_{GS} - V_T$$

$$k = k'_n \left(\frac{W}{L}\right)$$

$$I_G = 0$$

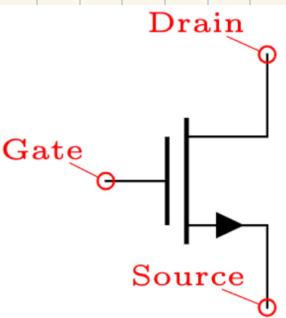
$$V_m = V_T$$

Cutoff $\longrightarrow V_{GS} < V_T \quad I_D = 0$

Triode $\longrightarrow V_{GS} > V_T$
 $V_{DS} < V_{ov}$ $I_D = K \left[V_{ov} V_{DS} - \frac{1}{2} V_{DS}^2 \right]$

Saturation $\longrightarrow V_{GS} > V_T$
 $V_{DS} > V_{ov}$ $I_D = \frac{1}{2} K V_{ov}^2$

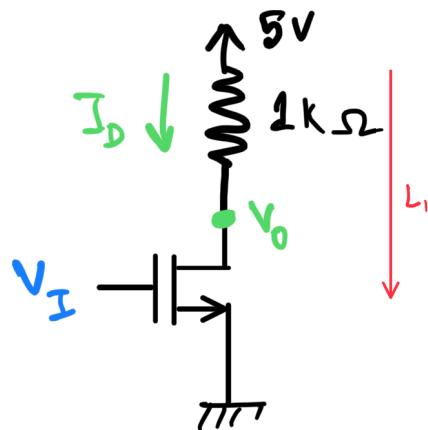
$$V_{ov} = V_{GS} - V_T$$



Solving Circuits with MOSFET

- Use **Method of Assumed State!**
- Three steps:
 - **Assume:** One of the modes (Cutoff, Triode, Saturation)
 - **Solve:** Use corresponding equation and KCL+KVL
 - **Verify:** Check if the conditions of V_{GS} and V_{DS} are satisfied. If not, repeat.
- Might need to solve quadratic equation ($ax^2 + bx + c = 0$).
- If we get two roots, choose the one that's *favorable* to your assumption

Example 1



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_o for $V_I = 2V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2} V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 2V$
Therefore, $V_{OV} = V_{GS} - V_T = 2 - 1 = 1V$

$$\therefore I_D = \frac{0.5}{2} (1)^2 = 0.25 \text{ mA}$$

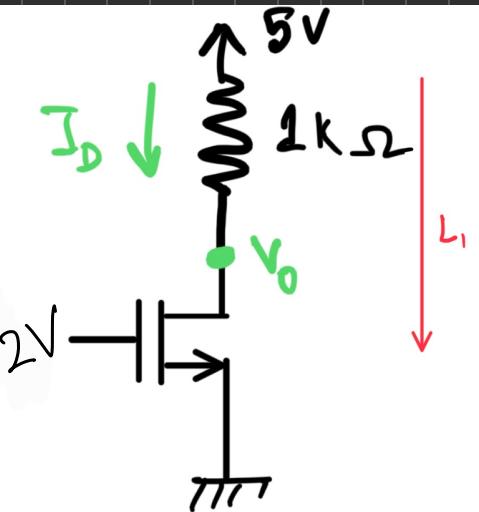
$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$$

KVL along L_1 : $I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega$
 $\Rightarrow V_o = 5 - 0.25 \times 1 = 4.75 \text{ V} = V_{DS}$

Step 3: $V_{GS} = 2V > V_T \checkmark$ Therefore, **assumption correct!**

$V_{DS} = 1V > V_{OV} \checkmark$ Correct ans: $I_D = 0.25 \text{ mA}$, $V_o = 4.75 \text{ V}$

The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$.
 Find I_D and V_O for $V_I = 2V$.



$$\begin{aligned}
 V_{GS} &= V_G - V_S \\
 &= 2 - 0 \\
 \Rightarrow V_{GS} &= 2 \\
 \Rightarrow V_T &= 1V \\
 \Rightarrow V_{OV} &= 2 - 1 = 1V \\
 k &= 0.5 \text{ mA/V}^2
 \end{aligned}$$

$V_{GS} > V_T$
 \therefore Either Triode or Saturation

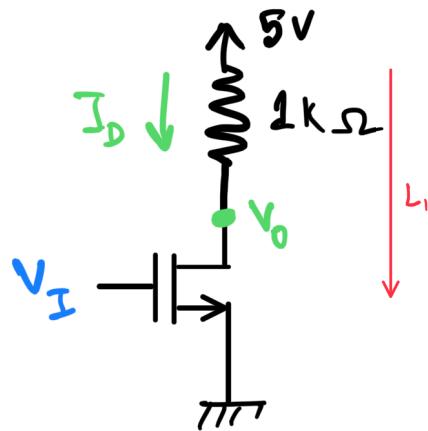
Let's assume,
 Saturation mode

$$\begin{aligned}
 \therefore I_D &= \frac{1}{2} k V_{OV}^2 \\
 &= \frac{1}{2} \times 0.5 \times 1 \\
 I_D &= 0.25V
 \end{aligned}$$

$$\begin{aligned}
 \frac{5 - V_O}{1} &= I_D \\
 \Rightarrow V_O &= 5 - 0.25 \\
 &= 4.75
 \end{aligned}$$

$V_{GS} > V_T$
 $V_{DS} > V_{OV}$
 $\therefore 4.75 > 1$
 Assumption verified.
 (Ans)

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_o for $V_I = 5V$.

Solution:

Step 1: Assume the MOSFET in **saturation**

Step 2: $I_D = \frac{k}{2} V_{OV}^2$ Here, $V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$
Therefore, $V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$

$$\therefore I_D = \frac{0.5}{2} (4)^2 = 4 \text{ mA}$$

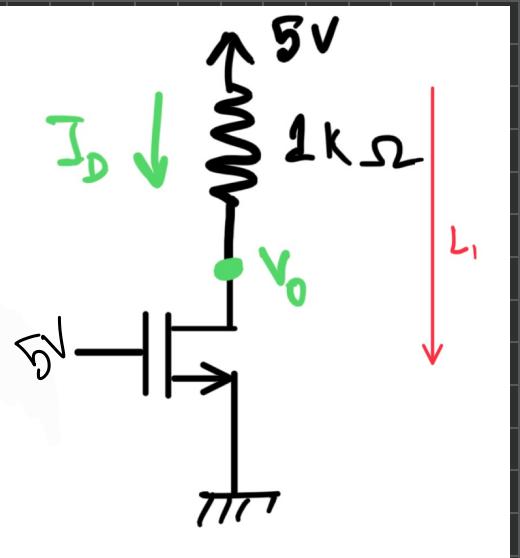
Again, $V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o$

KVL along L_1 : $I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow V_o = 5 - I_D \times 1k\Omega$

$$\Rightarrow V_o = 5 - 4 \times 1 = 1V = V_{DS}$$

Step 3: $V_{GS} = 5V > V_T$ ✓ Therefore, **assumption wrong!**

$$V_{DS} = 1V \neq V_{OV} \times$$



$$V_{GS} = 5V$$

$$V_T = 1V$$

$$\therefore V_{OV} = 5 - 1 = 4V$$

$$K = 0.5$$

$V_{GS} > V_T \therefore$ Saturation on Triode

Let's, assume saturation.

$$\begin{aligned} \therefore I_D &= \frac{1}{2} K V_{OV}^2 \\ &= \frac{1}{2} \times 0.5 \times 4^2 \\ &= 4 \text{ mA} \end{aligned}$$

$$\therefore 5 - V_D = 4 \times 1$$

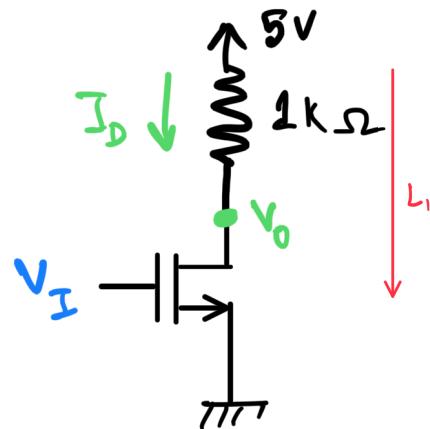
$$\Rightarrow V_D = 1$$

$$\therefore V_{DS} = 1$$

$$\therefore V_{DS} \neq V_{OV}$$

Assumption Wrong.

Example 2



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_o for $V_I = 5V$.

Repeat:

Step 1: Assume the MOSFET in **triode**

$$\text{Step 2: } I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - 0 = V_G = V_I = 5V$$

$$\text{Therefore, } V_{OV} = V_{GS} - V_T = 5 - 1 = 4V$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - 0 = V_D = V_o. \text{ Assuming } V_{DS} = x$$

$$\text{KVL along } L_1: I_D \times 1k\Omega + V_o = 5 - 0 \Rightarrow I_D = \frac{5 - V_{DS}}{1} = 5 - x$$

$$\therefore I_D = 0.5 \left[4 \times V_{DS} - \frac{1}{2} V_{DS}^2 \right] \Rightarrow (5 - x) = 0.5 \left[4x - \frac{1}{2} x^2 \right]$$

$$\Rightarrow 5 - x = 2x - 0.25x^2 \Rightarrow 0.25x^2 - 3x + 5 = 0$$

$$\text{Solving, } x = 2V, \cancel{x = 10V}$$

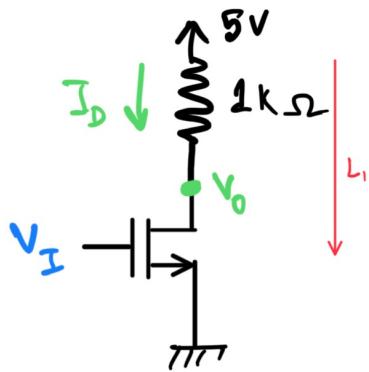
Since $V_{DS} = x$ is small in triode, smaller value of x is favorable

$$\text{Therefore, } V_o = V_{DS} = x = 2V, \text{ and } I_D = 5 - x = 3 \text{ mA}$$

Step 3: $V_{GS} = 5V > V_T \checkmark$ Therefore, **assumption correct!**

$$V_{DS} = 2V < V_{OV} \checkmark$$

Correct ans: $I_D = 3 \text{ mA}, V_o = 2V$



The MOSFET is specified as $V_T = 1V$ and $k = 0.5 \text{ mA/V}^2$. Find I_D and V_O for $V_I = 5V$.

Let's assume Triode,

$$\begin{aligned} \therefore I_D &= k \left[V_{ov} V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= 0.5 \left[4x - \frac{1}{2} x^2 \right] \\ &= -0.25x^2 + 2x \end{aligned}$$

Again,

$$\begin{aligned} \frac{5 - V_D}{1} &= I_D = -0.25x^2 + 2x \\ \Rightarrow 5 - x &= -0.25x^2 + 2x \\ \Rightarrow 0.25x^2 - 3x + 5 &= 0 \end{aligned}$$

$$x = 10$$

$$x = 2 \quad \left[\text{we will take this value} \right]$$

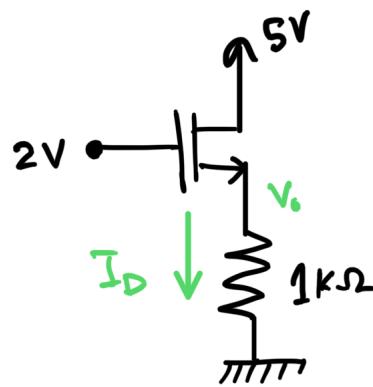
$$\therefore x = 2$$

$$\therefore V_{DS} = 2, V_{GS} = 5 > V_T, V_{ov} = V_{GS} - V_T = \frac{5-1}{4} = 4$$

$$\therefore V_{DS} < V_{ov}$$

∴ Assumption correct. Triode mode.

Example 3



The MOSFET is specified as $V_T = 1V$ and $k = 4 \text{ mA/V}^2$.

Find I_D and V_o

Solution:

Step 1: Assume the MOSFET in **saturation**

$$\text{Step 2: } I_D = \frac{k}{2} V_{ov}^2$$

Let's assume $V_0 = V_S = x$

$$\text{Here, } V_{GS} = V_G - V_S = V_G - V_0 = 2 - x$$

$$\text{Therefore, } V_{ov} = V_{GS} - V_T = (2 - x) - 1 = 1 - x$$

$$\text{Again, } V_{DS} = V_D - V_S = V_D - V_0 = 5 - x$$

$$\text{Ohm's law for the resistor: } I_D = \frac{V_0 - 0}{1k\Omega} = x$$

$$\therefore x = \frac{4}{2} (1 - x)^2 \Rightarrow x = 2(1 - 2x + x^2) \Rightarrow x = 2 - 4x + 2x^2$$
$$\Rightarrow 2x^2 - 5x + 2 = 0$$

$$\text{Solving, } x = 0.5, \cancel{x = 2V}$$

Since $V_{DS} = 5 - x$ is large in saturation
smaller value of x is favorable

$$\therefore V_0 = V_S = x = 0.5V, I_D = x = 0.5 \text{ mA},$$

$$V_{DS} = 5 - x = 4.5V, V_{GS} = 2 - x = 1.5V, \text{ and } V_{ov} = 1 - x = 0.5V$$

Step 3: $V_{GS} = 1.5V > V_T \checkmark$ Therefore, **assumption correct!**

$V_{DS} = 4.5V > V_{ov} \checkmark$ Correct ans: $I_D = 0.5 \text{ mA}, V_o = 0.5 V$

Practice

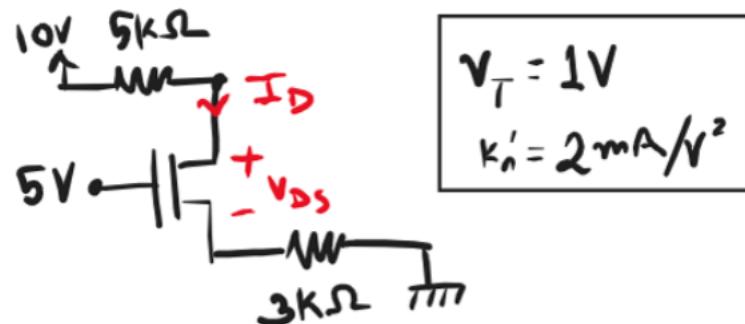
Question 4 [CO1, CO4]

10

Analyze the following circuit to find the values of I_D and V_{DS} using the Method of Assumed State. You must validate your assumptions.

[7 + 3]

Hint: Use I_D as unknown x . Use Ohm's law to represent V_D and V_S in terms of x .



Hint Explanation

Assume $I_D = x$. For $5k\Omega$: $I_D = \frac{10 - V_D}{5} \Rightarrow V_D = 10 - 5x$.

For $3k\Omega$: $I_D = \frac{V_S - 0}{3} \Rightarrow V_S = 3x$.

Therefore, $V_{GS} = V_G - V_S = 5 - 3x$, and $V_{OV} = V_{GS} - V_T = (5 - 3x) - 1$

Also, $V_{DS} = V_D - V_S = (10 - 5x) - 3x = 10 - 8x$

Now if you assume saturation:

$$I_D = \frac{k}{2} V_{OV}^2 \Rightarrow x = \frac{2}{2} (4 - 3x)^2$$

And if you assume triode:

$$I_D = k [V_{OV} V_{DS} - \frac{1}{2} V_{DS}^2]$$

$$\Rightarrow x = 2[(4 - 3x)(10 - 8x) - 0.5 \times (10 - 8x)^2]$$

Solve for x , take the _____ root



$$x = \frac{2}{2} (4 - 3x)^2$$

$$\Rightarrow x = 16 - 2 \cdot 3x \cdot 4 + 9x^2$$

$$\Rightarrow 9x^2 - 24x - x + 16 = 0$$

$$\Rightarrow 9x^2 - 25x + 16 = 0$$

$$\therefore x = 1 \text{ or } 1.78$$

$$\therefore V_{GS} = 5 - 3x = 2$$

$$V_{OV} = 4 - 3x = 1$$

$$\uparrow V_{DS} = 10 - 8x = 2$$

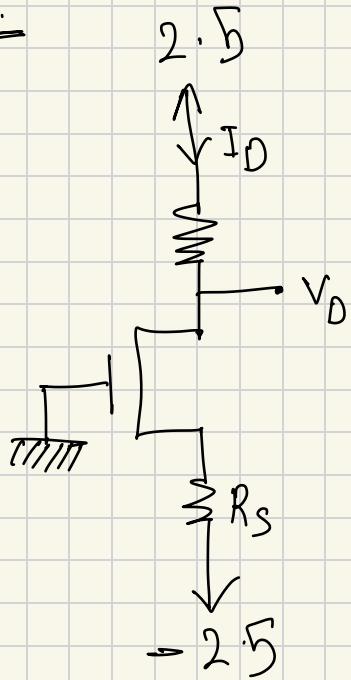
$$\begin{aligned} V_{GS} &\geq V_T \\ 2 &> 1 \end{aligned}$$

$$V_{DS} > V_{OV}$$

$$2 > 1$$

\therefore Assumption correct;

Example:



$$\boxed{\begin{aligned}V_T &= 0.7V \\K &= 3 \cdot 2 \text{ mA/V}^2 \\I_D &= 0.4 \text{ mA} \\V_D &= 0.5V \\V_S &=? \\R_S &=?\end{aligned}}$$

$$R_D = \frac{2.5 - 0.5}{0.4} = 5k\Omega$$

$$\therefore V_{DS} = 0 - V_S = -V_S = -x$$

$$V_{OV} = V_{GS} - V_T = -V_S - 0.7 = -x - 0.7$$

$$V_{DS} = 0.5 - V_S = 0.5 - V_S = 0.5 - x$$

Saturation

$$I_D = \frac{k}{2} V_{ov}^2$$

$$\Rightarrow 0.4 = \frac{3.2}{2} (-n - 0.7)^2$$

$$\therefore n = ?$$

if $n = -0.2$

$$\therefore V_{GS} = 0.2$$

$$V_{ov} = 0.2 - 0.7 = -0.5$$

$$V_{DS} = 0.5 - 0.2 = 0.3$$

$$0.25 = (n + 0.7)^2$$

$$\Rightarrow \pm 0.5 = n + 0.7$$

$$\Rightarrow n = -0.2, -1.2$$

$$\boxed{V_{DS} > V_{ov} \\ 0.7 > -0.5}$$

$$V_{GS} > V_T$$

$$0.2 > 0.7$$

$$\text{if } V_S = -1.2 \text{ V}$$

$$V_{GS} = 1.2$$

$$V_{OV} = 1.2 - 0.7 = 0.5$$

$$V_{DS} = 0.5 + 1.2 = 1.7$$

$$\therefore V_{GS} > V_T$$

$$1.2 > 0.7$$

$$V_{DS} > V_{OV}$$

$$1.7 > 0.5$$

$$\therefore V_S = -1.2$$

$$\therefore R_S = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega \quad (\text{Ans})$$

Diode

1 ଟୀ ବ୍ୟବହାର କରିଲେ 2 ଟୀ state

2 "", " 4 "", "

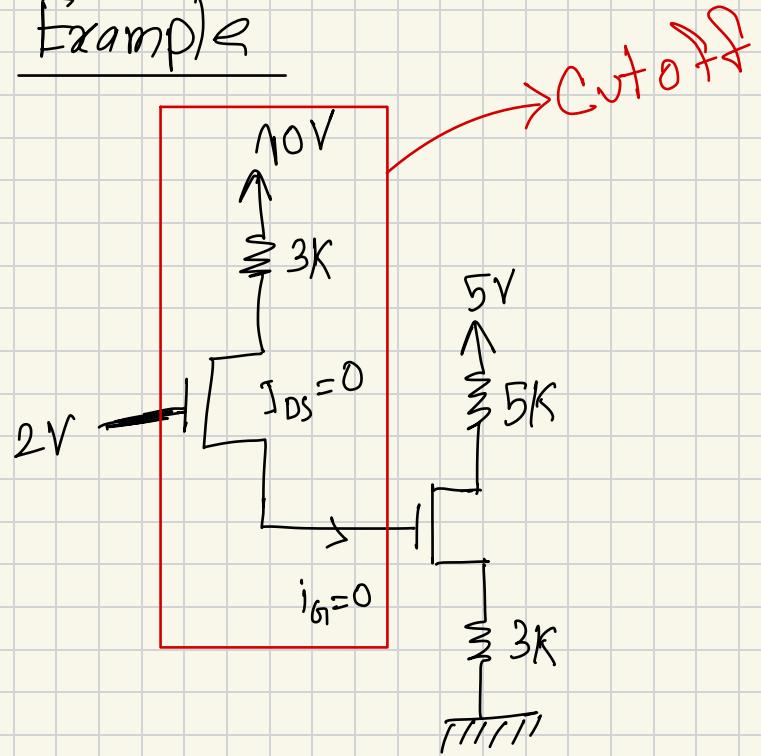
Mosfet

1 \rightarrow 3

2 \rightarrow 9

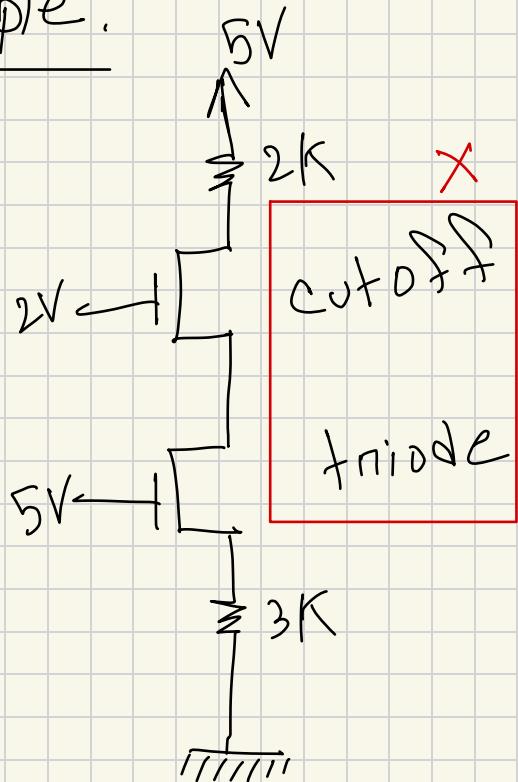
3 \rightarrow 27

Example



KCL

Example :



cut off

cut off

triode

triode/Saturation

saturation

triode/ saturation

Assignment:

Deadline : 19 Sept

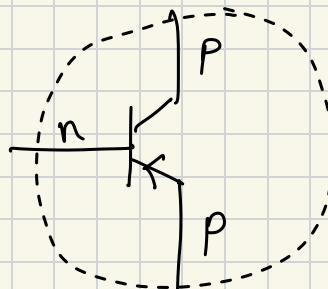
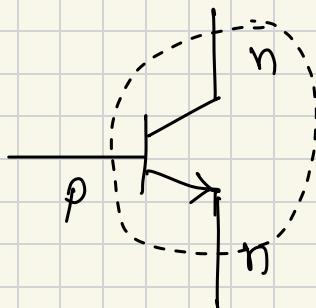
Quiz : 03

Sunday, 15 Sept

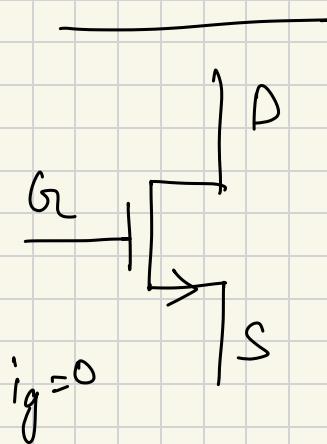
MOSFET

BJT

(Bipolar Junction Transistor)

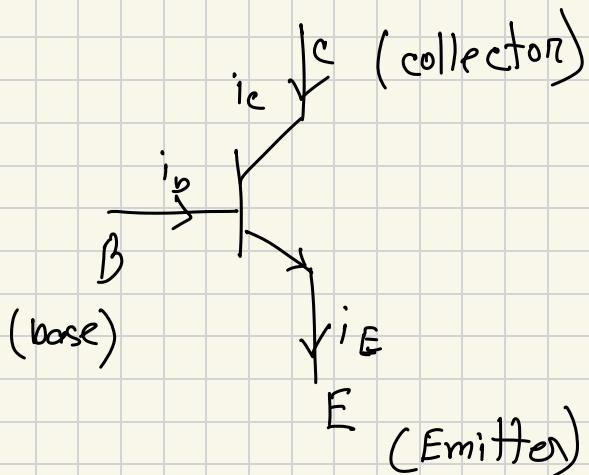


MOSFET



$$I_D = I_S = I_{DS}$$

BJT



off হাবেল $i_B = 0$

$i_B \neq 0$

$$i_E = i_B + i_C$$

$\therefore i_C \neq i_E$

(have to use this formula)

control Terminal (G)

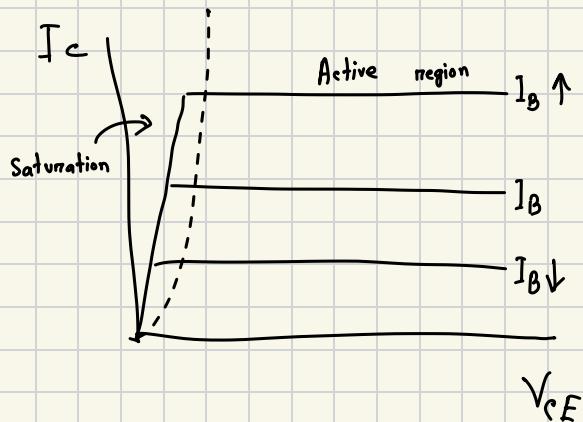
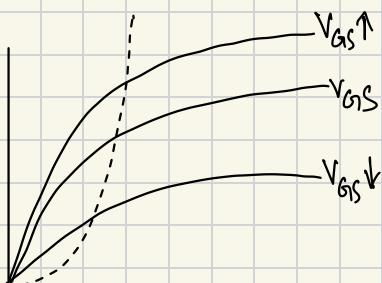
control Terminal (B)

Voltage controlled (V_{GS})

V_{DS} vs I_{DS}

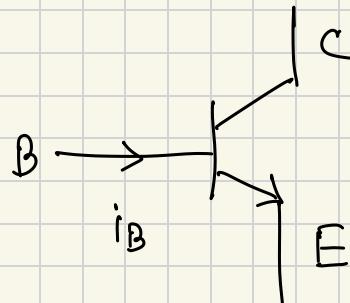
Current controlled (I_B)

I_C vs V_{CE}



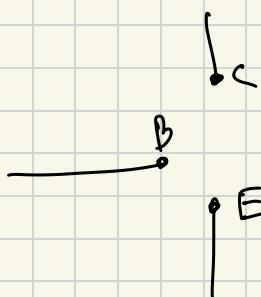
BJT S-model

same as MOSFET



BJT OFF

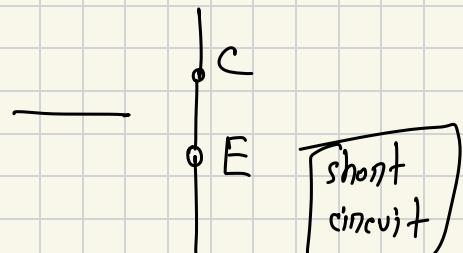
$$i_B = 0 \text{ [open circuit]}$$



$$\therefore i_C = 0$$

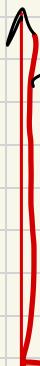
BJT ON

$$i_B \geq i_{th} (0.2mA)$$



$$V_{CE} = 0$$

I_c



BJT ON

$$V_{CE} = 0$$

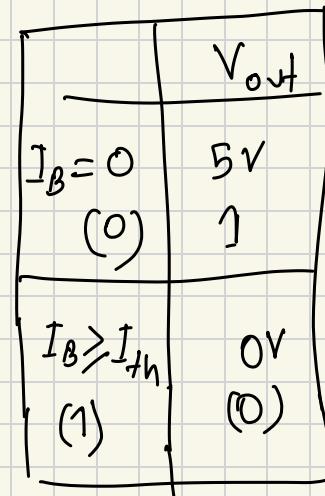
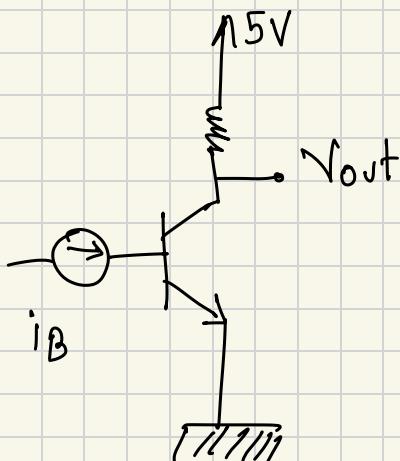
V_{CE}
BJT off

Same as MOSFET

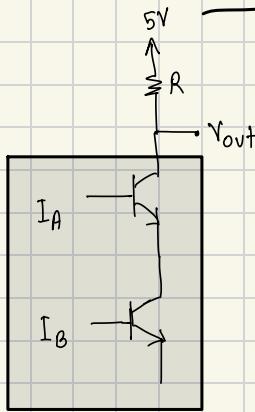
Logic Gate

with BJT

NOT



NAND

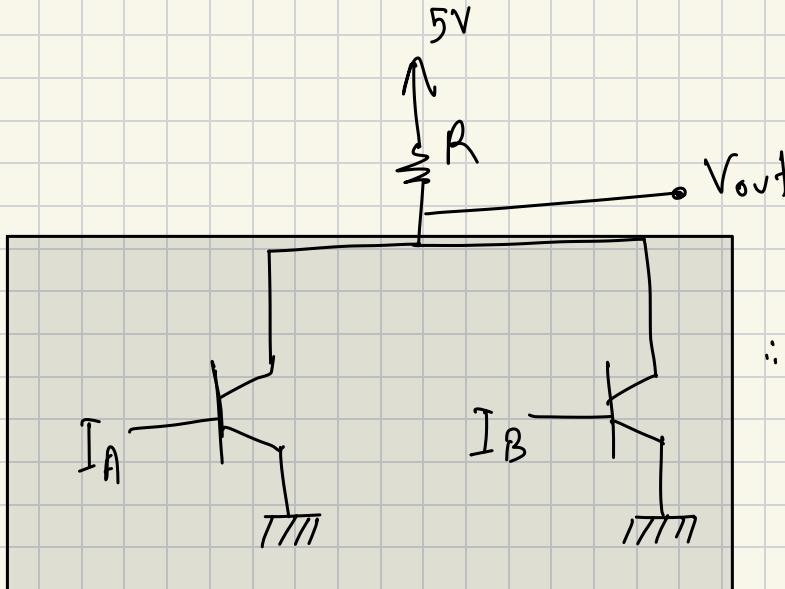


$$V_{out} = \overline{I_A I_B}$$

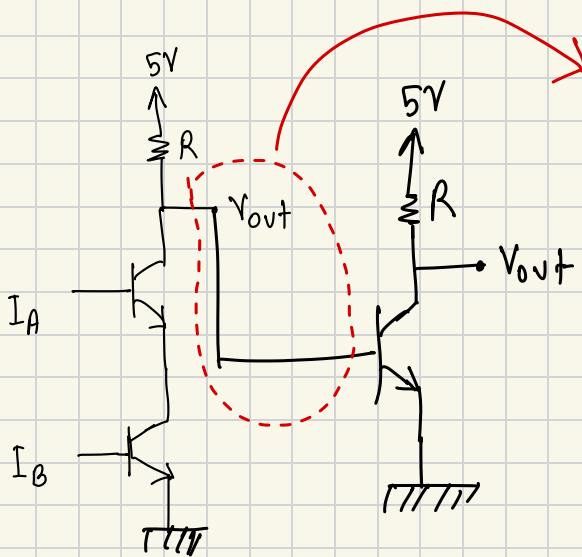
$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\therefore \overline{AB} = \overline{A} + \overline{B}$$

NOR



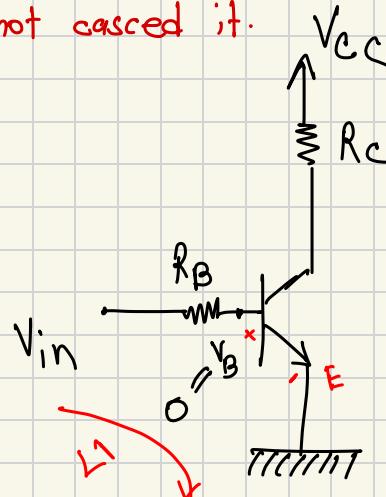
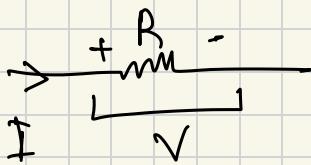
$$\therefore V_{out} = \overline{I_A + I_B}$$



Input Current,
input current with
V.
So, we can not
cascade BJT for
logical operation

Controlling BJT with Voltage

We are trying to control a BJT because it takes input as current and gives output as voltage. that's why we can not cascade it.



Normally, (We know this from BJT's Switch Model)

$$I_B = 0 \quad \text{then} \quad V_{out} = 1$$

$$I_B > I_{th} \quad \text{then} \quad V_{out} = 0$$

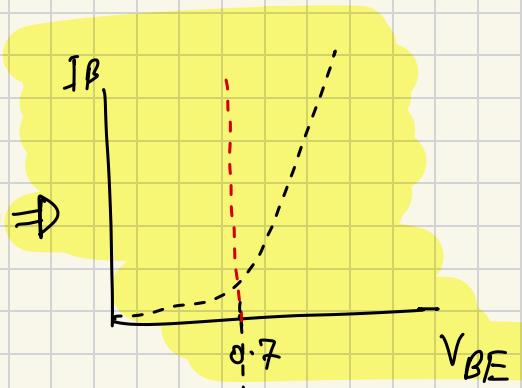
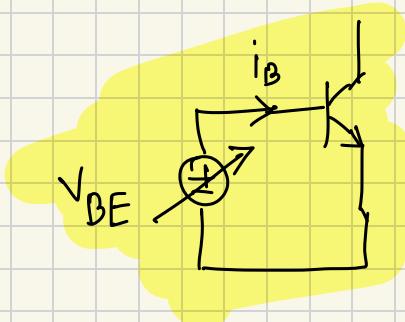
for L1,

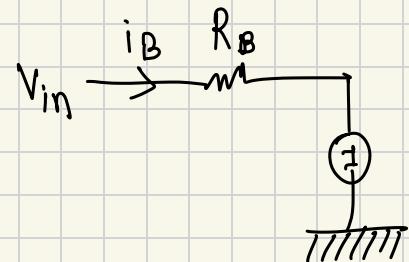
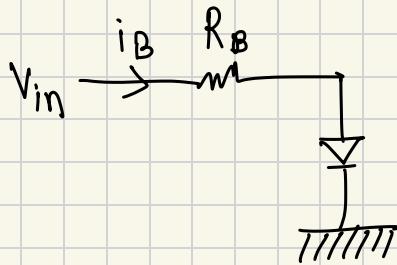
$$V_{in} - 0 = i_B R_B + V_{BE}$$

$$\Rightarrow i_B = \frac{V_{in} - V_{BE}}{R_B}$$

$$V_{BE} = f(I_B)$$

2 way lock.
It's a loop.





Diode OFF

$$V_{in} < 0.7$$

$$\Rightarrow i_B = 0$$

Diode ON

$$V_{in} - 0.7 = i_B R_B + 0.7$$

$$V_{in} - 0.7 = i_B R_B$$

$$\Rightarrow V_{in} = 0.7 + i_B R_B$$

$$\Rightarrow V_{th} = i_{th} R_B + 0.7$$

$$V_{in} < 0.7 \leftarrow i_B = 0$$

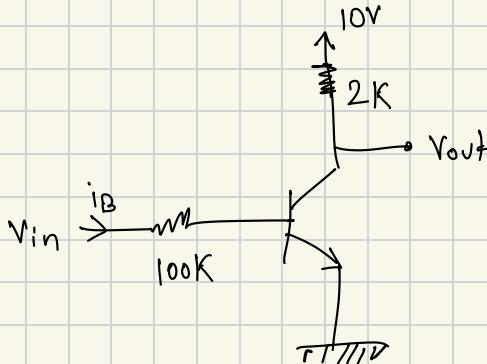
$$V_{out} = 1$$

$$V_{in} \geq V_{th} \leftarrow i_B \geq i_{th}$$

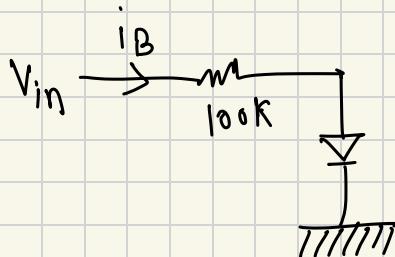
$$V_{out} = 0$$

$$f(R_B, i_{th})$$

EN



(?) find the value of V_{in} for which $i_B \geq i_{th}$, $i_{th} = 0.2mA$



<u>OFF</u>	<u>ON</u>
$V_{in} < 0.7$	$V_{in} - 0.7 = i_B \times 100K$
$= i_B = 0$	

$$\Rightarrow V_{th} = 0.7 + i_{th} \times 100K$$

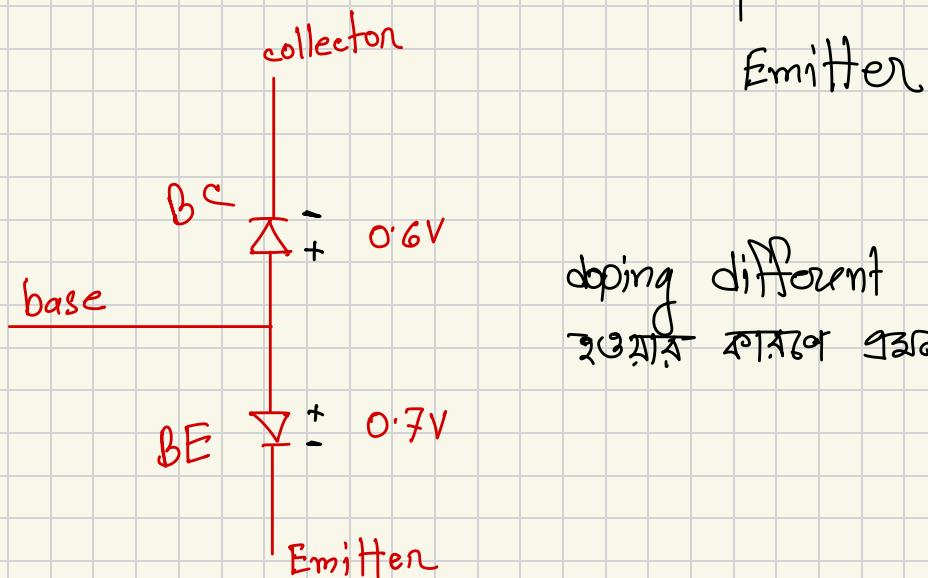
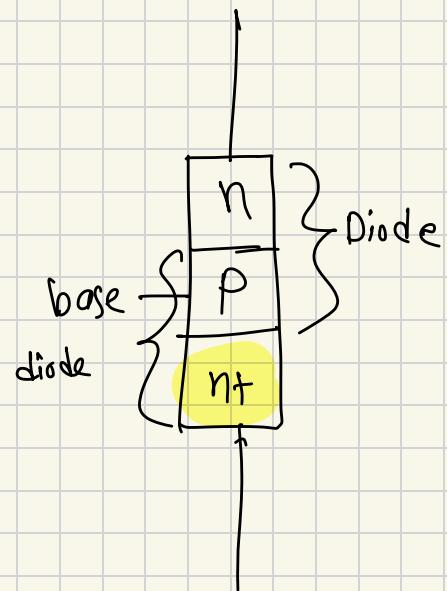
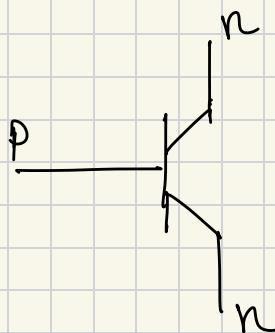
$$V_{Th} = 0.2 \times 100 + 0.7$$

$$V_{Th} = 20.7V \quad (\text{Ans})$$

BJT

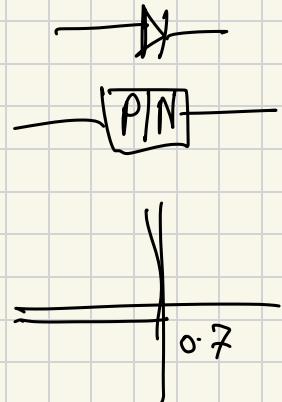
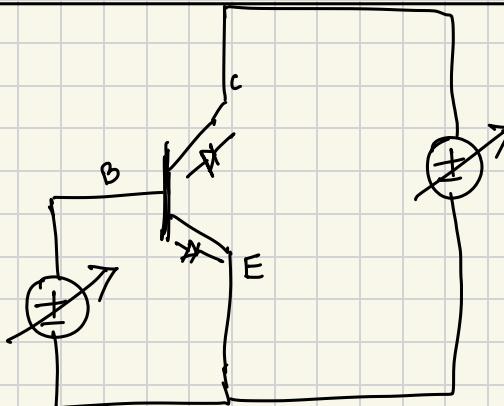
Collector

Diode model .



doping different
ইওনিক কারণে প্রয়োগ

$$I_E = I_B + I_C$$



BE diode (OFF)

$$V_{BE} < 0.7$$

BC diode (OFF)

$$V_{BC} < 0.6$$

$$\Rightarrow V_B - V_C < 0.6$$

$$\Rightarrow V_B - V_E - (V_C - V_E) < 0.6$$

$$\Rightarrow V_{BE} - V_{CE} < 0.6$$

$$\Rightarrow V_{CE} > V_{BE} - 0.6$$

$$\Rightarrow V_{BE} < V_{CE} + 0.6$$

States of diode :

BE \rightarrow ON, OFF

BC \rightarrow ON, OFF

	BE	BC
cutoff	OFF	OFF
saturation	ON	ON
Active	ON	OFF
Reverse active	OFF	ON

Case I

BE OFF

$$V_{BE} < 0.7$$

Cutoff

$$I_C = 0$$

$$I_B = 0$$

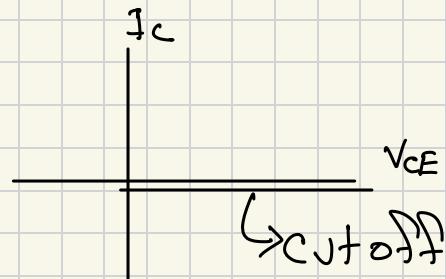
$$I_E = 0$$

BC OFF

$$V_{CE} > V_{BE} - 0.6$$



only for this course



Case II

Active

BE ON

$$I_B > 0$$

BC OFF

$$V_{CE} > V_{BE} = 0.6$$

$$I_C = \beta I_B$$

$$\Rightarrow \beta = \frac{I_C}{I_B}$$

\therefore BJT acts as an amplifier.

$$I_E = I_B + I_C$$

$$= I_B + \beta I_B$$

$$I_E = I_B (1 + \beta)$$

$$I_E = I_B + I_C$$

$$\Rightarrow I_E = \frac{I_C}{\beta} + I_C$$

$$= \left(1 + \frac{1}{\beta}\right) I_C$$

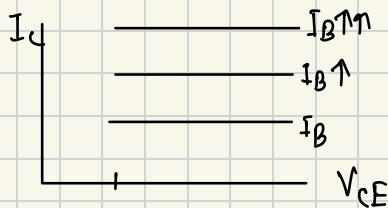
$$I_E = \left(\frac{\beta + 1}{\beta}\right) I_C$$

$$\Rightarrow I_C = \left(\frac{\beta}{1 + \beta}\right) I_E$$

$$\Rightarrow I_C = \alpha I_E$$

যদি active mode র থার্ড গোল্ডে
collection current, base current র থার্ড
অনেক কম হয় ।

emitter Current, base current এবং same
 $I_E = I_B + I_C$

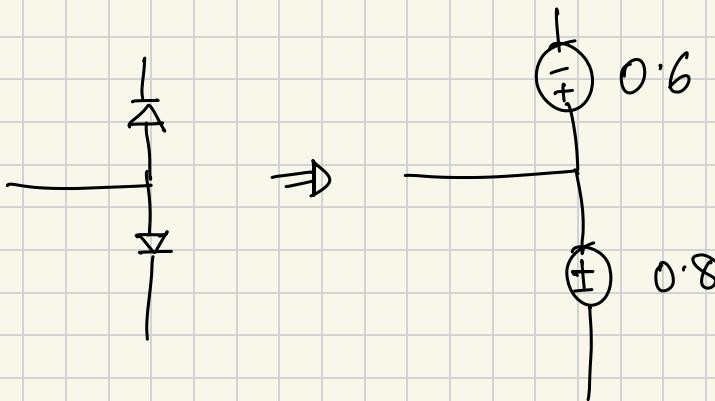


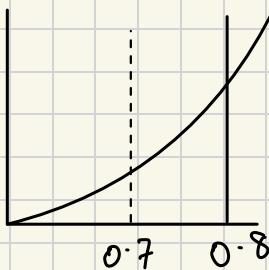
Saturation

2 diode on.

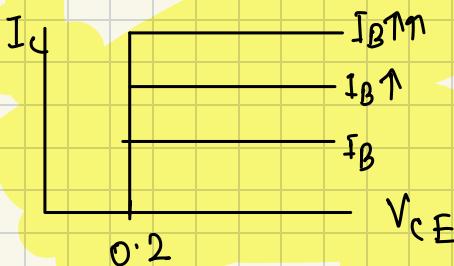
BE ON

BC ON





current অনুসরে ধোরণ ফ্লো
 হ্যাঁ B and E ফিল্ড।
 তাঁর 0.8 V



In Active, $I_C = \beta I_B$

$$\Rightarrow \beta = \frac{I_C}{I_B}$$

In saturation,

$$I_C \downarrow$$

$$I_B \uparrow$$

$$\frac{I_C}{I_B} < \beta$$

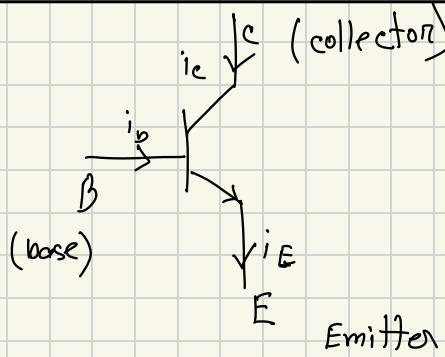
BJT Method of Assumption

- ① Assumption
- Active $[V_{BE} = 0.7, I_C = \beta I_B]$
 - Saturation $[V_{BE} = 0.8, V_{CE} = 0.2]$
 - Cutoff $[I_C = I_B = I_E = 0]$
- ② Solve $[KCL, KVL, Nodal]$

③ Verification:

- Active $[V_{CE} > 0.2]$
- Saturation $\left[\frac{I_C}{I_B} < \beta \right]$
- Cutoff $\left[V_{BE} < 0.7, V_{BC} < 0.5 \right]$

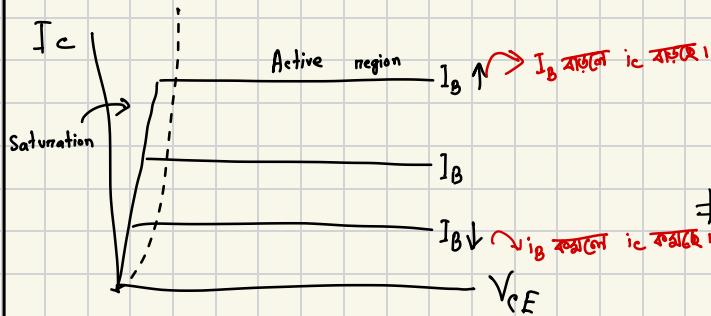
Summary over BJT



BJT দিয়ে আমরা mainly i_B use করে।
collector and emitter এর মধ্যে current flow control করে।

$i_B \neq 0$, if $i_B = 0$ then the BJT is in cutoff mode.

I_C vs V_{CE}

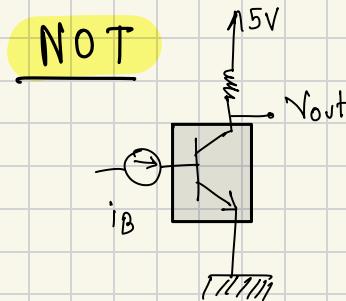


BJT S-Model (Switch Model)

BJT OFF	BJT ON
$i_B = 0$ [open circuit] $\therefore i_C = 0$	$i_B \geq i_{th}$ ($0.2mA$) $V_{CE} = 0$

i_C $\therefore V_{CE} = 0$	$V_{out} = 1$
--------------------------------------	---------------

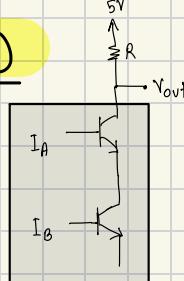
Logic Gate with BJT



$i_B = 0$	$5V$
$i_B \geq i_{th}$	$0V$

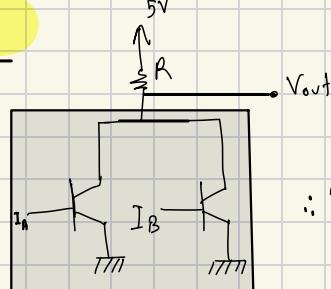
i_B	V_{out}
0	1
1	0

NAND



$$V_{out} = \overline{i_A i_B}$$

NOR



$$\therefore V_{out} = \overline{i_A + i_B}$$

BJT input নেয় current, but output দিয়ে voltage দেয় cascading করে logical operation করা যায় না।

OR voltage দিয়ে BJT কে control করতে base এর আঙুনে প্রক্টা resistance লাগানো হয়।

Diode OFF	Diode ON
$V_{in} \rightarrow i_B R_B$ $\therefore i_B = 0$	$V_{in} \rightarrow i_B R_B$ $\therefore V_{in} = i_B R_B + 0.7$
$V_{in} < 0.7$ $\therefore i_B = 0$	$V_{in} - 0 = i_B R_B + 0.7$ $\Rightarrow V_{in} = i_B R_B + 0.7$ $\therefore V_{th} = i_{th} R_B + 0.7$

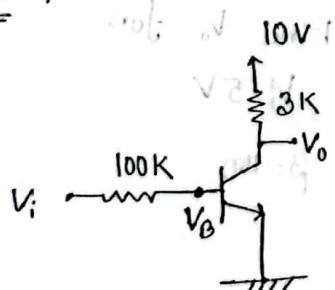
Method of Assumed State:

- ① Assume -
- Active $[V_{BE} = 0.7V, I_c = \beta I_B]$
 - Saturation $[V_{BE} = 0.8V, V_{CE} = 0.2V]$
 - Cutoff $[I_B = I_c = I_F = 0]$

- ② Solve [KCL, KVL, Nodal]

- ③ Verify -
- Active $[V_{CE} > 0.2V]$
 - Saturation $[I_c/I_B < \beta]$
 - Cutoff $[V_{BE} \leq 0.7V \text{ and } V_{BC} \leq 0.5V]$

① Example 1:



Find V_o for

$$V_i = 1V$$

$$\beta = 100$$

Assume: Active

$$\textcircled{1} \quad V_{BE} = 0.7V$$

$$\textcircled{2} \quad I_c = \beta I_B$$

$$\textcircled{3} \quad V_B = 0.7V$$

$$\Rightarrow V_B - V_E = 0.7V$$

$$\Rightarrow V_B - 0 = 0.7$$

$$\Rightarrow V_B = 0.7$$

$$I_B = \frac{V_i - V_B}{100}$$

$$= \frac{1 - 0.7}{100}$$

$$= \frac{0.3}{100}$$

$$= 0.003 \text{ mA}$$

$$I_c = \beta I_B$$

$$= 100 \times 0.003$$

$$= 0.3 \text{ mA}$$

$$I_C = \frac{10 - V_C}{3}$$

$$\Rightarrow 0.3 = \frac{10 - V_C}{3}$$

$$\Rightarrow V_C = 9.1 V$$

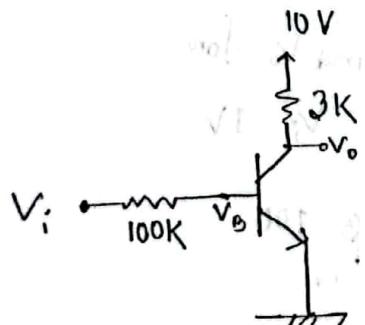
$$V_{CE} = V_C - V_E$$

$$= 9.1 - 0$$

$$= 9.1 V > 0.2$$

Assumption correct.

Example 2:



Find V_o for

$$V_i = 5V$$

$$\beta = 100$$

Assume Active

$$V_{BE} = 0.7V$$

$$I_C = \beta I_B$$

$$V_{BE} = 0.7V \quad I_B = \frac{V_i - V_B}{100}$$

$$\Rightarrow V_B - V_E = 0.7 \quad \Rightarrow I_B = \frac{5 - 0.7}{100}$$

$$\Rightarrow V_B = 0.7 \quad = 0.043 \text{ mA}$$

$$I_C = 100 \times I_B$$

$$= 100 \times 0.043$$

$$= 4.3 \text{ mA}$$

$$I_C = \frac{10 - V_C}{3}$$

$$\Rightarrow 4.3 = \frac{10 - V_C}{3}$$

$$\Rightarrow V_C = -2.9V$$

$$V_{CE} = V_C - V_E$$

$$= -2.9 - 0$$

$$= -2.9 \neq 0.2$$

Assumption wrong

Assume saturation

$$\textcircled{i} V_{BE} = 0.8V$$

$$\textcircled{ii} V_{CE} = 0.2V$$

$$V_{BE} = V_B - V_E \quad ; \quad I_B = \frac{5 - 0.8}{100} = 0.042 \text{ mA}$$

$$\Rightarrow 0.8 = V_B - 0$$

$$\Rightarrow V_B = 0.8$$

$$V_{CE} = V_C - V_E \quad ; \quad \Rightarrow 0.2 = V_C - 0$$

$$\Rightarrow V_C = 0.2V$$

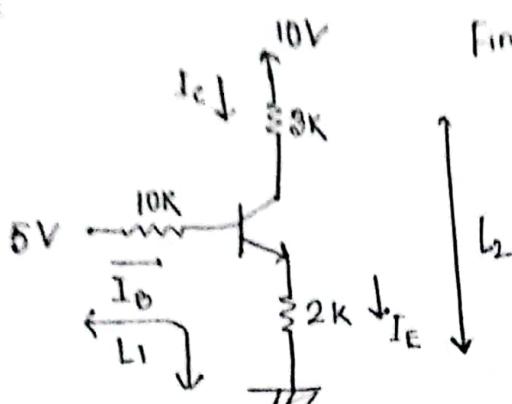
$$\frac{I_C}{I_B} = \frac{3.29}{0.042} = 78.33 < \beta$$

$$\boxed{V_B = 0.2V}$$

Assumption correct.



Example 3:



Find I_B , I_E , I_F , V_{CE}

① Assume Active.

$$V_{BE} = 0.7V$$

$$I_C = \beta I_B \sim I_E = \alpha I_E, \quad \alpha = \frac{\beta}{1+\beta}$$

$$\cancel{I_C = \frac{\beta}{\alpha} I_B} \quad I = \frac{\beta}{\alpha} \frac{I_B}{I_E} \Rightarrow I_E = \frac{\beta}{\alpha} I_B$$

$$5 - 0 = 10I_B + V_{BE} + 2I_E$$

$$\Rightarrow 5 = 10I_B + 0.7 + 2 \times \frac{\beta}{\alpha} I_B$$

$$\Rightarrow 5 = 10I_B + 0.7 + 2 \times \frac{\beta}{\alpha + \beta} I_B$$

$$\Rightarrow 5 = 10I_B + 0.7 + 2 \times (1 + \beta) I_B$$

$$\Rightarrow 5 = 10I_B + 0.7 + 2 \times (1 + 100) I_B$$

$$\therefore I_B = 0.02 \text{ mA}$$

$$I_C = \beta I_B$$

$$= 100 \times 0.02$$

$$= 2 \text{ mA}$$

$$I_F = I_B + I_C$$

$$= 0.02 + 2$$

$$= 2.02 \text{ mA}$$

$$I_E = \frac{V_T - 0}{2}$$

$$\Rightarrow V_T = 2 \times 2.02 = 4.04V$$

$$V_{CE} = V_C - V_E$$

$$= 4 - 0.04 = 3.96V$$

$$-0.04V > 0.2V$$

$$I_C = \frac{10 - V_C}{3}$$

Wrong assumption.

$$\Rightarrow I_C = \frac{10 - V_C}{3}$$

$$\Rightarrow V_C = 4V$$

Assume saturation.

$$\textcircled{1} \quad V_{BE} = 0.8V$$

$$\textcircled{2} \quad V_{CE} = 0.2V$$

$$I_E = I_C + I_B$$

KVL L1:

$$5 - 0 = 10I_B + 0.8 + 2I_E \quad \text{--- (1)}$$

$$I_B = 0.03 \text{ mA}$$

$$I_C = 1.95 \text{ mA}$$

KVL L2:

$$10 - 0 = 3I_C + 0.2 + 2I_E \quad \text{--- (2)}$$

$$I_E = 1.98 \text{ mA}$$

$$I_E = I_C + I_B \quad \text{--- (3)}$$

$$\frac{I_C}{I_B} = \frac{1.95}{0.03}$$

$$= 65 < \beta$$

Assumption correct.