中山大学软件学院软件工程专业 **2009** 级 (2010 学年秋季学期)

《SE-211 Digital Circuits and Logic Design》 期末试题

(A 卷)

(考试形式：闭　卷　　考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____　　姓名：_____　　学号：_____

1. Multiple choice questions (2 points for each question, 20 points total).

(1) If the period of a clock signal is 500 ps, the frequency is
- **a. 20 MHz**
- **b. 200 MHz**
- **c. 2 GHz**
- **d. 20 GHz**

(2) The time measurement between the 90% point on the trailing edge of a pulse to the 10% point on the trailing edge of the pulse is called the
- **a. rise time**
- **b. fall time**
- **c. period**
- **d. pulse width**

(3) When two positive signed numbers are added, the result may be larger than the size of the original numbers, creating overflow. This condition is indicated by
- **a. a change in the sign bit**
- **b. a carry out of the sign position**
- **c. a zero result**
- **d. smoke**

(4) Assume that a floating point number is represented in binary. If the sign bit is 1, the
- **a. number is negative**
- **b. number is positive**
- **c. exponent is negative**
- **d. exponent is positive**

(5) A Boolean expression that is in standard SOP form is
- **a. the minimum logic expression**
- **b. contains only one product term**

c. has every variable in the domain in every term

d. none of the above

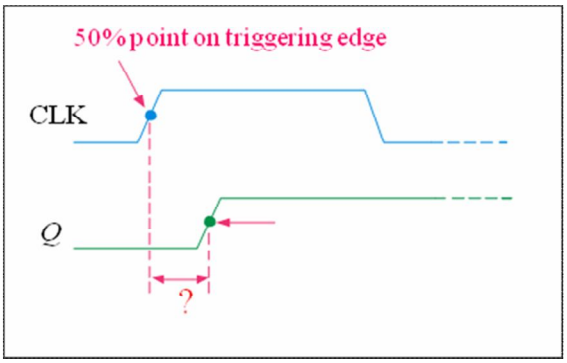
(6) The time interval illustrated is called

a. t_{PHL}

b. t_{PLH}

c. set-up time

d. hold time



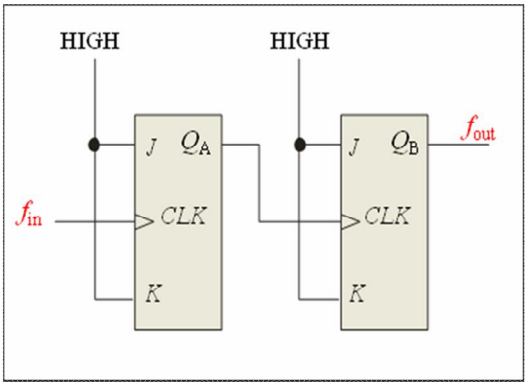
(7) The application illustrated is a

a. astable multivibrator

b. data storage device

c. frequency multiplier

d. frequency divider



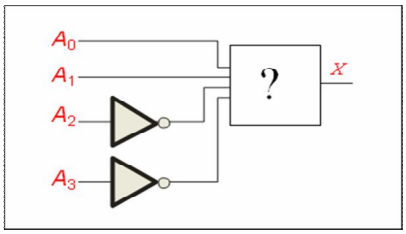
(8) Assume you want to decode the binary number 0011 with an active-HIGH decoder. The missing gate should be

a. an AND gate

b. an OR gate

c. a NAND gate

d. a NOR gate



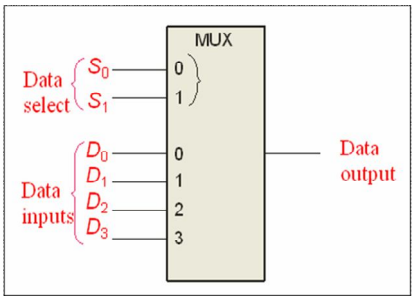
(9) If the data select lines of the MUX are $S_1S_0 = 11$, the output will be

a. LOW

b. HIGH

c. equal to D_0

d. equal to D_3



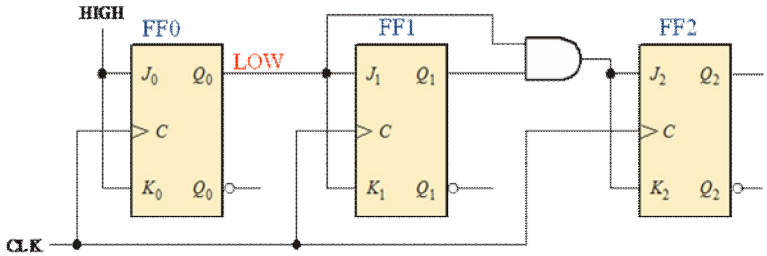
(10)Assume Q_0 is LOW. The next clock pulse will cause

a. FF1 and FF2 to both toggle

b. FF1 and FF2 to both latch

c. FF1 to latch; FF2 to toggle

d. FF1 to toggle; FF2 to latch



2. Please solve the following number conversion problems (total 15 points)

(1) Convert binary number 10111000.10101 to decimal (2 points)

(2) Convert decimal number 100.625 to binary (2 points)

(3) Express decimal number -85 as 8-bit number in 1's complement form (2 points)

(4) Express decimal number -85 as 8-bit number in 2's complement form (2 points)

(5) Convert decimal number 126 to (3 points)

(a) Hexadecimal number

(b) Octal number

(c) 8421 BCD number

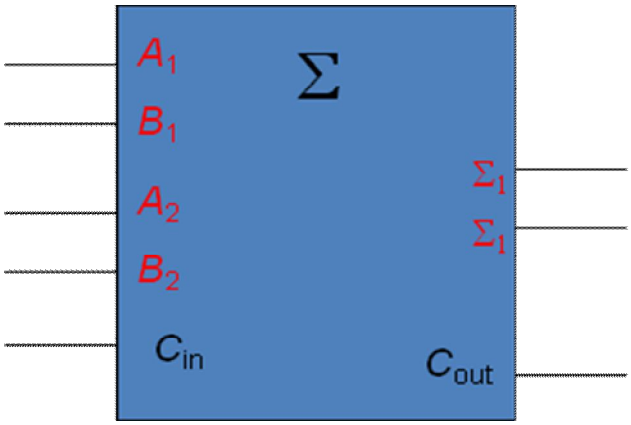
(6) Convert the decimal number 3.248 x 10^4 to a single-precision floating point binary number. Please show your procedure (4 points)

3. **We need to design a circuit with 4 inputs(marked as A, B,C,D) and 2 outputs X, Y. Based on system analysis, we should have true table as shown in the following (total 20 points):**

A	B	C	D	*X*	*Y*
0	0	0	0	*0*	*1*
0	0	0	1	*1*	*0*
0	0	1	0	*1*	*1*
0	0	1	1	*1*	*0*
0	1	0	0	*0*	*1*
0	1	0	1	*1*	*0*
0	1	1	0	*1*	*1*
0	1	1	1	*1*	*0*
1	0	0	0	*0*	*1*
1	0	0	1	*1*	*0*
1	0	1	0	*1*	*1*
1	0	1	1	*1*	*1*
1	1	0	0	*1*	*1*
1	1	0	1	*1*	*1*
1	1	1	0	*0*	*1*
1	1	1	1	*1*	*1*

(1) Express the above circuit's outputs in minimum Sum-of-Product (SOP) form (4 points)
(2) Show the implementation of the circuit in SOP form by using only AND, OR, or NOT gates (3 points)
(3) Show the implementation of the circuit in SOP form by using only NAND gates (3 points)
(4) Express the above circuit's outputs in minimum Product-of-Sum (POS) form (4 points)
(5) Show the implementation of the circuit in POS form by using only AND, OR, or NOT gates (3 points)
(6) Show the implementation of the circuit in POS form by using only NOR gates (3 points)

4. **Design a 2-bit look-ahead-carry full adder using only basic logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR). (total 15 points)**



5. **Design a Moore FSM to detect a bit sequence 11001. If such sequence is found, output will**

be set to 1, otherwise, output will be set to 0. Overlap sequence, if exists, should be detected. Please use J-K flip flop for the system. (total 30 points).

(1) Derive state diagram (4 points)

(2) Encode states (state assignment) (2 points)

(3) Create state-assigned state table (4 points)

(4) Express J-K Flip-Flop excite table to use (3 points)

(5) Determine minimum Flip-Flop input equations and FSM output equation(s) (8 points)

(6) Verify that there is no state that will stay outside the FSM for ever (2 points)

(7) Draw circuit diagram (7 points)