中山大学软件学院 **2010** 级软件工程专业 (2011 学年秋季学期)

《SE-211 Digital Circuits and Logic Design》 期末试题

(A 卷)

(考试形式：闭卷　　考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____　　姓名：_____　　学号：_____

1. MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question. (2 points for each question, 20 points total).

1) The expression $AB+(A\oplus B)\cdot C_{in}$ represents _____.

A. The carry output of a half-adder
B. The summing output of a half-adder
C. The summing output of a full-adder
D. The carry output of a full-adder

2) This is the truth table for a(n) _____.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

A. NAND gate　　B. AND gate　　C. OR gate　　D. NOR gate

3) What is the duty cycle of a digital pulse train where the pulse width is 10ms and the period of the waveform is 90 ms? _____

A. 10%　　B. 9%　　C. 90%　　D. 11.1%

4) Which converts data from a serial to a parallel form? _____

A. Comparator　　B. Encoder　　C. Demultiplexer　　D. Multiplexer

5) Which statement below best describes a Karnaugh map? _____

A. The Karnaugh map eliminates the need for using NAND and NOR gates.
B. A Karnaugh map can be used to replace Boolean rules.
C. Variable complements can be eliminated by using Karnaugh maps
D. Karnaugh maps provide a cookbook approach to simplifying Boolean expressions.

6) What type of logic circuit is shown in Fig.1.6, and what logic function is being performed?___

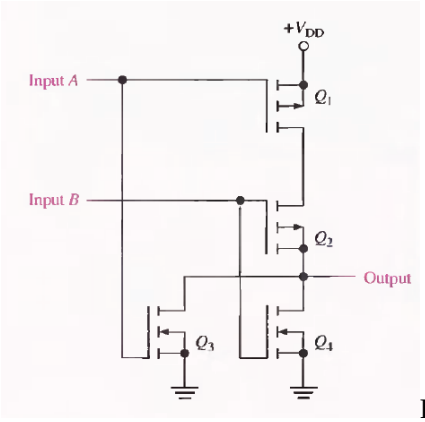


Figure 1-6

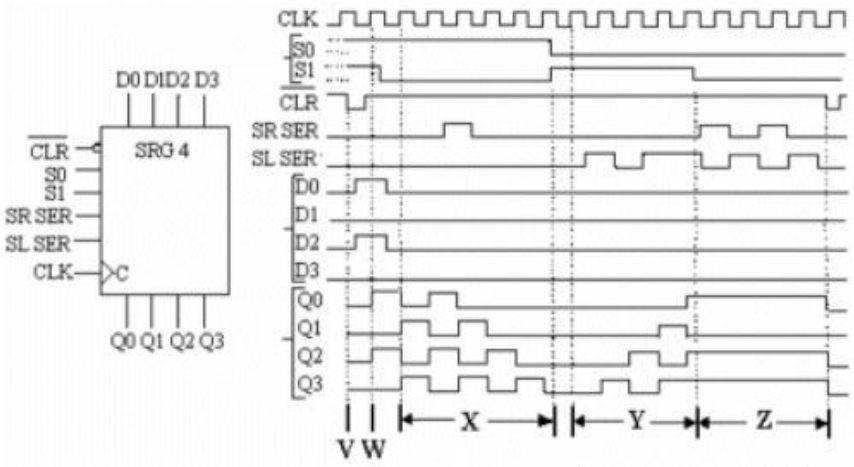
A. It is a PMOS NOR gate
B. It is a COMS AND gate
C…It is a CMOS NOR gate
D. It is a NMOS AND gate

7) A FIFO _____

A. Allows data to be clocked in and out at different clock rates.
B. Can be used to smooth out bursts of data into a continuous stream
C. Outputs the data in the same order that it was input
D. All of the above

8) Which one of the following is made up of flip-flops? _____

A. Multiplexer B. Converter C. Register D. Comparator



INPUTS									OUTPUTS			
CLEAR	MODE		CLK	SERIAL		PARALLEL						
	S1	S0		LEFT	RIGHT	D0	D1	D2	D3	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDN	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

Fig. 1-10

9) A logic gate draws 10mA when its output is HIGH and 20mA when its output is LOW. When operating from a 12V supply with a 10% duty cycle the average power dissipation will be ___

A. 189mW B. 228mW C. 324mW D. 360mW

10) What type of device is shown in Fig.1-10? _____

A. 2-bit serial-in 4-bit parallel-out bidirectional shift register.

B. Paralle-in parallel-out shift register with bidirectional data flow.

C. 4-bit bidirectional universal shift register.

D. 2-way parallel-in serial-out bidirectional register.

2. Generate a Boolean expression for the circuit shown in Fig. 2 and reduce. (10 points)

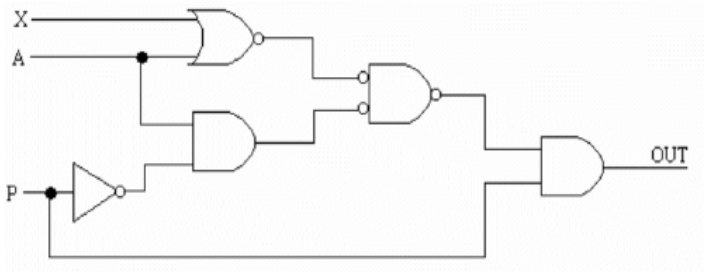


Fig. 2

3. Design the logic to control the temperature in a tank. The temperature must stay between 72 degrees and 80 degrees. If the temperature is below 72 degrees, a heater must be activated. If the temperature is above 80 degrees, a cooler must be started. There are 2 sensors. One outputs a high if the temperature is below 72 degrees and one outputs a high if the temperature is above 80 degrees. These sensors are prone to failure so the design must be able to detect both sensors are on at the same time. If that happens, the circuit must turn off the heater, turn off the cooler, and set an alarm for maintenance. (10 points)

4. 74HC153 has two identical 4-input multiplexers. Information on the data inputs of each multiplexer is selected by the address on the A_1 and A_0 inputs, and is presented on the Y outputs. For one multiplexer within 74HC153, denote D_0 to D_3 as the data-inputs, $\overline{S}$ the output enable input, and Y the output. What is the logic relationship between output and inputs? Please implement the following logic with one half of 74HC153 (see Fig. 4) and a NOT gate. (12 points)

$Z = \overline{R}\overline{A}\overline{G} + \overline{R}AG + R\overline{A}G + RA\overline{G} + RAG$

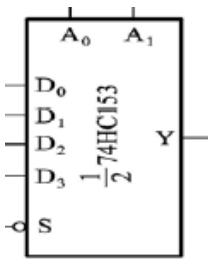


Fig. 4

RAM

Fig. 5

5. Use 128×8 RAMs and a 2-line-to-4-line decoder to implement a 512×8 memory. Please provide the design diagram. See Fig.5 for the logic diagram of a 128×8 RAM. (10 points)

6. Develop a modulus-12 counter with 74LS161. The counter is required to go through the following sequence: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 0, 1, …
   (1) Use the Asynchronous Reset mode;
   (2) Use the Synchronous Load mode. (18 points in total)

Table 6. Function table of 74LS161

Clear	Load	Enable		Clock	Input Data				Output				Mode
CLRN	LDN	ENT	ENP	CP	D	C	B	A	Q_D	Q_C	Q_B	Q_A	
0	×	×	×	×	×	×	×	×	0	0	0	0	Asynchronous Reset
1	0	×	×	↑	d	c	b	a	d	c	b	a	Synchronous Load
1	1	×	0	×	×	×	×	×	No change				Holding
1	1	0	×	×	×	×	×	×	No change				Holding
1	1	1	1	↑	×	×	×	×	Count UP				Counting

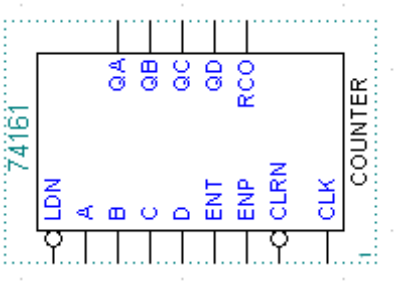


Fig. 6 Logic diagram of 74LS161

7. Develop a synchronous counter with positive-edge-triggered D flip-flops. Denote X as the input to control the counting mode. When X is LOW, the counter is a modulus-5 UP counter. If X is HIGH, the counter works as a modulus-7 UP counter. The detailed design procedure is required. (20 points)