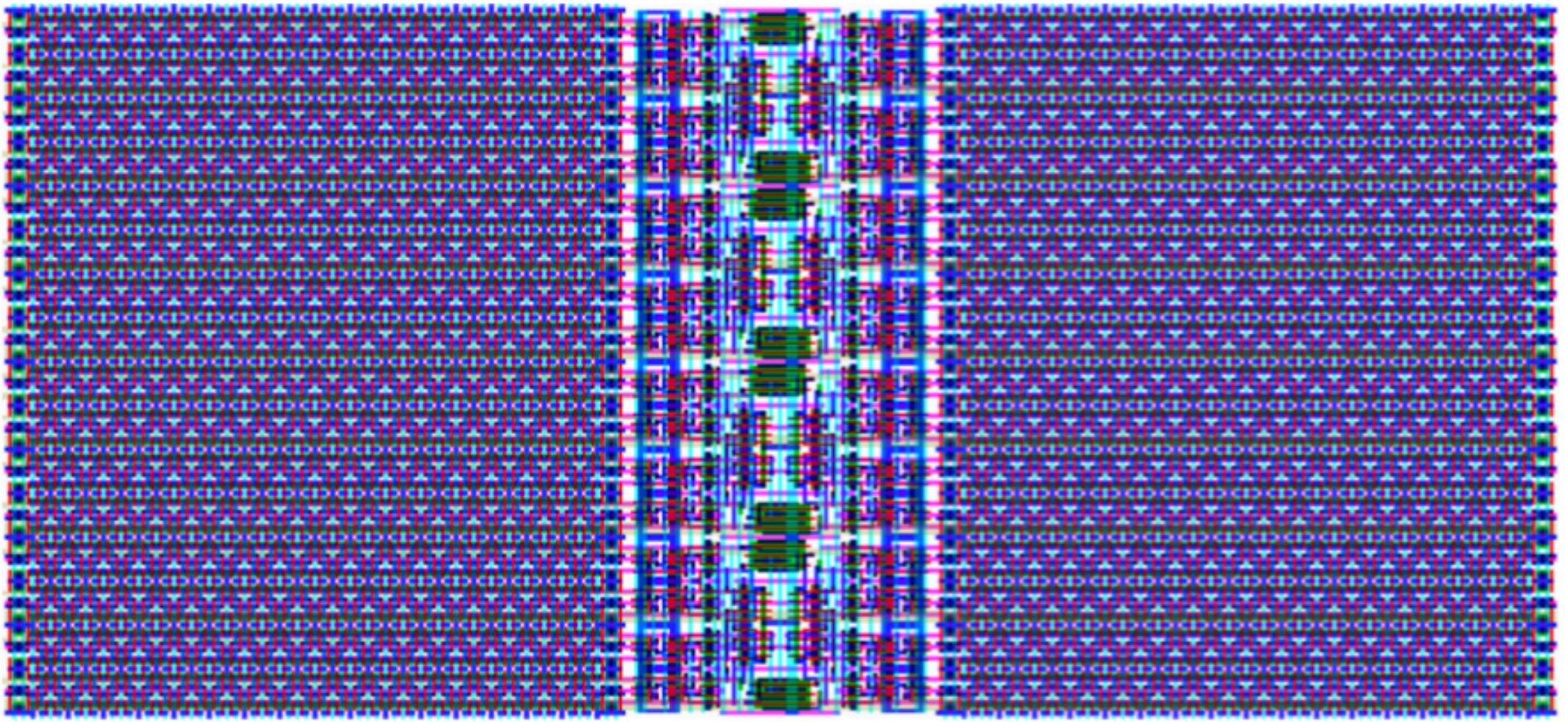
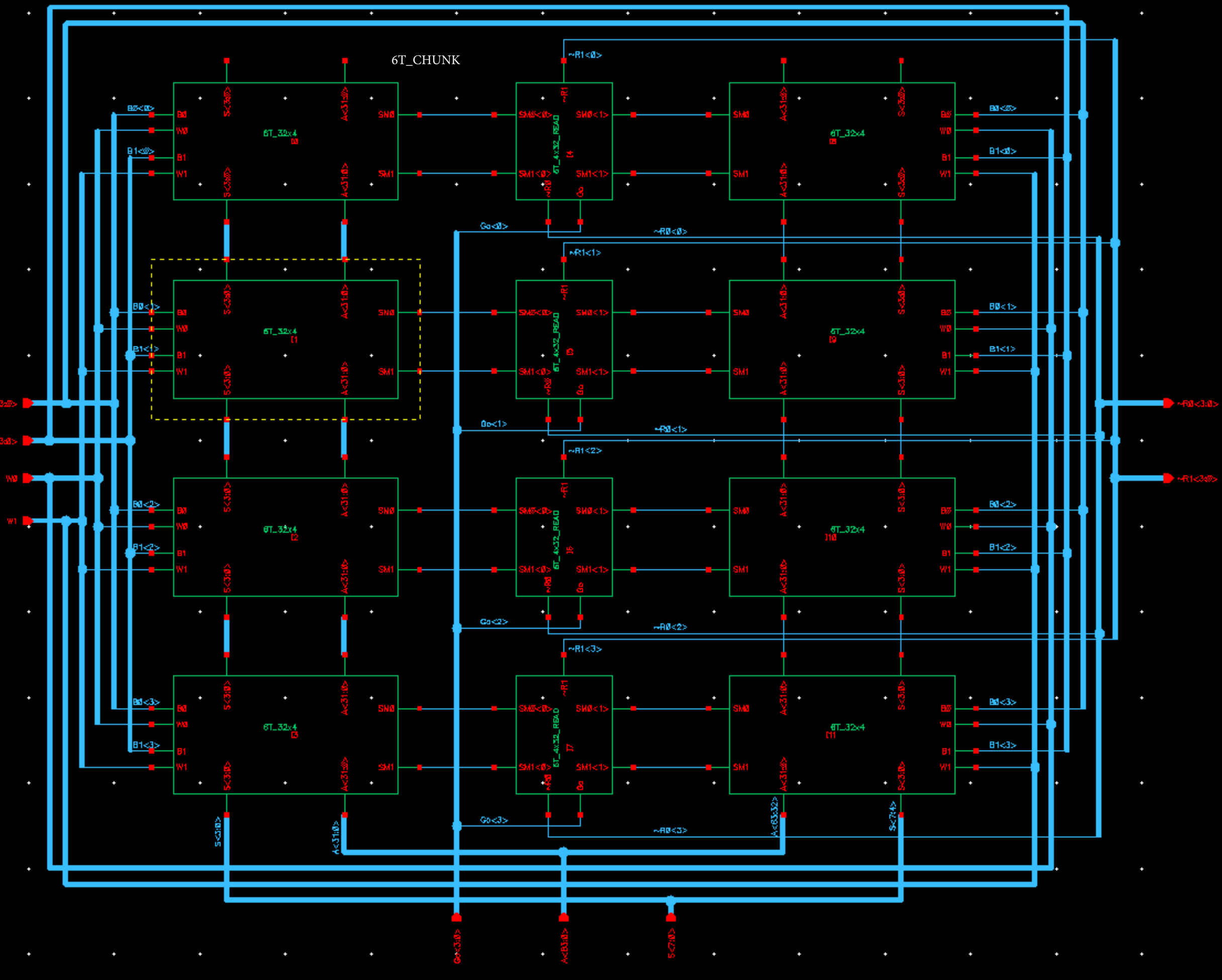
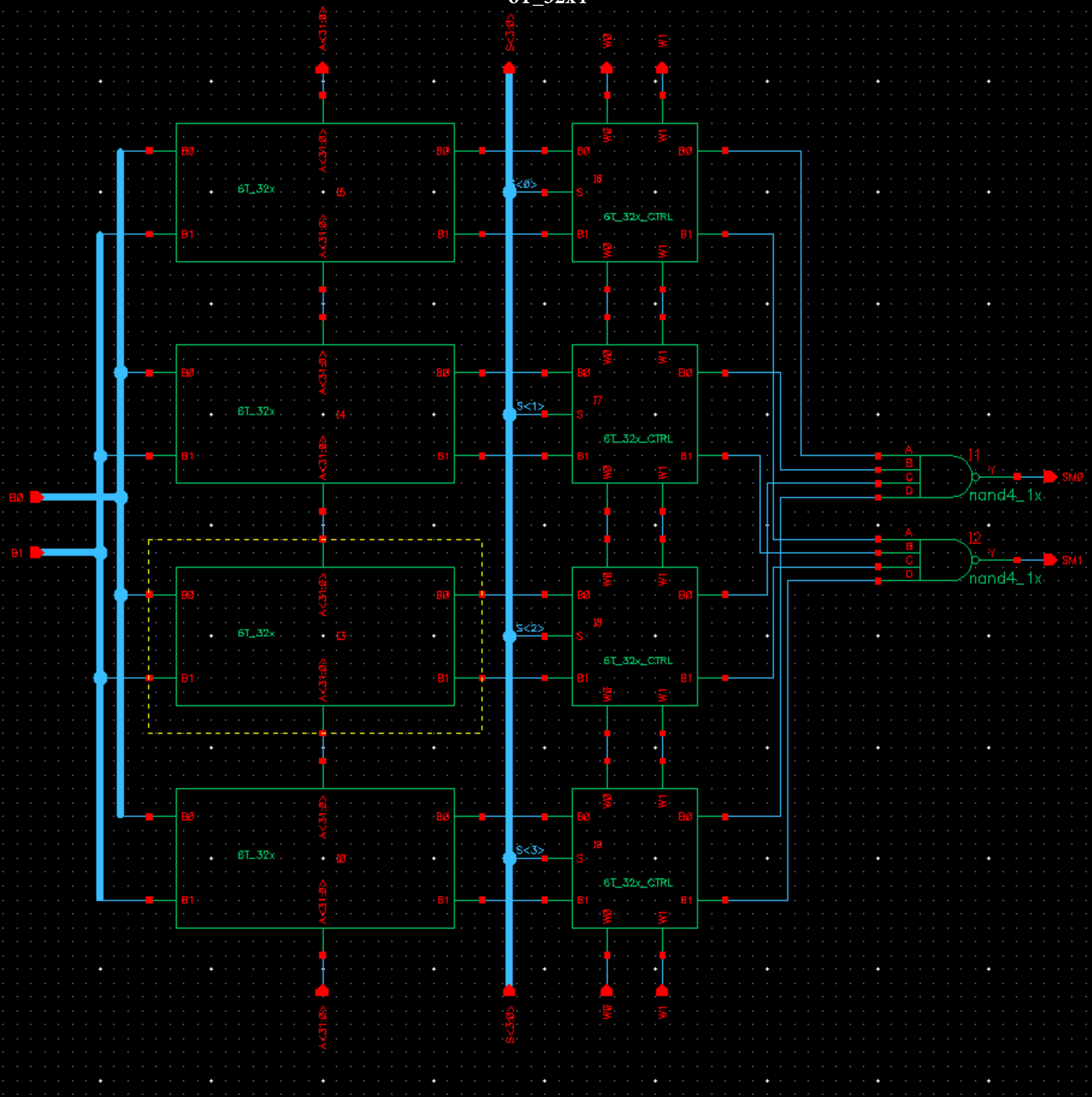
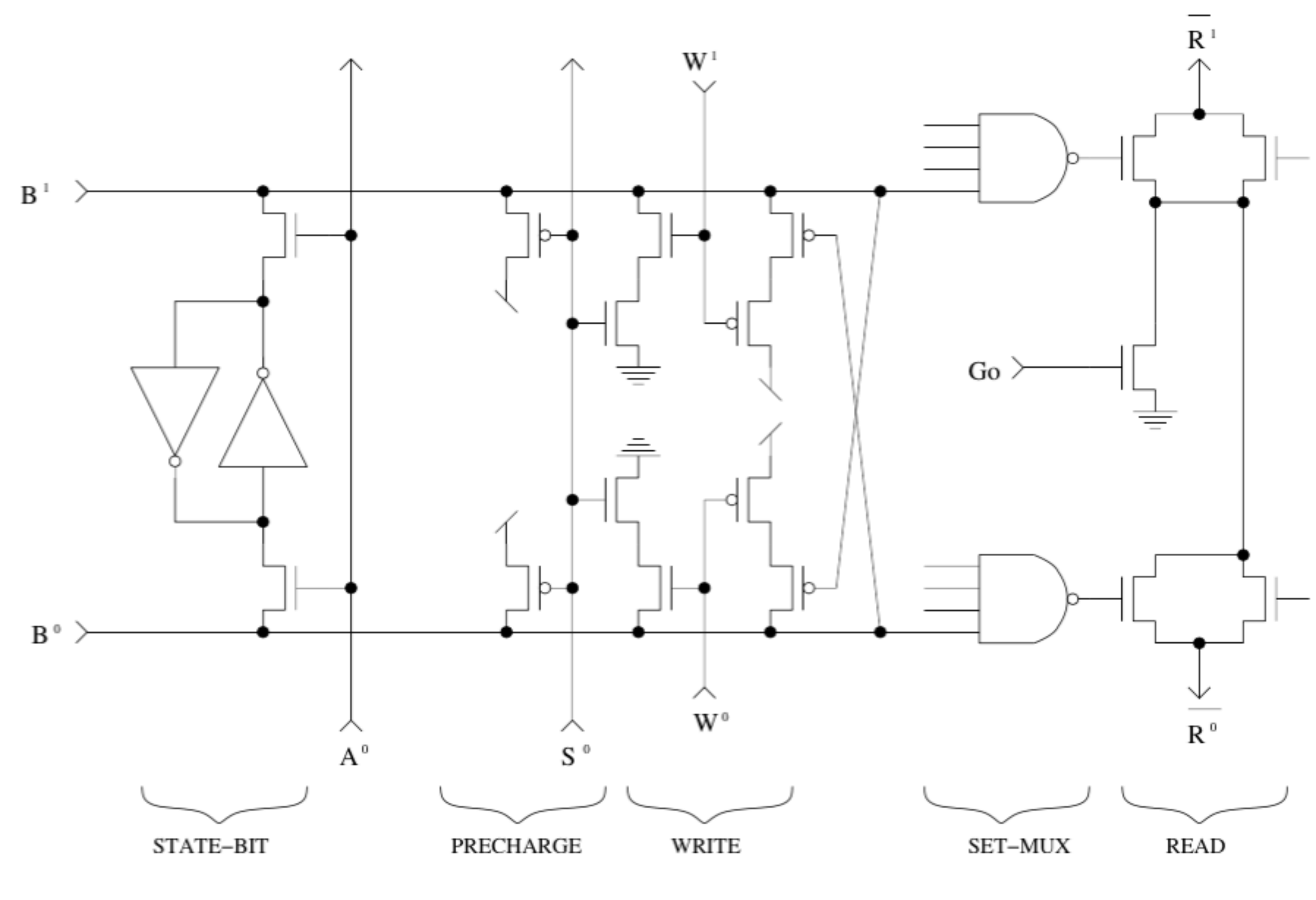


Fig. 5. First level of 6T SRAM hierarchy (CHUNK)

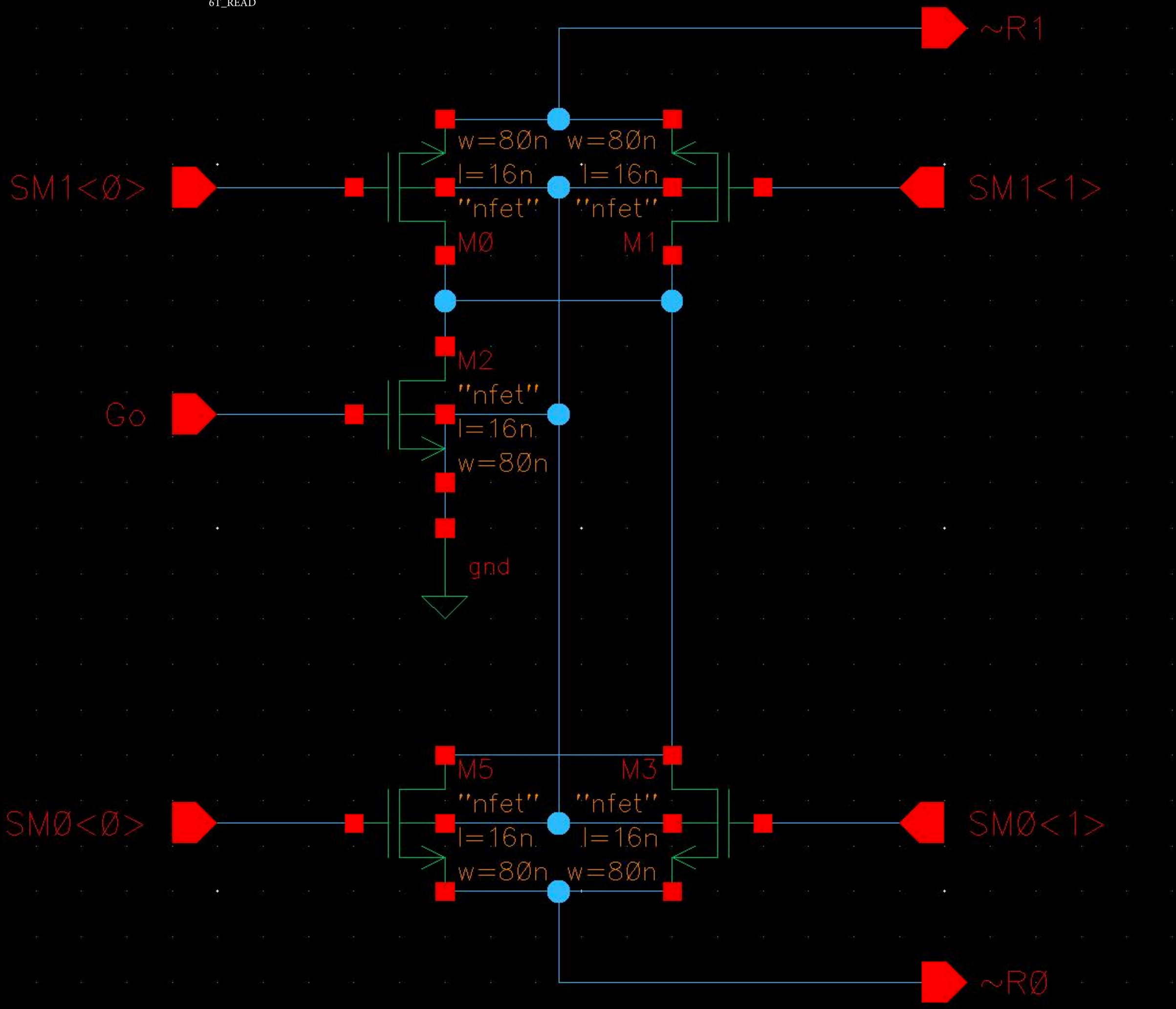

6T_CHUNK
6T_32x4
6T_4x32_READ
~R1<0>
~R0<0>
~R1<1>
~R0<1>
~R1<2>
~R0<2>
~R1<3>
~R0<3>
Go<0>
Go<1>
Go<2>
Go<3>
B0<0>
B1<0>
B0<1>
B1<1>
B0<2>
B1<2>
B0<3>
B1<3>
B0<3:0>
B1<3:0>
W0
W1
~R0<3:0>
~R1<3:0>
S<3:0>
A<31:0>
A<63:32>
S<7:4>
Go<3:0>
A<63:0>
S<7:0>
SN0
SM0<0>
SM0<1>
SM1
SM1<0>
SM1<1>
B0
B1
W0
W1

6T_32x4


A<31:0>
S<3:0>
W0
W1
B0
B1
6T_32x
6T_32x_CTRL
I6
I7
I8
I9
S<0>
S<1>
S<2>
S<3>
I1
I2
A
B
C
D
Y
nand4_1x
SM0
SM1


$\overline{R}^1$
W^1
B^1
Go
B^0
W^0
A^0
S^0
$\overline{R}^0$
STATE–BIT
PRECHARGE
WRITE
SET–MUX
READ

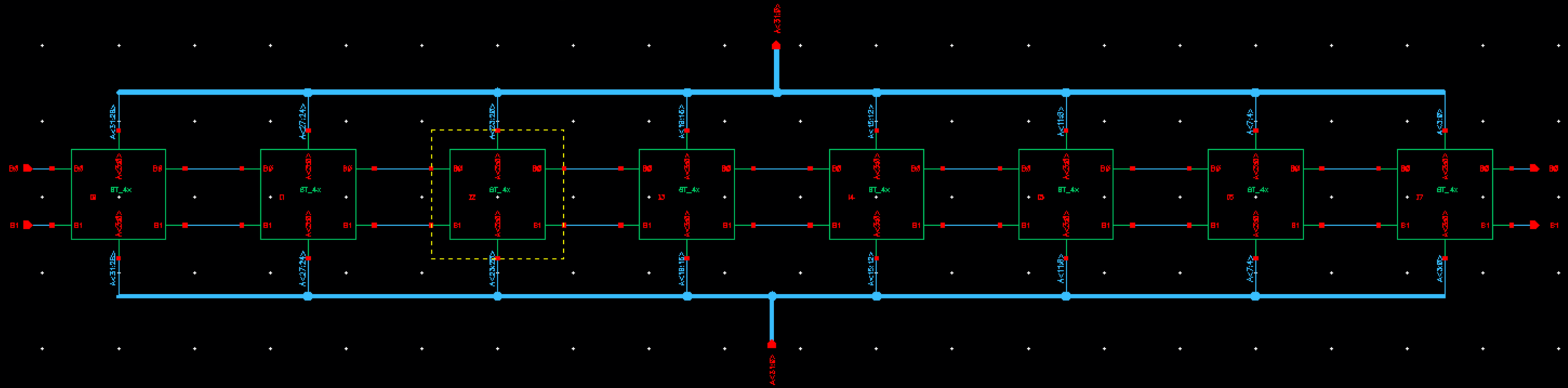
6T_READ


~R1
w=80n
w=80n
l=16n
l=16n
SM1<0>
"nfet"
"nfet"
SM1<1>
M0
M1
M2
"nfet"
Go
l=16n
w=80n
gnd
M5
M3
"nfet"
"nfet"
SM0<0>
l=16n
l=16n
SM0<1>
w=80n
w=80n
~R0

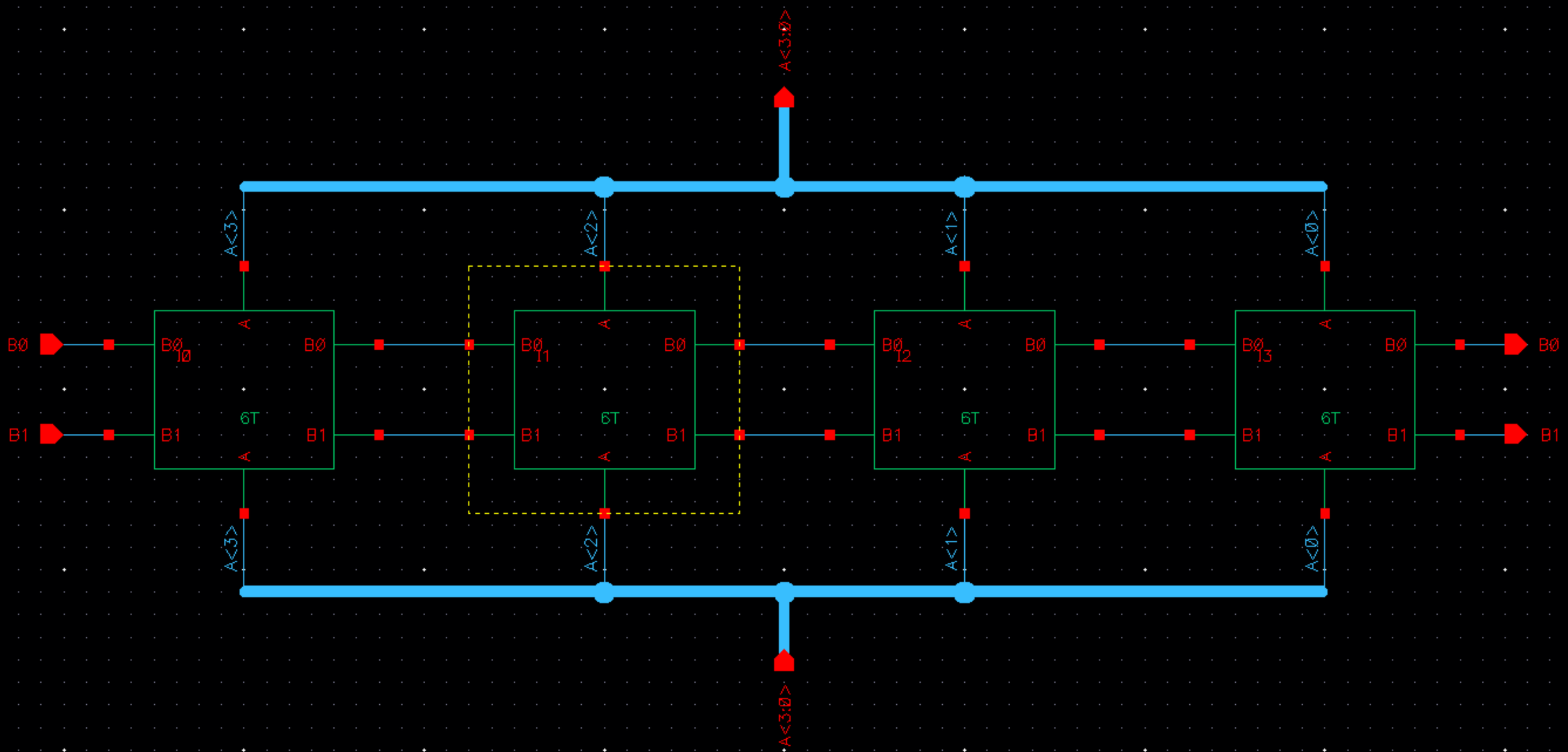
6T_32x4_CTRL

W1
B1
W1
B1
w=80n
l=16n
"pfet"
M2
M6
"nfet"
l=16n
w=40n
M5
"nfet"
l=16n
w=40n
w=80n
l=16n
"pfet"
M10
w=80n
l=16n
"pfet"
M9
vdd
gnd
vdd
w=40n
l=16n
"nfet"
M4
M7
"pfet"
l=16n
w=80n
M8
M0
"pfet"
l=16n
w=80n
w=40n
l=16n
"nfet"
M3
"pfet"
l=16n
w=80n
B0
B0
W0
S
W0

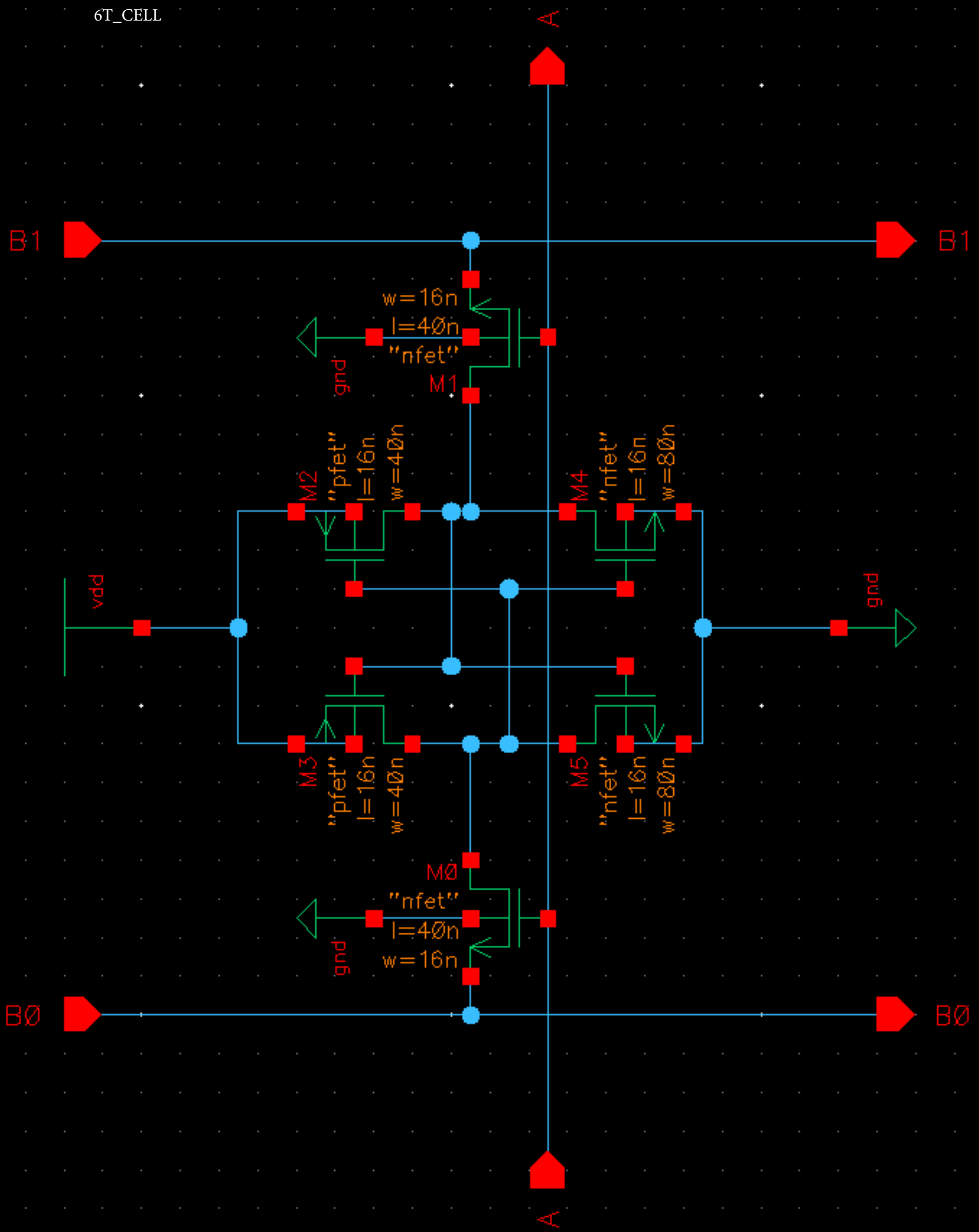
6T_32x


A<31:0>
A<31:28>
A<27:24>
A<23:20>
A<19:16>
A<15:12>
A<11:8>
A<7:4>
A<3:0>
B0
B1
BT_4x
I0
I1
I2
I3
I4
I5
I6
I7

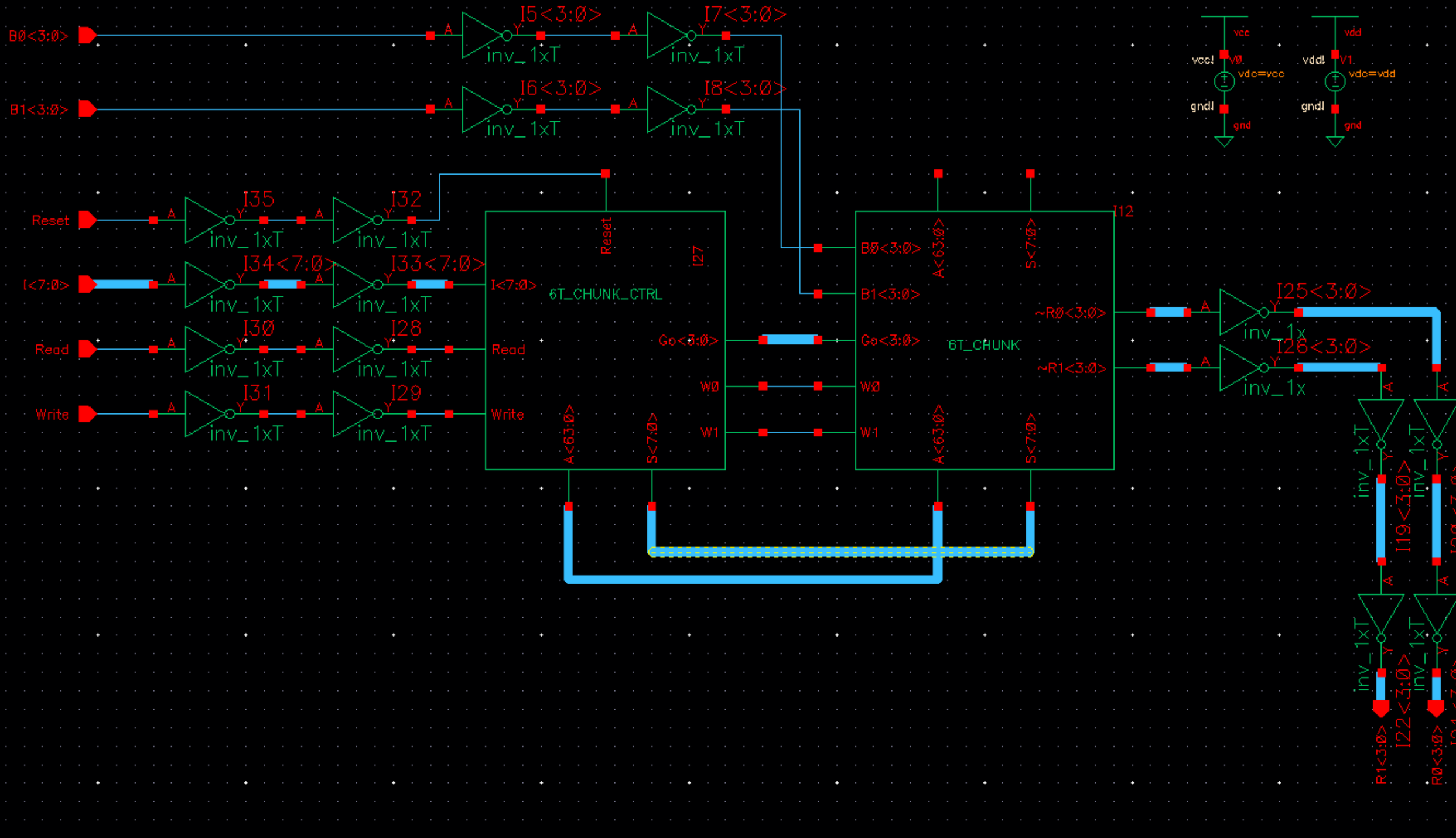
6T_4x



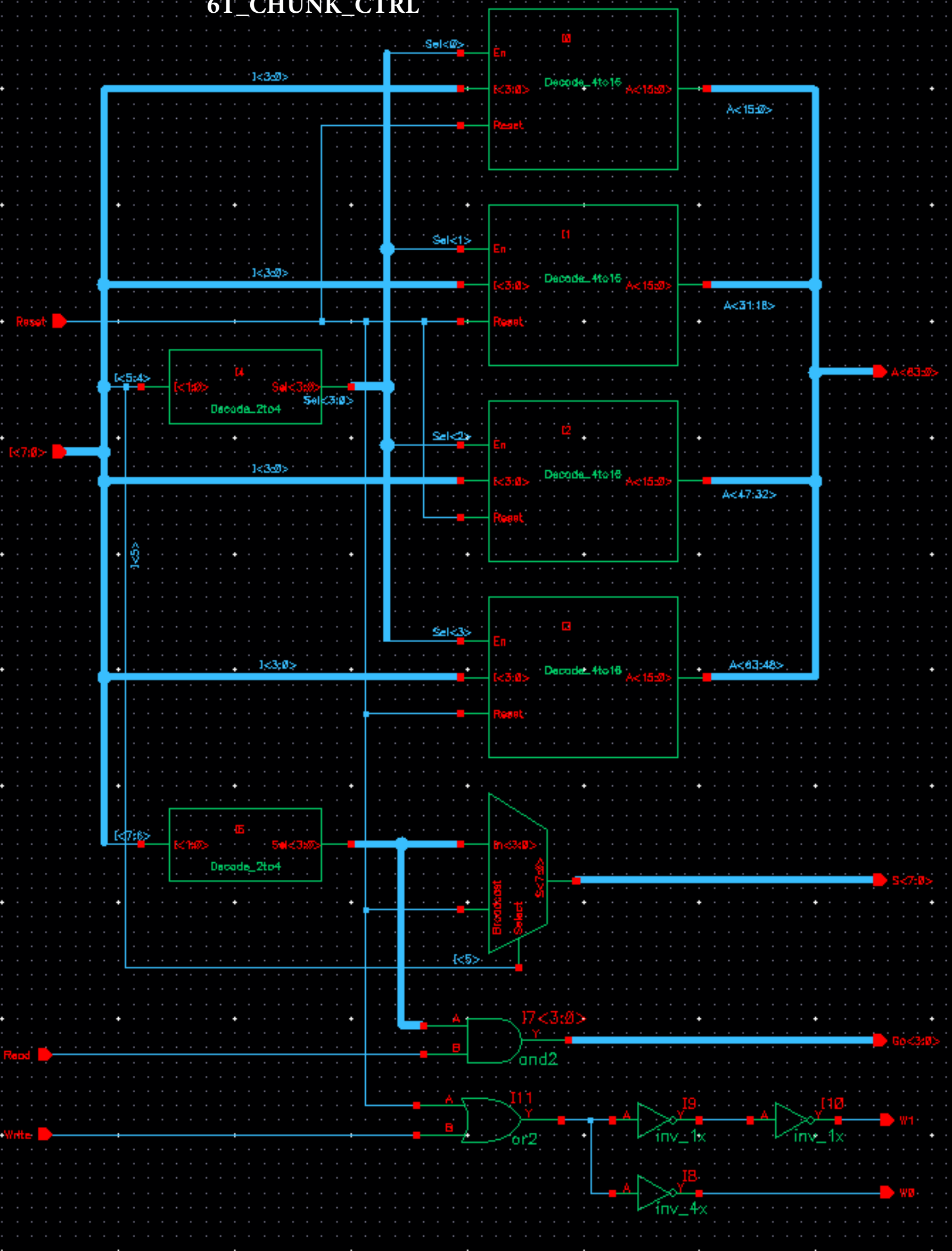
6T_CELL


A
B1
B1
w=16n
l=40n
"nfet"
M1
gnd
M2
"pfet"
l=16n
w=40n
M4
"nfet"
l=16n
w=80n
vdd
gnd
M3
"pfet"
l=16n
w=40n
M5
"nfet"
l=16n
w=80n
M0
"nfet"
l=40n
w=16n
gnd
B0
B0
A

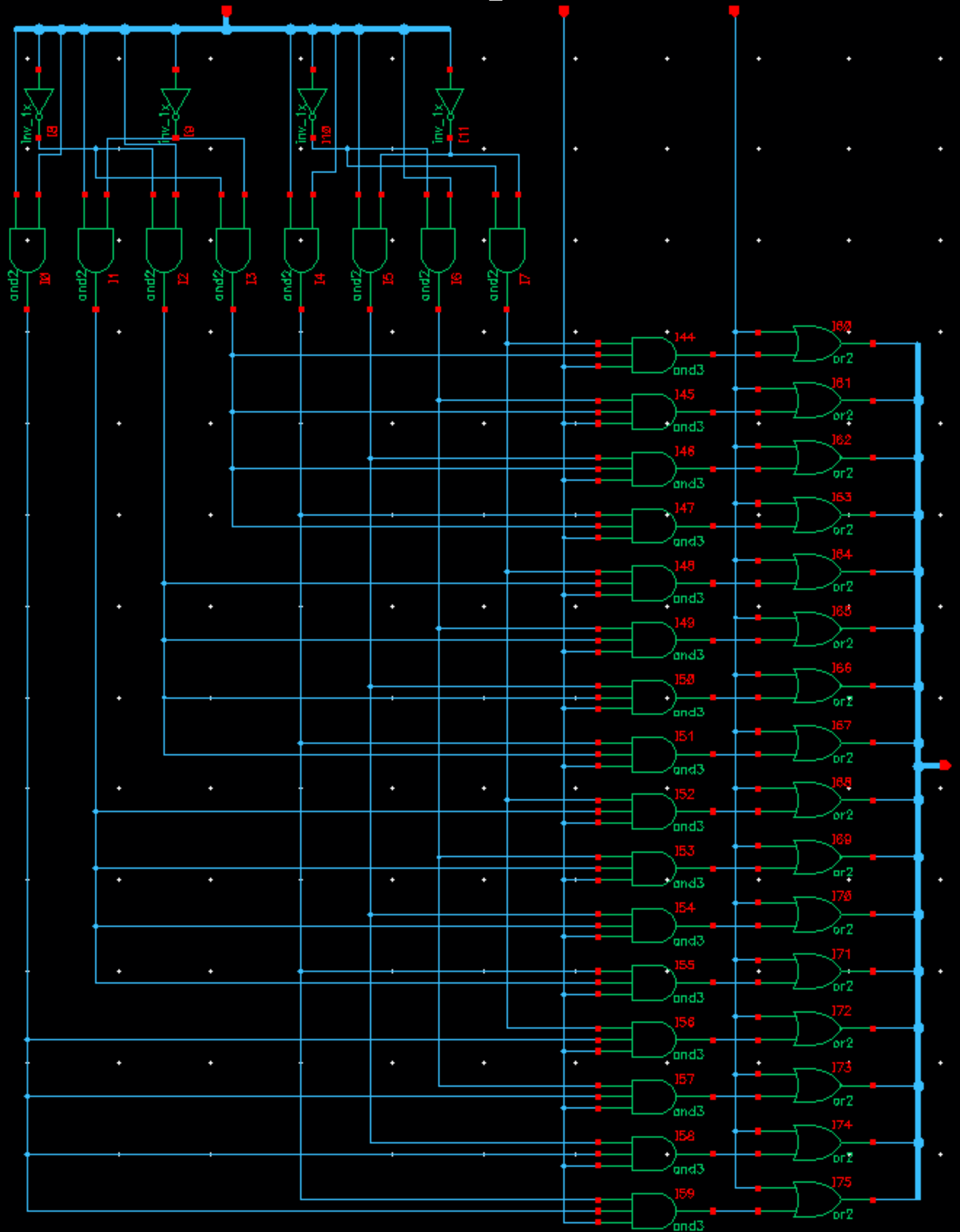
6T_Testbench



6T_CHUNK_CTRL



Decoder_4to16



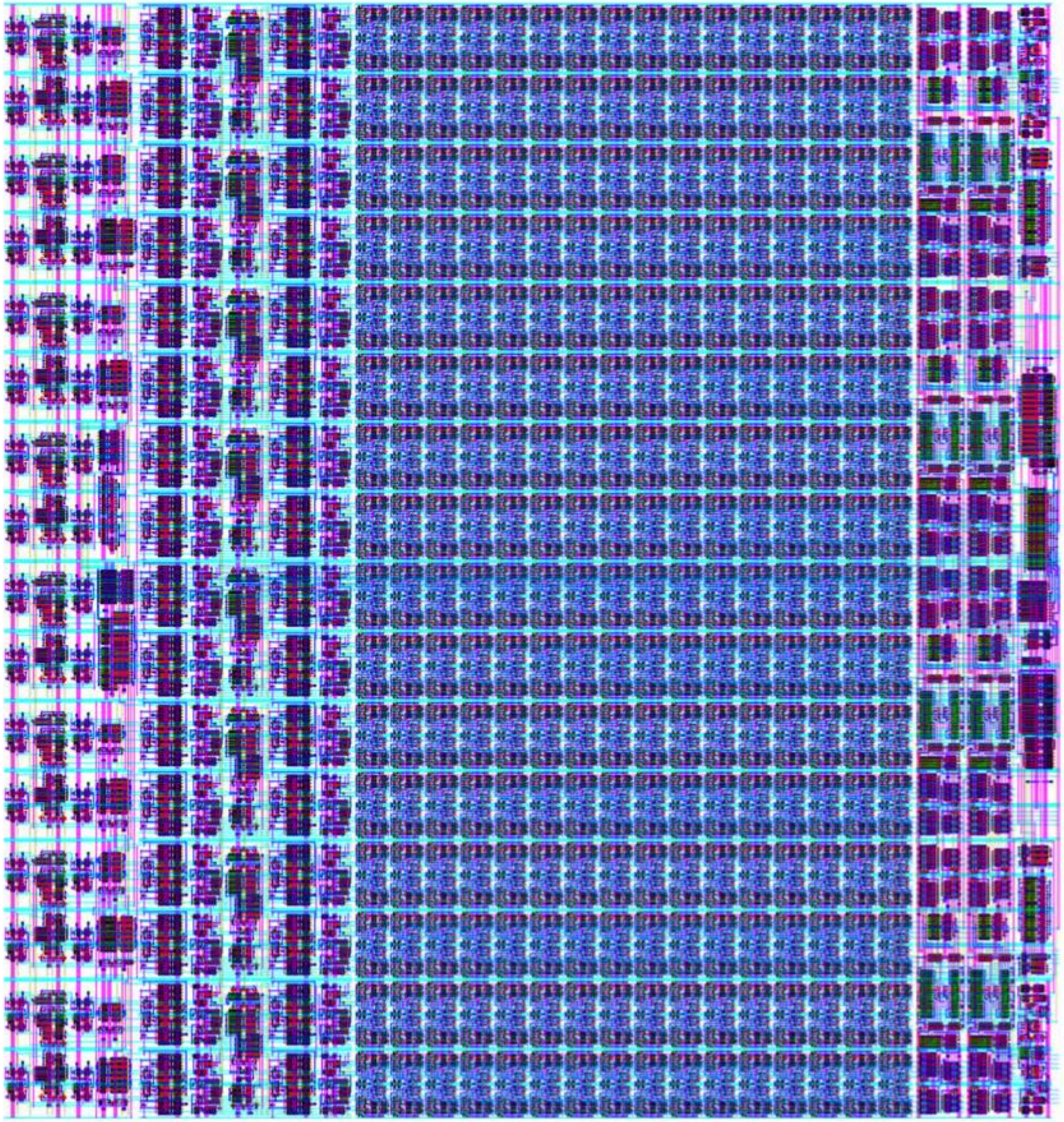
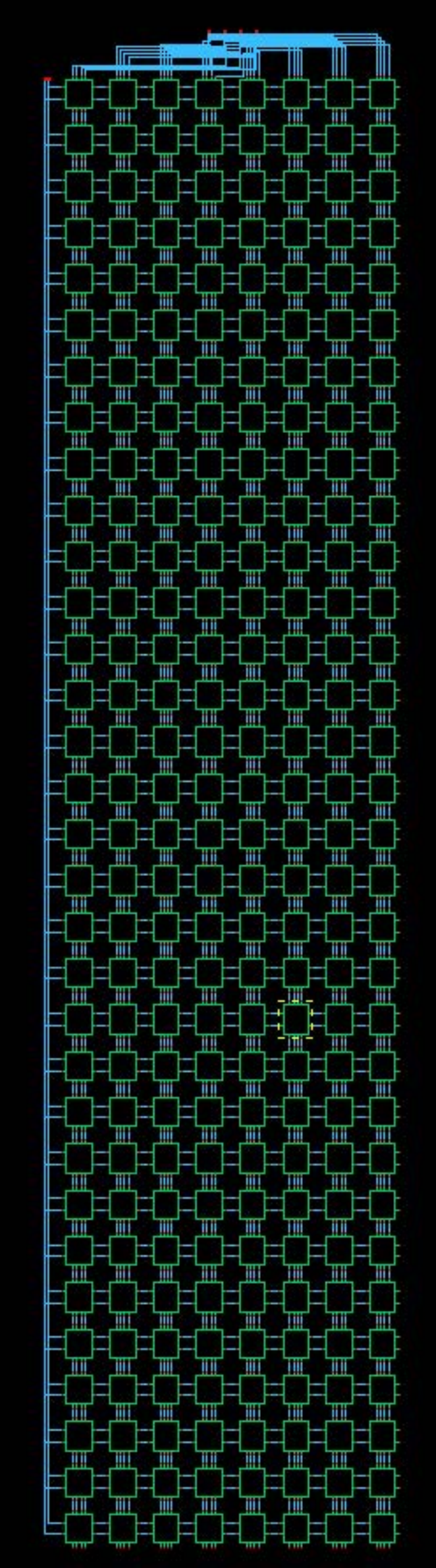


Fig. 3. Dual-ported Bit-maskable 32 by 32 bit 10T Register File



Schematic L Editing: 16nm 10T_32x schematic

Launch File Edit View Create Check Options Window Help

cadence

Basic

Search

Navigator

Default

Search

Name

JR<11>
JR<12>
JR<13>
JR<14>
JR<15>
JR<16>
JR<17>
JR<18>
JR<19>
JR<20>
JR<21>
JR<22>
JR<23>
JR<24>
JR<25>
JR<26>
JR<27>
JR<28>
JR<29>
JR<30>
JR<31:0>
JR<31>
JW<0>
JW<1>
JW<2>
JW<3>
JW<4>
JW<5>
JW<6>
JW<7>
JW<8>
JW<9>

Property Editor

~R0<31:28> ~R1<31:28> ~W0<31:28> ~W1<31:28> ~R0<27:24> ~R1<27:24> ~W0<27:24> ~W1<27:24> ~R0<23:20> ~R1<23:20> ~W0<23:20> ~W1<23:20> ~R0<19:16> ~R1<19:16> ~W0<19:16> ~W1<19:16> ~R0<15:12> ~R1<15:12>

JR JW ~R0<3:0> ~R1<3:0> ~W0<3:0> ~W1<3:0> 10T_4x I0 I1 I2 I3 I4 I8 I9 I70 I101 I132

mouse L: schSingleSelectPt()

M: schHiMousePopUp()

R: schHiMousePopUp()

1(2) >

Cmd: Sel: 0

[root@rob:~/Desktop] root@bull:~/Desktop/... virtuoso Cadence Library Mana... 10T_32x

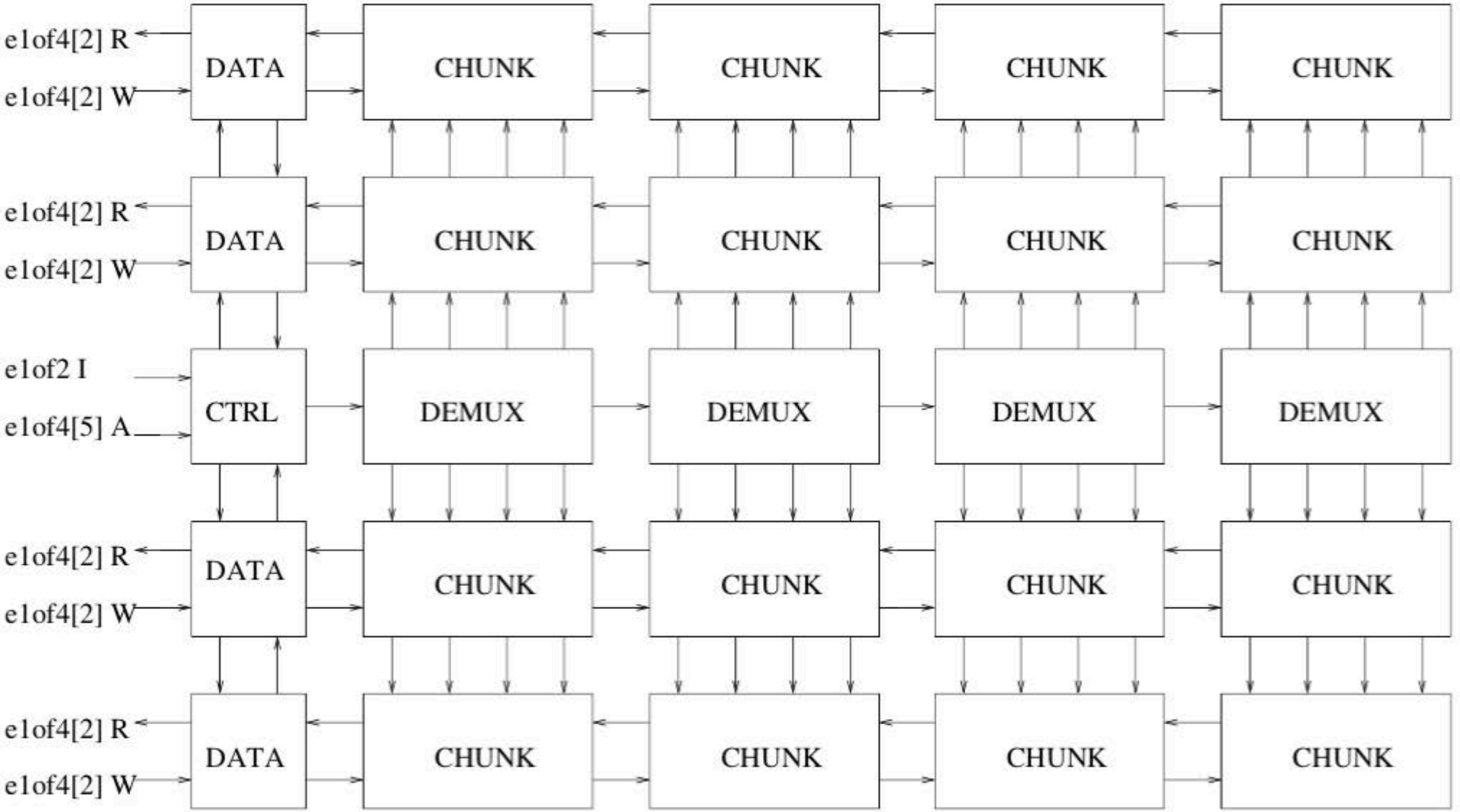


Fig. 6. 6T SRAM1024_16 bank structure

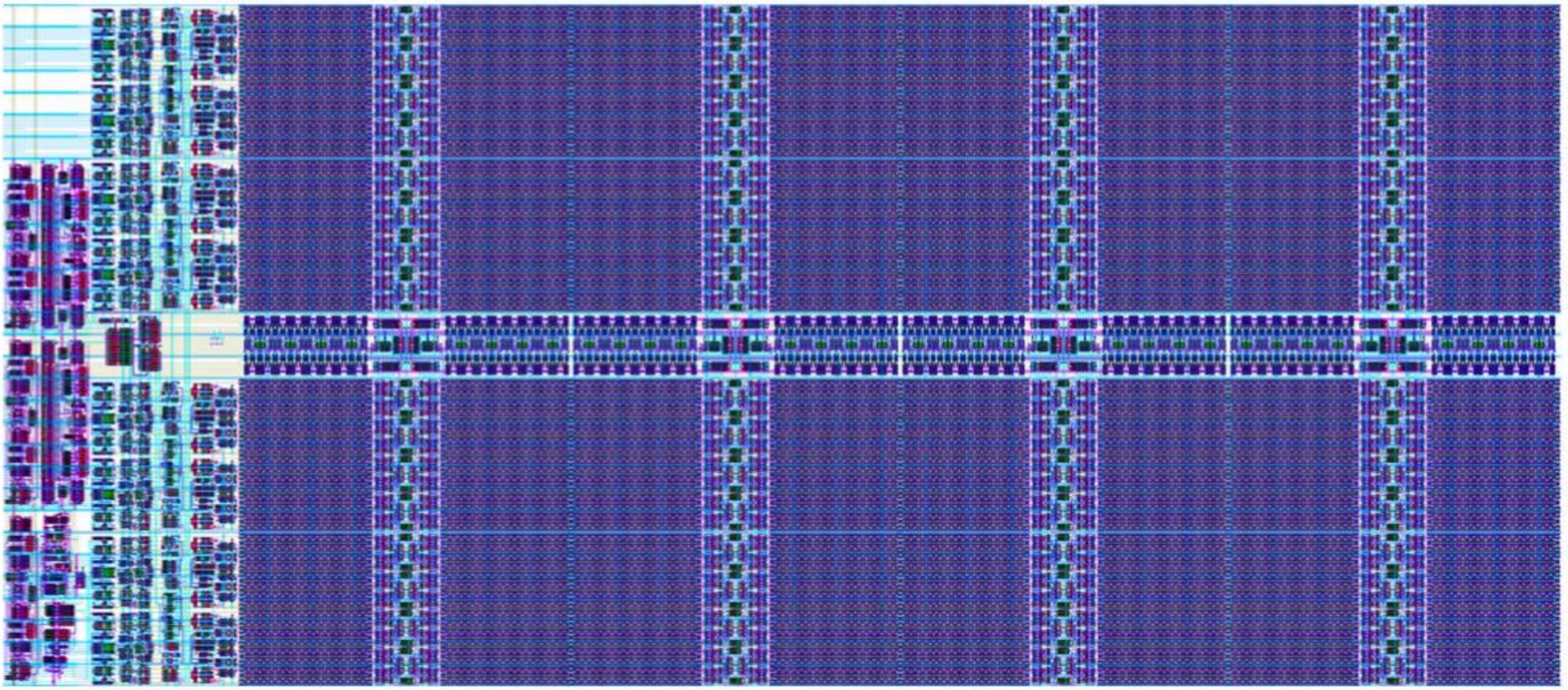


Fig. 7. Pipelined 1K by 16 bit SRAM bank