Research Overview

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Overview

- Part I: Foundations for Location Virtualization
- Part II: Foundations for Specification Evolution
- Part III: Semantic Type Assertions for Deferred Memory-Reclamation Schemes

Part I

Foundations for Location Virtualization

The Essentials in Systems Programming

a supposedly allocated physical resource

```
1    pointer va  :=  malloc (size)
```

a virtual reference

Memory Location Virtualization

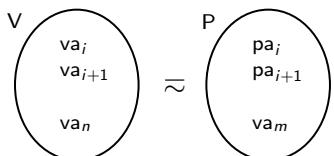


Figure: Virtualization: The Deception of Abundance

Memory Location Virtualization: Abstraction

An Address Space with Logical Name γ

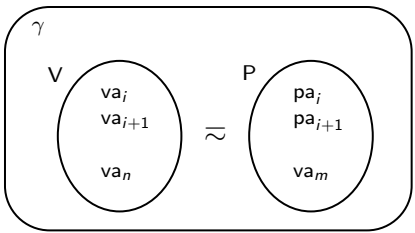


Figure: Address-Spaces: Named Containers for Virtual Memory Mappings

A Program Named γ_n

```
pointer va :=
  malloc(size)
```

A Program Named γ_m

```
pointer va :=
  malloc(size)
```

- A program is abstracted as a *named address-space*
- A container of *virtual-to-physical* memory resource mappings

Page Tables

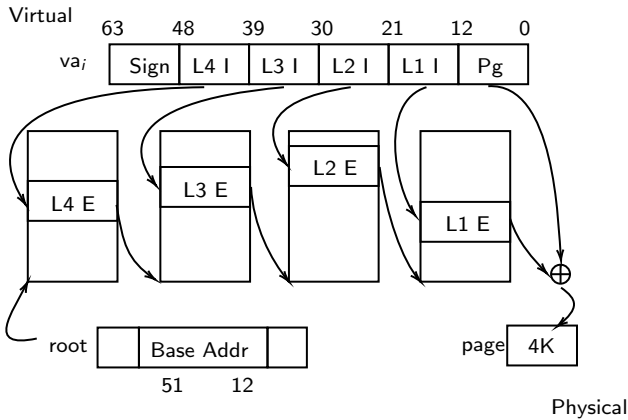


Figure: Page-Tables (**PT**): Data Structures for Address-Translation

A Complete Picture of Address-Space Abstraction

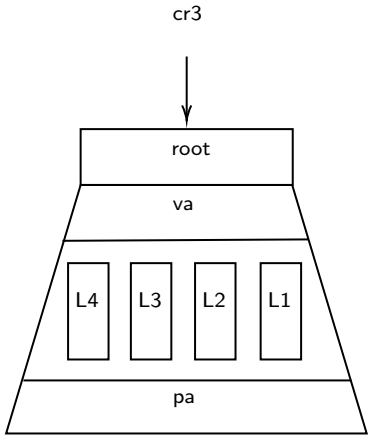


Figure: Depicting an Address-Space with its Essential Aspects

The Current View of Memory

The register cr_3 points to the current view of the memory, i.e., the loaded address space in the memory

.

Virtual Memory Management (VMM)

VMM as a General Resource Provider

"the virtual memory sub-system can be considered the core of a Solaris instance, and the implementation of Solaris virtual memory affects just about every other subsystem in the operating system" [McDougall and Mauro(2006)]

Sharing Physical Page Tables

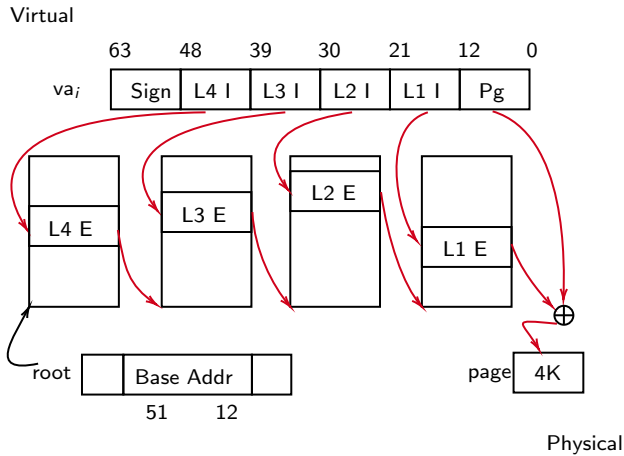
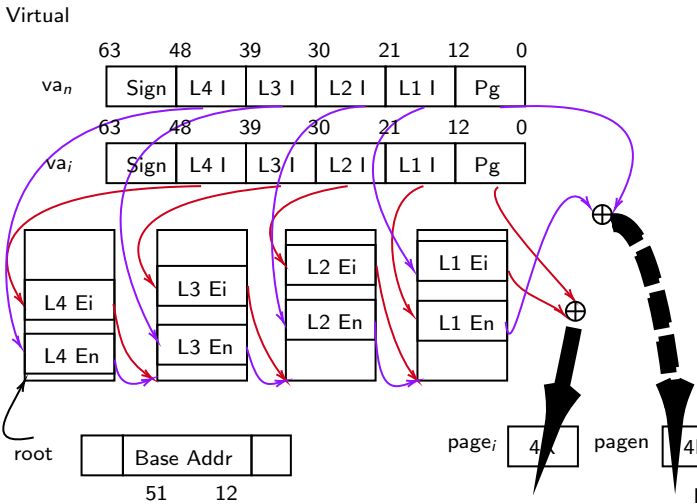


Figure: Accessing to the Page Referenced by L1 Entry

```
static pte_t *pte_nxt_table (pte_t *entry){
 pte_t *next;
 // If not already present, try to allocate
 if (!entry->present){
  if (!pte_alloc(&next)) {
   return NULL;
  }
  entry->pfn = PTE_PFN((uintptr_t) next);
  entry->present = 1;
  } else {
   uintptr_t next_phys_addr =
     PTE_PFN_TO_ADDR(entry->pfn);
   uintptr_t next_virt_addr = (uintptr_t)
     P2V(next_phys_addr);
   next = (pte_t *) next_virt_addr;
  }
  return next;
}
pte_t *walkpgdir(pte_t *l4, void *va){
 pte_t *l4_entry = &l4[L4I(va)];
 pte_t *l3 = pte_nxt_table(l4_entry);
 pte_t *l3_entry = &l3[L3I(va)];
 pte_t *l2 = pte_nxt_table(l3_entry);
 pte_t *l2_entry = &l2[L2I(va)];
 pte_t *l1 = pte_nxt_table(l2_entry);
 pte_t *l1_entry = &l1[L1I(va)];
 return l1_entry
}
```

Breaking Soundness in Sharing



Soundness of Traversal

Any update on the *shared page-tables*, which themselves are referenced with *physical memory* addresses, would break the soundness of any other traversal!

Managing Agnostic Memory Mappings

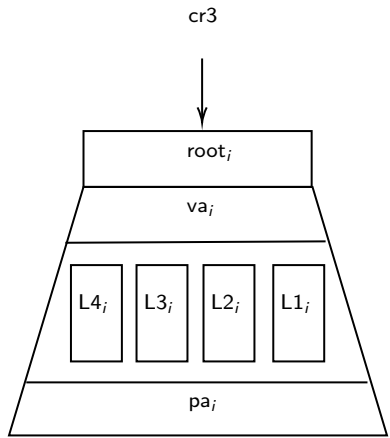


Figure: An Address Space with Unique Root Address root$_i$

Managing Agnostic Memory Mappings

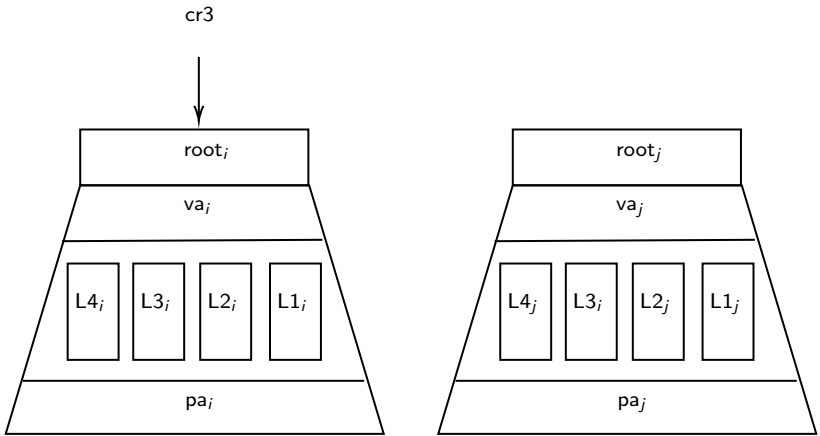


Figure: Two Address-Spaces with the Unique Root Addresses root$_i$ and root$_j$

Managing Agnostic Memory Mappings

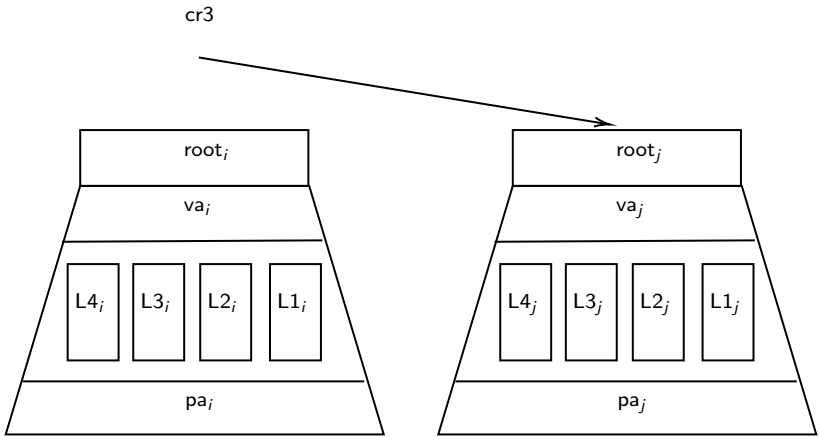


Figure: Switching Address-Spaces

Managing Agnostic Memory Mappings

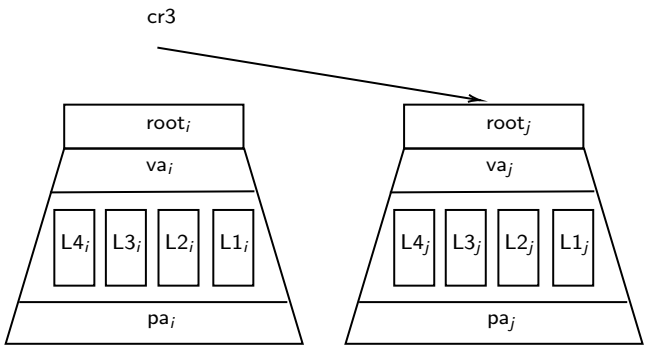


Figure: Switching Address-Spaces

Referring to Agnostic Resources

Unless we bookkeep to which address-space each of these virtual-to-physical mappings belongs, *which we never see in the practice of using virtual memory references*, we need to figure out a way of referring to these mappings as *they are only valid in their own address-spaces*.

Specifying Programs

$$\{P\}\ C\ \{Q\}$$

Separation Logic: Separating Conjuction

$$\textsc{Frame}\ \frac{\{P\}\ e\ \{Q\}}{\{P * R\}\ e\ \{Q * R\}}$$

Separation Logic: Ownership

- Well-known points-to assertion, e.g., memory_ref $\mapsto_q$ val
- Regarding the logical machinery, Iris **SL** enables encoding a generalized form ownership of *logical resources*
- A fragmental $\boxed{P}^{\gamma}$ ownership
  - Enabling coordinated access to logical resources
- Full $\boxed{P}^{\gamma}$ ownership
  - Enabling access to *update* logical resources, presented as *invariants*

Separation Logic: Invariants

$$\textsc{Inv}\ \frac{\{P * R\}\ \alpha\ \{P * Q\}_{\epsilon} \qquad \alpha \text{ physically atomic}}{\boxed{P}^{n} \vdash \{R\}\ \alpha\ \{Q\}_{\epsilon \uplus \{n\}}}$$

Defining Some Ownersip Assertions

- Expected to have register ownership to be defined : reg $\mapsto_r$ reg_val
- Expected to have *physical memory* ownership defined: pa $\mapsto_p$ val
- How about virtual memory references?

A Naive Attempt on Virtual-Pointsto

- Page and page table addresses are *physical*
- Purple (or red) path + bold black page references are *physical*
- Why don't we define *virtual* memory references in terms of the physical page-table and the final page references?

$$L_4\_L_1\_\text{PointsTo}(\text{va}, \text{l4e}, \text{l3e}, \text{l2e}, \text{l1e}, \text{paddr}) + \textit{paddr} \mapsto_p \text{page\_val}$$

Tokens for Traversals

$$\underbrace{\mathsf{va} \hookrightarrow^{\delta}_{\mathsf{q}} \mathsf{pa}}_{\text{Ghost translation}} \; * \underbrace{\mathsf{pa} \mapsto_{\mathsf{p}} \{\mathsf{qfrac}\}\ \mathsf{val}}_{\text{Physical location}}$$

- Abstract the purple and red segment of page-table traversal into *logical summarization of the walk*
- Distribute the fragmental ownersip of the logical page-table summarization to virtual memory ownership

Some Parts from Kernel Invariant

Definition (The Kernel Invariant for Page-Table Traversal with Virtual Page-Table Pointers)

$$\mathcal{I}\mathsf{ASpace}_{\mathsf{id}}(\theta,\Xi,m) \triangleq \mathsf{ASpace\_Lookup}_{\mathsf{id}}(\theta,\Xi,m) * \mathsf{GhostMap}(\mathsf{id},\Xi) *$$

$$\left(\mathop{\Large *}_{(\mathsf{va},\mathsf{paddr})\in\theta} \exists\ (\mathsf{l4e},\ \mathsf{l3e},\ \mathsf{l2e},\ \mathsf{l1e},\ \mathsf{paddr}).\ \mathsf{L_4\_L_1\_PointsTo}(\mathsf{va},\ \mathsf{l4e},\ \mathsf{l3e},\ \mathsf{l2e},\ \mathsf{l1e},\ \mathsf{paddr})\right) *$$

$$\mathop{\Large *}_{(\mathsf{pa},\mathsf{level})\in\Xi} \exists\ (\mathsf{qfrac},\ \mathsf{q},\ \mathsf{val},\mathsf{va}).\ \ulcorner \mathsf{va} = \mathsf{pa} + \mathsf{KERNBASE}\ \mathsf{level} > 1 \urcorner * \underbrace{\mathsf{va} \hookrightarrow^{\delta}_{\mathsf{q}} \mathsf{pa}}_{\text{Ghost translation}} * \underbrace{\mathsf{pa} \mapsto_{\mathsf{p}} \{\mathsf{qfrac}\}\ \mathsf{val}}_{\text{Physical location}} *$$

$$\underbrace{\ulcorner \mathsf{qfrac} = 1 \leftrightarrow\ \neg \mathsf{entry\_present}\ (\mathsf{val}) \urcorner}_{\text{Entry validity}} *$$

$$\underbrace{\left(\ulcorner \mathsf{present\_L}(\mathsf{val},\mathsf{level}) \urcorner \mathrel{-\!\!*} \forall_{\mathsf{i}\in 0..511}.\ ((\mathsf{entry\_page}\ \mathsf{val}) + \mathsf{i} * 8) \hookrightarrow^{\mathsf{id}} \mathsf{level\text{-}1}\right)}_{\text{Indexing into next level of tables}}$$

where

$$\mathsf{present\_L}(\mathsf{val},\mathsf{level}) \triangleq \mathsf{entry\_present}(\mathsf{val}) \wedge \mathsf{level} > 0$$

Specifying P2V

$\{P * \mathcal{I}\mathrm{ASpace}_{\mathrm{id}}(\theta, \Xi \setminus \{\mathrm{entry}\}), m) * \mathrm{rbp\text{-}8} \mapsto_{\mathrm{v}} \mathrm{entry} * \mathtt{rcx} \mapsto_{\mathrm{r}} \_ * \mathrm{entry} \mapsto_{\mathrm{id}} \_ * \mathrm{rtv} \hookrightarrow^{\delta s} \delta\}_{\mathrm{rtv}}$
$\{\mathrm{entry{+}KERNBASE} \mapsto_{\mathrm{vpte,qfrac}} (\mathrm{pte\_initialized}\ (\mathrm{entry\_val.pfn}))^{\neg}\}_{\mathrm{rtv}}$
$\{\mathtt{rbp\text{-}16} \mapsto_{\mathrm{v}} (\mathrm{pte\_initialized}\ (\mathrm{entry\_val.pfn}))) * \mathtt{rax} \mapsto_{\mathrm{r}} \mathrm{table\_root}\ (\mathrm{pte\_initialize}(\mathrm{entry\_val.pfn}))\}_{\mathrm{rtv}}$
$\{\forall_{i \in 0 \ldots 511}. ((\mathrm{table\_root}\ (\mathrm{pte\_initialized}\ (\mathrm{entry\_val.pfn})))) + \mathrm{i} * 8) \hookrightarrow^{\mathrm{id}} \mathrm{v\text{-}1}\}$

```
;; uintptr_t next_virt_addr = (uintptr_t) P2V(entry.pfn<<12);
movabs KERNBASE, rcx  {... * rcx ↦r KERNBASE * ...}rtv
add    rcx, rax
{... * rax ↦r table_root (pte_initialize(entry_val.pfn)) + KERNBASE * ...}rtv
... ;; clean up the stack and return the rax value
```

Figure: Converting a physical address of a PTE to a virtual address (w/o instruction pointer or flag updates).

The Current Status of Machinery

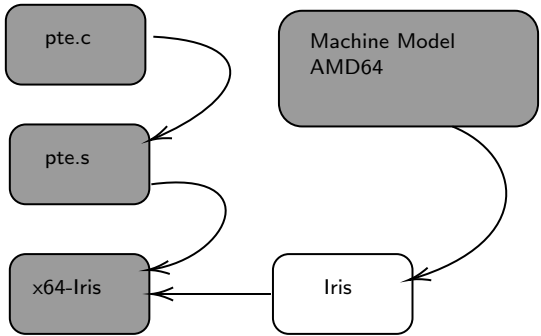


Figure: x64-Iris

- Dumping **.o** files
- Manuel treatment on **Xabs** instructions and field access

A Rough Quantification on the Current Status

Table: Line-of-Code Numbers for pte Verification

	C LoC A	Assembly LoC	Roqc Proof LoC
pte_get_next_table	12	45	3200
pte_walkpgdir	8	44	3200
pte_p2v	–	1	75
pte_switch_addrspace	–	18	350
pte_map_page	7	28	1750
pte_initialize	4	20	700

Table: Line-of-Code Numbers for x64-Iris Logic

	Roqc LoC
Soundness of Instructions Mentioned in the Presentation	50176 (The Complete Set of Instructions $\geq$ 1 Million)
VMM Related Logical Constructions	5554
Machine Model	6172

Part II

Foundations for Specification Evolution

Protocols

- Interfaces are well-known abstractions in low-level systems
  - Device drivers, Virtual-File-Systems (VFS) etc.
- Protocols are well-know for specifying them

Specifying Protocols for Systems with STSes

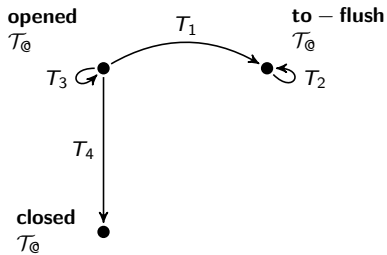


Figure: STS for Distributed File Protocol

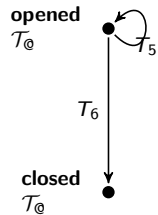


Figure: STS for Traditional File Protocol

Interacting with **STS**es

Modelling interactions of a client with a state machine via *token exchange*

Defining STSes

Definition (**STS** Definition following CaReSL's presentation [Turon et al.(2013)])

An STS π is given by:

1. a set of states $\mathcal{S}$,
2. a map from a state set of tokens $\mathcal{T} : \mathcal{S} \to \text{TokSet}$,
3. a transition relation $\rightsquigarrow$ on states, which is then lifted to pairs of a state and token set:

$$(s; T) \rightsquigarrow (s'; T') \triangleq s \rightsquigarrow s' \wedge \mathcal{T}(s) \uplus T = \mathcal{T}(s') \uplus T'$$

4. an interpretation mapping states to state assertions $\varphi : \mathcal{S} \to \text{Prop}$.

Propositional Kripke Model

Definition ((Propositional) Kripke Model [Hughes and Cresswell(1996)])

A Kripke model $\mathfrak{M}$ is a triple (W, R, V) where

- W is a set of "worlds"
- $R \subseteq W \times W$ is a relation called the *accessibility* relation between worlds
- $V : \text{PropVar} \to \mathcal{P}(W)$ gives for each propositional variable p a set of worlds $V(p)$ where p is considered true

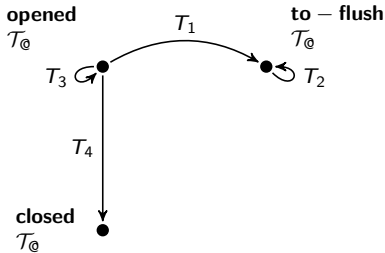
Bisimulations over Kripke Models

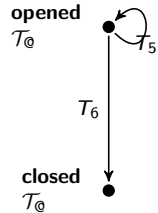
Definition ((Propositional) Bisimulation of Kripke Structures: $\mathfrak{M} \sim \mathfrak{M}'$.)

A *bisimulation* between (multimodal) Kripke structures $(W, R_{i \in I}, V)$ and $(W', R'_{i \in I}, V')$ is a relation $E \subseteq W \times W'$ satisfying:

- If $w \; E \; w'$, then w and w' satisfy the same propositional variables.
- If $w \; E \; w'$ and $w \; R \; v$, then there exists $v' \in W'$ such that $v \; E \; v'$ and $w' \; R' \; v'$
- If $w \; E \; w'$ and $w' \; R' \; v'$, then there exists $v \in W$ such that $v \; R \; v'$ and $w \; R \; v$

Intuition on Bisimulations over STSes





- More than just relating **STS**es in representation invariants per state.
- Bisimilar states can have different representation invariants.

Proof Indistinguishability

Knowing the proof of a client against the right (target STS conventionally π') *enables* deducing the proof against the bisimilar on the left (source STS conventionally π).

A Quick Tour on STS Assertions

- Invariants $\boxed{\varphi}^{\gamma}_{\pi}$, client capability $\boxed{s; \mathsf{T}}^{\gamma}$

$$\frac{}{\varphi(s) \Rrightarrow \exists \gamma. \boxed{\varphi}^{\gamma}_{\pi} * \boxed{s; \mathsf{AllTokens} \setminus \mathcal{T}(s)}^{\gamma}} \textsc{StsAlloc}$$

$$\frac{}{\boxed{\varphi}^{\gamma}_{\pi} * \boxed{s; \mathsf{T}}^{\gamma} \Rrightarrow (\exists\, s'. \ulcorner (s0, \mathsf{T}) \overset{\mathsf{rely}^*}{\sqsubseteq}_{\pi} (s', \mathsf{T}) \urcorner * \varphi(s) * \forall s\mathsf{l}',\ \mathsf{T}'. \ulcorner (s', \mathsf{T}) \overset{\mathsf{guar}.^*}{\sqsubseteq}_{\pi} (s\mathsf{l}', \mathsf{T}') \urcorner * \varphi(s\mathsf{l}') \Rrightarrow \boxed{s\mathsf{l}; \mathsf{T}'}^{\gamma})} \textsc{StsOpen}$$

$$\frac{\alpha \text{ physically atomic} \qquad \forall s_0\ .\ ((s; \mathsf{T}) \overset{\mathsf{rely}^*}{\sqsubseteq}_{\pi} (s_0; \mathsf{T})) \vdash \{\varphi(s_0) * P\}\ \alpha\ \{\exists s'\ ,\ \mathsf{T}'\ .\ (s_0; \mathsf{T}) \overset{\mathsf{guar}^*}{\sqsubseteq}_{\pi} (s'; \mathsf{T}') * \varphi(s') * Q\}}{\boxed{\varphi}^{\gamma}_{\pi} \vdash \{\boxed{s; \mathsf{T}}^{\gamma} * P\}\ \alpha\ \{\exists\, s', \mathsf{T}'. \boxed{s'; \mathsf{T}'}^{\gamma} * Q\}} \textsc{UpdIsl}$$

Figure: Iris STS Library [Jung et al.(2015)] simplified with later modality and invariant masks omitted

Decomposing Bisimilarity in STSes

The bisimulation $(\mathcal{M}(\pi, \pi', \varphi, \varphi', s, \mathsf{T}, \mathsf{U}))$ between two state machines, π and π' is composed of

- The source STS – π
- The target STS – π'
- The source STS's state interpretation function – φ
- The target STS's state interpretation function – φ'
- Token Embedding – $\epsilon_{\mathcal{S}} : \ \mathcal{S}(\pi) \mapsto \mathcal{S}(\pi')$
- State Embedding – $\epsilon_{\mathcal{T}} : \ \mathcal{T}(\pi) \mapsto \mathcal{T}(\pi')$
- The Law of Rely
- The Law of Guarantee
- The Law of Tolerance
- The state of source STS from which bisimulation is considered against any client interference with the token set T

Proof Translation

Obtain a proof rule utilizing the bisimulation to translate proofs between bisimilar state machines!

We Need This

$$\textsc{Bisim}\quad \frac{\pi \sim \pi' \qquad q \;\epsilon_{\mathcal{S}}\; s \qquad q' \;\epsilon_{\mathcal{S}}\; s' \qquad \{\ulcorner s; \epsilon_{\overline{\mathcal{T}}}(\mathcal{T})\urcorner^{\gamma}_{\pi'} * P\}\ C\ \{\ulcorner s'; \mathsf{T}'\urcorner^{\gamma}_{\pi'} * Q\}}{\boxed{\varphi}^{\gamma}_{\pi} \vdash \{\ulcorner q; \overline{\mathsf{T}}\urcorner^{\gamma}_{\pi} * P\}\ C\ \{\ulcorner q'; \mathsf{T}'\urcorner^{\gamma}_{\pi} * Q\}}$$

We Use This

UpdIsl

$$\frac{\alpha \text{ physically atomic} \qquad \forall s_0 \,.\, ((s;\mathsf{T}) \overset{\mathsf{rely}^*}{\sqsubseteq}_{\pi} (s_0;\mathsf{T})) \vdash \{\varphi(s_0) * P\}\ \alpha\ \{\exists s' ,\ \mathsf{T}' \,.\, (s_0;\mathsf{T}) \overset{\mathsf{guar}^*}{\sqsubseteq}_{\pi} (s';\mathsf{T}') * \varphi(s') * Q\}}{\boxed{\varphi}^{\gamma}_{\pi} \vdash \{\ulcorner s;\mathsf{T} \urcorner^{\gamma} * P\}\ \alpha\ \{\exists\, s', \mathsf{T}' . \ulcorner s';\mathsf{T}' \urcorner^{\gamma} * Q\}}$$

Bisim

$$\frac{\pi \sim \pi' \qquad q \,\epsilon_{\mathcal{S}}\, s \qquad q' \,\epsilon_{\mathcal{S}}\, s' \qquad \{\lfloor s; \epsilon_{\overline{\mathcal{T}}}(\mathcal{T}) \rfloor^{\gamma}_{\pi'} * P\}\ C\ \{\lfloor s';\mathsf{T}' \rfloor^{\gamma}_{\pi'} * Q\}}{\boxed{\varphi}^{\gamma}_{\pi} \vdash \{\lfloor q;\mathsf{T} \rfloor^{\gamma}_{\pi} * P\}\ C\ \{\lfloor q';\mathsf{T}' \rfloor^{\gamma}_{\pi} * Q\}}$$

Invariants of File Protocols

Definition (File Protocol Invariants)

$$\varphi_{\text{distributedfile}}\ (\ \ell\ ,\ \mathsf{R}\ )(\ s\ ) \triangleq \left\{ \begin{array}{ll} \text{match s with} & \\ \text{to} - \text{flush} \Rightarrow & \mathsf{R} * \exists\ \text{fs. isValidDirty(fs)} * \\ & \quad \ell \mapsto (\text{fs}.id, \text{fs.status} = \text{dirty}) \\ \text{opened} \Rightarrow & \mathsf{R} * \exists\ \text{fs. isValid(fs)} * \\ & \quad \ell \mapsto (\text{fs}.id, \text{fs.status} = \text{clean}) \\ \text{closed} \Rightarrow & \exists\ \text{fs. isValidClosed(fs)} * \\ & \quad \ell \mapsto (\text{fs}.id, \text{fs.status} = \text{closed}) \end{array} \right\}$$

$$\varphi_{\text{file}}\ (\ \ell\ \mathsf{R}\ )(\ s\ ) \triangleq \left\{ \begin{array}{ll} \text{match s with} & \\ \text{opened} \Rightarrow & \mathsf{R} * \exists\ \text{fs. isValid(fs)} * \ell \mapsto (\text{fs}.id, \text{fs.status} = \text{clean} \vee \text{dirty}) \\ \text{closed} \Rightarrow & \exists\ \text{fs. isValidClosed(fs)} * \ell \mapsto (\text{fs}.id, \text{fs.status} = \text{closed}) \end{array} \right\}$$

Keeping Promises

Transfer File Write

$$\frac{\pi \sim \pi' \qquad \text{opened } \epsilon_{\mathcal{S}}\ s \qquad q' \ \epsilon_{\mathcal{S}}\ s' \qquad \{\boxed{s; \epsilon_{\mathcal{T}}(\mathcal{T})}^{\gamma}_{\pi'} * P\}\ \text{write}\ \ell\ \text{new\_val}\ \{\boxed{s'; \mathsf{T}'}^{\gamma}_{\pi'} * Q\}}{\boxed{\varphi_{\text{distributedfile}}}^{\gamma}_{\pi} \vdash \{\boxed{\text{opened}; \mathsf{T}}^{\gamma}_{\pi} * P\}\ \text{write}\ \ell\ \text{new\_val}\ \{\boxed{q'; \mathsf{T}'}^{\gamma}_{\pi} * Q\}}$$

The Law of Rely

Theorem (The Law of Rely)

$$\forall s'.(s;\, T) \overset{\text{rely}^*}{\sqsubseteq}_{\pi} (s';\, T) \leftrightarrow$$
$$(\forall_{s_1, s_1', T_1}.\, \epsilon_{\mathcal{S}}(s, s_1) \to \epsilon_{\mathcal{S}}(s', s_1') \to \epsilon_{\overline{\mathcal{T}}}(T, T_1) \to (s_1;\, T_1) \overset{\text{rely}^*}{\sqsubseteq}_{\pi'} (s_1';\, T_1)$$

- We do not drop any client interference with capabilities T
- Indetification of the states that are tolerant to the client interference from which the STS can take steps (Guarantee)
- Bookkeeping of the client interference needed!
- Identifying the valid *pre* state

The Law of Guarantee

Theorem (Guarantee Bisim without Invariants)

$$\forall_{q',q,T'}.\, \epsilon_{\overline{\mathcal{T}}}(T) \equiv T' \to \epsilon_{\mathcal{S}}(s,q) \to (q;T') \overset{\text{rely}^*}{\sqsubseteq}_{\pi'} (q';T') \to$$
$$\forall_{q'',T''}.\, (q';T') \overset{\text{guar.}}{\sqsubseteq}_{\pi'} (q'';T'') \to$$
$$\exists_{s',s'',T_0',T_0''}.\, (s';T_0') \overset{\text{guar.}}{\sqsubseteq}_{\pi} (s'';T_0'') \wedge$$
$$\epsilon_{\mathcal{S}}(s') = q' \wedge \epsilon_{\mathcal{S}}(s'') = q'' \wedge \epsilon_{\overline{\mathcal{T}}}(T_0') \equiv T' \wedge \epsilon_{\overline{\mathcal{T}}}(T_0'') \equiv T''$$

- *Under the embedded client interference*, the steps taken by the target STS must be countered by a one in the source STS
- From target STS to source STS
- Identifying the valid *post* state

Soundness

Theorem (Soundness)

The updated state from UpdIsl *is preserved by the bisimulation.*

Ongoing Work

- Homomorphisms for general form of specifications (i.e., more than STSes)
- Exploit another obvious application fields, e.g., device drivers
- Only Iris pluggable?

Part III

Semantic Type Assertions for Deferred Memory Reclamation Schemes

What is Deferred Memory Reclamation?

- Both *reader* and *writer* threads accessing to a memory location *simultaneously*
- The write *waits* the readers that are already on the same memory location — i.e., *Grace Period*
- After the grace period end, the grace period ends, i.e, the readers leave the memory location, it is safe to *reclaim* the memory location
- Different schemes: Hazard Pointers (Maged M. Michael 2004), Read-Copy-Update (PE McKenney and JD Slingwine [McKenney and Slingwine(1998)])

RCU Semantics

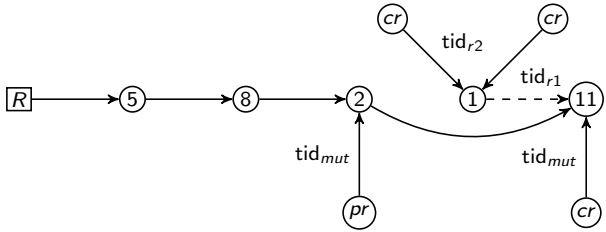
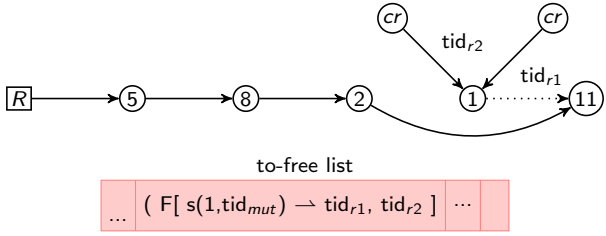


Figure: tid$_{mut}$ unlinks the node with value 1.



RCU Semantics

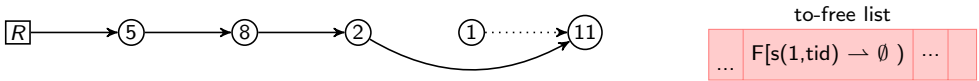


Figure: Bounding threads, tid_{r1} and tid_{r2} exit ReadBlock.

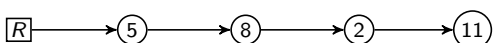


Figure: Reclaimed the node 1

Type Assertions for RCU

```
struct BagNode{
  int data;
  BagNode<rcuItr> Next;
}
BagNode<rcuRoot> head;
```

```
void add(int toAdd){
WriteBegin;
BagNode nw = new;
{nw: rcuFresh{}}
nw.data = toAdd;
{head: rcuRoot, par: undef, cur: undef}
BagNode<rcuItr> par,cur = head;
{head: rcuRoot, par: rcuItrϵ{}}
{cur: rcuItrϵ{}}
cur = par.Next;
{cur: rcuItrNext{}}
{par: rcuItrϵ{Next ↦ cur}}
while(cur.Next != null){
  {cur: rcuItr(Next)^k.Next{}}
  {par: rcuItr(Next)^k{Next ↦ cur}}
  par = cur;
  cur = par.Next;
}
...
WriteEnd;
}
```

A Taste of Soundness on Type System for RCU

- Soundness on top of Views Framework (Dinsdale-Young et.al. [**?**])
  - Logical state with its observation-map , free-list etc.
  - Denotation of types encoding the post-environment of any type accurately

$$[\![\Gamma,\ x : \mathsf{rcultr}\,\rho\,\mathcal{N}[y : \mathsf{rcultr}]]\!]_{M,tid}$$

- Global Invariants
  - Unlinked Reachability:
  - Delayed Ownership Transfer and Reader in Freelist:
- Discharging these invariants once as a part of soundness
  - No need to prove them for each different client

Remarks

- Simpler that full-blown program logics: Tassarotti et al. (PLDI 2015) [Tassarotti et al.(2015)], Fu et.al., Gotsman et.al.(ESOP 2013)
- The first general operational model for RCU-based memory management
- Based on our suitable abstractions for RCU in the operational semantics
  - Decoupling the memory-safety proofs from the underlying reclamation model
  - Similar is done for correctness by Meyer and Wolff (POPL 2019)
- Applicability/Usability
  - The first safety proof RCU client Citrus Binary Search Tree (Maya Arbel and Hagit Attiya PODC 2014)
  - Linked-list based bag implementation (McKenney Technical Report 2015)
- More type rules in the paper
  - Refinement rules for control flows
  - A simple type system for readers
  - Entering and exiting read/write-side critical sections

Future Directions

- Deploying it as Clang front-end
  - Abstract operational semantics can handle "classical RCU"
  - But optimized "batch lists" in Linux kernel? Refinement with our abstract model?
- Rust ownership
  - When published Rust's ownership was not able to handle RCU-like programming pattern
  - Now there is a set of RCU types
- Go adopted similar pattern in the existence of garbage-collector
  - Captured by our operational semantics
  - Async-free + Free list
- Beyond memory-safety? Tolerance to *stale data*

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