Final Lab Design - FPGA Alarm Clock

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1 Overview

For the Final Design project for Digital System Design, I am proposing an Alarm Clock design in Verilog using Xilinx's Vivado. This design will feature two functions: a digital clock and a programmable alarm. It will have as input four buttons for programming the clock and alarm, one button for snooze, and one switch for toggling the alarm. The design will also include the FPGA's Seven Segment Display to display the clock, an LED to display the alarm state, and RGB LED's to display the alarm going off. This system should function identical to a simple alarm clock without the alarm sound.

2 Goals

1. **Seven Segment Display:** The display should show three or four digits with a colon to the left of the right two digits.
2. **Clock Function:** The clock function should keep two numbers, one for the minute and one for the hour. The minute number should increment every one minute and rollback after 59 minutes. The hour number should increment every hour and rollback after 23. Both numbers should be displayed on the seven segment display.
3. **Alarm Function:** Similar to the clock function, the alarm function should keep two numbers, minute and hour. When the alarm minute and hour equals the clock's minute and hour, RGB LED's should blink. When the snooze button is pressed, the alarm should stop for 9 minutes, then repeat. Only when the alarm switch is turned off, the alarm should completely stop.
4. **Programming Functions:** The design should have four buttons as input to program the alarm clock. Two buttons should be the clock set and alarm set. The other two buttons should be the hour increment and the minute increment. When the clock set button is held, users should be able to press the hour increment to adjust the clock hour. The minute button should be similar to the hour increment except it should increment the minute. The alarm set should be equivalent to the clock set with the alarm hour and minute changing.

5. **Above and Beyond:** If the goals aforementioned, are met with limited difficulty, a variable number of applicable features will be added. One addition includes a switch to control the brightness of the seven segment display. This could be necessary for users who desire dim-lit LED's at night. Another addition could be a switch to control whether the clock uses military time or standard time. This feature could increase the amount of users interested in the alarm clock. Any additions made to the design not specified in this document will still suit the objectives of being easy-to-use and applicable.

3 Specifications

To meet the project minimum requirements, the design will implement the Architectural Wizard found in Xilinx's Vivado to provide clocking control, the seven segment display to provide easy-to-read digital numbers, and simple button and switch input to provide easy user experience. The ultimate goal for this design is to mimic the hardware used in simple, commercial alarm clocks. To go above and beyond the project requirements, the design could implement a number of features not commonly found in the simplest alarm clocks, yet applicable to many users.

4 Milestones

1. **Seven Segment Display**

   Numbers should be displayed on three or four of the digits along with a colon, replicating a clock output. When the alarm is being set, the alarm should replace the clock output on the display.

2. **Programming**

   Once accomplished, the user should be able to set the clock and alarm to whatever times they desire.

3. **Clock**

   The design should increment the clock every second. The minute digits should not go above 60, and the hour digits should not go above 23.

4. **Alarm**

   When the alarm goes off, there should be indications to the user until snooze is pressed or the alarm switch is toggled. Once accomplished, the alarm clock should be fully functional.