B38DF **Lab 1 Report Template**

**PRINT NAME: ……………**

**Matriculation No: ………………**

Complete the following sections:

1. Section 7 Checking the Simulation Result

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| ***Does the actual truth table found from simulation match the intended truth table on page 5?*** |

1. Section 8 Modifying the Logic Function

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| ***Your K-map and your derived logic expression derived should be shown below*** |

1. Modified Verilog Source file

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| ***(i)Give verilog code for the correct logic expression. (ii)Is this structural or behavioural representation?***  ***(iii)Give your modified source file.*** |

1. Simulator Waveforms for 3 above.

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1. Verilog code for Section 10.

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1. Simulator Waveforms for 5 above.

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