

Pin 8 is high when the pin 7 voltage exceeds the comparison reference voltage of COMP 1.

Due to the operation of the DOC circuit, noise may arise because of switching at the instant when returning to the original signal or when replacing the signal with a 1H delay signal. When short-term dropouts are compensated for under such circumstances, the effect may instead be noticeable on the picture and even if the dropout section has finished, the replacement by the delay signal will continue for a certain period of time. In other words, even if the pin 7 voltage drops, the pin 8 voltage will drop in an exponential curve by the external integrating circuit (R249, C250) and when this voltage falls as far as the comparison reference voltage of COMP 2, the output voltage of COMP 2 is inverted to a high level.

Contained in the vertical blanking period of the video signal are H periods into which the various data have been inserted, and these data are read out by the CONT section of the SRVB circuit board.

When it is necessary to avoid the data being replaced by the DOC and erroneously judged by the CONT section, that is, when this leads to a relatively serious malfunction as a function of the player, the DOC operation can be inhibited by a command (DOC INH signal) from the CONT section. This signal is supplied to pin 15 and the COMP 2 output is switched on or off by the internal switch.

This switched output is the control signal of the DOC switch which selects the original video signal and 1H delay signal.

The above-mentioned 220 ns delay signal enters pin 13 of Z201 and it is connected to one side of the DOC switch to become, under normal circumstances, the video signal in which this signal is output.

The 220 ns delay signal is, moreover, supplied to the CCD circuit of Z205 (MN8038) through the low-pass filter (LPF). The LPF is installed in order to suppress the high-range components exceeding the CCD circuit band and avoid the effects produced by radiation internally, and it has a cut-off frequency of 850kHz. The CCD circuit is composed of 112 transfer stages, and it is driven by a 2-phase clock frequency of 1.79MHz. The clock signal is produced inside Z205 from the 3.58MHz frequency provided by the color phase compensation circuit which will be described later. The video signal is delayed by a time which is approximately equivalent to 62.57  $\mu$ s (produced by dividing 112 by 1.79MHz) by this CCD circuit.

The CCD circuit output is amplified by the differential amplifier circuit and it passes through the

2nd low-pass filter to filter out the clock components. This filter has a suppression ratio of about -36dB with a frequency of 1.79MHz.

The 62.57  $\mu$ s delay produced by the CCD circuit and the delays produced by the two low-pass filters are added to form a 1H, 63.57  $\mu$ s delay, it is adjusted (1H delay video level, VR202) to 2Vp-p in this output, it is supplied to pin 11 of Z201 and connected to one end of the DOC switch.

The output video signal selected by this DOC switch is de-emphasized (R250, R251, C252) in respect of the pre-emphasis provided during recording.

### 8.3 SYNC SEPARATOR CIRCUIT

The video signal, resulting when the undesirable high-range components are eliminated by the 1MHz low-pass filter from the video signal output from the DOC circuit, is supplied to pins 15, 9 and 12 of Z202 (PA0009) through the Z212 (TC4016BP) switch circuit.

The dummy sync signal mentioned later is supplied when a CD disc is being played.

The composite sync signal (COMP SYNC), horizontal sync signal (H SYNC), vertical sync signal (V SYNC) and the frame number and other data inserted in the vertical blanking period are separated from the video signal in Z202.

#### 1) COMP SYNC Signal

The video signal is coupled by C279, biased by R284, supplied to pin 15, and clamped at the sync tip of the video signal. It is then supplied to a comparator with a slightly higher comparison reference voltage than the clamp potential where it becomes the COMP SYNC signal and it is output to pin 14 (open collector).

#### 2) V SYNC Signal

The COMP SYNC signal output to pin 14 is supplied through the external integrating circuit (R288, C283, R289, R284) to pin 16. The integral waveform is sliced by the comparator and its output is formed the width (680  $\mu$ s) by the monostable multivibrator and it is output from pin 1.

#### 3) H SYNC Signal

The voltage at pin 3 to which the integrating circuit (R292, C290) is connected starts to drop in an exponential curve with the timing of the COMP SYNC signal rise (sync end). The comparator judges that the pin 3 voltage is between two voltages and its output serves as the key pulse for clamping the video signal.

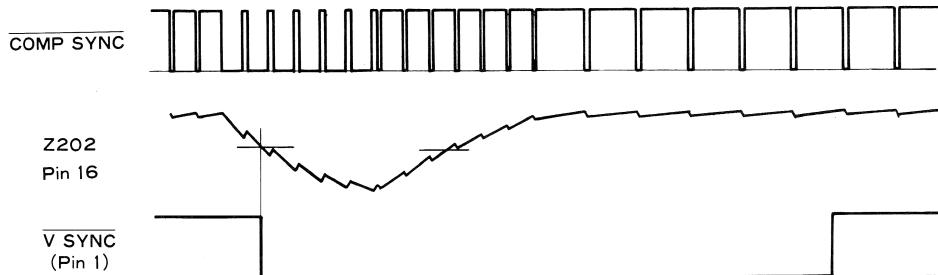


Fig. 8.4 Separation of the Vertical Sync Signal

The video signal is coupled by C278, supplied to pin 9 and clamped with the key pulse at the back-porch timing. It is here that the undesirable video information parts are suppressed by the clipper. The signal is output to pin 11, made into the pulse signal by the differentiation circuit, returned to pin 8, waveform-shaped by the comparator, given a width of  $1\mu s$  by the monostable multivibrator and finally output to pin 7 (open collector).

In this circuit it is possible to further reduce the low jitter whose generation cannot be avoided with conventional sync separator, although on the other hand the vertical sync data is lost by the differentiation circuit (the H/2 pulse of the vertical blanking period remains).

This is why the COMP SYNC and V SYNC signals are separated by different circuits, as described above.

#### 4) DATA Signal

The video signal is further coupled by C280, supplied to pin 12 and clamped by the key pulse. The level near the center of the video data part is judged by the comparator using the comparison voltage and output to pin 13.

The DATA signal includes not only the data but also the video signal saturated although only the data are read out by the CONT section.

#### 8.4 SYNC PROCESSING CIRCUIT

The COMP SYNC and H SYNC signals separated from the video signal by Z202 are sent to Z203 (PA9001).

The H/2es are removed from the COMP SYNC signal in Z203, so that the HD signals are made. The COMP SYNC signal supplied to pin 2 of Z203 first sets the internal flip-flop. Pulses with a width determined by the integrating circuit (R310, C302) connected to pin 26 are produced from the flip-flop output, and the charging voltage of C304 connected to pin 23 is reset by these pulses. After this C304 is again charged by a constant current and the pin 23 voltage becomes a ramp signal which rises linearly. The ramp slope is adjusted by VR207 which is connected to pin 22.

The COMP SYNC signal supplied to pin 2 is frequency/voltage converted by the pulse count system. This converted voltage (pin 24 voltage) and the pin 23 ramp voltage are compared by the comparator. At the point where the ramp voltage increases further, the output is inverted and the flip-flop, which was set by the above-mentioned COMP SYNC signal, is reset. The flip-flop output becomes the HD signal from which H/2 included in the vertical blanking period of the COMP SYNC signal is removed, and this is called the HD 1 signal.

Furthermore, a signal with a  $10\mu s$  width is produced by the comparator output. This is called

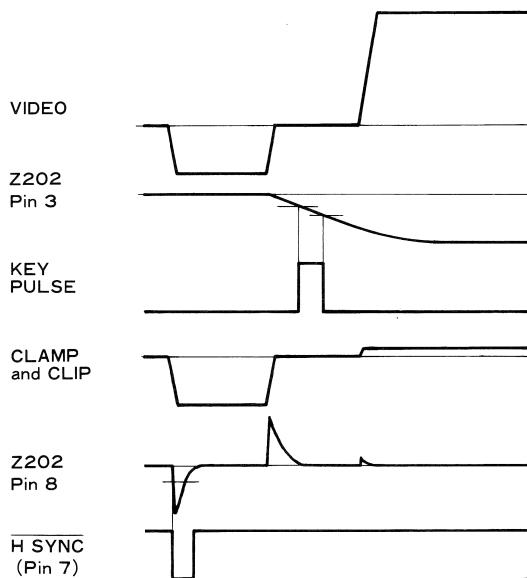


Fig. 8.5 Separating of the Horizontal Sync Signal

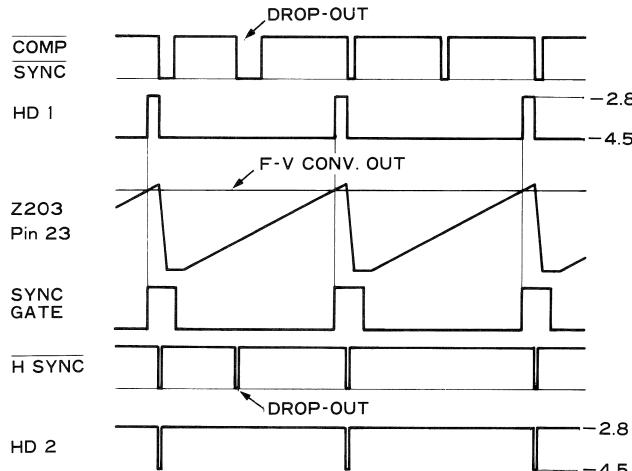


Fig. 8.6 H/2 Removal and Dropout Compensation

the sync gate signal and H/2 is removed by separating only the H SYNC signal during this 10  $\mu s$ . The HD signal produced in this way is called the HD 2 signal.

In the range where DOC does not function reliably due to this circuit (in which the H cycle is not 63.57  $\mu s$ , in other words during the start-up of the spindle motor, or during the vertical sync period), it is possible to remove the "false" sync caused by dropouts.

The sync gate signal can vary the generation cycle in accordance with the cycle of the COMP SYNC signal which is supplied.

This means that when the COMP SYNC signal cycle is long (low disc speed), the frequency/

voltage converter circuit's output voltage (pin 24 voltage) rises and the sync gate signal output is also delayed by the delay in the timing of the voltage inversion with the ramp.

When the COMP SYNC signal cycle is short (high disc speed), the sync gate output cycle is shortened by means of the reverse operation.

The tracking operation for the COMP SYNC signal cycle of the sync gate signal is limited to a particular range (approx. 55 to 85  $\mu s$ ) and when the disc speed deviates greatly from the prescribed value, it is not possible to obtain a dependable HD signal.

However, when the disc speed is normal (or nearly normal), the jitter generated by the separator circuit in the H SYNC signal is minimal which means that the HD 2 signal which will be produced will serve as a time base signal which can be depended on and which contains no jitter.

The HD 2 signal is used to detect the time base error in the tangential servo circuit.

The HD 1 signal is produced from the COMP SYNC signal which has more jitter than the H SYNC signal and so its reliability as a high-accuracy time base signal is low. However, since it is output immediately if the spindle motor starts and the video signal is demodulated, it is used to detect servo lock in the tangential servo circuit.

It has already been mentioned that the ramp slope can be adjusted by VR207 connected to pin 22, and this adjustment depends on the fact that the amount of constant current charging C304 changes in accordance with the current flowing from pin 22.

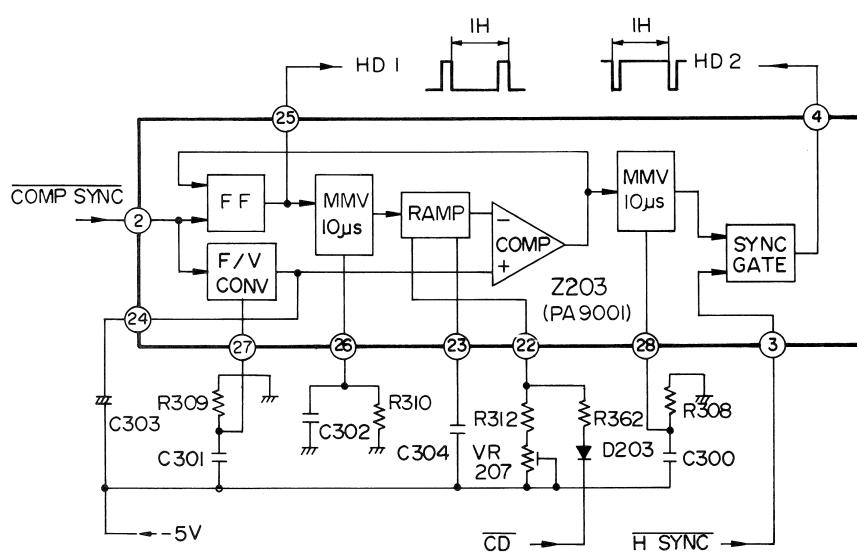


Fig. 8.7 Sync Processing Circuit

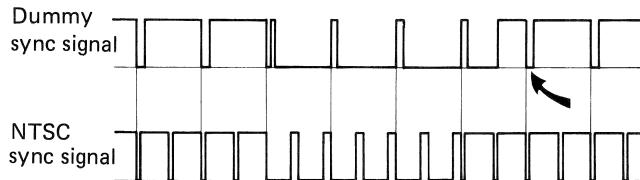


Fig. 8.8 Vertical Blanking Period of Dummy Sync Signal

When a CD disc is being played, this current is increased by R362 and D203 connected to pin 22 for the reason which will be described below. With the dummy sync signal described later, there is a place shown in Fig. 8.8 where the sync signal is delayed from the H timing in the vertical blanking period. In this circuit which starts operating from the sync fall, there are cases where the sync signal indicated by the arrow in the figure cannot be separated. This gives rise to the symptom where the data indicated on the screen while a CD disc is being played will shake.

This is why, when a CD disc is being played, the inversion timing of the ramp voltage and output voltage of the frequency/voltage converter circuit is speeded up, and the sync separation is made more reliable, by increasing the angle of the ramp slope.

## 8.5 COLOR PHASE COMPENSATION CIRCUITRY

Contained in the demodulated video signal are residual time base errors which cannot be converged by the tangential servo. These errors affect the phase (hue) of the color signal.

The color phase compensator circuit is therefore designed to detect the phase errors from the color burst signal and reference signal and to control the phase of the video signal accordingly.

### 1) Phase Error Detector Circuit

A gate signal for separating the color burst signal from the video signal is created inside Z203 (PA9001) from the HD 2 signal produced by the above-mentioned sync processing circuit. The gate signal timing is adjusted by VR205 which is connected to pin 5.

Only the high-frequency components of the video signal are supplied to pin 9 and the color burst signal is separated by the gate signal, and tuned by the tank (L214, C317) connected to pins 10 and 11 and amplified.

The color burst signal is first supplied to the PLL circuit. The PLL circuit is composed of a phase comparator inside Z203, a phase-locked loop compensation filter (C314, R317) connected to pin 13, and a voltage-controlled crystal oscillator (VCXO circuit) composed in turn of an internal circuit and external Q223 and X201, etc.

The color burst signal and output signal of the VCXO circuit are both supplied to the phase comparator.

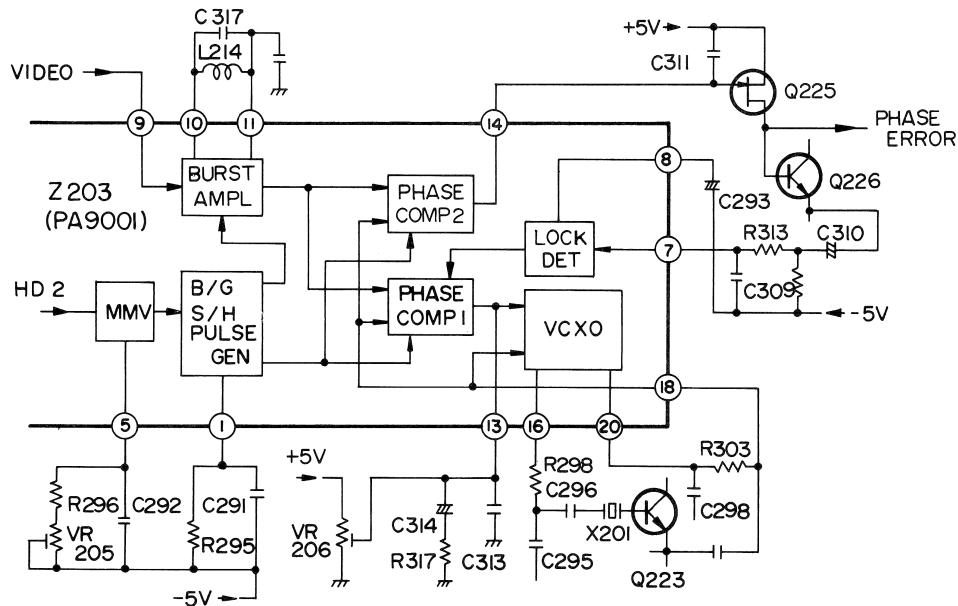


Fig. 8.9 Phase Error Detector Circuit

A sampling signal which determines the timing of the phase comparison is created along with the burst gate signal from the HD 2 signal, the comparison results are output as a voltage by this signal and they are held in C313 which is connected in parallel with the pin 13 loop filter. The VCXO circuit is controlled by this voltage and its oscillation frequency is varied.

Due to this loop the VCXO circuit generates a frequency signal in phase-synchronization with the color burst signal, but this operation has a certain limited range (pull-in range) for the amplitude of the phase error. In other words, when the phase difference is excessively high, the VCXO circuit ceases to be capable of generating the signal in accordance with this difference. VR206 connected to pin 13 is adjusted so that the VCXO circuit will operate at the center of the pull-in range with a phase difference of zero.

A second phase comparator is provided to compare the phases of the color burst signal and continuous signal produced by the PLL circuit.

The sampling comparison results of this second phase comparator are held in C311 connected to pin 14.

When the PLL circuit is not in a state of phase synchronization, frequency components serving as the difference in frequency between the output signal of the VCXO circuit and color burst signal are included in the pin 14 phase error signal. These components alone are filtered out by the band-pass filter and the signal is supplied to pin 7 of Z203.

When the signal supplied to pin 7 is greater than a certain value, it is judged that the PLL circuit is in a state of asynchronization and its loop gain is increased. This extends the pull-in range mentioned above and the PLL circuit is pulled into a state of synchronization. Conversely, when the signal supplied to pin 7 is less than the certain value, the PLL circuit's loop gain is reduced. In this way, the phase error between the color burst signal and reference continuous wave is output from the second phase comparator.

The PLL circuit thus creates a continuous wave which is phase-synchronized with the color burst signal for a relatively long time rate and the phase difference of the high frequency between this wave and the color burst signal becomes the desired phase error. When a high loop gain is maintained even with the PLL circuit in a state of synchronization, even the desired phase error is converged.

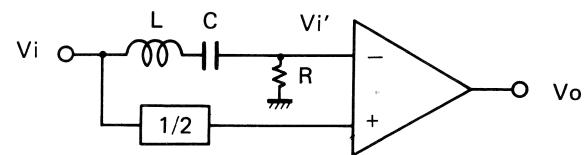
## 2) Color Phase Compensator Circuit

The DC component and high-frequency component by means of sampling in the detected phase error are suppressed by the band-pass filter. They are supplied to the differential amplifier circuit composed of Q218 and Q219 but when the spindle servo is not in a state of synchronization, this is inhibited by Z207.

The phase error level and in its turn the compensation sensitivity based on the phase error are adjusted by VR208. They are added to the high-range components of the video signal which is output from the above-mentioned dropout compensator circuit via the Q217 buffer.

The color phase-compensated video signal is produced by supplying the video signal and this addition signal which has passed through the LCR circuit into the differential circuit inside Z204 (PA9003).

The phase error components shift the color signal phase by varying the bias, or capacitance, of the VC201 variable-capacitance device.



$$Vi' = \frac{R}{jwL + \frac{1}{jwC} + R} Vi \quad Vi = \frac{jwCR}{(1 - w^2LC) + jwCR} Vi$$

$$Vo = 2 \left\{ \frac{1}{2} Vi - Vi' \right\} = 2 \left\{ \frac{1}{2} - \frac{jwCR}{(1 - w^2LC) + jwCR} \right\} Vi$$

$$F(jw) = \frac{Vo}{Vi} = 1 - \frac{2jwCR}{(1 - w^2LC) + jwCR} = \frac{(1 - w^2LC) - jwCR}{(1 - w^2LC) + jwCR}$$

$$\therefore |F(jw)| = 1 \quad \angle F(jw) = 2 \tan^{-1} \frac{-wCR}{1 - w^2LC}$$

Fig. 8.10 Principle of Color Phase Compensation

## 8.6 DUMMY SYNC SIGNAL GENERATOR CIRCUIT

When a CD disc is played, the elapsed time and remaining play time, among other data, are indicated on the TV screen. The dummy sync signal generator serves to produce the dummy video signal for this video output.

Fig. 8.12 is a timing chart of the dummy sync signal generation for the vertical blanking period. The dummy sync signal with a luminance of approximately 40 IRE is obtained from the Q230 output.

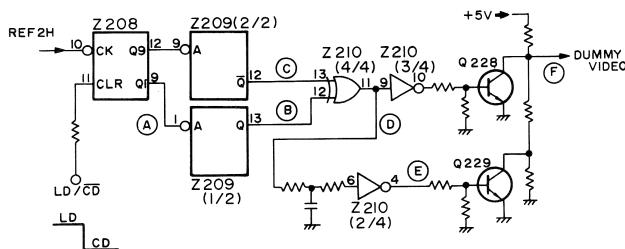


Fig. 8.11 Dummy Sync Signal Generator Circuit

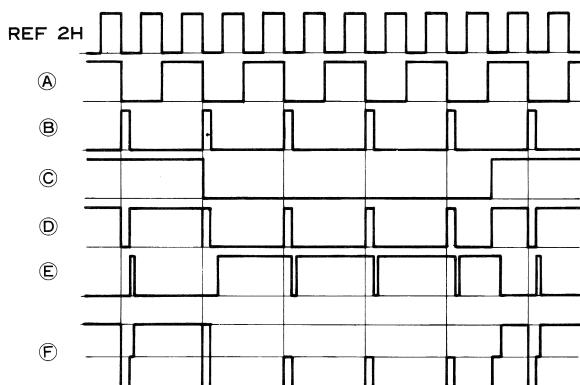


Fig. 8.12 Dummy Sync Signal Timing Chart

## 8.7 VIDEO OUTPUT PROCESSING CIRCUIT

The color-phase compensated video signal is output from pin 13 of Z204 (PA9003) and it is supplied via the Q220 buffer again to pin 12.

The video signal is supplied from the Q221 buffer to pin 11 through a low-pass filter with a cut-off frequency of approximately 700kHz.

### 1) Sync Clamping Circuit

The color signal and other high-range components are removed from the pin 11 signal from which the COMP SYNC signal has been removed inside

Z204. The video signal supplied to pin 12 has its sync tip clamped by the COMP SYNC signal.

### 2) MCA Code Suppressor Circuit

Data called the MCA code are included in the 10H and 11H (273H) of the video signal's vertical blanking period and, regardless of the blanking period, these data sometimes appear on the screen with some TV monitors. These data are therefore suppressed inside Z204 and clipped to approximately 19 IRE.

In actual fact, all the sections in which the V SYNC signal input into pin 6 is low, or the period of the 4H - 14H (267H-277H), the parts where exceeds the pedestal level are clipped.

### 3) Video Squelch Circuit

The video squelch circuit is composed of a 3-position switch. When pin 4 is low, the video signals played back from the LD disc are output; and when pin 4 is high, output is inhibited and, instead, DC higher than the video signal sync tip by an amount equivalent to 1V is output. This is the average level of the picture in general and this operation is carried out so that sudden fluctuations in the operating point are not generated in the later stage circuitry including the TV monitor. When pin 4 is in the high-impedance state, the dummy sync signal supplied to pin 5 is output when a CD disc is played.

The VIDEO SQ signal from the CONT section on the SRVB circuit board is supplied to pin 4.

### 4) Display Data Inserter Circuit

The data displayed on the screen is inserted into the video signal by superimposing the DISP signal sent from the CONT section.

In actual fact, when the DISP signal is low, the video signal is switched to a DC voltage corresponding to 100 IRE.

In order to make this display stand out on the screen, the luminance of the part corresponding to the display background is halved (the color signal is also halved).

The video signal which has undergone these processes is output from pin 1, it passes through the Q222 buffer and it sent to the PNJB (rear panel VIDEO OUT connector) and also to the RF modulator for the VHF output.

## 9. DESCRIPTION OF AUDIO PLAYBACK CIRCUITRY

The audio signals of the LD discs are played back and output by the circuits described below.

The audio playback circuitry includes the circuit which demodulates the audio signals from the RF signal sent from the VIDEO section, the circuit which detects dropouts in the signals, the switch circuit which controls the audio output and the CX decoder circuit which decodes the signals recorded by the CX system.

The audio signals are composed of the 1/L and 2/R channel signals and the circuitry configuration in each case is identical. The following description, therefore, is confined mainly to the 1/L channel circuitry.

### 9.1 AUDIO DEMODULATOR CIRCUIT

The RF signal sent from the VIDEO section on the DEMB circuit board first passes through the low-pass filter with a cut-off frequency of about 4MHz where the video signal components are filtered out. D9 and D10 are installed in order to limit the spike-like noise in the RF signals.

The RF signals are then demodulated separately for each channel. As mentioned above, the description is confined mainly to the 1/L channel.

Only the audio signal frequency components are separated from the RF signals by the band-pass filter. The carrier frequency is 2.3MHz for the 1/L channel and 2.8MHz for the 2/R channel.

The RF signals supplied to pin 1 of Z1 (PA3001A) pass through the limiter and are frequency-demodulated by the same system as that used for the video signals. In other words, the output signal of the limiter circuit output from pin 9 is supplied again to pin 10 through the phase shift circuit. The demodulation signal is obtained by multiplying this signal and the limiter signal, it is amplified and output to pin 6.

The level of the signal which is amplified by Q5 and output from the Q6 buffer is adjusted by VR1 (VR2 in the case of the 2/R channel).

This signal passes through the low-pass filter with a cut-off frequency of 26kHz where the carrier components are filtered out and it is sent to the audio signal switch circuit through the Q7 buffer. The Q6 output signal is sent to the dropout detector circuit which will now be described.

### 9.2 DROPOUT DETECTOR CIRCUIT

The level detection signal of the RF signal is output from pin 15 of Z1 and when dropouts are caused, Q13 is driven into conduction.

Spike-like noise is sometimes mixed in with the demodulated audio signals by the dropouts and these are detected by the window comparator as described below.

Only the noise components of 160 kHz or above are separated from the demodulated audio signals by the high-pass filter. When an amplitude exceeding a certain value is produced in these noise

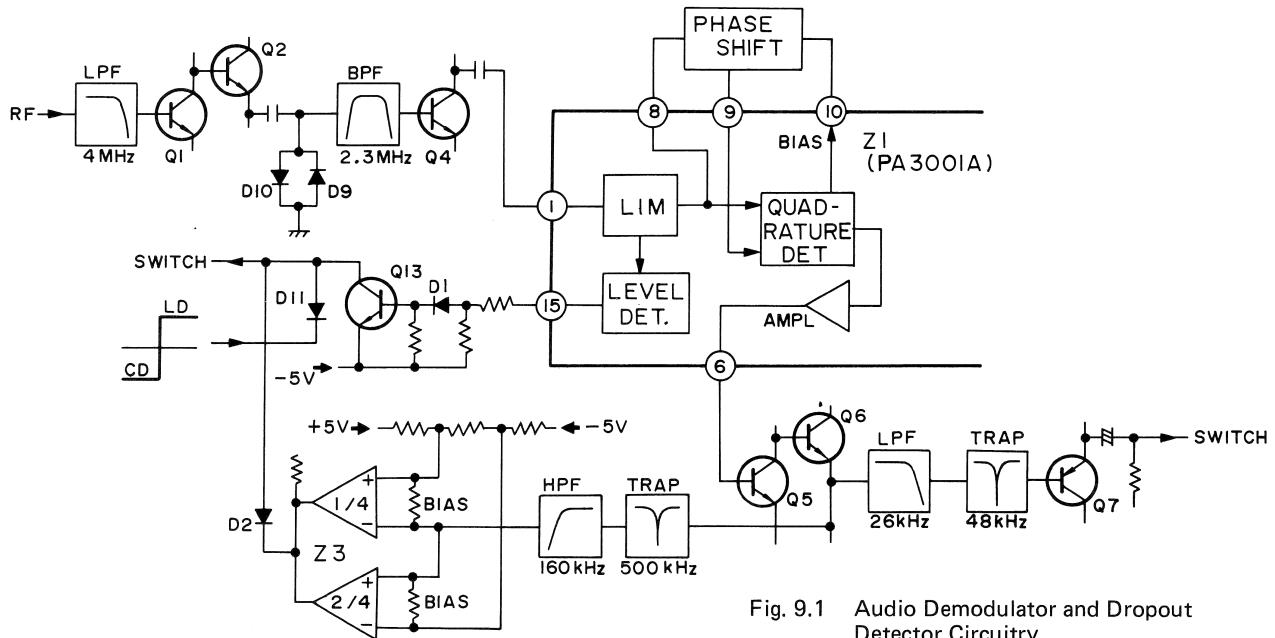


Fig. 9.1 Audio Demodulator and Dropout Detector Circuitry

signals, Z3 ( $\mu$ PC339C) 1/4 is responsible for its detection and output with a positive amplitude and Z3 2/4 with a negative amplitude.

### 9.3 AUDIO SWITCH CIRCUIT

The audio signal output is inhibited in the following cases:

- It is inhibited by the Q13 being driven into conduction when dropouts in the RF signal are detected.
- It is inhibited by the window comparator output being set low when spike-like noise is detected in the audio signals.
- It is inhibited by the command (AUD 1/L SQ, AUD 2/R SQ) from the CONT section on the SRVB circuit board through the function of the player (any function except play) or when the user presses the VDP AUDIO key on the remote control unit.

In actual fact, on/off operation is performed by the Z4 (TC4106BP) switch circuit.

A case in which the 1/L or 2/R channel sound has been selected by the user is now considered.

For instance, when the 2/R key on the remote control unit is pressed, the AUD 1/L SQ signal is set high and Q12 is turned off. This sets SW1 to open.

Q16 is driven into conduction by either Q12 or Q14 (2/R channel) or by both Q12 and Q14 being turned off. This sets SW2 to close. These operations ensure that the 2/R channel signal will be output for both audio channels.

When the output of both channels is inhibited by the SQ signal, Q20 is turned off by Q21 being turned off. The Z7 output is set high and, as mentioned later, the output of the audio signal sent to CDDM is inhibited by driving Q19 into conduction for the 1/L channel and by driving Q18 into conduction for the 2/R channel.

Even during the instant when the power switch is switched on/off, Q20 turns off to inhibit the output.

The noise arising with switch circuit on/off operations is removed by C63 and rapid voltage fluctuations even in the signal line are suppressed by C68. Furthermore, when the switch has been turned off only for a short period of time by dropouts, the signals are interpolated by the voltage held in C68.

### 9.4 DE-EMPHASIS AND CX DECODER CIRCUITS

The switch circuit output is supplied to the de-emphasis circuit composed of Z5 (2/2) and other parts and the pre-emphasis is compensated for by R80 and C69.

The CX system decoding is performed by Z6 (HA12043) for both channels.

The CX system is a type of noise reduction system which works as follows. When the amplitude of the source signal is high for frequencies of 500kHz and above, the dynamic range is kept constant and the recording level is expanded by "compressing" the signal. During playback, conversely, the source signal is restored by "expanding" the high amplitude.

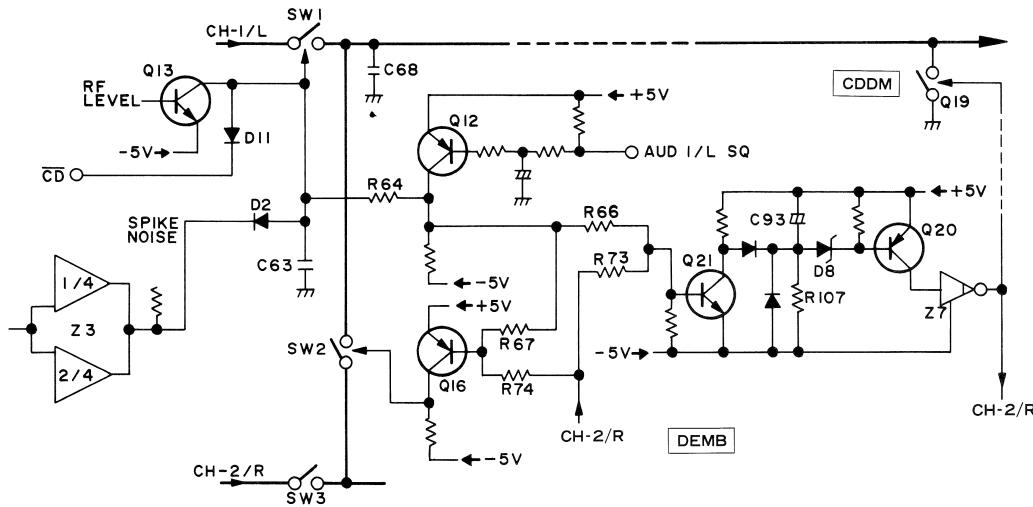


Fig. 9.2 Audio Switch Circuit

Fig. 9.3 shows the characteristics of the CX system. As shown in the figure, the amplitude is compressed above a  $-28\text{dB}$  input during recording. The  $0\text{dB}$  serving here as a reference is  $40\%$  modulation, or in other words modulation of  $\pm 40\text{kHz}$  centering on the carrier frequency.

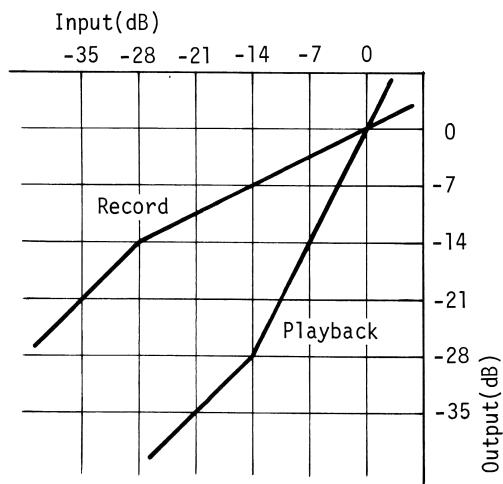


Fig. 9.3 Characteristics of the CX System

For instance, with a  $-28\text{dB}$  input the source signal is recorded at  $-14\text{dB}$  and during playback the  $-14\text{dB}$  level is returned to  $-28\text{dB}$ . The signal supplied to pin 11 is amplified and besides being supplied to the amplifier circuit permitting gain control, it is output to pin 3. The frequencies exceeding  $500\text{kHz}$  in the pin 3 signal pass through the high-pass filter (C86, R94), the signal itself is returned to pin 2 and the signal which controls the amplifier gain is produced.

When an amplitude of  $-14\text{dB}$  or more is detected, the gain switching time constant is determined by the time constant circuit.

High-amplitude signals are expanded by increasing the gain of the amplifier circuit and this is performed with a particular time constant to ensure that the switching is natural. The normal switching time constant is 2 seconds both when increasing the gain and when reducing the gain to its former level. When the amplitude has increased greatly, however, the gain is increased in 30 ms and especially when fluctuations are sudden, it is increased in 1 ms. Conversely, when the amplitude is greatly reduced, the gain is reduced by the 200 ms time constant. The control signal may be mixed in with the audio signal to result in audible noise at the instant when the gain is switched. This is caused by unbalance in the differential circuit in-

side Z6 and is improved by adjusting the DC value (offset) of the input signal with VR5 (VR6 for the 2/R channel).

The decoder circuit of the CX system is activated by the  $\overline{\text{CX}}$  signal from the CONT section.

With LD discs recorded by the CX system, a code indicating such is recorded as data. The CONT section sets the  $\overline{\text{CX}}$  signal low by reading out this code. On/off operations are possible using the CX SYSTEM key on the front panel, but it is not possible to switch this off when it has been judged that a CX disc is being played depending on the disc data.

The audio signals are output from Z6 pin 16 (1/L channel) and pin 14 (2/R channel) and sent to CDDM.

On CDDM the signal reference is converted to the CDDM GND by Z17 (BA4558DX) and sent to PNJB (rear panel AUDIO 2 OUT connector). The audio signals mixing both channels are output from Z6 pin 15 and sent to the RF modulator for VHF output.

## 10. DESCRIPTION OF CD PLAYBACK CIRCUITRY

The encoding system used with the CD system will be briefly described in the paragraphs below.

The source signal is sampled at a frequency of 44.1kHz and one sample is A/D converted into a 16-bit signal. The 16 bits are divided into two sets of 8 bits each and processed and one set of 8 bits is called a symbol.

For the encoding 24 symbols (or 12 samples) is treated as a single processing unit and with each unit an 8-symbol parity signal and a 1-symbol control/display signal are added.

The 1-symbol, 8-bit NRZ signal has a  $2^8 = 256$  pattern and this is converted into the 14-bit NRZI signal.

The NRZ and NRZI signals are transmission formats for serial signals. The NRZ (Non-Return-to-Zero) signal is such that the "1" and "0" correspond to high and low levels; the NRZI (Non-Return-to-Zero Inverted) signal is such that the high level is inverted to low and vice versa with "1".

The 14-bit signal has a  $2^{14} = 16384$  pattern. The pattern is selected as per 256 so that the following two conditions are met simultaneously,

- (1) That the transition shall not occur in any interval shorter than 3 bits.
- (2) That a state of no transition shall not continue for more than 11 bits.

and conversion is made to correspond with the 8-bit 256 pattern. This is known as EFM (8-to-14 modulation) conversion.

When EFM conversion is performed, it is possible to limit the frequency band in which the modulation signals to be transmitted are to be played back. In other words, the high-limit is determined by the above-mentioned condition (1) and the low-limit by condition (2).

The EFM-converted 14-bit signal is continuously combined through the merging bits which each contain three bits. The digital value of these three bits is determined so that the duty cycle, as seen over the prolonged time of the EFM-converted signal, becomes 50%.

In this way, the 24-symbol data signal, 8-symbol parity signal and 1-symbol control/display signal are combined. A signal unit of the encoding signal, to which the sync signal has been added at its head, is known as a frame.

CD discs are played back by CDDM. CDDM is composed of the DCDR and AUDF section.

The DCDR section includes the circuits which demodulate the EFM signal (the picked-up RF signal is also called the EFM signal because of the modulation system), generate the clock signal for demodulation, correct errors in the demodulated signals and compensate for time base errors.

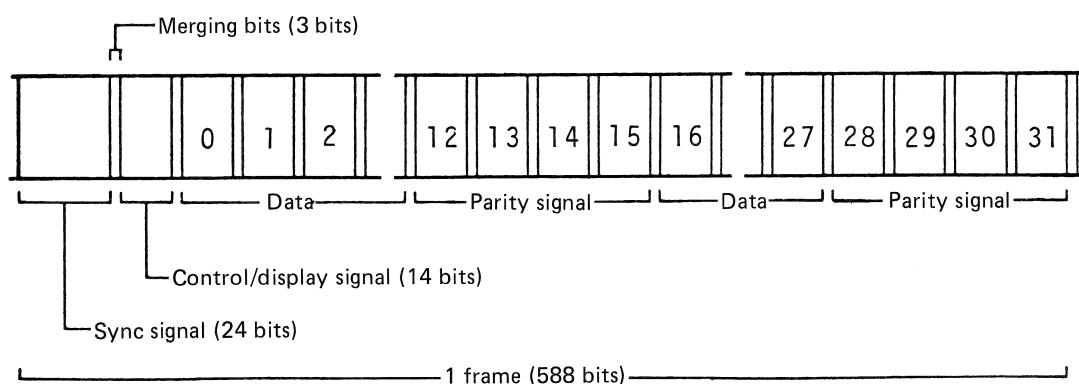


Fig. 10.1 Configuration of a single frame

### 10.1 RF EQUALIZER CIRCUIT

If the RF signal, detected by the pick-up and amplified by the PREB circuit board, is now considered, the high-frequency components are attenuated from the original spectrum. This is because just as the electrical system has certain characteristics with respect to the time frequency, the optical path system also has characteristics with respect to the spatial frequency and these characteristics are such that the delay time is constant.

The Q3, Q4 and Q5 RF equalizer circuit on the LDDB circuit board is installed in order to compensate for these characteristics. Because of this compensation, the aperture in the amplitude direction of the diamond shapes aligned at the center of the RF waveforms becomes larger and the error rate after demodulation is greatly enhanced.

### 10.2 ATC CIRCUIT

The EFM signal loses its low- and high-range frequency components while it is transmitted through the disc and pick-up.

It is thus necessary to return the signal to a form approaching the waveforms produced when encoding the signal before demodulation. With waveforms approaching sine waves, the signals are converted into square-wave digital signal with a high level for when the voltage is higher than the set threshold voltage and a low level for when it is lower.

However, even the EFM signal waveforms differ since the pit configuration is not constant due to the discs and the set threshold cannot be made constant.

Furthermore, the threshold voltage serves to determine the timing when the high level is switched to low and vice versa and thus is an important value in enhancing the error rate at the time of demodulation.

The ATC circuit therefore makes use of the properties of the above-mentioned EFM signal to provide conversion into digital signals which closely resemble what they were when they were encoded by controlling the threshold level.

The RF signal which has passed through the equalizer circuit is capacitive-coupled by C1 and supplied to the inverter circuit connected to the cascade. The inverter's threshold level may be considered to be virtually  $V_{cc}/2 = 2.5V$  and the inverted signals are output in sequence.

The final inverter input/output is connected to the differential amplifier which has a particular time constant. This output biases the capacitive-coupled RF signal. Due to the time constant of the differential amplifier, the bias voltage serves as the value corresponding to the final inverter duty cycle. In cases of a prolonged time in which the RF signal voltage is high (high-level time is long, as the EFM signal, and the duty cycle is higher than 50%), the duty cycle of the final inverter's input waveform is made lower than 50% and that of the output is made higher than 50%. This means that the Z2 (1/2) output drops and that, by pulling down the RF signal in the DC negative direction, the threshold value is increased in relative terms and the output of the final inverter stabilizes at a position near the 50% duty cycle.

Thus, any variation, produced by the disc and pick-up, in the duty cycle of the RFM signal close to the original value of 50% is returned to its original value by returning it to 50% once more.

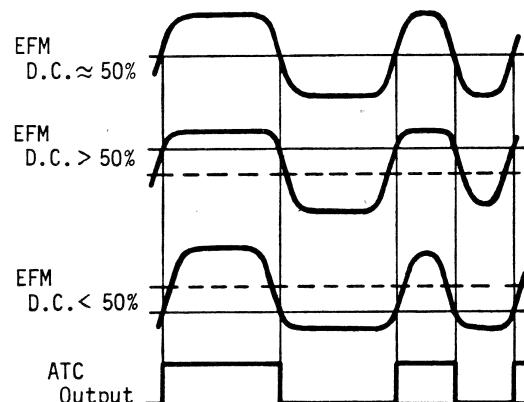


Fig. 10.2 Operation of ATC circuit

### 10.3 RF DETECTOR CIRCUIT

During a search operation the CONT section on the SRVB circuit board performs calculations from the data read from the TOC (which will be described later), it establishes the number of tracks up to the target address and moves the slider as it counts the tracks crossed.

During actual operation it is possible for the laser beam to extend as far as the area (mirror surface part) where there are no pits on the signal surface.

The RF detector circuit monitors the presence of pits on the signal surface by detecting the RF signal.

This output is sent to the CONT section on the SRVB circuit board as the  $\overline{RF}$  signal. The CONT

section knows when the mirror surface part has been reached from this signal and the slider is drawn back to the inner circumference until the  $\overline{RF}$  signal is set low.

Since it is also conceivable that the RF signal will be detected temporarily because of the disc eccentricity or other factors, the  $\overline{RF}$  signal is first set low and then the slider is drawn back with a margin of 5 msec.

#### 10.4 PLL CIRCUIT

Consideration of the frequency spectrum of the EFM signal will reveal that it contains 4.3218MHz components as the bit repeat frequency. The PLL circuit functions to generate continuous signals (PLCK) synchronized with these components.

Q4, D7 and other parts configure an oscillator circuit (VCO) in which the frequency is controlled by means of the supplied voltage. The output is supplied to pin 9 of Z4 (TD6315AP), its frequency is divided by 4 by the frequency divider to form the PLCK signal and this is output from pin 12.

The EFM signal (EFM 2), which has been waveform-shaped by the ATC circuit, is supplied from pin 14. The phases of the EFM 2 signal and PLCK signal are compared inside Z4 with each timing during which the EFM 2 signal is changed from high to low or vice versa. The comparison results are ascertained from the difference in the pulse widths of the two signals which are output from pins 7 and 8. The two pulse signals are added and supplied to the built-in operational amplifier.

The operational amplifier configures a low-band pass filter by C11 and R28 in the feedback circuit and its output serves as the voltage which controls the VCO's oscillation frequency.

In this way, based on the transition timing of the EFM 2 signal, the operational amplifier output (pin 4) voltage is formed whether the PLCK signal phase advances or lags. If the phase advances, for instance, operation ensures that the VCO oscillation frequency is reduced by reducing the voltage and that the phase difference is set to zero.

The PLCK signal is further used as the clock signal for creating the EFMI signal. More specifically, when the EFM 2 signal is connected as the data input and the PLCK signal is connected as the D-type flip-flop clock signal inside Z4, it is possible to obtain an EFM signal in which the transition timing coincides with the PLCK signal rise. This signal is called the EFMI signal and it is output from pin 13.

The  $\overline{G}$  pin (pin 11) is provided to prevent the PLL circuit from malfunctioning. When it is set low, the two pulse signals of the phase error data

are no longer output and both pins 7 and 8 are set to the high-impedance state. When this happens, the voltage charged in C11 does not discharge and so pin 4 maintains its on-going voltage state and the oscillation frequency of the VCO is made constant.

The  $\overline{RF}$  signal and FSPS signal are connected to the  $\overline{G}$  pin. Malfunctioning is thus prevented by keeping the PLL circuit in its on-going state when the EFM signal is not picked up, when the spindle servo is not stable and when dropouts are contained in the EFM signal.

The TMO signal is sent from pin 48 (TC9178F) as the PLCK signal's frequency error data to the PLL circuit.

Based on the maximum non-transition time in the period with the EFM 2 signal, the TMO signal makes a comparison with the time of 11 PLCK signal cycles and this enables rises or drops in the PLCK signal frequency to be judged. When  $f(\text{EFM } 2) > f(\text{PLCK})$ , a low-level signal is output; when  $f(\text{EFM } 2) < f(\text{PLCK})$ , a high-level signal is output. When  $f(\text{EFM } 2) = f(\text{PLCK})$  and when the output is inhibited, the output pin (pin 48) is set to the high-impedance state.

The criterion for judgment may be switched with the input of the pin 43 TMWS signal. When this signal is low,  $11 \pm 1$  cycles of the PLCK signal are made the criterion; when it is high,  $11 \pm 0.5$  cycles become the criterion.

In order to enhance the reliability of the judgment, the TMO signal is output after the same judgment results have been continuous for a certain number of times. The number of check times can be selected by the input of the pin 46 TMGS signal. When this signal is low, the number of times is 7 and when high, it is 4.

In the actual circuit, the  $\overline{ATT}$  signal from the CONT section is connected to pin 43 and the  $\overline{SCAN}$  signal is connected to pin 46. The results judged in this way as the TMO signal are effective in enlarging the capture ratio of the PLL circuit during normal playback. Also, as a criterion for judgment, the picked-up EFM 2 signal is used and so PLL circuit lock-in operations are also prevented at the stage when the spindle motor starts up or at the stage when it is reset from a state of trouble. As a result, the TMO signal output is controlled even by external conditions. When the pin 21 P/S (Play/Stop) signal is low, the TMO signal is made forcibly high; when it is high and the pin 50 TMOE signal is low, the TMO signal output pin (pin 48) is placed in the high-impedance state. The FSPS signal (pin 51), which will be described later, is connected to pin 50.

## 10.5 TC9178F

Z7 (TC9178F) is a special-purpose IC in the CD player system.

Numbering among its main functions are 1) sync signal separation, 2) EFM signal demodulation, 3) subcode signal demodulation, 4) subcode signal P demodulation, 5) subcode signal Q demodulation, 6) CLV servo control signal generation and 7) PLL frequency control signal generation.

Each of the above functions is described below block by block.

### 1) Sync Signal Separation

The CD encoding signal configures a frame in 558T [558T indicates the length of time equivalent to 588 bits:  $588/(4.3218 \times 10^6)$ , which is approximately equal to 136  $\mu$ sec].

A sync signal, known as the frame sync (F.S) signal, is added at the head of the frame. Its pattern is such that it is set high for 11T only and then low for 11T only.

In the sync signal separation block the F.S pattern is first detected by the logic circuit from the EFMI signal supplied from the PLL circuit. Depending on the quality of the EFMI signal, there is a possibility that errors will be detected and a thorough check is undertaken.

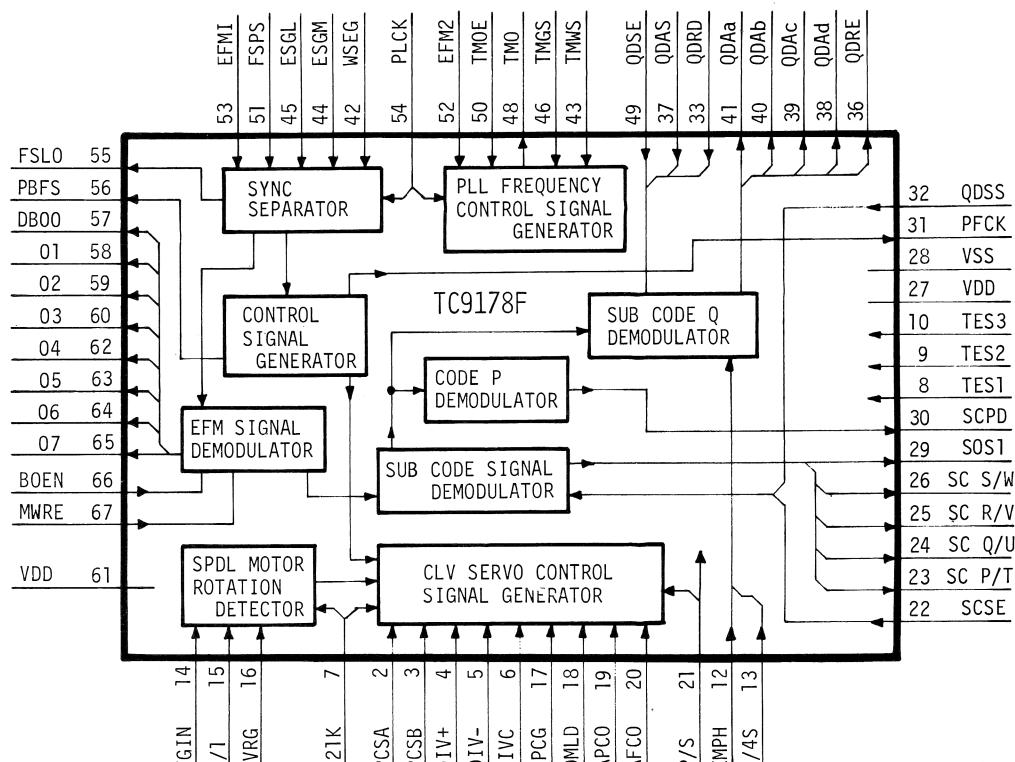
The PLCK signal created by the PLL circuit is supplied to the 588 counter circuit which creates a single detection window signal in the 588 cycles of the PLCK signal. This detection window has a particular time width which is set by the input of the pin 42 WSEG signal. When the WSEG signal is low, the time width is  $\pm 3$  cycles, centered on the 588 count completion timing; when high, the time width is  $\pm 7$  cycles.

When the F.S pattern is detected in the random period) of this detection window, the counter circuit is reset by the detected timing and the PLCK signal counting starts again.

Through a repetition of the above operation it is possible to separate an F.S signal which can depend on every 588T. Besides being used inside the IC, the F.S signal is output to pin 56 PBFS signal.

If the PLL circuit is operating normally, the signal is equivalent to 588T and is detected at the center of the W period. If it coincides precisely with the 588 cycles of the PLCK signal, the pin 55 FSLO signal is set low for the frame period only.

Besides being used inside the IC, the FSLO signal is sent to the CONT section on the SRVB control board and used to control the muting of the audio signals.



When errors, caused by dropouts in the EFM signal, have been detected in the F.S signal pattern outside the W period, they are ignored.

Even when the F.S signal pattern is not detected in the W period, the counter circuit concludes the 588 counting and, at the same, it is automatically reset. However, when the pattern is not detected continuously for several frames, the pin 51 FSFS signal is set high and this is sent to the PLL circuit as the data designating a state of asynchronous. The frame number judged as being asynchronous is determined by a combination of the pin 44 ESGM signal and pin 45 ESGL signal. For both pins 44 and 45 the ATT signal from the CONT section is input and the asynchronous judgment is delayed in the scanning operation.

| ESGL | ESGM | Frame number |
|------|------|--------------|
| L    | L    | 12           |
| H    | L    | 8            |
| L    | H    | 4            |
| H    | H    | 2            |

Fig. 10.4 Switching based on the ESGL and ESGM signals

## 2) EFM Signal Demodulation

As already mentioned, the data signals and parity signals totalling an equivalent of 32 symbols only are included in one frame of the encoding signal. The EFM demodulator circuit serves to return the 14 bits or 1 symbol into the original 8-bit NRZ signal.

The demodulated 32-symbol 8-bit signals are called U0 to U31, respectively: U0 through U11 and U12 through U27 are the data signals while U12 through U15 and U28 through U31 are the error correcting signals.

When the 1-symbol, 8-bit signal is demodulated, it is set in the latch circuit. (The parity signals are demodulated and then inverted.) This serves to complete the preparations with which the data are sent externally and to set the pin 67 MWRE signal low. This signal is supplied to pin 3 of Z6 (TC9179F) which sets the BOEN signal low so that data are sent out.

TC9178F receives this signal at pin 66 and the latch circuit's 8-bit data are output to DBO0-DBO7 (pins 65, 64, 63, 62, 60, 59, 58 and 57) by activating the data bus. These data are input and written into the Z8 HM6116P-4 RAM.

The pin 56 PBFS signal is sent to TC9179F as the data which indicates the boundary between frames.

## 3) Subcode Signal Demodulation

The symbol following the sync signal (F.S) of the encoding signal is the control/display signal, and control/display signals equivalent to 98 continuous frames are integrated to form one block. The 8 bits of the nth frame control/display signal are known as Pn, Qn-Wn ( $n = 0-97$ ) in sequence from the head.

The control/display signal in the head frame of the 98 frames in the block and in the following frame are called S0 and S1, respectively, by the sync signals indicating the start of the block. In other words, P0-W0 designate S0 and P1-W1 designate S1.

The 98-frame signals are integrated for P through W respectively and called channel P, channel Q and so on in each case. These are collectively called the subcode signals.

Among these subcode signals only channel P and channel Q are used at present.

Channel P includes the data as to whether its block is the disc in-track, between-track, lead-in or lead-out area.

Channel Q includes the disc track number, elapsed play time and other data as well as the disc catalog number, copyright code and other attribute data. Included in the lead-in area of the channel Q are the data indicating the contents of the disc known as TOC. Details on TOC will be given later.

The subcode signals are separated and demodulated at the PBFS signal timing and output as the SCP/T, SCQ/U, SCR/V and SCS/W signals (pins 23, 24, 25 and 26). The double signal output is switched by the pin 22 SCSE signal input.

| SCSE | SCP/T | SCQ/U | SCR/V | SCS/W |
|------|-------|-------|-------|-------|
| L    | P     | Q     | R     | S     |
| H    | T     | U     | V     | W     |

Fig. 10.5 Switching based on the SCSE signal

#### 4) Subcode Signal P Demodulation

After the subcode signal channel P has been demodulated, it is not only output as the SCPD( /T) signal but also supplied to the counter circuit in order to enhance the reliability of the subcode signal. Only when the same signal is input continuously for 5 frames is it output at pin 30 as the SCPD signal. However, when S0 and S1 are detected, when the FSFS signal is set high and a frame is started and when the input data pattern is judged as having an error, the counter circuit is reset and the SCPD signal is held at its previous value. The SCPD signal is, however, not used.

#### 5) Subcode Signal Q Demodulation

The 98 bits making up the subcode signal channel Q are described below.

- 0-1 (2 bits): Used for S0, S1.
- 2-5 (4 bits): Called CONTROL, serving as emphasis on/off, 2-channel/4-channel flags.
- 6-9 (4 bits): Called ADR, serving as flags indicating the contents of the following DATA-Q.

ADR=1: Normal mode, details given later.

ADR=2: Disc catalog number

ADR=3: Copyright code, serial No., etc.

- 10-81 (72 bites): Called DATA-Q; when the above ADR is 1, these bits have the following contents in 8-bit units in the program area and lead-out area:

10-17 (TNO): Track number

18-25 (X): Index number in a track

26-33 (MIN): Minute units for time elapsed of the current track.

34-41 (SEC): Second units for time elapsed of the current track

42-49 (FRAME): Number dividing 1 second into 75.

50-57 (ZERO): All zero.

58-65 (AMIN): Minute units for time elapsed from start point of disc's program area.

66-73 (ASEC): Second units for time elapsed from start point of disc's program area.

74-81 (AFRAME): Number dividing 1 second into 75.

In the lead-in area DATA-Q contains the data indicating the disc's program contents. This is known as TOC (table of contents), and this indicates the point, at which the track of the number indicated by bits 18-25 is started, by the 24 bits of 58 through 81. TOC is read out as soon as the play operation is started and it is stored in the register.

- 82-97 (16 bits): Called CRC, the parity signal of the channel Q data.

The 80 bits of the channel Q's CONTROL, ADR, DATA-Q are divided into 20 units of 4 bits each for processing.

First, the sets of 4 bits are written into the internal RAM and CRC-based error detection and correction are undertaken for these data.

Upon completion of the detection and correction, the QDRE signal is high and it outputs the fact that preparations for transmitting the 4-bit data are completed to the CONT section. The QDRE signal is output from pin 36 and it can also be output from pin 41. Pin 41 is used with this system.

Upon receipt of the QDRE signal, the CONT section sends the QDRD signal to pin 33 as the clock signal for data transfer.

In this way, the 4-bit data are transferred to the CONT section as the QDAa-QDAd signals (pins 41-38). From these four pins the above-mentioned QDRE signal and CRC-based error detection results are also output and these double signals are switched by the pin 37 QDAS signal.

| QDAS   | Pin 41       | Pin 40       | Pin 39       | Pin 38    |
|--------|--------------|--------------|--------------|-----------|
| L<br>H | QDRE<br>QDAa | QDEa<br>QDAb | QDEb<br>QDAC | L<br>QDAd |

| QDEa | QDEb | Judgements            | Data output      |
|------|------|-----------------------|------------------|
| H    | H    | No error              | Output directly  |
| L    | H    | 1-bit error in CRC    | Output directly  |
| H    | L    | 1-bit error in Q data | 1-bit correction |
| L    | L    | 2 or more bits error  | Output directly  |

Fig. 10.6 Switching based on QDAS signal

In actual fact, the CONT section first sets the QDAS signal low, and then TC9178F outputs the QDRE signal from the pin 41. The CONT section checks the data output standby in the QDRE's high-level state, and then checks that the data are sufficiently reliable from the error detection results QDEa and QDEb. In addition to this, it switches the QDAS signal to the high level and it demands the data output from TC9178F using the QDRD signal.

Unless the QDRD signal is now sent from the

CONT section, the data output is inhibited by TC9178F setting the QDRE signal low. When the 4-bit data transfer is repeated 20 times and completed, the QDRE signal returns to the low level.

Pins 38 through 41 of TC9178F are connected to the extended I/O port and these connections can be electrically isolated so that the port is used effectively. By setting the pin 49 QDSE signal low, the pin 38-41 outputs are placed in the high-impedance state although this function is not used in this system.

The channel Q CONTROL is output with the 4-bit transfer, these bits are decoded inside the TC9178F and output. In other words, when pre-emphasis is applied to the source signals, the 12 pin EMPH signal is set high and the de-emphasis circuit in the AUDF section is activated. The 2-channel/4-channel flag is output as the pin 13 2/4S signal but this is not used in this system (4 channels are indicated with a high-level 2/4S signal).

The subcode signals are separated in synchronization with the S0 and S1 detection although dependable separation is not possible unless the picked-up EFM signal and TC9178F circuit operations are properly synchronized by the PLL circuit. This is why the subcode signal Q demodulator circuit is provided with functions for checking these synchronizations and expediting the subcode signal separation. The synchronization criterion of this function is switched by the pin 32 QDSS signal. When this signal is high, the subcode signal is read out only if the FSPPS signal is low and both S0 and S1 have been detected properly.

When the QDSS signal is low, the readout of the subcode signal is expedited when the conditions of the high-level setting are met or when the FSLO signal is low and both S0 and S1 have been detected properly. With this system, however, the QDSS signal is fixed at the high level.

## 6) Disc Speed Error Detection

The EFM signals picked up from the disc are demodulated, written in sequence into the Z8 RAM and error correction and other processes are performed by the clock signals generated by the oscillator circuit. The data must therefore be picked up so that no excess or deficiency is produced vis-a-vis the internal clock signals.

In order to control the disc speed accurately, the speed errors are detected from the played back frame sync signal.

Errors are detected for both the frequency and phase.

The frequency error in the played back frames is detected by the number of clock signals in a particular frequency within 4 frames.

The clock signal (2.1168MHz) serving as the reference is input from TC9179F as the pin 7 C21K signal. It is counted for four F.S cycles ( $4/7.35\text{kHz} \approx 544 \mu\text{sec}$ ). When the frequency error is zero, the clock signal is counted 1152 times exactly.

The error detection range is  $1152 \pm 128$  clock signals and any error in this range is output as a pulse-width-modulated digital signal. This is the pin 20 AFCO signal. With errors exceeding the detection range the AFCO does not become a pulse signal. In fact, when the count number is low, or in other words when the disc is rotating too quickly, it is set low and when the count number is high, it is fixed at the high level and output.

When the error count goes out of the  $1152 \pm 128$  clock signal range, the pin 18 DMLD signal is set low and then it is within the  $1152 \pm 64$  clock signal range, it is set high. The DMLD thus detects and outputs the frequency servo lock state with hysteresis.

Phase errors in the frame sync signal are detected by comparing the phase of this signal with that of the reference clock signal which is used to detect phase errors and which is created by counting down the C21K signal.

Errors are detected for each N frame and N is set by combining the PCSA and PCSB signals (pins 2 and 3). In this system, N is made equal to 12 by setting the PCSA signal low and the PCSB signal high.

| PCSA | PCSB | N  | Fc (Hz) |
|------|------|----|---------|
| L    | L    | 6  | 1225    |
| H    | L    | 8  | 918.75  |
| L    | H    | 12 | 612.5   |
| H    | H    | 16 | 459.375 |

$$Fc = 7.35\text{kHz}/N$$

Fig. 10.7 Switching based on the PCSA and PCSB signals

As with the AFCO signal of the frequency error, the detected phase error is output from pin 19 as a pulse-width-modulated signal. This is the APCO signal.

The quantity of data written into the RAM is monitored constantly by TC9179F. When this quantity is either excessive or insufficient with

respect to the norm, TC9179F seeks compensation of the time base with the DIV+ and DIV- signals. These signals are input into pins 4 and 5 of TC9178F and the incremental or decremental number of the countdown, which adjusts the apparent phase error by increasing or reducing the countdown number which creates the reference signal from the C21K signal, can be set by the pin 6 DIVC signal. In this system, it is fixed at the low level and the number is  $\pm 1$ .

The pin 17 APCG signal is provided in order to inhibit the detection of the phase error, which is done by setting this signal low.

It is not possible to detect phase errors accurately unless the frequency servo is in the lock state. Therefore, the DMLD signal which judges the lock for the frequency, is connected to the APCG signal.

When the phase error detection is inhibited, the APCG signal sets the phase error to zero and so its duty cycle is fixed at 50%. When it is set so that the phase of the reference signal coincides with the phase of the detection signal and the inhibiting is released, the phase error is detected smoothly from zero and the servo operation is performed both speedily and stably.

The disc speed error detection block also contains a function for controlling the disc speed using the FG signal but this is not used in this system.

### 7) PLL Frequency Control

This block creates the TMO signal as described with the PLL circuit.

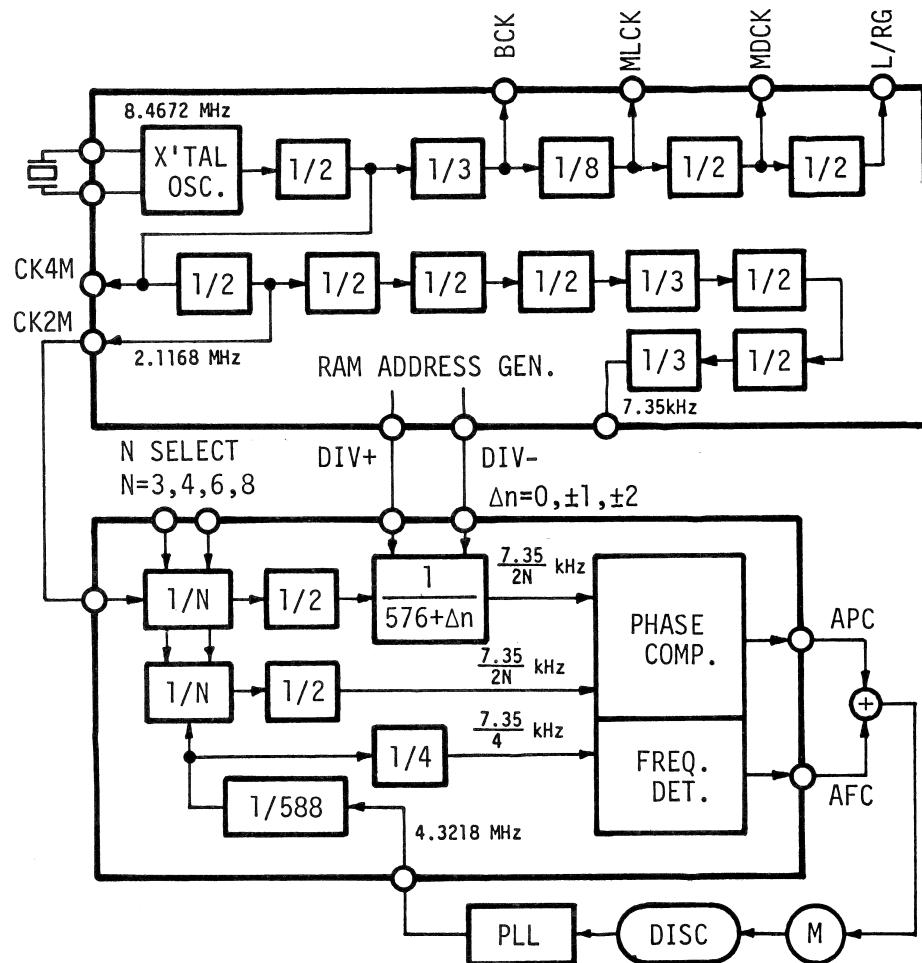


Fig. 10.8 Timing signals and frequency and phase control

## 10.6 TC9179F

In CD player systems the Z6 TC9179F is a special-purpose IC which detects and corrects errors and which absorbs data jitter.

Reference should be made to the P-D1 Technical Information (VRT-017) for details on the theory and processes of error detection and correction.

The main TC9179F functions are: 1) clock signal generation, 2) RAM control, 3) C1 and C2 error correction, 4) data correction, 5) digital attenuation, 6) muting signal generation, 7) data output and 8) data status output.

Each of these function blocks will now be described.

### 1) Clock Signal Generation

The clock signals required inside TC9179F and in TC9178F are produced by connecting crystal oscillator to pins 52 and 53. The pin 54 CKSE signal is input in accordance with the frequency of the connected oscillator. With this system the frequency is 8.4672MHz and so the CKSE signal is set high.

The master oscillation frequency is halved and output as the pin 55 CK4M signal, and then it is halved again and output as the pin 56 CK2M signal. The CK2M signal is sent to pin 7 of TC9178F.

### 2) RAM Control

Upon completion of the EFM signal demodulation, TC9178F is advised by the MWRE signal that the data can be sent out. As a result, TC9179F sets the RAM to the writing mode by the CE1 signal (pin 17) and R/W signal (pin 15), and it requests TC9178F using the BOEN signal (pin 4) to send the data. The address storing the data is controlled by the AD-0 through 10 signals (pins 5-14, 18) which are created with the PBFS signal (pin 2) as the sync signal.

The quantity of data stored in the RAM is monitored constantly and when it is either excessive or deficient with respect to the RAM capacity and its processing capability, the spindle motor is requested to deal with the quantity by the DIV+ and DIV- signals (pins 65 and 64). Normally, both signals are low.

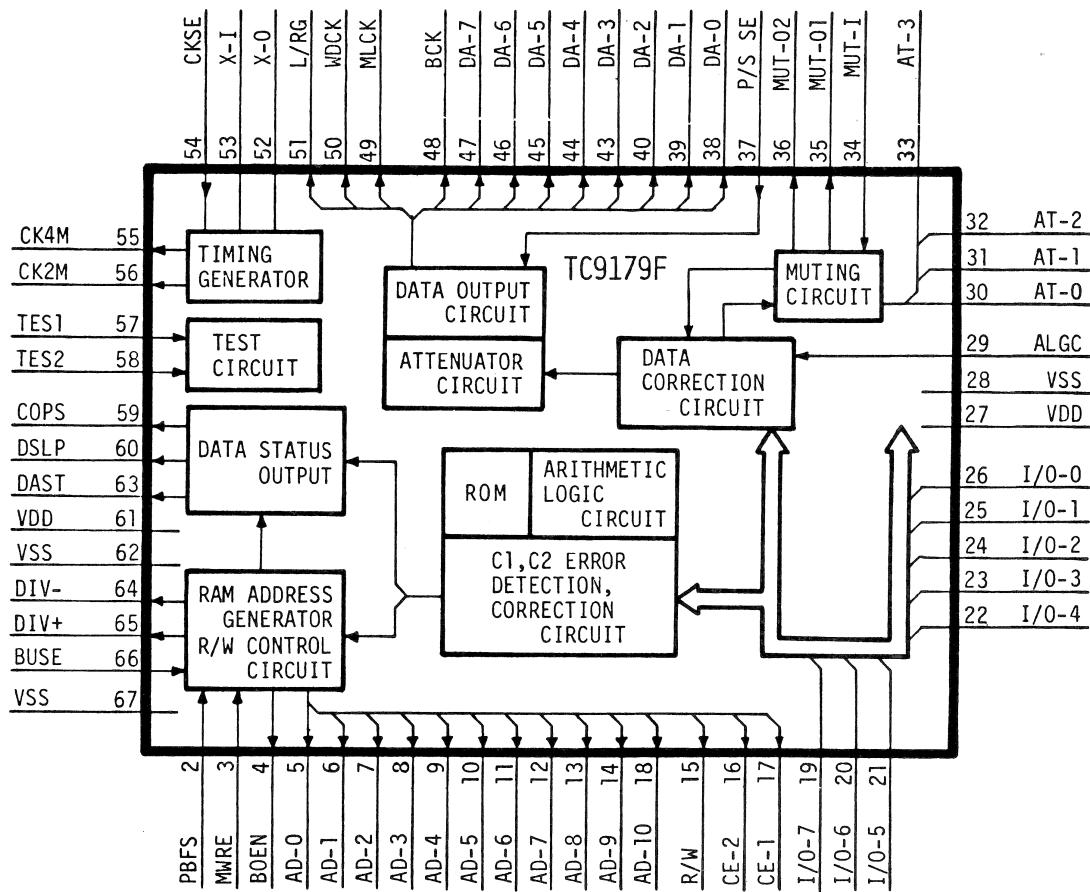


Fig. 10.9 Block diagram of TC9179F

The criterion for judging whether the quantity is too high or too low can be switched by the pin 66 BUSE signal. In this system, the signal is fixed at the low level and the quantity is made equivalent to  $\pm 3$  frames. In other words, when the data quantity is deficient for more than 3 frames, the DIV+ signal is set high; conversely, when it is excessive for more than 3 frames, the DIV- signal is set low.

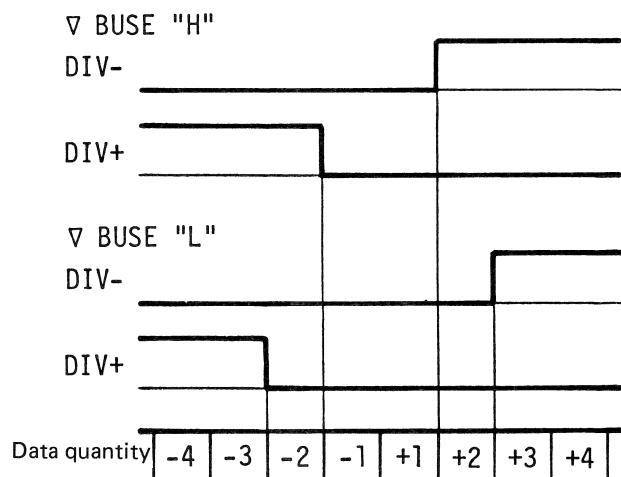


Fig. 10.10 DIV- and DIV+ signals

### 3) C1 and C2 Error Correction

Error detection and correction in the CD player system is conducted by two processes, known as C1 and C2.

In order to safeguard against part of the continuous sampling data from being lost in a group during the encoding process, the data's continuity is broken up and the data are dispersed by a sequence of three difference stages. This dispersion is called interleaving and with decoding the data must be reconstituted (de-interleaved) by the reverse sequence.

First is de-interleaving which forms the initial stage in which a delay equivalent to one frame is provided at every other symbol and the data are read out from the RAM. The odd number order symbols therefore become the data prior to one frame and by this process the C1-corrected frame is reconstituted.

In the C1 process, the 28th-31st order parity symbols (P parity) among the reconstituted frames are used for correction. However, the C1 correction is undertaken only when the errors among the 32 symbols in one reconstituted frame are in 2 or less symbols. If errors in 3 or more symbols are

detected, they are not corrected and the C1 error pointer of all the symbols including the symbols whose errors have not been detected is set. When errors are in two symbols, then there is a theoretical possibility that correction itself will be erroneous and the pointer is set, besides the errors being corrected.

In other words, when two or more error symbols are detected, the error pointer is set for all the symbols in the frame and the attribute of having low dependability as data is referred to in the C2 process.

The P parity used for correction in the C1 process is discarded here and a frame is hereafter treated as 28 symbols.

Symbols whose errors are detected and corrected are returned to the RAM and rewritten.

Next, a delay equivalent to  $4n$  frames is provided in the nth order symbols for the 28 symbols and they are read out from the RAM. This means that the 0th order symbol from a particular frame, the 1st order symbol from the 4 previous frames, etc. as far as the last 27th order symbol from the  $4 \times 27 = 108$  previous frames are read out and that a C2-corrected frame is created.

(This is the second stage de-interleaving process.)

In the C2 process, errors are corrected using the 12th-15th order parity symbols (Q parity) among the frames reconstituted in this way. The C2 correction can be undertaken with errors in up to 3 symbols among the 28 symbols.

The C1 error detection results are ascertained from the C1 error pointer of these symbols and the C2 correction process is undertaken only when there is a low probability that the correction itself will be performed erroneously while these results are contrasted with its own error detection. If the symbol data are not very dependable, the C2 error pointer is set as with C1 and the error symbols inside the RAM are written as corrected symbols.

The C2 error pointer is set while the C1 error pointer is checked and when the pin 29 ALGC signal is high, the C1 pointer is copied as it is. In actual fact, the ALGC signal is set high during scanning operations.

| Dn+1         |             |             | Dn           |                            |             | Output data                |  |                    |
|--------------|-------------|-------------|--------------|----------------------------|-------------|----------------------------|--|--------------------|
| MSB<br>-30dB | MSB<br>C2EP | LSB<br>C2EP | MSB<br>-30dB | MSB<br>C2EP                | LSB<br>C2EP | Processing                 |  | Processing details |
| x 0 0        | x 0 0       |             | x 0 0        | 0 0 1                      |             | Dn                         |  | Direct             |
| x x x        | 0 0 1       |             | x 1 x        | (Dn-1/2)+(Dn+1/2)          |             | Dn(MSB+80H)                |  | Direct             |
| x 0 0        | x 1 x       |             | x 1 x        | (Dn-1/2)+(Dn+1(MSB+80H)/2) |             | (Dn-1/2)+(Dn+1/2)          |  | Mean average       |
| 0 0 1        | x 1 x       |             | x 1 x        | (Dn-1/2)+(Dn+1(MSB+80H)/2) |             | (Dn-1/2)+(Dn+1/2)          |  | Mean average       |
| 1 0 1        | x 1 x       |             | x 1 x        | Dn-1                       |             | Dn-1                       |  | Previous value     |
| x 1 x        | x 1 x       |             | x 1 x        | Dn-1                       |             | Dn-1                       |  | Previous value     |
| x 0 0        | 1 0 1       |             | 1 0 1        | (Dn-1/2)+(Dn+1/2)          |             | (Dn-1/2)+(Dn+1/2)          |  | Mean average       |
| 0 0 1        | 1 0 1       |             | 1 0 1        | (Dn-1/2)+(Dn+1(MSB+80H)/2) |             | (Dn-1/2)+(Dn+1(MSB+80H)/2) |  | Mean average       |
| 1 0 1        | 1 0 1       |             | 1 0 1        | Dn-1                       |             | Dn-1                       |  | Previous value     |
| x 1 x        | 1 0 1       |             | 1 0 1        | Dn-1                       |             | Dn-1                       |  | Previous value     |

Dn: Processing word data

Dn-1: Word data already output before processing word data

Dn+1: Word data after processing word data

MSB-30dB: "1" is set when MSB data is -30dB or less.

MSB C2EP: MSB data C2 error pointer ("1" is set when errors cannot be corrected)

LSB C2EP: LSB data C2 error pointer ("1" is set when errors cannot be corrected)

MSB+80H: LSB is set in 80H (1000 0000)

Fig. 10.11 Data correction

#### 4) Data Correction

As per the specifications, the C2-corrected data are scrambled and delayed by 2 frames. (This constitutes the third stage of de-interleaving.)

The data are sent in sequence from the LSB side 8 bits in the output word order. When they are output, the C2 error pointer is checked and selection is made in accordance with the reliability of the data as to whether the data should be output directly, whether mean average correction should be performed using the data before and after or whether the previous data should be output again. This selection is undertaken in consideration of the level when the MSB and LSB data C2 error pointers and MSB data are converted into audio signals.

#### 5) Digital Attenuation

The level when the TC9179F output is converted into audio signals can be set digitally by the AT-3 ~ 0 signals (pins 33-30). The attenuation corresponds to the digital value of the 4 bits of which the AT-3 signal is responsible for the MSB and the AT-0 signal for the LSB. However, due to the negative logic, "1111" is 0dB and '0000' is infinity zero.

During scanning, the AT-0, AT-1 and AT-2 signals are set low by the ATT signal sent from the CONT

section and so an attenuation of -12dB is produced. When the MUT-01 signal (which is described later) is set low, only AT-3 is set low and an attenuation of -14.5dB is produced.

| AT-0 | AT-1 | AT-2 | AT-3 | (dB)   |
|------|------|------|------|--------|
| 1    | 1    | 1    | 1    | 0      |
| 0    | 1    | 1    | 1    | - 1.15 |
| 1    | 0    | 1    | 1    | - 2.5  |
| 0    | 0    | 1    | 1    | - 4.0  |
| 1    | 1    | 0    | 1    | - 6.0  |
| 0    | 1    | 0    | 1    | - 8.5  |
| 1    | 0    | 0    | 1    | -10.1  |
| 0    | 0    | 0    | 1    | -12.0  |
| 1    | 1    | 1    | 0    | -14.5  |
| 0    | 1    | 1    | 0    | -18.0  |
| 1    | 0    | 1    | 0    | -24.0  |
| 0    | 0    | 1    | 0    | -30.0  |
| 1    | 1    | 0    | 0    | -36.1  |
| 0    | 1    | 0    | 0    | -48.2  |
| 1    | 0    | 0    | 0    | -60.4  |
| 0    | 0    | 0    | 0    | - ∞    |

Fig. 10.12 Attenuation with AT-0 through 3 signals

Pins 33 through 30 are input/output pins which switch between input and output with the pin 50 WDCK signal (88.2kHz) as the clock signal. The AT-3 through AT-0 signal settings are read when the WDCK signal is high and when it is low, the attenuation state is output.

Sudden data abnormalities are corrected by the above data correction function. However, for continuously abnormal signals where such short-term signals appear repeatedly, the repeat frequency becomes an audible noise and, furthermore, with long-term abnormalities, ill effects are produced such as direct current being output. Yet when these abnormalities are detected and the output is inhibited instantaneously, these signals have a low quality as far as the hearing is concerned.

For this reason fade-out and fade-in functions are provided which serve to switch natural muting on and off.

The MUTE signal is connected to pin 34 from the CONT section and it is supplied as the MUT-I signal. When this signal is low, muting is conducted gradually over 7 steps every 16 frames. Muting from 0dB to infinity zero is conducted at 1.36msec. When the MUT-I signal is set high, the muting is gradually returned to 0dB in the same way.

## 6) Muting Signal Generation

Apart from the muting command output from the CONT section, TC9179F detects internally the state in which muting is to be performed. When data errors which cannot be corrected continue for more than a certain number of frames and when the excessive or insufficient RAM data quantity reaches a range where it cannot be absorbed by the spindle motor, the pin 35 MUT-01 signal is low and -14.5dB muting is applied.

When de-interleaving is erroneous for 3 times in succession, the MUT-02 signal is low although this signal is not used.

## 7) Data Output

The audio signal data processed by TC9179F can be output in serial or parallel format. The format is selected by the pin 37 P/SSE signal. In this system, this signal is set high for serial transfer.

The data are transferred in sequence from the 16-bit MSB and output as the pin 47 DA-7 signal. The bits are synchronized with the pin 48 BCK signal and a change is made to the following bit at the rise timing. The pin 50 WDCK signal is inverted every 8 bits and 1 symbol, and 1 word starts at the rise timing. The pin 51 L/RG signal is inverted every word, with a low level indicating the left channel signal and a high level the right channel signal.

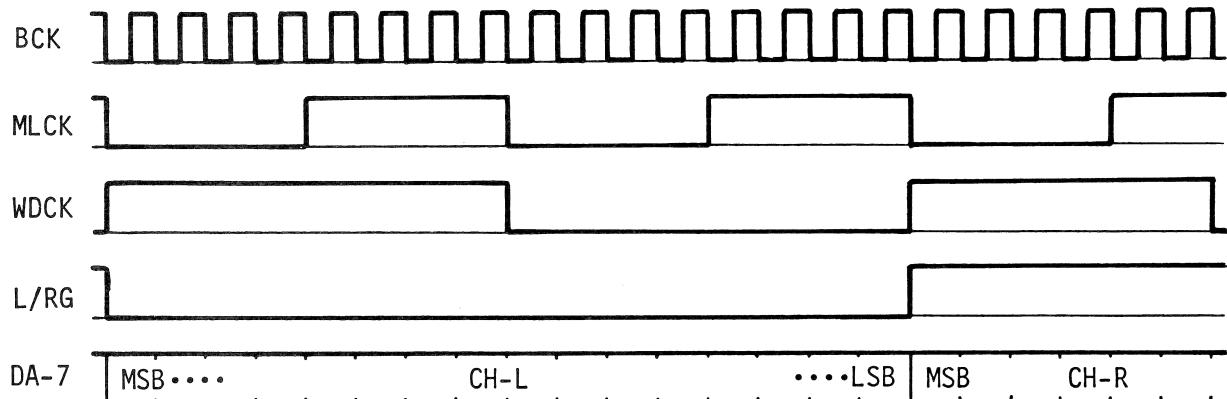


Fig. 10.13 Serial data output timing chart

### 8) Data Status Output

The signal for monitoring externally the error detection results of the C1 and C2 correction and the RAM data quantities is created at the data status output.

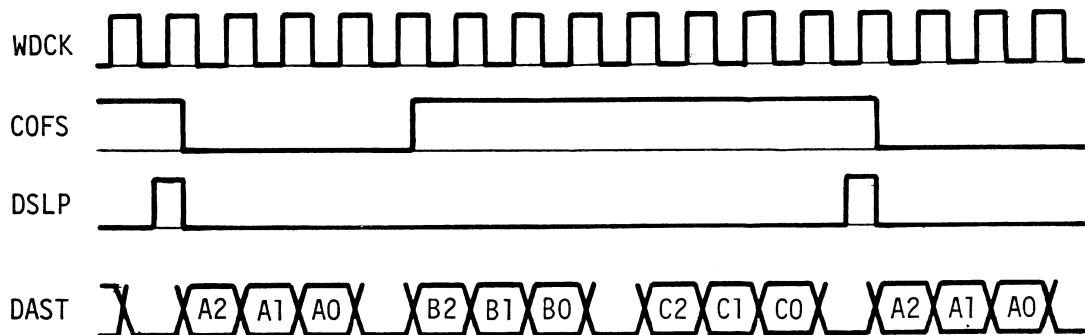


Fig. 10.14 Data status output timing chart

- A0,A1 and A2 indicate the data quantities inside the RAM.

| A0 | A1 | A2 | Data quantity |
|----|----|----|---------------|
| 0  | 0  | 0  | -4 frames     |
| 1  | 0  | 0  | -3 frames     |
| 0  | 1  | 0  | -2 frames     |
| 1  | 1  | 0  | -1 frame      |
| 0  | 0  | 1  | +1 frame      |
| 1  | 0  | 1  | +2 frames     |
| 0  | 1  | 1  | +3 frames     |
| 1  | 1  | 1  | +4 frames     |

- B0,B1 and B2 indicate the error detection results with C1 correction.

| B0 | B1 | B2 | Contents                     | Correction | C1EP |
|----|----|----|------------------------------|------------|------|
| 0  | 0  | 0  | No error                     | ---        | 0    |
| 1  | 0  | 0  | 1 symbol error               | 1 symbol   | 0    |
| 1  | 1  | 0  | 2 symbols error              | 2 symbols  | 1    |
| 0  | 0  | 1  | Error detection not possible | ---        | 1    |

- C0,C1 and C2 indicate the error detection results with C2 correction.

| C0 | C1 | C2 | Contents                     | Correction | C2EP |
|----|----|----|------------------------------|------------|------|
| 0  | 0  | 0  | No error                     | ---        | 0    |
| 1  | 0  | 0  | 1 symbol error               | 1 symbol   | 0    |
| 0  | 1  | 0  | 2 symbols error              | 2 symbols  | 0    |
| 1  | 1  | 0  | 3 symbols error              | 3 symbols  | 0    |
| 0  | 0  | 1  | Data correction not possible | ---        | 1    |
| 1  | 0  | 1  | Uncorrectable frame          | ---        | A    |

A : A=1 (ALGC=low )  
A=C2EP (ALGC=high)

Fig. 10.15 Contents of data status signal

### 10.7 CD/SPINDLE MOTOR DRIVE CIRCUIT

When the loop of the focus servo circuit on the SRVB circuit board closes, the FOCS LOCK signal is sent to LOLB and CDDM. Z1 (PD3032) on the LOLB circuit board sets pin 32 (B port 7 bits) high. As a result, Q6 is turned off, after which Q7 is driven into conduction, and the switch based on the Q8 FET is set to the closed state.

The FOCS LOCK signal sent to CDDM is further sent to Z24 and Z25 and the spindle motor starts rotating in the forward direction by the differential pulses created by C33.

The FOCS LOCK signal inverted by Z24 is supplied to pin 21 of Z7 (TC9178F) as the P/S signal. The circuit for detecting frequency errors starts operating by the pin 21 P/S signal being set high but since the motor speed is still slow, the AFCO signal is kept fixed at the high level and the frequency servo is not locked and so the APCO signal is fixed at a duty cycle of 50%.

The FSPS signal is, naturally, high and the  $\bar{G}$  pin of the PLL circuit is low which means that the PLL operation is inhibited. During this time the AFCO signal is high and so the spindle motor starts accelerating at maximum capacity.

Shortly thereafter until the F.S. signal pattern is detected, the FSPS signal is low, the PLL circuit starts operating and the TMO signal output is permitted.

When being frequency-locked is judged from the PBFS signal, the DMLD signal is high, the phase servo also starts operating and it reaches a stable state.

Since both the AFCO and APCO are pulse-width-modulated signals, they are converted into level data by the low-pass filter.

When the stop mode is established, the FOCS LOCK signal is high. When, further, the Z7 P/S signal is low, the AFCO signal is fixed at the low level.

However, Q8 on the LOLB circuit board is kept on for approximately 0.5 sec. by the integrating circuit, and a drive input of the reverse direction is supplied to the spindle motor which then decelerates rapidly. When it stops during playback at the outer circumference, the playback speed is low and so after stopping, it reaches the region where it rotates in reverse.

VR1 of the integrating circuit serves to adjust this braking time and to set the time until the spindle motor stops at the inner and outer circumferences to the same level.

| P/S | OVRG   | AFCO | APCO             |
|-----|--------|------|------------------|
| L   | L or H | L    | D.C.=50%         |
| H   |        | L    | Normal operation |

Fig. 10.16 Frequency and phase servo inhibiting

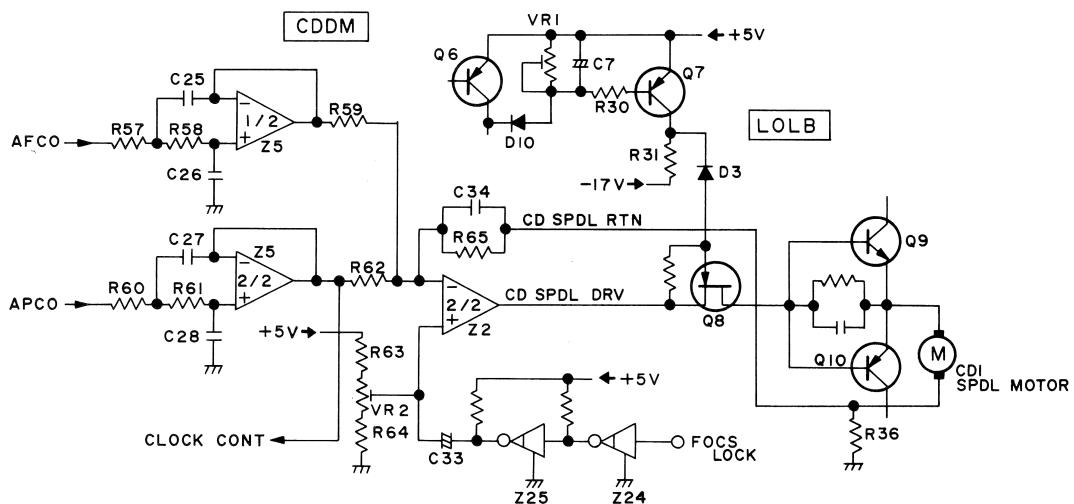


Fig. 10.17 CD/spindle motor drive circuit

## 10.8 D/A CONVERTER CIRCUIT

The digital data demodulated at the DCDR section are sent to the AUDF section as the serial signal. In order to indicate the data timing, the BCK signal, L/RG signal and WDCK signal are all sent along with the digital data. The BCK signal is the bit clock signal ( $0.71\mu s$  cycle) and the WDCK signal is the word (16 bits) clock signal ( $11.4\mu s$  cycle). The L/RG signal is inverted word by word and it indicates the left and right channels.

Z13 (CX-20017) in the AUDF section is a special-purpose D/A converter IC for CD player systems. The data and other signals are first input into Z13. The D/A conversion operations, consisting of the data storage, integration using the stored data and sending of the integrating signal, are repeated word by word. A time equivalent to 3 words is required for D/A conversion and the present data are delayed by a time equivalent to 2 words and output.

The various operations are described below centering mainly on the left channel signals.

### 1) Data Storage

The data are sent in sequence from the MSB, the 16 bits are divided into the high-order 8 bits and low-order 8 bits and these are respectively stored in separate registers.

### 2) Integration Using Storage Data

The WDCK signal is inverted by Z18 (TC40H004P) 2/6 and supplied to pin 8 of Z13 as the WCLK signal and also to pin 12 as the CC signal.

When the WCLK signal is low, the register circuit contents are sent to the latch circuits. When the CC signal is low, the DCL signal at pin 23 is high (0V) for about  $2\mu s$ , the switch composed of the Q10 FET closes and the C50 charge is discharged. At the same time, the data in the latch circuits are sent to the counter circuits where they become the preset values.

Using the counter circuit outputs, the high-order and low-order bit circuits control the constant-current circuit switches. The two current values output from the constant-current circuits are set in proportion to the current flowing to pin 16 and the current controlling the high-order bits is 256 times higher than that controlling the low-order bits.

The two switches are closed when the counter circuit presetting is completed.

When the DCL signal returns to low (negative potential), Q10 is switched off. At the same time, the counter circuits start the countdown of the clock signal (30MHz) inside the IC from the preset value, and C50 is charged linearly by the constant current.

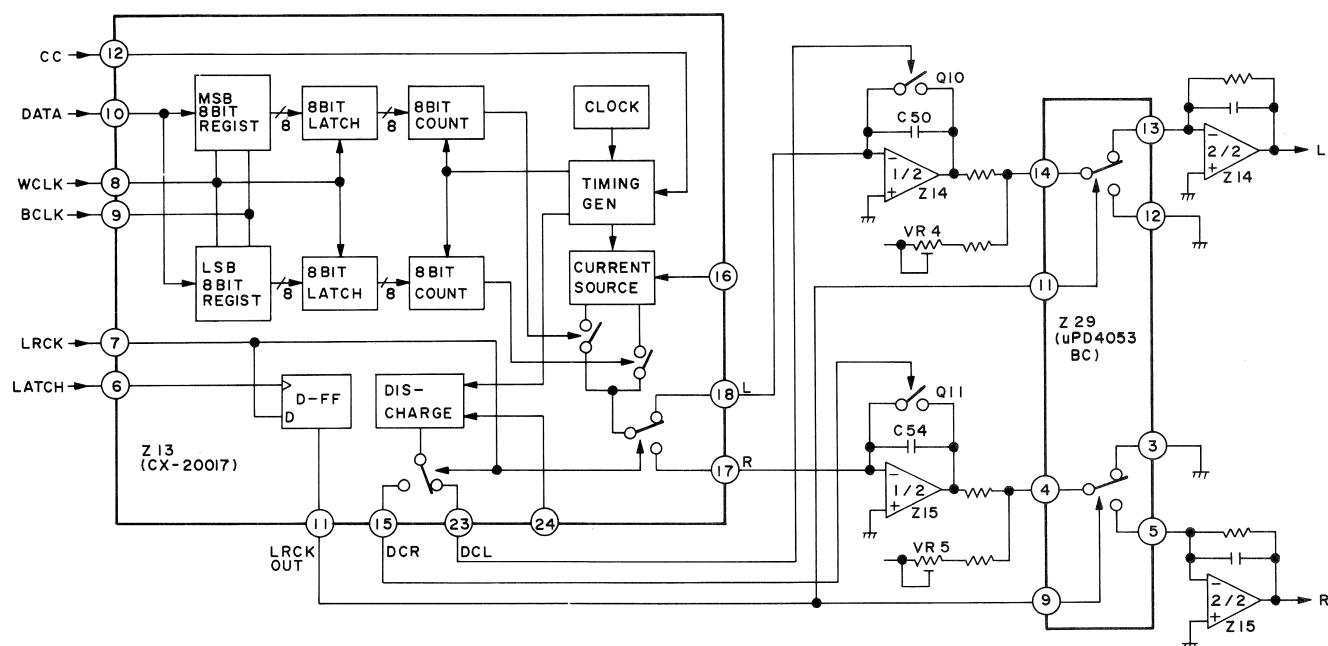


Fig. 10.18 D/A converter circuit

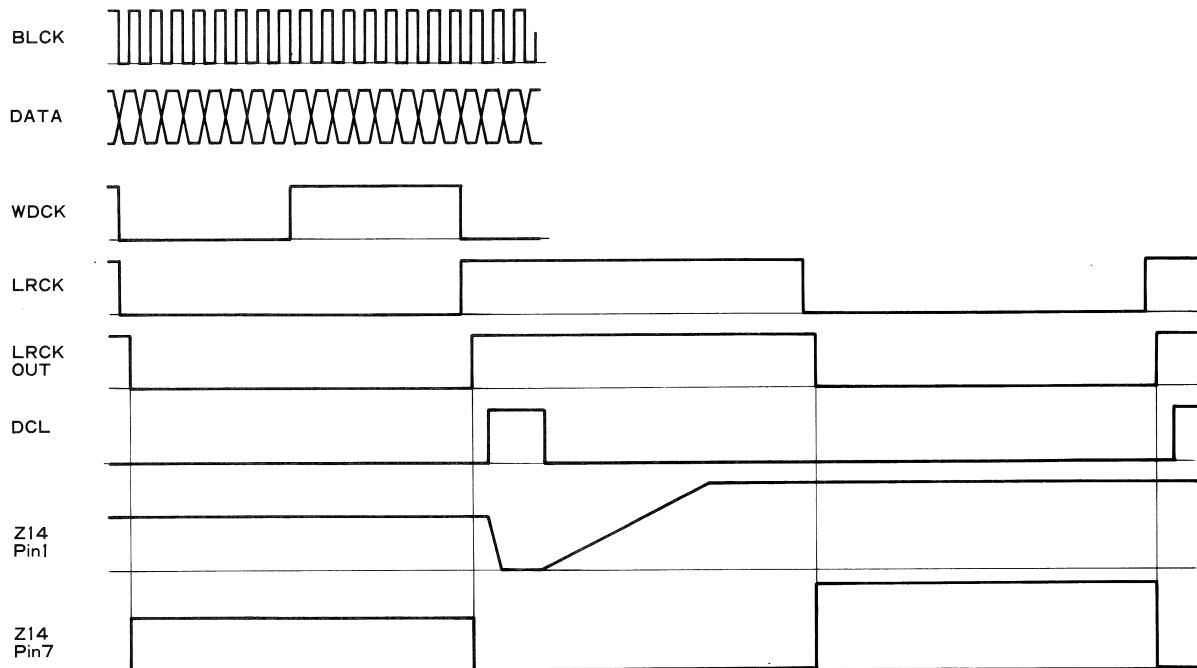


Fig. 10.19 D/A conversion

When the count is completed, the 11 clock offset is first provided and then the constant-current circuit switches are turned off.

This means that the two constant-current circuit currents are added together and output from pin 18 only for a period of time corresponding to the data, and that a voltage appears in the Z14 1/2 output by the charging of C50. The charging is approximate and rapid from the high-order bits but exact and gentle from the low-order bits.

### 3) Integrating Signal Sending

When the LRCK signal is next low, the pin 11 LRCK OUT signal is low and the voltage produced by integration is sent out through Z29 ( $\mu$ PD4053BC).

When the LRCK signal contains jitter, an error arises in the D/A conversion. For this reason, the jitter is absorbed by passing the signal through the D-type flip-flop whose pin 6 LATCH signal (same as BCLK signal) is made a clock signal.

The signals produced by a repetition of these operations are pulse-amplitude-modulated digital signals called PAM signals. Since they include sample frequency components, upper and lower side band components and high-frequency components as noise, this noise is filtered out by passing the signals through the F1 low-pass filter.

F1 is an active filter with a cut-off frequency of 20kHz and extremely sharp characteristics.

### 10.9 DE-EMPHASIS, AUDIO SWITCH CIRCUITS

The analog converted audio signals are amplified by Z16 (NE5532P) 1/2. This circuit also contains a de-emphasis function.

During the recording of CD discs and LDD discs, which will be described later, constant pre-emphasis may be performed whereby the high-range components of the source signals are raised. In such cases, the code indicating this is recorded into the Q channel of the disc's subcode signal. The EMP signal sent to the AUDF section is set low (normally about +11V at the high level) by the readout of this code at Z7 (TC9178F) of the DCDR section.

The Z6 1/2 amplifier circuit is provided with de-emphasis characteristics through the switch being closed by the relay RL4.

The EMP signal is low when the SCAN key on the remote control unit is pressed and this serves to suppress the undesirable high-range noise accompanying the scanning operation.

Relays RL1, RL2 and RL3 are provided to switch the audio signals which are output to the rear panel's AUDIO 1 OUT connector.

RL1 is controlled by the AUD 1/L SQ signal, RL2 by the AUD 2/R SQ signal and RL3 by the DIGITAL signal. The control signals are output from the CONT section, and both the AUD 1/L SQ and AUD 2/R SQ signals are inverted through the DEMB circuit board and sent to CDDM.

The DIGITAL signal is low with both CD discs and LDD discs. However, with LDD discs the signal is not low when the VIDEO DISC AUDIO switch is set to the ANALOG ONLY position. In such cases and in cases where LD discs are used, audio signals which have been demodulated by the DEMB circuit board are output to the AUDIO 1 OUT connector.

The level of the same signal as that output to the AUDIO 1 OUT connector is adjusted in the HPVB circuit board, and the signal is amplified by Z1 (NJM4560DX) on the HPJB circuit board and output to the PHONES jack.

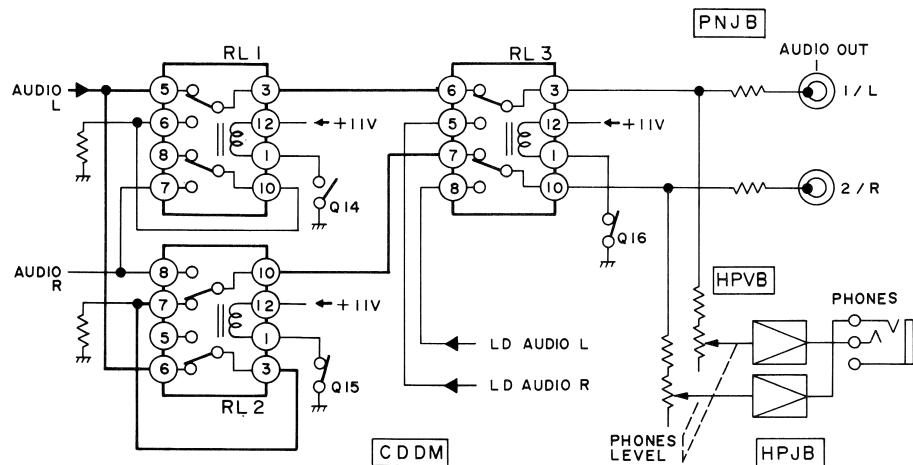


Fig. 10.20 Audio switch circuit

## 11. DESCRIPTION OF LDD PLAYBACK CIRCUITRY

LaserVision with digital sound discs, abbreviated here to LDD discs, are discs in which the encoded PCM signals have been inserted by the compact disc format into the empty frequency band below 2MHz in the spectrum of the signals recorded onto the LD discs.

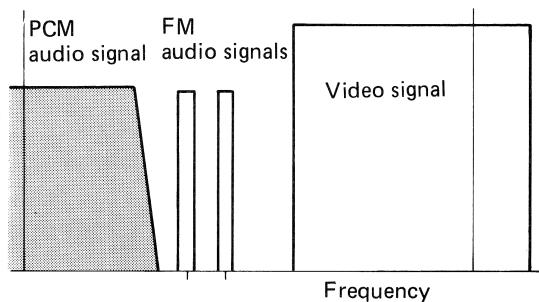


Fig. 11.1 LDD disc spectrum

The main specifications of the LD discs still apply without modification and so the servo circuitry for the playback of LDD discs functions in the same way as with LD discs.

Furthermore, the playback circuitry of the CD discs can be used virtually without modification for signal decoding.

The picked-up RF signals are first supplied to the LDDB circuit board.

They are amplified by Q12, the components of the video signals and FM audio signals are then suppressed by the 1.75MHz low-pass filter and only the PCM RF signals (EFM signals) are separated.

The signals are then de-emphasized (R22, R23, C17), amplified by Q9 and Q8 and then sent to CDDM.

LDDB is also provided with RF equalizer circuits for the CD discs. Their operation is such that the power to these circuits is turned on and off by the LD/CD signal and only one of these circuits is selected.

The most salient problem with LDD disc playback consists in the disc speed being controlled by the LD playback signal only.

As has already been mentioned, the speed of CD discs is controlled so that the phase and frequency of the frame sync signal, which has been separated from the EFM signal, are synchronized with the phase and frequency of the reference signal. LDD discs, too, cannot be played back unless the frame sync signal is synchronized with the reference signal.

This is why CDDM is provided with a circuit which synchronizes the reference signal with the playback frame sync signal using the APCO signal (pin 19 of Z7 TC9178F). The APCO signal is the data of the phase difference between the playback frame sync signal and reference signal.

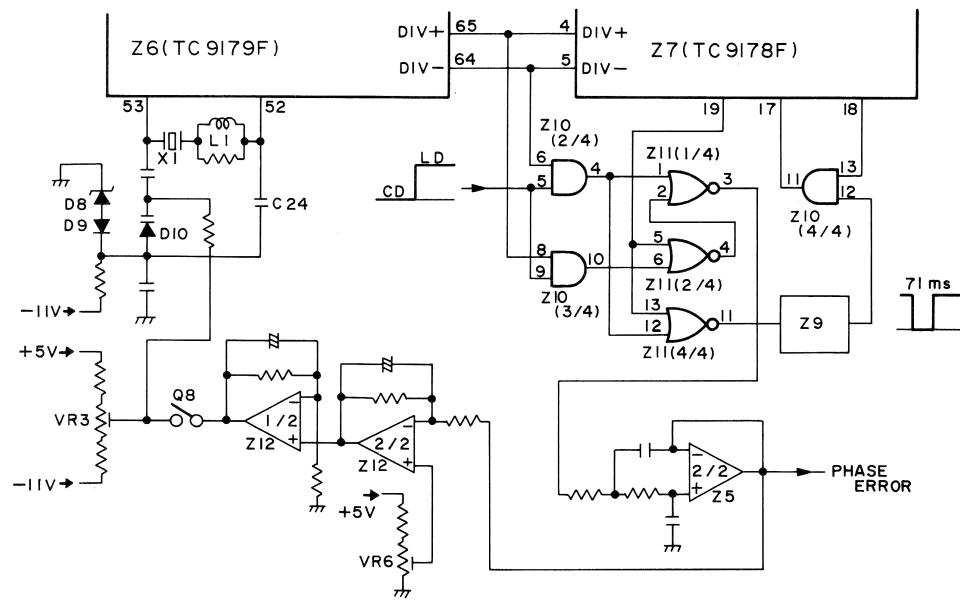


Fig. 11.2 Control circuit of reference signal frequency

The APCO signal passes through the logic circuit (which will be described later), which is configured with Z10, Z11 and other parts, and it is converted into a voltage signal from a pulse-width-modulated signal by the low-pass filter composed of Z5 2/2. The components in this signal generated by disc eccentricity are suppressed by the low-pass filter composed of Z12 (BA4558DX) 1/2 and 2/2, and the signal is then passed through the Q8 switch, which has been turned on by the LD/CD signal, to become the control signal of the voltage-controlled crystal oscillator (VCXO circuit).

When a CD disc is being played back, Q8 is turned off and the VCXO circuit frequency is made 8.4672MHz by the voltage which is set by VR3. With LDD discs, this frequency is controlled by a variable width of about  $\pm 3\text{kHz}$  centering on this frequency. With CD discs, the quantity of data stored in the RAM is kept constant by controlling the disc speed but this is not possible with LDD discs.

Because of this, a logic circuit composed of Z10, Z11 and other parts is installed.

When the RAM data quantity is deficient for 3 or more frames, the Z6 (TC9179F) DIV+ signal is high. This makes the Z11 pin 3 high regardless of the APCO signal. This in turn causes the oscillation frequency of the VCXO circuit to drop, the frequency of the playback signal to rise in relative terms and the RAM data to be made sufficient.

Conversely, when the RAM data quantity is excessive for 3 or more frames, the DIV- signal is high. Thus, the Z11 pin 3 signal is low, the frequency of the VCXO circuit rises, processing is accelerated and the RAM data are returned to normal.

Once the RAM data quantity returns to normal ( $-2$  to  $+2$  frames), the DIV+ signal or DIV- signal returns to low.

By setting either signal low, Z9 (SN74LS221N) 1/2 is triggered and the Z7 pin 17 APCG signal is set low temporarily. The APCO signal is fixed at a duty cycle of 50% (phase difference of zero) by the APCG signal being low and after the VCXO circuit frequency is returned to its center value, phase comparison is resumed.

The CDDM PLL circuit generates a continuous signal (PLCK signal) which is synchronized with the 4.3218MHz repeat frequency of the bits in the EFM signal and components close to this frequency are generated in the EFM signal on the unrecorded sections of the disc such as the areas between tracks.

If the search is terminated at an unrecorded section when it is no longer possible for the PLL circuit to maintain a state of synchronization by the search operation, a state of synchronization is established in error between the played-back signal frequency, which is not 4.3218MHz, VCXO frequency. This is called erroneous locking of the PLL circuit.

When this happens with a CD disc, the FSPS signal is high and the Z4 (TD6315AP) pin 11 is set low without the frame sync signal having been detected. This places Z4 pins 7 and 8 in the high-impedance state, the pin 4 voltage is held at the value immediately before by C11 and the VCO frequency is fixed.

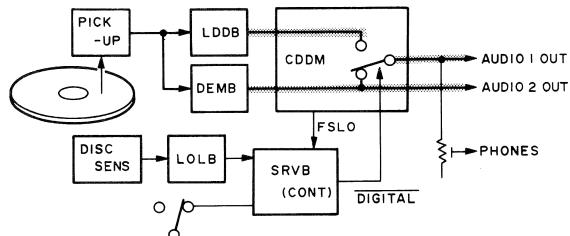
During this period the disc rotates in an irregular state and when in due course the bit repeat frequency is equal to the fixed frequency of the VCO circuit, the FSPS signal becomes low and the PLL circuit can be reset to the synchronized state.

When an LDD disc is played, the disc speed is stable irrespective of the PCM signal and so resetting is not possible using this process.

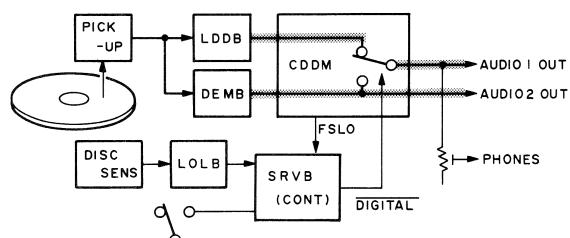
Therefore, the FSPS signal is isolated by Z10, Z9 2/2 is triggered at the SCAN signal fall, or in other words upon completion of the search, the Q5 switch is closed and the control input voltage of the VCO circuit is forcibly set to +5V. As a result, the frequency of the VCO circuit becomes virtually 4.3218MHz.

Since the disc is rotating stably, the bit repeat frequency can also be considered stable, the frequency is made equal and the PLL circuit can be reset to the synchronized state.

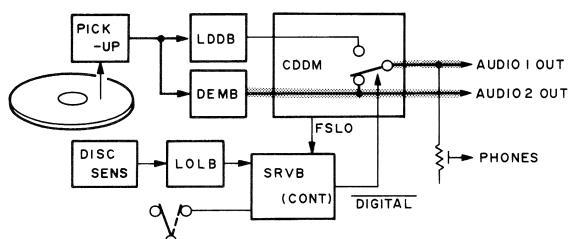
D5, D6 and Q3 connected to the VCO circuit control input are provided in order to limit the voltage so that the control voltage of the VCO circuit does not fall excessively and that the circuit does not stop oscillating when an LDD disc is played back.



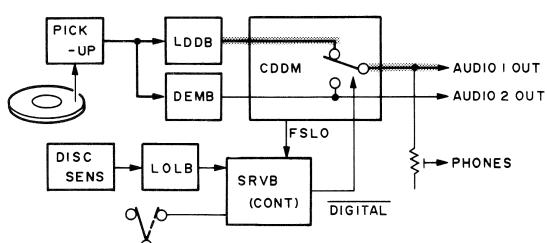
1) Output with ANALOG ONLY using an LDD disc



2) Output with AUTO DIGITAL using an LDD disc



3) Output using an LD disc



4) Output using a CD disc

Fig. 11.3 Audio signal output

## 12. DESCRIPTION OF CONTROL SYSTEM

### 12.1 DESCRIPTION OF HARDWARE

The CLD-900 system control centers on the LOLB circuit board and CONT section on the SRVB circuit board.

A brief description of the devices used now follows.

#### 1) Z9 (HD6305X2P)

Z9 in the CONT section is the main CPU. It is a 6305-type 8-bit CMOS IC containing a 128-byte RAM.

Its operating clock frequency is 4MHz.

This IC has three 8-bit I/O ports and an input port (7 bits) and the 0 through 5 bits (B0-B5) of the B port are connected to the data bus.

The data are transferred between the main CPU, and the sub-CPU, decoder IC and display IC, which will be described below, in this data bus and the operations are controlled by the statuses of the B6, B7, A0 and D7 ports as far as the main CPU is concerned.

#### 2) Z8 (VYW-061)

Z8 is an 8k-byte EPROM in which the main CPU's control program has been written.

#### 3) Z7 ( $\mu$ PD8255AC-5)

Z7 is an expansion port IC for the main CPU and is used mainly for inputting and outputting the signals related to the playback of CD and LDD discs.

#### 4) Z1 (PD4034)

Z1 is a sub-CPU which supports the main CPU. It is an 8-bit CMOS IC containing a 64-byte RAM.

Its operating clock frequency is 4.41MHz.

#### 5) Z3 (PD0011, Decoder IC)

The DATA signal, separated from the video signal in the sync separator circuit of the video playback circuit, is supplied to Z3.

Z3 reads and stores the data in 16, 17 and 18H (279, 280, 281H) in the DATA signal by the timing of the  $\bar{H}$  SYNC and  $\bar{V}$  SYNC signals sent from the sync separator circuit. In response to requests from the main CPU, the stored data are sent out through the data bus.

The DOC INH signal is a command which inhibits compensation so that the data are not replaced by the dropout compensator circuit in the video playback circuit.

In actual fact, the DOC INH signal is set low in

16H (279H) in which the code indicating the CX-recorded statuses and the code acting as the frame at which the pictures are to be stopped are included. When chapter search is conducted, the same signal is low even in 18H (281H) in which the chapter number is included.

#### 6) Z2 (PD0010, Display IC)

The display data inserted into the video signal in the output processing circuit of the video playback circuit are created in Z2.

The data for the characters and symbols to be displayed as well as the display positions are sent from the main CPU through the data bus.

Z2 stores these data and outputs the data of the portion which forms the characters and display background at a timing synchronized with the  $V$  SYNC and  $H$  SYNC signals.

#### 7) LOLB Z1 (PD3032, Loading CPU)

Z1 on the LOLB circuit board determines the type of disc and it controls the loading and eject operations of the disc table. It is a 6805-type 8-bit NMOS IC containing a 96-byte RAM.

### 12.2 DESCRIPTION OF SOFTWARE

When the power switch is turned on, the system reset signal is produced on the DRVB circuit board. This signal causes the sub-CPU (CONT section Z1) and loading CPU (LOLB Z1) to be reset. The main CPU (Z9) and expansion port IC (Z7) are reset by the sub-CPU. As the CPUs are reset, the ports and RAMs are initialized by their software.

The sub-CPU first checks that the LD/spindle motor is not rotating. If it is rotating, the sub-CPU and main CPU remain in the standby mode until the motor stops.

When it is confirmed that the motor is no longer rotating, the sub-CPU advises the main CPU of this. The main CPU now checks that the slider is moving to the park position and also that the spindle motor corresponding to the disc has been set.

After initialization, the loading CPU first checks that the disc table is securely interlocked and it remains in the standby mode until the table is interlocked.

Once the interlock is confirmed, it turns on the LEDs momentarily installed on the LDSB and CDSB circuit boards, it checks that the disc has been installed by detecting the light reflected from the disc and it determines the disc size.

When it determines that a CD disc has been installed, it turns on the CDP and TRACK indicators, and if an LD disc has been installed, it turns on the VDP indicator.

After checking that the spindle motor corresponding to the determined disc has been set, the loading CPU moves on to the table loading operation. When it necessary to change the spindle motor, it moves on to that operation.

When it is determined that a disc has not been installed, the loading CPU moves on to the table loading operation and, when the rear panel transit switch is pressed, the motor is switched to the LD/spindle motor.

When the spindle motor is switched, the CPU checks that the slider has been moved to the park position by the main CPU and the switching operation occurs after the table has been raised. Upon completion of the switching, the table loading operation is undertaken and when this is completed, the loading CPU stays in the standby mode until the focus servo circuit loop is closed.

The main CPU first checks that the spindle motor has been set and then it moves on to the operation which starts to place the system in the CD or LD disc playback mode.

The processes up to the start of LD disc playback will now be described.

As the slider is moved to the LD inside position, a check is carried out to confirm that the PLAY key has been pressed or not. If it is pressed, the PLAY indicator first starts blinking. Then, at the same time as the semiconductor laser is made to emit a beam, the focus servo operation is commenced.

When it is confirmed that the slider is at the LD inside position, the tracking servo operation is started after it is sent slightly to the outer circumference.

After it is confirmed that the focus servo has closed the loop, the slider servo operation is started. When the focus servo has not closed the loop, it is conceivable that a scratch or mark on the position at which the beam is directed is responsible, and the slider is moved slightly.

The loading CPU checks that the focus servo loop has been closed and it starts the spindle motor rotating the disc. While this is happening, it checks only whether the focus servo loop is open or not.

The main CPU checks that the spindle and tangential servos have reached a stable state of operation.

The signal sent from CDDM is checked and when it is ascertained that the reference signal and frame sync signal are synchronized, it is judged that an LDD disc has been installed. If the signal synchronization is not detected, it is judged that an ordinary LD disc has been installed.

If the front panel's VIDEO DISC AUDIO switch is at the AUTO DIGITAL position with an LDD disc, the DIGITAL indicator is turned on.

The data read out by the decoder IC determine whether the disc is a CLV or CAV disc. If it is a CLV disc, the CLV indicator is first turned on and the time number 0:00 is searched; if it is a CAV disc, the frame number 0 is searched.

In either case, the search is completed, the PLAY indicator is turned on and both video and audio output is allowed.

Next, the processes leading up to the start of CD disc playback will be described.

As the slider is moved to the CD inside position, a check is carried out to determine that the PLAY key has been pressed or not. If it has been pressed, the PLAY indicator first starts blinking.

After it is checked that the slider is at the CD inside position, the semiconductor laser is made to emit a beam and, simultaneously, the focus servo operation is started.

It is checked that the focus loop is closed and then that the RF signal has been detected by the CDDM RF detector circuit, and the tracking servo operation is started.

It is checked that the frame sync signal and reference signal are synchronized and the TOC data are read out.

The lead track is searched and the PLAY indicator is turned on.

The loading CPU checks only the state of the focus servo circuitry and it stops the spindle motor as soon as the loop is opened. Then it checks that this is based on the sub-CPU command, for instance, when the eject key on the front panel is pressed. When it is based on a focus servo circuit malfunction or other factor, the standby mode is retained until that the loop is closed again by the operation of the servo circuit, or that the eject command is sent from the sub-CPU with the servo resetting disable.

When the sub-CPU outputs the eject command, the loading CPU first waits the spindle stop and then moves on to the table eject operation.

Upon completion of the table eject operation, the plunger is attracted, the interlock is released and the table is projected. While this is happening, the software of various CPUs is returned to the initialization state.

When it is judged that some malfunction or other has occurred to make it impossible to continue operation during table control or spindle motor switching, this is advised the user by the blinking of the VDP indicator.