

Layer Name	Туре	Material	Thickness (mm)	Color	Epsilon R	Loss Tangent
F.Silkscreen	Top Silk Screen	Liquid Photo	0 mm	White	1	0
F.Paste	Top Solder Paste		0 mm		1	0
F.Mask	Top Solder Mask	Epoxy (JLC)	0.015 mm	Black	3.8	0.02
F.Cu	copper		0.035 mm		1	0
Dielectric 1	prepreg	FR4 (JLC 7628)	0.2104 mm	FR4 natural	4.4	0.02
In1.Cu	copper		0.0152 mm		1	0
Dielectric 2	core	FR4 (JLC Core)	0.4 mm	FR4 natural	4.6	0.02
In2.Cu	copper		0.0152 mm		1	0
Dielectric 3	prepreg	FR4 (JLC 7628)	0.2028 mm	FR4 natural	4.4	0.02
In3.Cu	copper		0.0152 mm		1	0
Dielectric 4	core	FR4 (JLC Core)	0.4 mm	FR4 natural	4.6	0.02
In4.Cu	copper		0.0152 mm		1	0
Dielectric 5	prepreg	FR4 (JLC 7628)	0.2104 mm	FR4 natural	4.4	0.02
B.Cu	copper		0.035 mm		1	0
B.Mask	Bottom Solder Mask	Epoxy (JLC)	0.015 mm	Black	3.8	0.02
B.Paste	Bottom Solder Paste		0 mm		1	0
B.Silkscreen	Bottom Silk Screen	Liquid Photo	0 mm	White	1	0

BOARD CHARACTERISTICS

Copper Layer Count: Board Thickness: 1.5844 mm

Board overall dimensions: 45.0000 mm x 30.0000 mm

0.1500 mm / 0.1500 mm Min hole diameter: 0.3000 mm Min track/spacing:

Copper Finish: FNIG Impedance Control: Yes Castellated pads: Plated Board Edge: No

Edge card connectors: No

ALL 0.3MM VIAS TO BE EPOXY FILLED AND CAPPED WITH COPPER.

NOTES: UNLESS OTHERWISE SPECIFIED.

- A. FR4 Tg 150 C OR EQUIVALENT.
- B. EQUIVALENT MATERIAL SHALL BE ROHS COMPLIANT, HALOGEN FREE AND APPROVED BY PANTS FOR BIRDS LLC. C. THICKNESS OF INDIVIDUAL COPPER CLAD SHEETS SHALL BE IN AS DEFINED IN STACK-UP.

2. ETCH GEOMETRY:

- A. MEASURE WIDTH FROM THE BASE OF THE METALIZATION.
- B. MINIMUM LINE WIDTH: 0.15 MM OUTER, 0.15 MM INNER LAYERS.
- C. FINISHED LINE WIDTH AND TERMINAL AREA SHALL NOT DEVIATE FROM THE 1-TO-1 MASTER PATTERN IMAGE BY MORE THAN +/- 0.025 MM OR 20%, WHICHEVER IS LESS.
- - A. ENIG PLATING PER CURRENT REVISION OF IPC-4552. EXPOSED METAL SHALL HAVE 118-236 MICRO INCHES ELECTROLESS NICKEL AND 2-5 MICRO INCHES GOLD.
- 4. IMPEDANCE (ALL TOLERANCES +/- 10%)
 A. ALL 0.35 MM WIDE/0.2 MM SPACE PAIRS ON OUTER LAYERS SHALL BE 90 OHMS DIFFERENTIAL.
 - B. ALL 0.6 MM WIDE/0.15 MM SPACE TRACES ON OUTER LAYERS SHALL BE 50 OHMS SINGLE ENDED.
 - C. VENDOR MAY ADJUST DESIGN GEOMETRIES UP TO $\pm /-20\%$ TO ACHIEVE TARGET IMPEDANCE. ADJUSTMENTS BEYOND 20% OF LINE WIDTH, SPACING OR DIELECTRIC THICKNESS SHALL REQUIRE APPROVAL FROM PANTS FOR BIRDS LLC.

5. HOLES:

- A. PLATING IN HOLES SHALL BE CONTINUOUS ELECTROLYTIC COPPER WITH 0.025 MM MINIMUM BARREL THICKNESS.
- B. MINIMUM FINISHED HOLE SIZE: 0.20 MM
- C. HOLE SIZE MEASURED AFTER PLATING.
- D. SEE DRILL CHART FOR FINISHED HOLE SIZE AND TOLERANCE.
- E. ALL HOLES SHALL BE LOCATED WITHIN 0.08 MM OF TRUE POSITION AS SUPPLIED IN CAD DATA.
- F. ALL HOLES < 1.0MM DIAMETER SHALL BE EPOXY FILLED AND CAPPED WITH COPPER.

6. SOLDERMASK:

- A. SOLDERMASK OVER BARE COPPER (SMOBC) ON PRIMARY AND SECONDARY SIDES USING SUPPLIED ARTWORK IN ACCORDANCE WITH CURRENT REVISION OF IPC-SM-840 TYPE B.
- B. COLOR: MATTE BLACK
- C. LIQUID PHOTO-IMAGEABLE (LPI) 0.001 MM TO 0.002 MM THICKNESS, HALOGEN FREE D. NO BLEED-OUT ALLOWED OVER EXPOSED SMD PADS.
- E. NO EXPOSED TRACES.

7. SILKSCREEN:

- A. SILKSCREEN PRIMARY AND SECONDARY SIDE WITH WHITE EPOXY, NON-CONDUCTIVE, NON-NUTRIENT INK.
- B. ANY UNSPECIFIED STROKE WIDTH SHALL BE 0.13 MM
- C. CLIP SILKSCREEN AWAY FROM ANY EXPOSED METAL.
- D. VENDOR DATE CODE, LOGO, UL AND ANY ADDITIONAL MARKING TO BE LOCATED ON THE SECONDARY SIDE.
- E. BAG AND TAG ACCEPTABLE FOR PCBS THAT ARE TOO SMALL FOR MARKING.

8. STANDARDS:

- A. FABRICATE PCB IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-6012, CLASS 2.
- B. INTERPRET DIMENSIONS AND TOLERANCES IN ACCORDANCE WITH THE CURRENT REVISION OF ASME Y14.5M. C. DO NOT SCALE DRAWING.

- A. BOW AND TWIST OF ASSEMBLY SUB-PANEL OR SINGULATED PCB SHALL NOT EXCEED .025 MM PER MM.
- B. TEST IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-TM-650 2.4.22

10. DESTRUCTIVE TESTING:

- A. SOLDER SAMPLE PROCESSED THROUGH SOLDERING SHALL BE INCLUDED WITH EACH SHIPMENT.
- B. X-OUT PANELS MAY BE USED FOR SOLDER SAMPLE.
- 11. REMOVE ALL BURRS AND BREAK SHARP EDGES RO.003 MIN.

12. NON-DESTRUCTIVE EVALUATION:

- A. ALL PCBS SHALL PASS 100% ELECTRICAL TEST USING SUPPLIED IPC-356 NETLIST IN ACCORDANCE WITH CURRENT REVISION OF IPC-9252, CLASS 2.
- B. CERTIFICATE OF CONFORMANCE SHALL BE SUPPLIED WITH EACH SHIPMENT.

13. X-OUTS:

A. X-OUT BOARDS THAT DO NOT MEET ALL SPECIFICATIONS USING PERMANENT MARKING ON BOTH SIDES OF THE AFFECTED PCB.

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- B. PANELS THAT DO NOT HAVE ANY X-OUTS SHALL BE PACKAGED TOGETHER.
- C. PANELS THAT HAVE 5 OR FEWER X-OUTS SHALL BE PACKAGED SEPARATE FROM NON-X-OUT PANELS.
- D. PANELS WITH MORE THAN 5 X-OUTS SHALL BE REJECTED.

14. PACKAGING REQUIREMENTS:

- A. PCBS SHALL BE PACKAGED IN VACUUM SEALED INNER CONTAINERS.
- B. OUTER CONTAINERS SHALL BE SUFFICIENT TO PREVENT DAMAGE DURING SHIPPING AND HANDLING.



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