SN74LVC1G3157 Single-Pole Double-Throw Analog Switch

1 Features

- ESD protection exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- 1.65-V to 5.5-V V_{CC} operation
- Qualified for 125°C operation
- Specified break-before-make switching
- Rail-to-rail signal handling
- Operating frequency typically 340 MHz at room temperature
- High speed, typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low ON-state resistance, typically ≠6 Ω (V_{CC} = 4.5 V)
- Latch-up performance exceeds 100 mA Per JESD 78, class II

2 Applications

- Wearables and mobile devices
- Portable computing
- Internet of things (IoT)
- Audio signal routing
- Remote radio unit
- Portable medical equipment
- Surveillance
- Home automation
- I2C/SPI/UART bus multiplexing
- Wireless charging

3 Description

This single channel single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

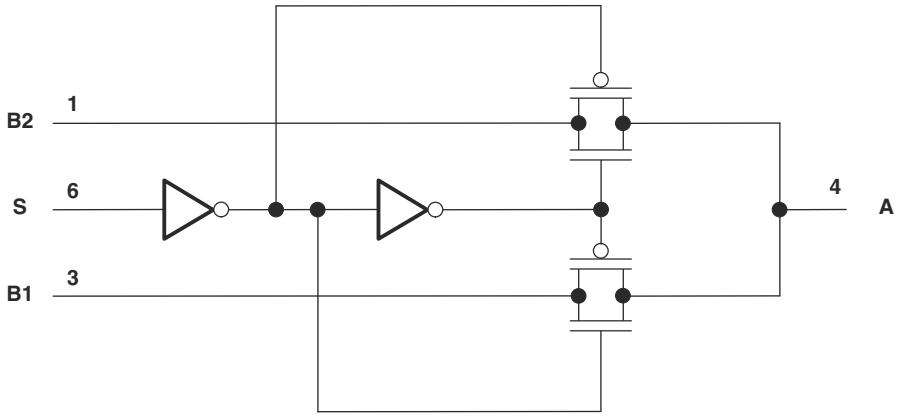
The SN74LVC1G3157 device can handle both analog and digital signals. The SN74LVC1G3157 device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G3157	SOT-23 (DBV) (6)	2.90 mm × 1.60 mm
	SC70 (DCK) (6)	2.00 mm × 1.25 mm
	SOT (DRL) (6)	1.60 mm × 1.20 mm
	SON (DRY) (6)	1.45 mm × 1.00 mm
	DSBGA (YZP) (6)	1.41 mm × 0.91 mm
	SON (DSF) (6)	1.00 mm × 1.00 mm
	X2SON (DTB) (6)	0.80 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (May 2017) to Revision M (August 2022) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Updated the *Pin Configuration and Functions* section....4
- Updated the equation in the *Detailed Design Procedure* section....18

Changes from Revision K (January 2017) to Revision L (May 2017) — **Page**

- Deleted *Feature* "Useful for Both Analog and Digital Applications"....1
- Deleted *Feature* "High Degree of Linearity"....1
- Changed the first sentence of the *Description* From: "This single-pole double-throw (SPDT)..." To: "This single channel single pole double-throw (SPDT)..."....1
- Added the X2SON (DTB) package to the *Device Information*....1
- Added the X2SON (DTB) Package, to the *Pin Configuration and Functions*....4
- Changed $I_{I/O}$ To: $I_{I/OK}$ for I/O port diode current in the *Absolute Maximum Ratings*....6
- Added the DTB (X2SON) package to the *Thermal Information* table....7
- Changed Note 1 and Note 2 n the *Analog Switch Characteristics* table....9
- Deleted Note 3 "Specified by design" from the *Analog Switch Characteristics* tables....9
- Deleted Note 4 "Specified by design" from the *Switch Characteristics 85°C* tables....10
- Deleted Note 4 "Specified by design" from the *Switch Characteristics 125°C* tables....10
- Changed Figure 7-2, From: SW1 = V_{IL} to SW1 = V_{IH}, From: SW2 = V_{IH} to: SW2 = V_{IL}....11
- Changed Figure 7-5....11
- Added a series 50-Ω resistor on B1 in Figure 7-6....11
- Changed Figure 7-7....11

Changes from Revision J (June 2016) to Revision K (January 2017) — **Page**

- Added new applications to *Applications* section....1
- Added Operating free-air temperature, T_A for BGA and all other packages in *Recommended Operating Conditions*....7
- Added 125°C data to *Electrical Characteristics* table....8
- Added 85°C to title to differentiate from new 125°C *Switching Characteristics* section....10

- Added 125°C *Switching Characteristics* section and data. 10

Changes from Revision I (June 2015) to Revision J (June 2016) **Page**

- Deleted 200-V Machine Model (A115-A) from *Features* 1
- Changed *Feature* From: "Operating Frequency Typically 300 MHz at Room Temperature" To: "Operating Frequency Typically 340 MHz at Room Temperature"..... 1
- Updated *Device Information* table..... 1
- Updated pinout images for all Packages..... 4
- Added temperature ranges for Storage temperature, T_{stg} and Junction temperature, T_J in *Absolute Maximum Ratings* 6
- Changed MAX value ±1 to ±0.1 for I_{off} and I_{IN} in *Electrical Characteristics* table..... 8
- Added *Receiving Notification of Documentation Updates* section..... 20

Changes from Revision H (May 2012) to Revision I (June 2015) **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated *Features*..... 1

Changes from Revision G (September 2011) to Revision H (May 2012) **Page**

- Changed YZP with correct pin labels. 4
- Added *Thermal Information* table..... 7
- Changed to correct Pin Label "S"..... 8

5 Pin Configuration and Functions

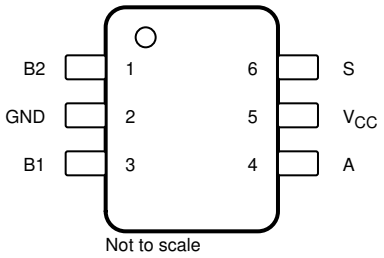


Figure 5-1. DBV Package, 6-Pin SOT-23 (Top View)

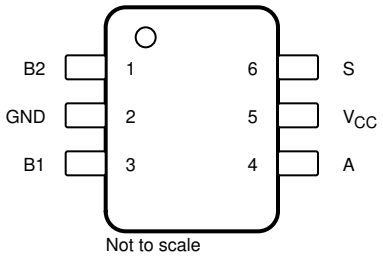


Figure 5-2. DCK Package, 6-Pin SC70 (Top View)

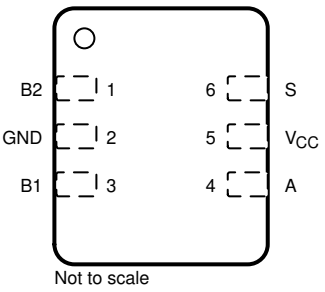


Figure 5-3. DRY Package, 6-Pin SON (Top View)

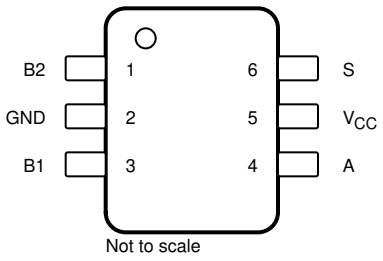


Figure 5-4. DRL Package, 6-Pin SOT (Top View)

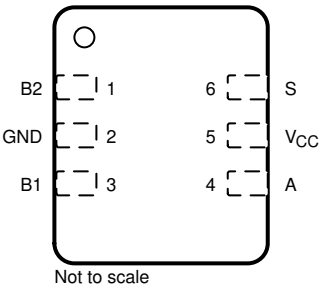


Figure 5-5. DSF Package, 6-Pin SON (Top View)

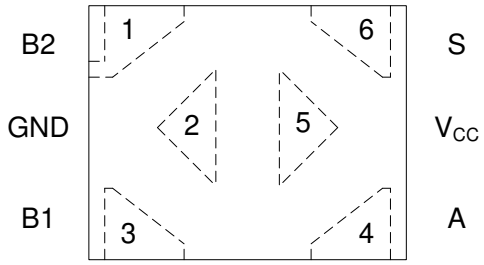


Figure 5-6. DTB Package, 6-Pin X2SON (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	SOT-23, SC70, SON, X2SON, or SOT		
B2	1	I/O	Switch I/O. Set S high to enable.
GND	2	P	Ground
B1	3	I/O	Switch I/O. Set S low to enable.
A	4	I/O	Common terminal
V_{CC}	5	P	Power supply
S	6	I	Select

(1) I = input, O = output, P = power

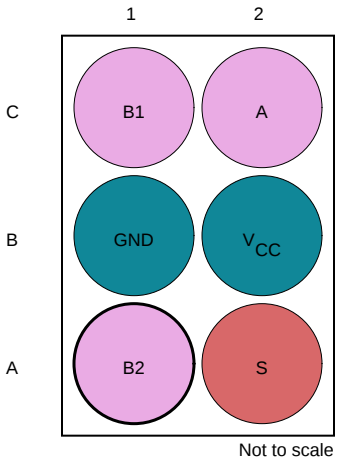


Figure 5-7. YZP Package, 6-Pin DSBGA (Bottom View)

Legend	
Input	Input or Output
Power	

Table 5-2. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
A1	B2	I/O	Switch I/O. Set S high to enable.
A2	S	I	Select
B1	GND	P	Ground
B2	V_{CC}	P	Power supply
C1	B1	I/O	Switch I/O. Set S low to enable.
C2	A	I/O	Common terminal

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6.5	V
V_{IN}	Control input voltage(2) (3)		–0.5	6.5	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4) (5)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		±50	mA
$I_{I/O}$	On-state switch current(6)	$V_{I/O}$ = 0 to V_{CC}		±128	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	Switch input or output voltage		0	V_{CC}	V
V_{IN}	Control input voltage		0	5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.75		V
		V_{CC} = 2.3 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.25	V
		V_{CC} = 2.3 V to 5.5 V		V_{CC} × 0.3	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		$V_{C\ C}$ = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature	BGA package (YZP)	–40	85	°C
		All other packages (DBV, DCK, DRL, DRY, DSF)	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G3157						UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	234.9	269.5	244.1	284.2	324.5	129.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	150.4	189.5	112.5	138.6	150.5	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.4	84.7	109.9	170.9	239.0	40.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	60.8	62.7	9.3	13.7	17.2	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	86.1	84.0	109.3	167.9	238.3	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			V_{CC}	T_A = -40 to 85°C			T_A = -40 to 125°C			UNIT
						MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
r_{on}	ON-state switch resistance(2)	See Figure 6-1 and Figure 7-1	V_I = 0 V	I_O = 4 mA	1.65 V		11	20		11	20	Ω
			V_I = 1.65 V	I_O = –4 mA			15	50		15	50	
			V_I = 0 V	I_O = 8 mA	2.3 V		8	12		8	12	
			V_I = 2.3 V	I_O = –8 mA			11	30		11	30	
			V_I = 0 V	I_O = 24 mA	3 V		7	9		7	9	
			V_I = 3 V	I_O = –24 mA			9	20		9	20	
			V_I = 0 V	I_O = 30 mA	4.5 V		6	7		6	7	
			V_I = 2.4 V	I_O = –30 mA			7	12		7	12	
			V_I = 4.5 V	I_O = –30 mA			7	15		7	15	
r_{range}	ON-state switch resistance over signal range(2) (3)	0 ≤ V_{Bn} ≤ V_{CC} (see Figure 6-1 and Figure 7-1)		I_A = –4 mA	1.65 V			140			140	Ω
				I_A = –8 mA	2.3 V			45			45	
				I_A = –24 mA	3 V			18			18	
				I_A = –30 mA	4.5 V			10			10	
Δr_{on}	Difference of ON-state resistance between switches(2) (4) (5)	See Figure 7-1	V_{Bn} = 1.15 V	I_A = –4 mA	1.65 V		0.5			0.5		Ω
			V_{Bn} = 1.6 V	I_A = –8 mA	2.3 V		0.1			0.3		
			V_{Bn} = 2.1 V	I_A = –24 mA	3 V		0.1			0.3		
			V_{Bn} = 3.15 V	I_A = –30 mA	4.5 V		0.1			0.2		
$r_{on(flat)}$	ON resistance flatness(2) (4) (6)	0 ≤ V_{Bn} ≤ V_{CC}		I_A = –4 mA	1.65 V		110			110		Ω
				I_A = –8 mA	2.3 V		26			40		
				I_A = –24 mA	3 V		9			10		
				I_A = –30 mA	4.5 V		4			5		
I_{off} (7)	OFF-state switch leakage current	0 ≤ V_I, V_O ≤ V_{CC} (see Figure 7-2)			1.65 V to 5.5 V			±1			±1	μA
							±0.05	±0.1(1)		±0.05	±0.1	
$I_{S(on)}$	ON-state switch leakage current	V_I = V_{CC} or GND, V_O = Open (see Figure 7-3)			5.5 V			±1			±1	μA
								±0.1(1)			±0.1(1)	
I_{IN}	Control input current	0 ≤ V_{IN} ≤ V_{CC}			0 V to 5.5 V			±1			±1	μA
							±0.05	±0.1(1)		±0.05	±0.1	
I_{CC}	Supply current	S = V_{CC} or GND			5.5 V		1	10			35	μA
ΔI_{CC}	Supply-current change	S = V_{CC} – 0.6 V			5.5 V			500			500	μA
C_i	Control input capacitance	S			5 V		2.7			2.7		pF
$C_{io(off)}$	Switch input/output capacitance	Bn			5 V		5.2			5.2		pF
$C_{io(on)}$	Switch input/output capacitance	Bn			5 V		17.3			17.3		pF
		A					17.3			17.3		

(1) T_A = 25°C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not production tested.
(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.
(7) I_{off} is the same as $I_{S(off)}$ (off-state switch leakage current).

6.6 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[1] (switch on)	A or Bn	Bn or A	R_L = 50 Ω, f_{in} = sine wave (see Figure 7-5)	1.65 V	340	MHz
				2.3 V	340	
				3 V	340	
				4.5 V	340	
Crosstalk[2] (between switches)	B1 or B2	B2 or B1	R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 7-6)	1.65 V	–54	dB
				2.3 V	–54	
				3 V	–54	
				4.5 V	–54	
Feed through attenuation[2] (switch off)	A or Bn	Bn or A	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 7-7)	1.65 V	–57	dB
				2.3 V	–57	
				3 V	–57	
				4.5 V	–57	
Charge injection	S	A	C_L = 0.1 nF, R_L = 1 MΩ (see Figure 7-8)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V_I = 0.5 V_{p-p}, R_L = 600 Ω, f_{in} = 600 Hz to 20 kHz (sine wave) (see Figure 7-9)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

(1) Set f_{in} to 0 dBm and provide a bias of 0.4 V. Increase f_{in} frequency until the gain is 3 dB below the insertion loss.
(2) Set f_{in} to 0 dBm and provide a bias of 0.4 V.

6.7 Switching Characteristics 85°C

T_A = –40 to +85°C (see Figure 7-4 and)Figure 7-10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	A or Bn	Bn or A		2		1.2		0.8		0.3	ns
t_{en} (2)	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t_{dis} (3)			3	13	2	7.5	1.5	5.3	0.8	3.8	
t_{B-M}			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.

6.8 Switching Characteristics 125°C

T_A = –40 to +125°C (see Figure 7-4 and Figure 7-10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	A or Bn	Bn or A		2		1.2		0.8		0.5	ns
t_{en} (2)	S	Bn	1	24.5	1	14.5	2.5	8	1.7	6	ns
t_{dis} (3)			2.5	13.5	2	8	1.5	5.5	0.8	4	
t_{B-M}			0.5		0.5		0.5		0.5		ns

6.9 Typical Characteristics

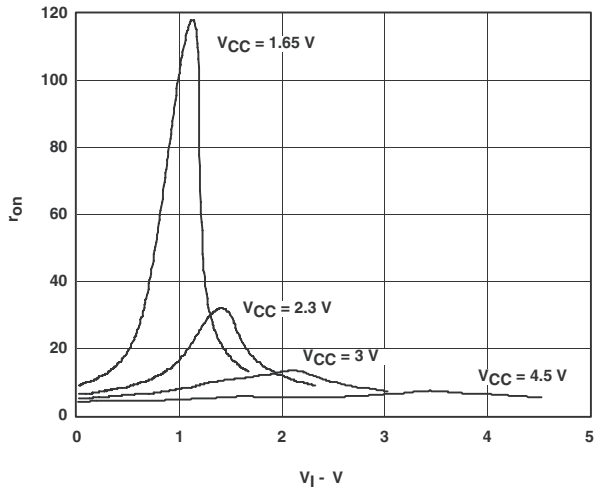


Figure 6-1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

7 Parameter Measurement Information

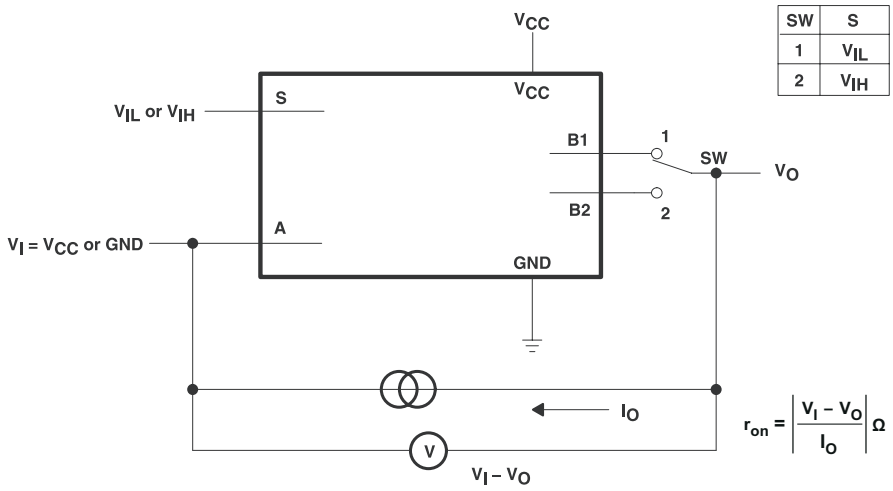
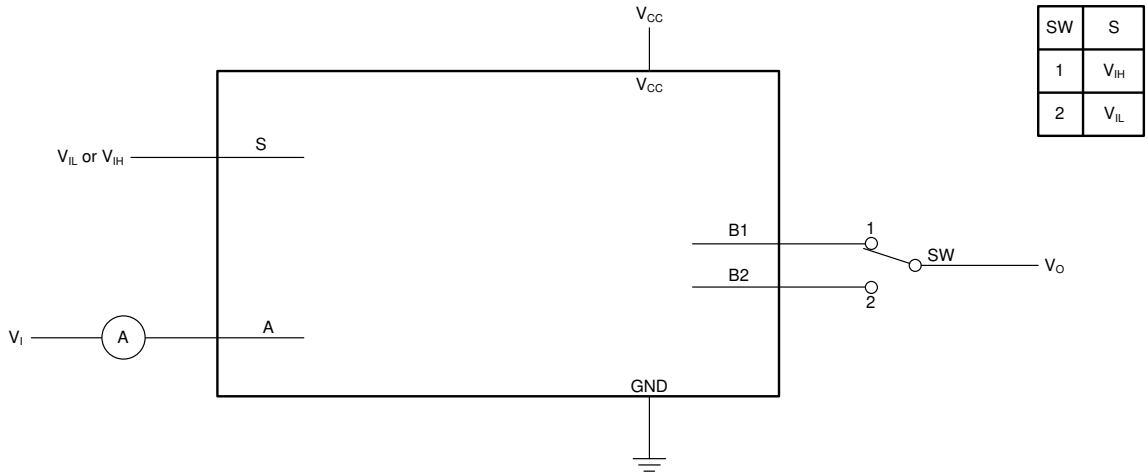


Figure 7-1. ON-State Resistance Test Circuit



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 7-2. OFF-State Switch Leakage-Current Test Circuit

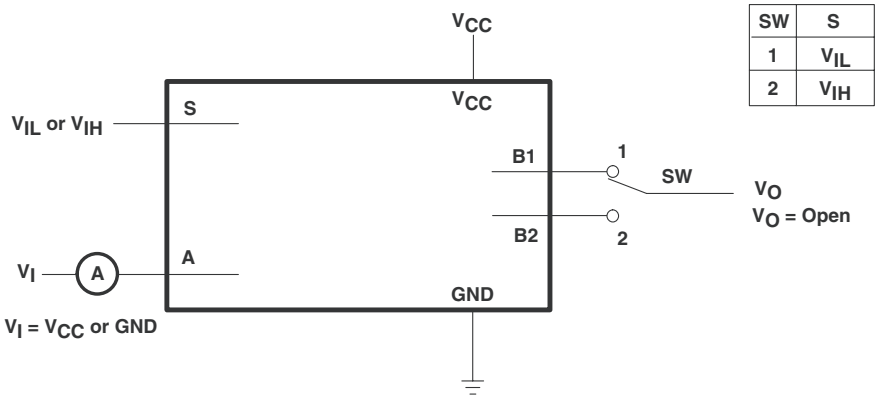
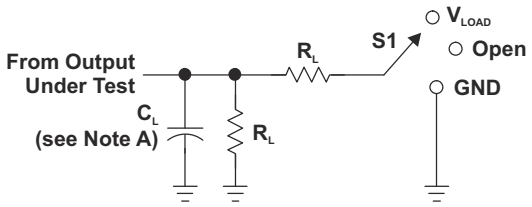


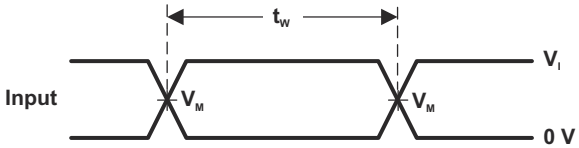
Figure 7-3. ON-State Switch Leakage-Current Test Circuit



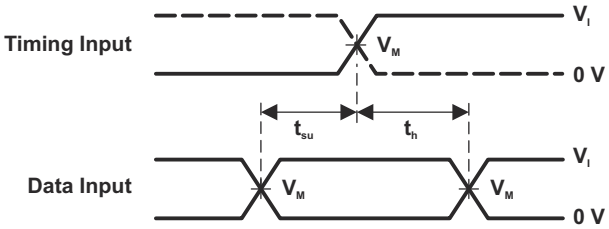
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

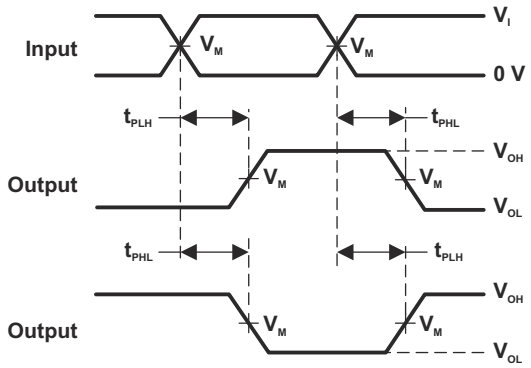
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



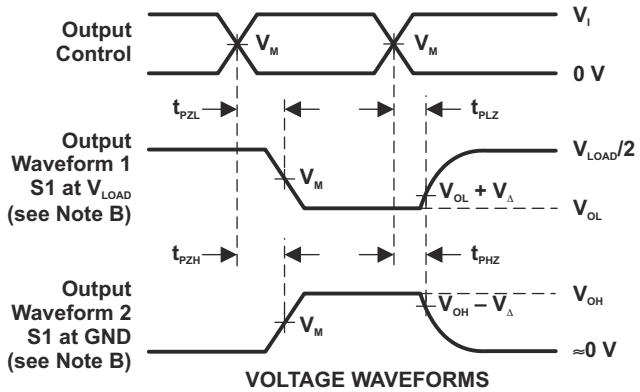
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-4. Load Circuit and Voltage Waveforms

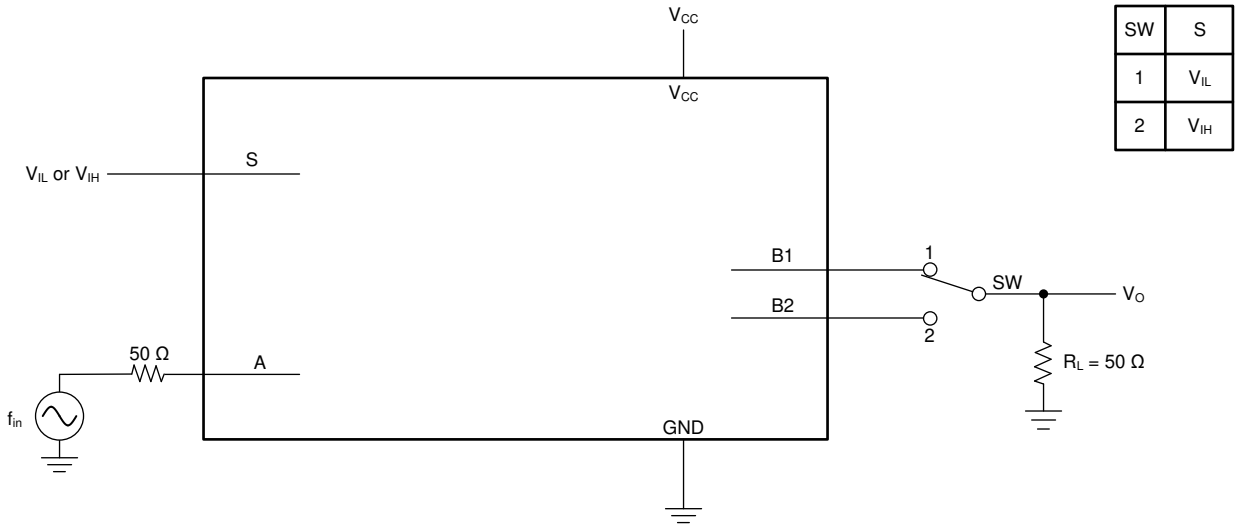


Figure 7-5. Frequency Response (Switch On)

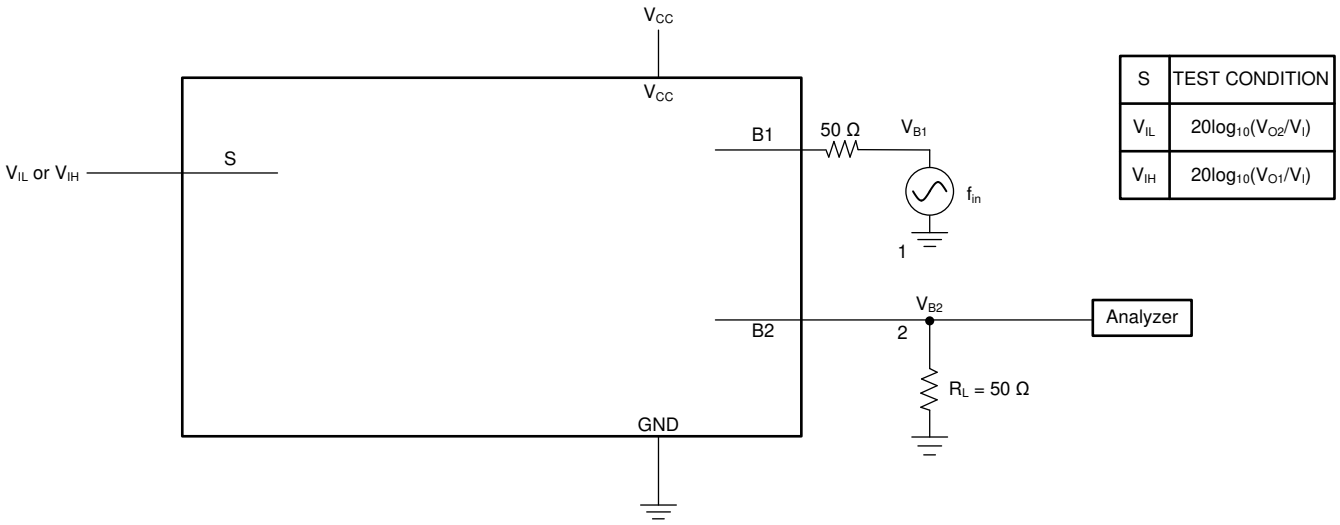


Figure 7-6. Crosstalk (Between Switches)

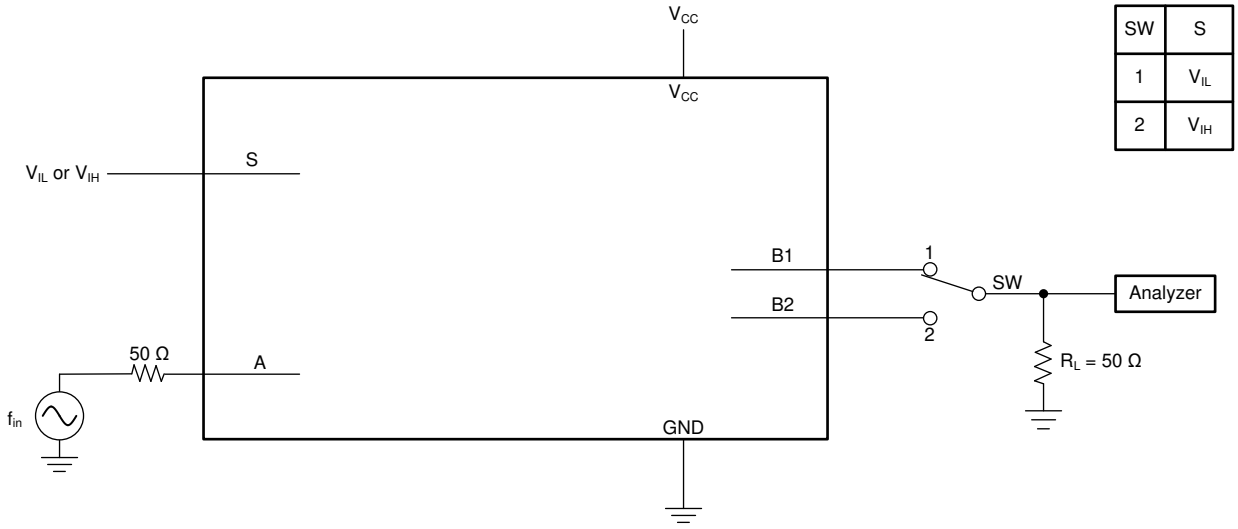


Figure 7-7. Feed Through

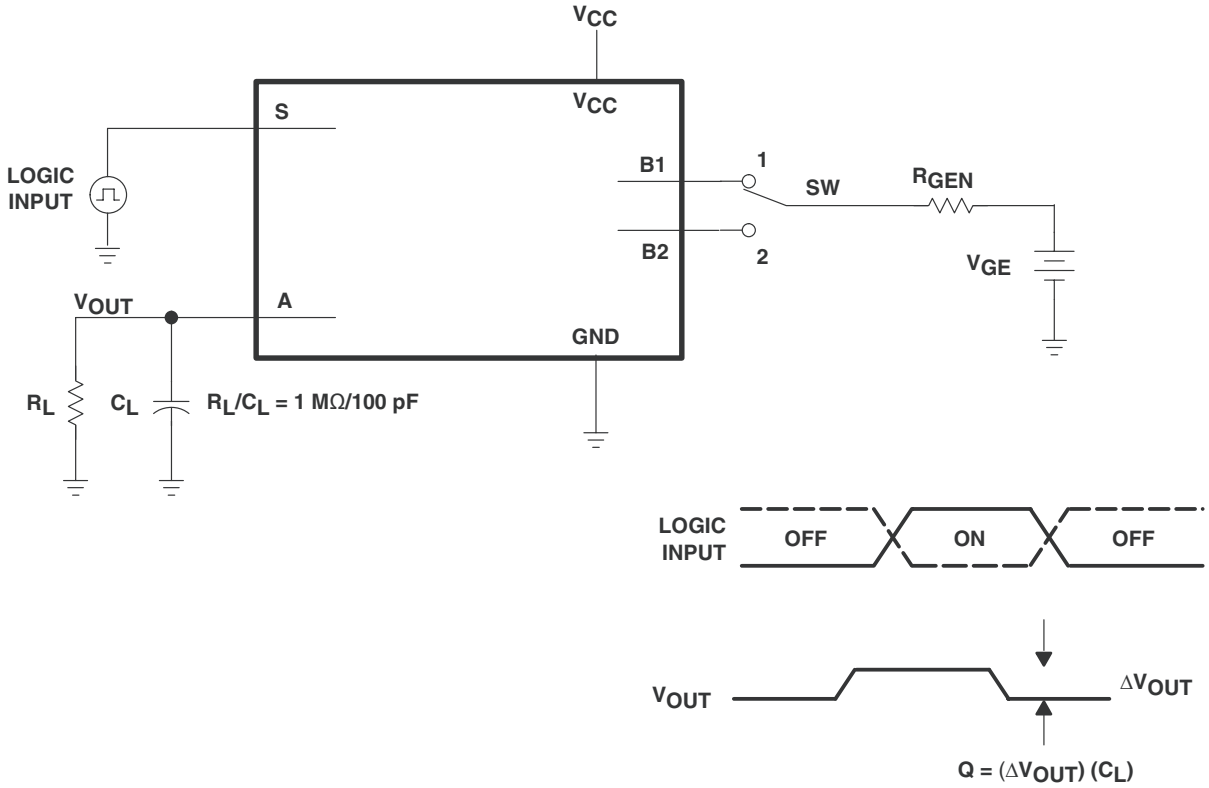


Figure 7-8. Charge-Injection Test

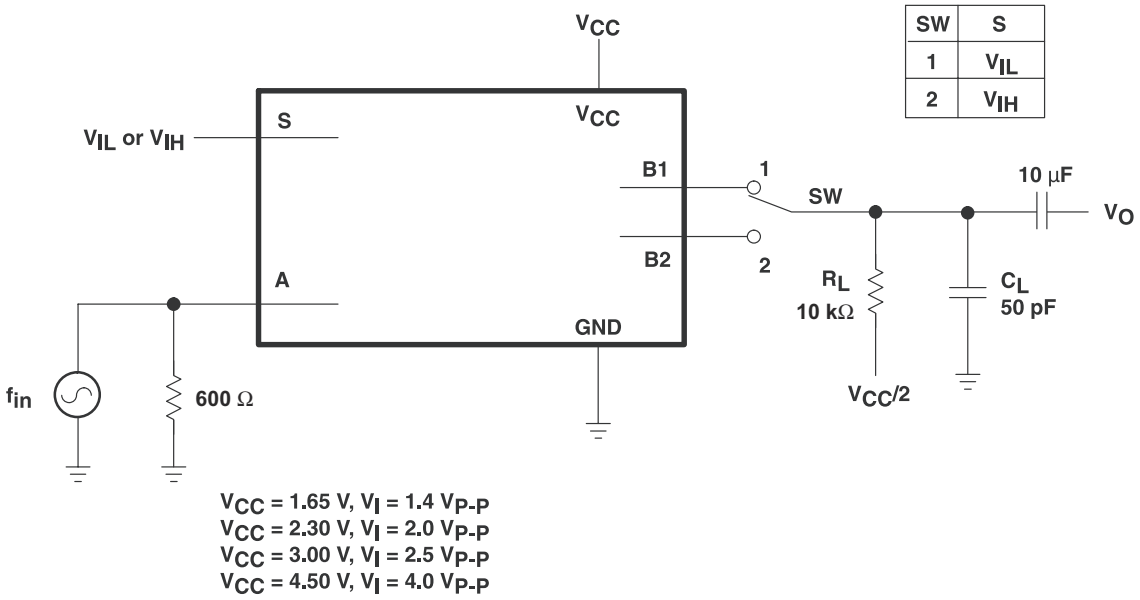


Figure 7-9. Total Harmonic Distortion

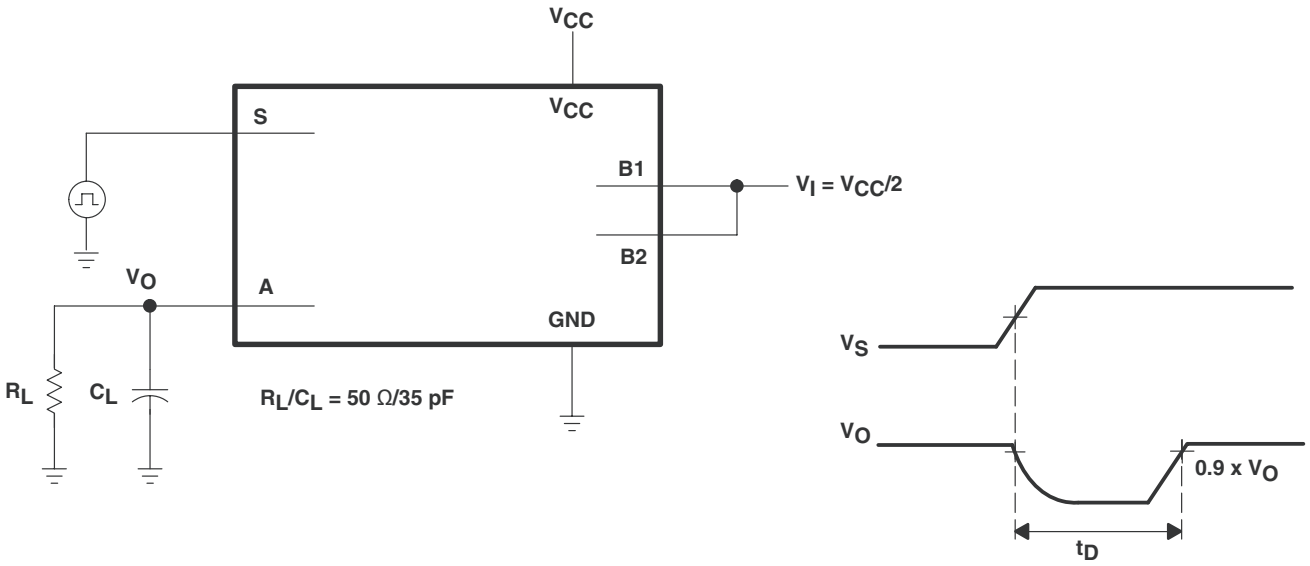


Figure 7-10. Break-Before-Make Internal Timing

8 Detailed Description

8.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

8.2 Functional Block Diagram

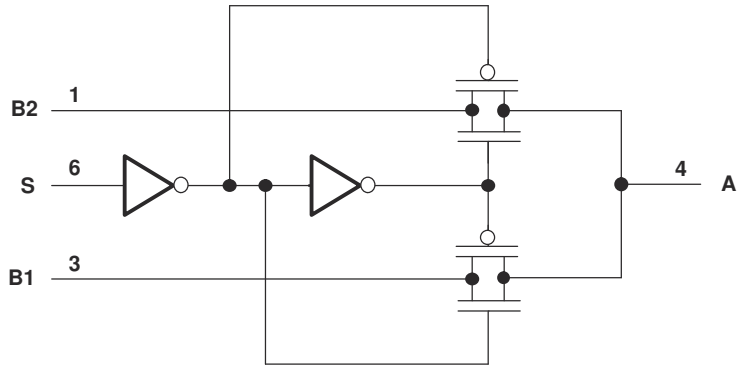


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

8.4 Device Functional Modes

Table 8-1 lists the ON channel when one of the control inputs is selected.

Table 8-1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches.

9.2 Typical Application

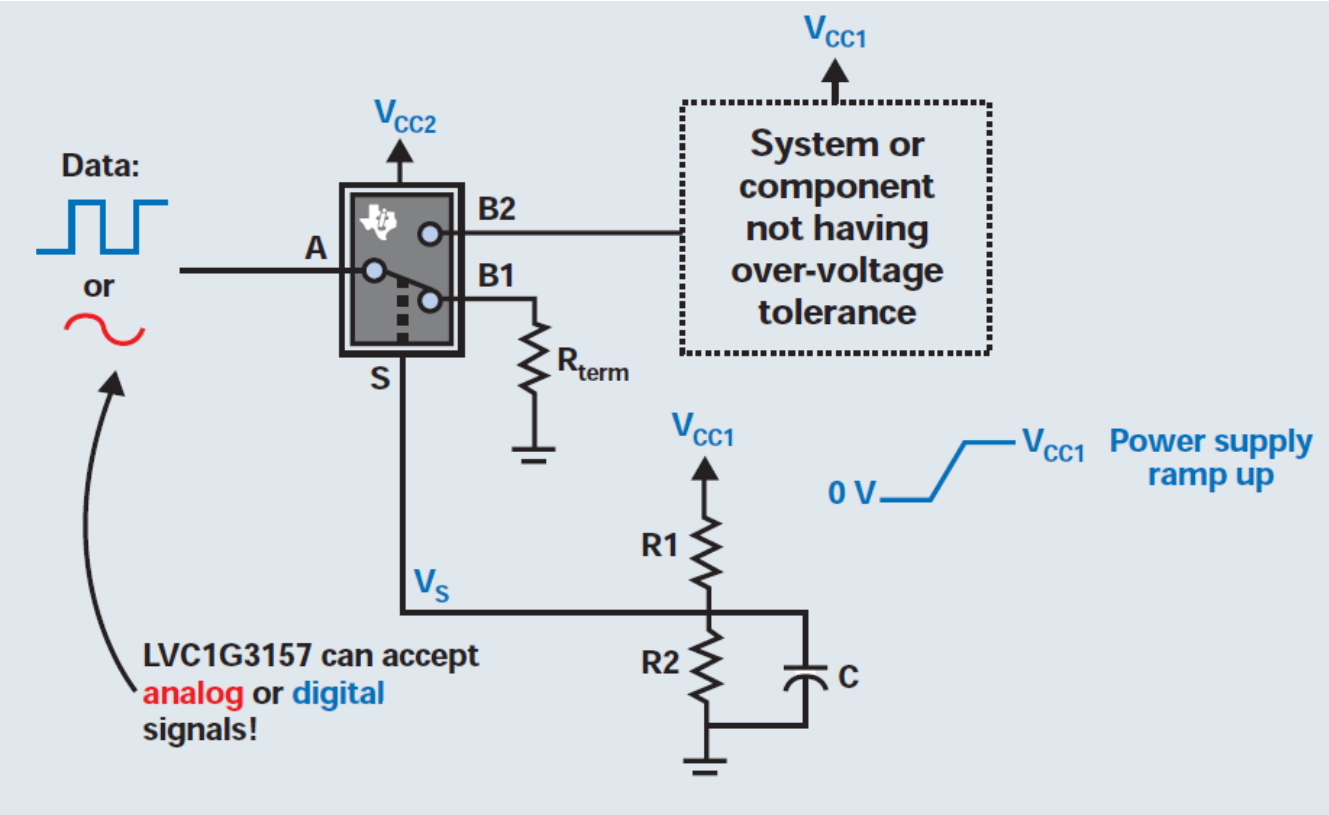


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until V_{CC} has ramped to a level in *Section 6.3* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set}\left(\frac{R2}{R1 + R2} \times V_{CC1} > V_{IH}\right) \text{of the select pin} \tag{1}$$

Choose Rs and C to achieve the desired delay.

When V_S goes high, the signal will be passed.

9.2.3 Application Curve

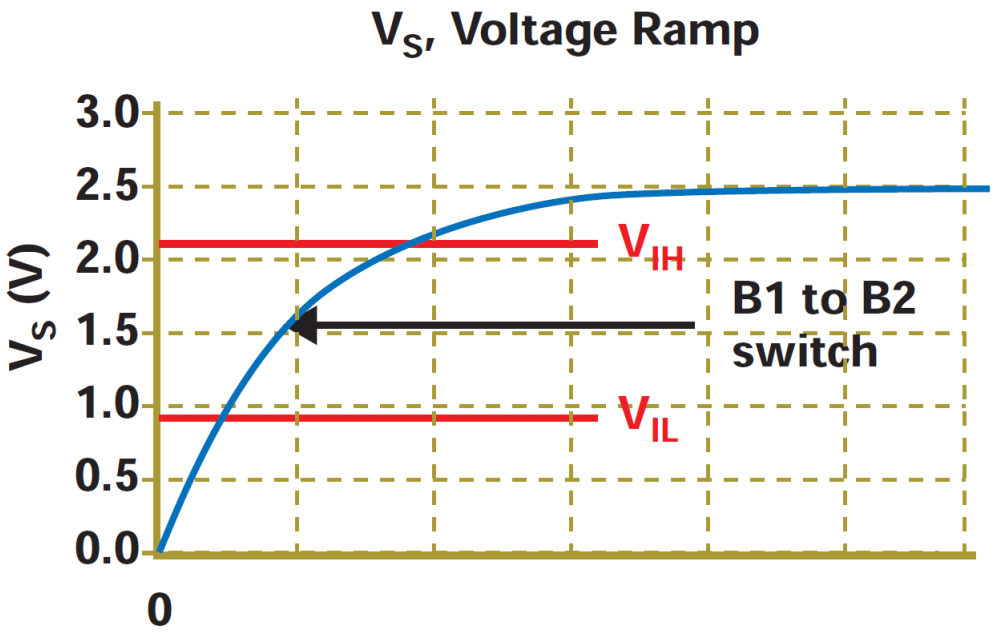


Figure 9-2. V_S Voltage Ramp

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

11 Layout

11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

11.2 Layout Example

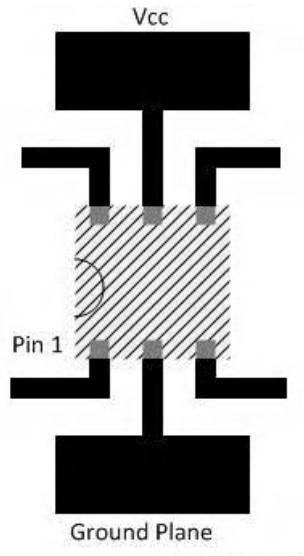


Figure 11-1. Recommended Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G3157DBVRE4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CC5F, CC5R)	Samples
74LVC1G3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CC5F, CC5R)	Samples
74LVC1G3157DCKRE4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	Samples
74LVC1G3157DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	Samples
74LVC1G3157DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S	Samples
SN74LVC1G3157DCK3	LIFEBUY	SC70	DCK	6	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 125	C5Z	
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)	Samples
SN74LVC1G3157DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)	Samples
SN74LVC1G3157DRY2	LIFEBUY	SON	DRY	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DTBR	ACTIVE	X2SON	DTB	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X	Samples
SN74LVC1G3157YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

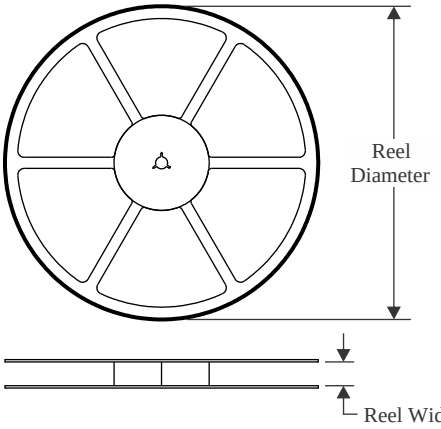
- Automotive : SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

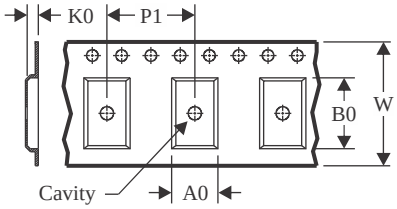
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

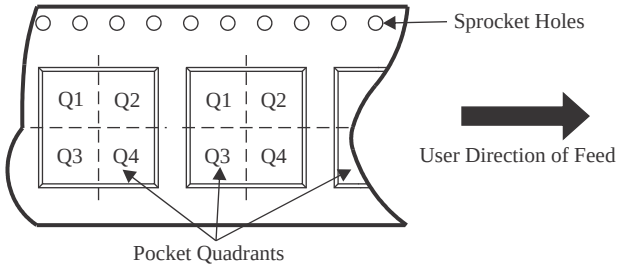


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

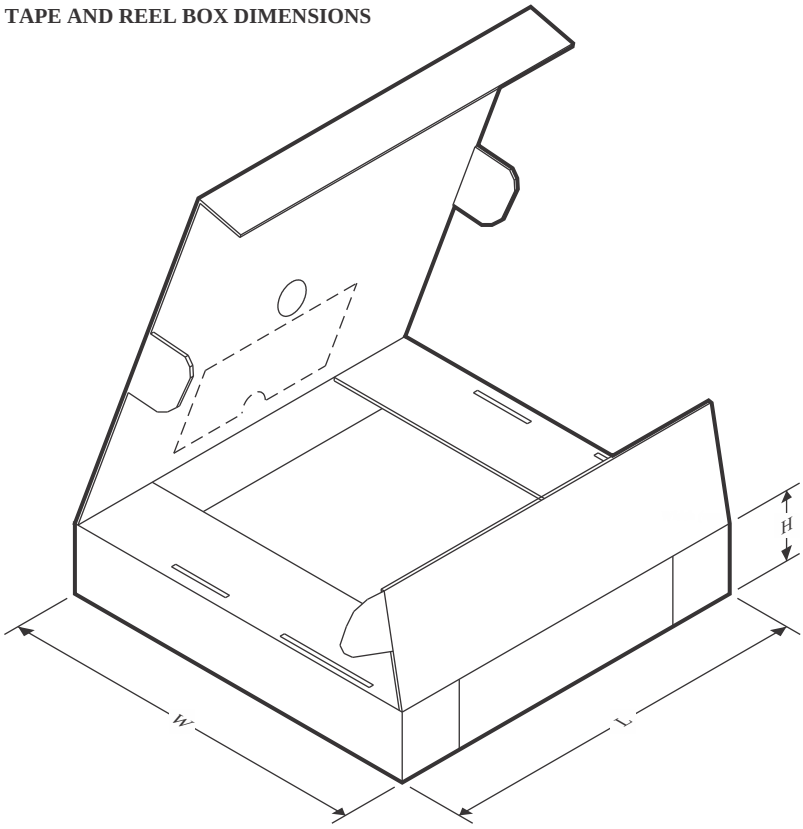
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

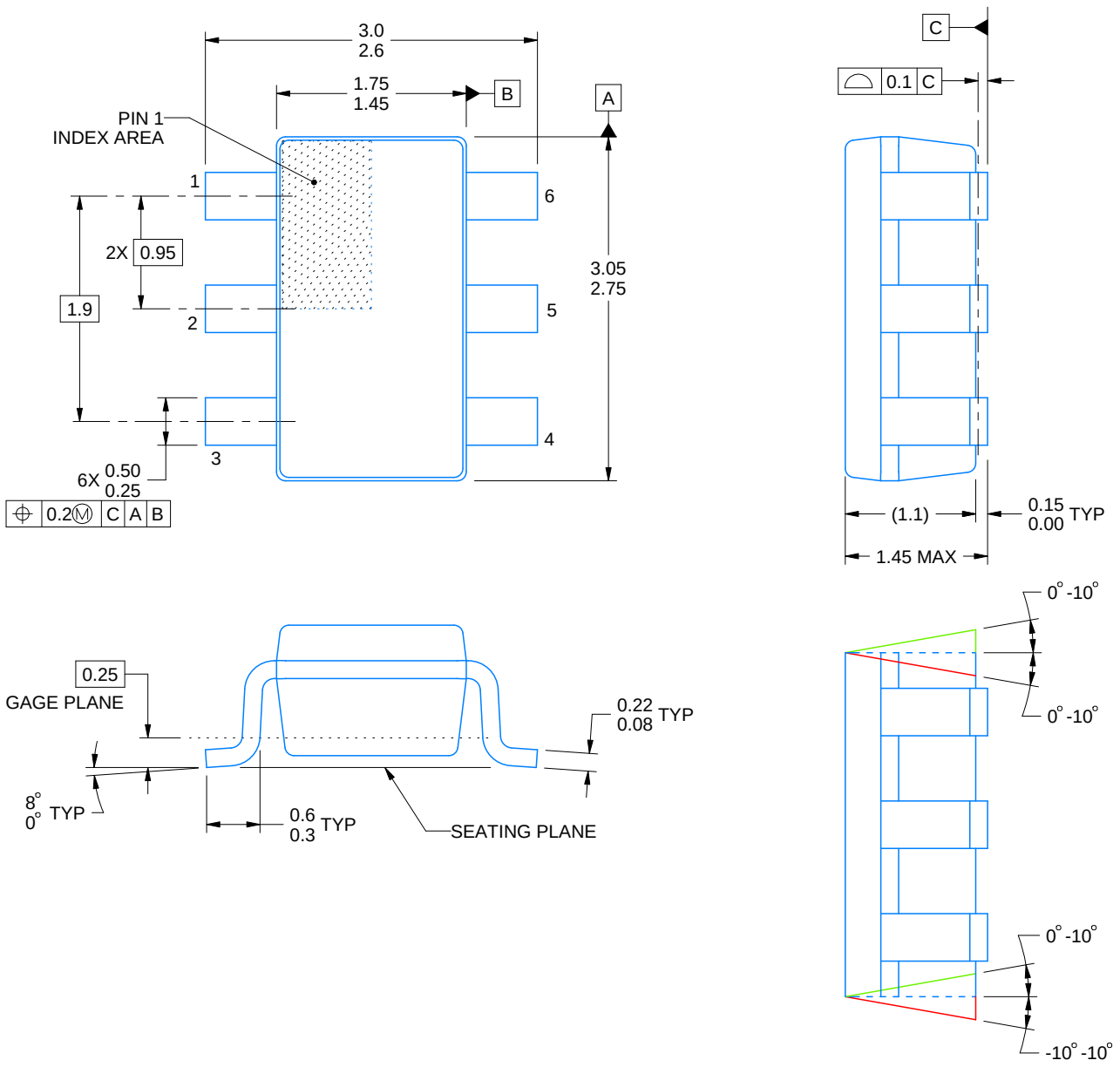
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

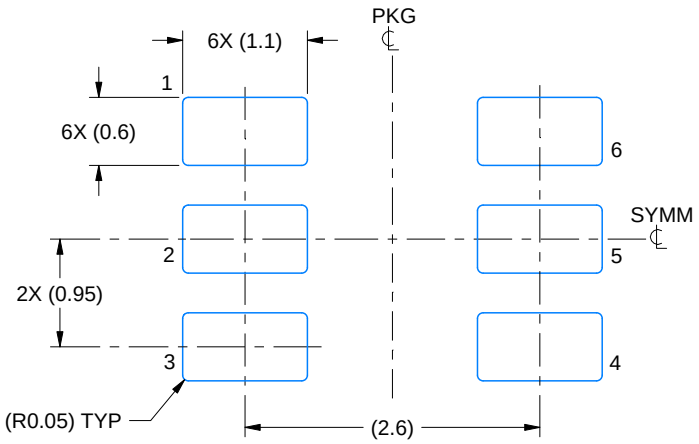


ALTERNATIVE PACKAGE SINGULATION VIEW

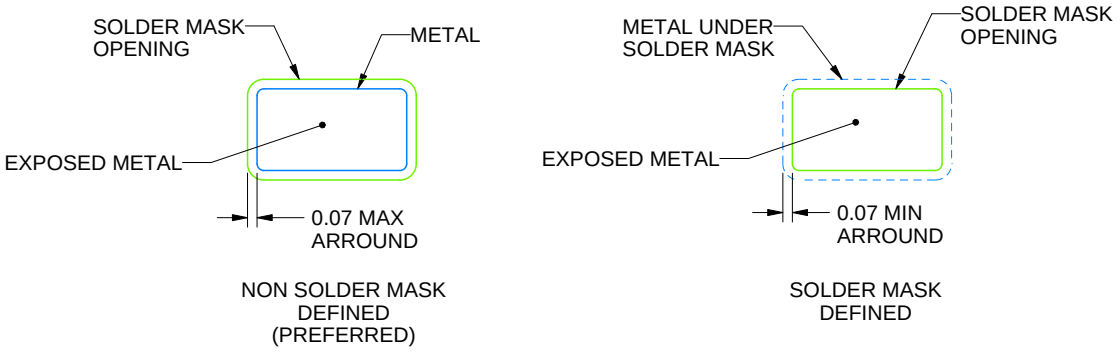
4214840/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

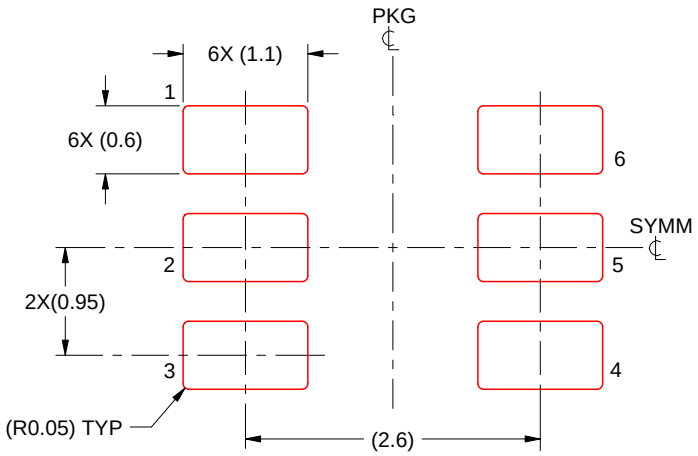


SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



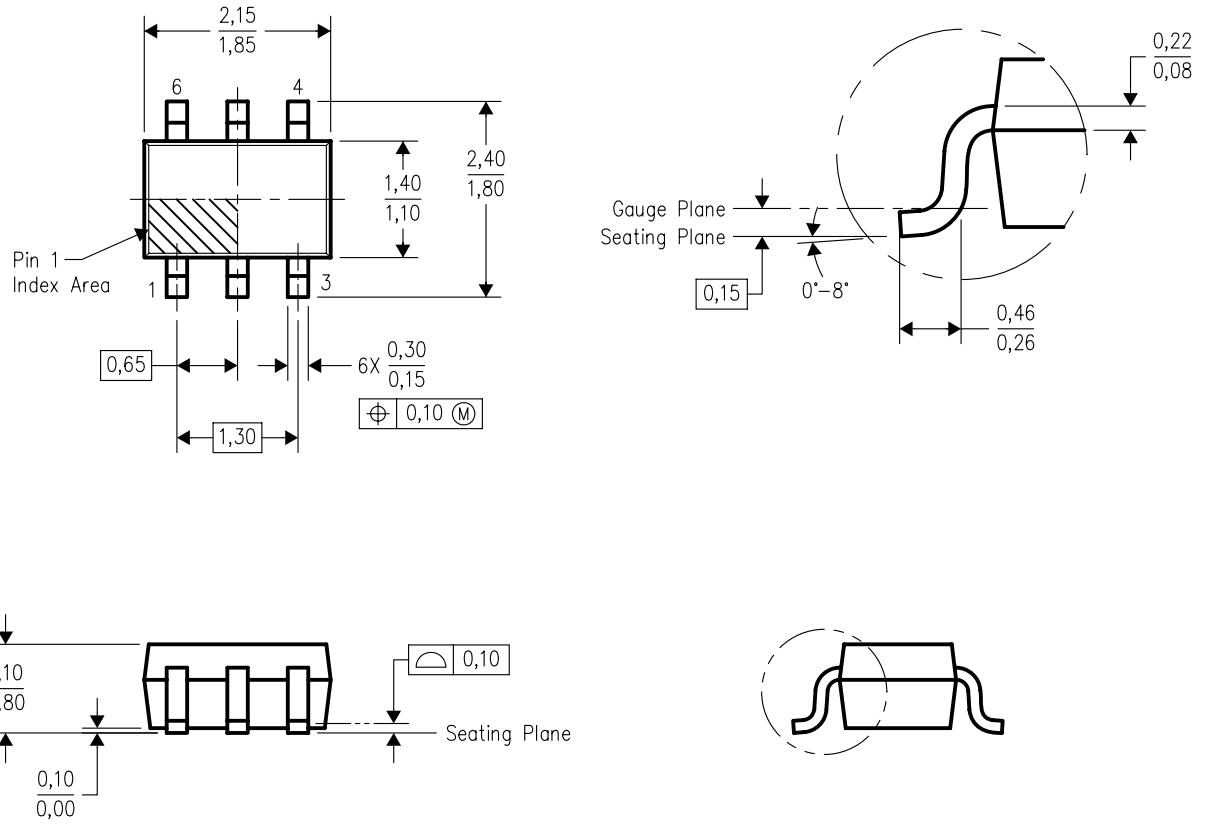
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/D 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

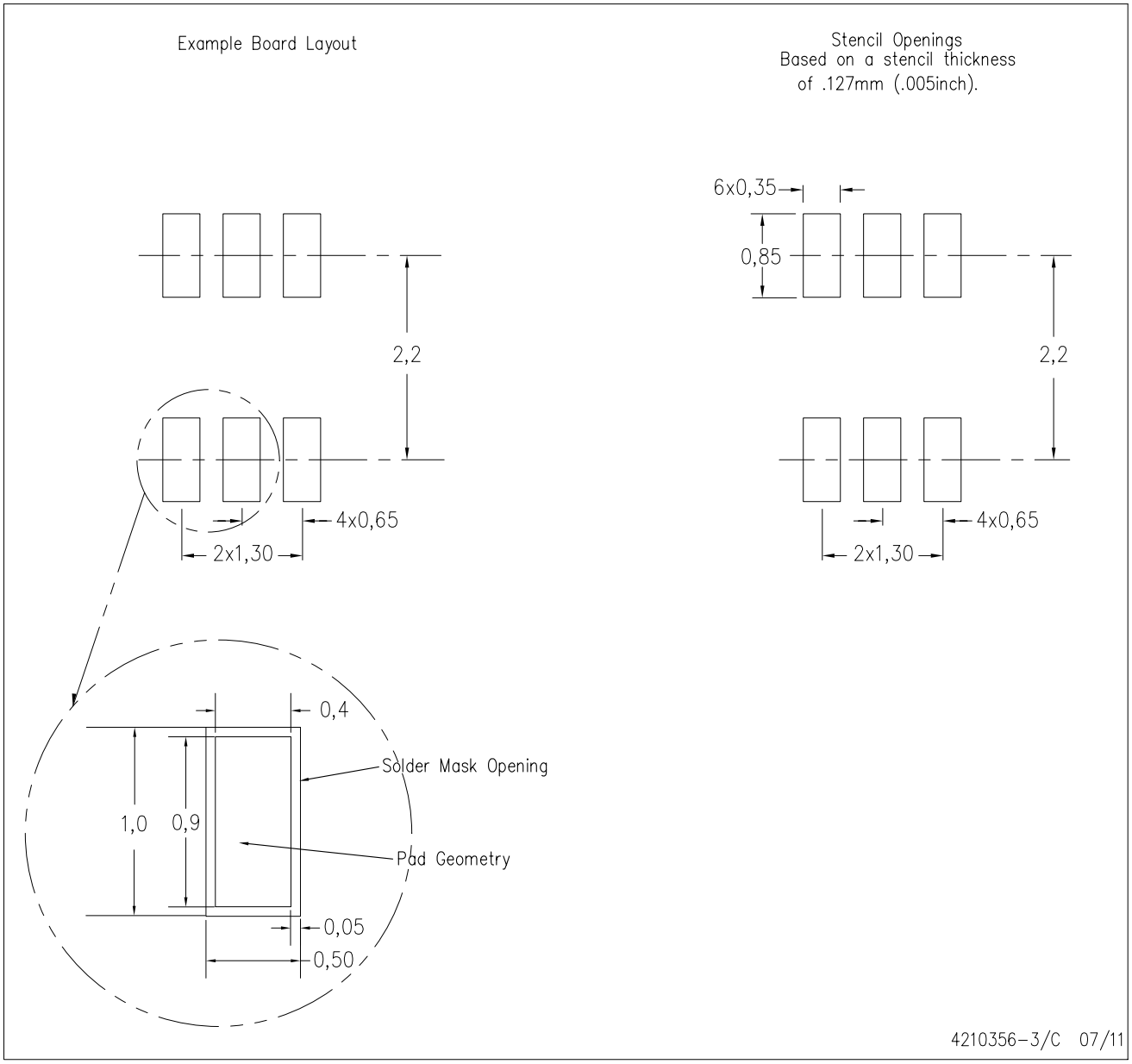
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



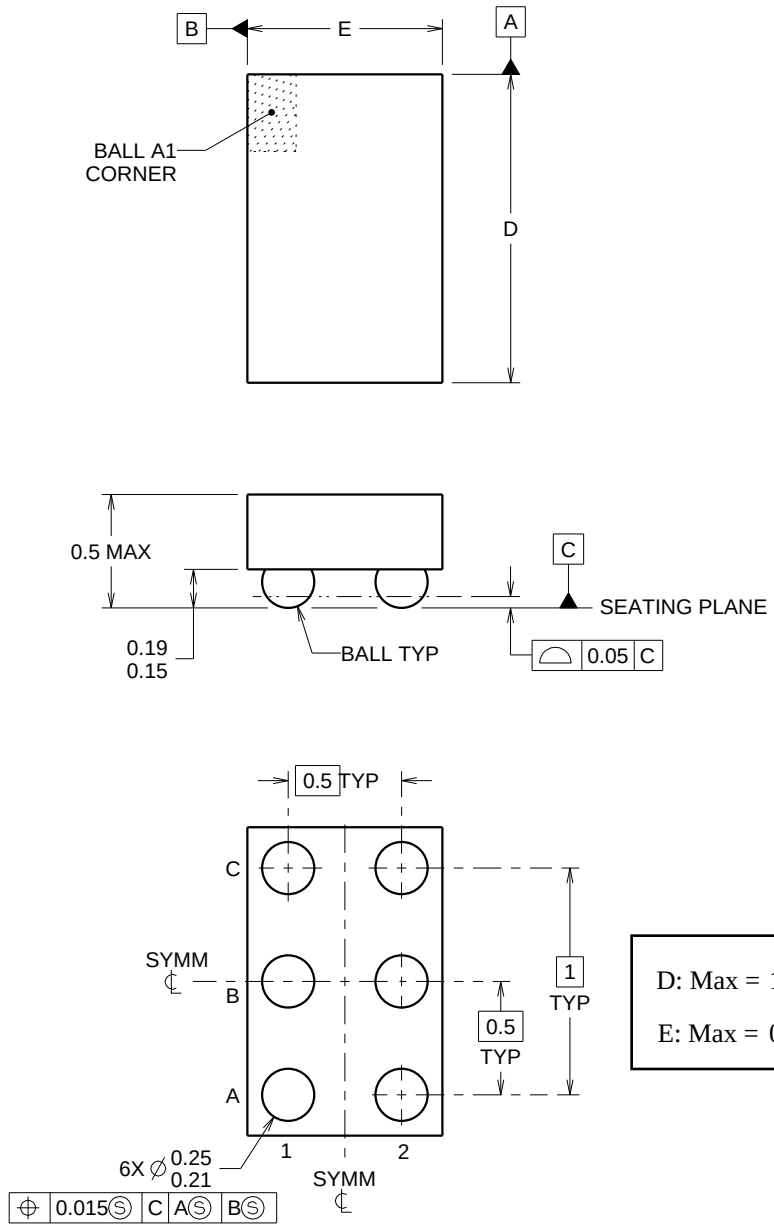
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.357 mm

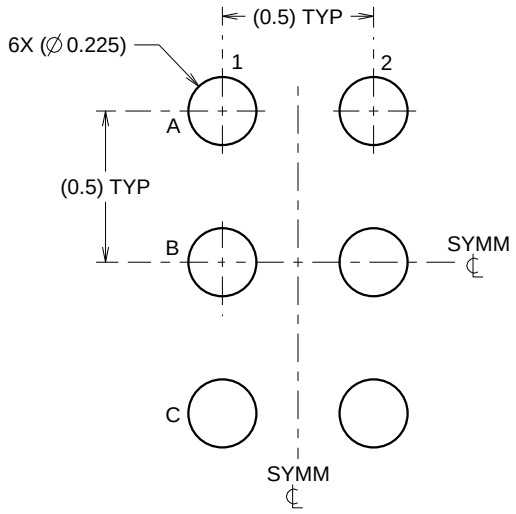
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

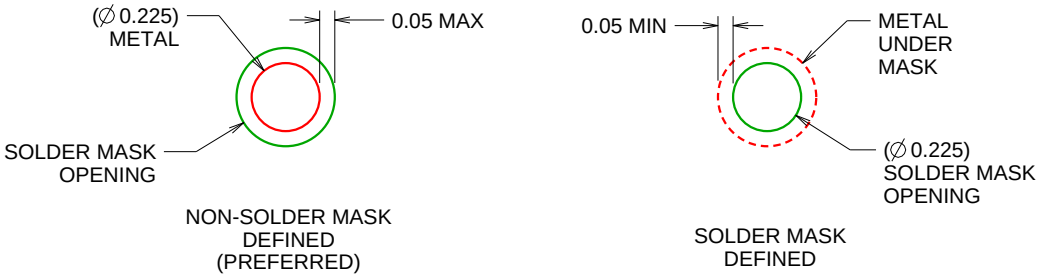
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

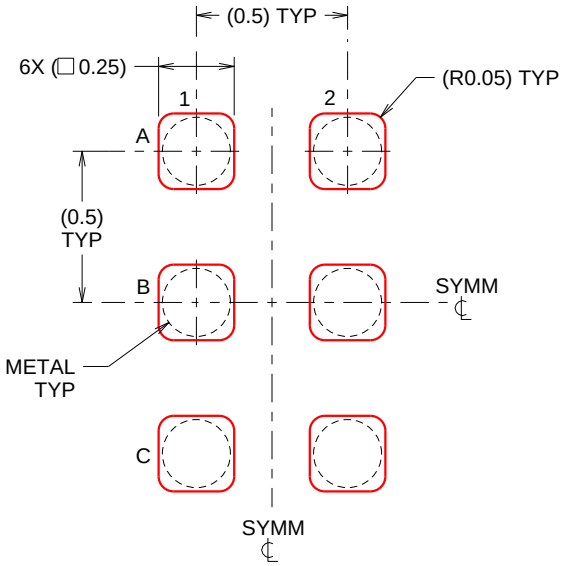


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

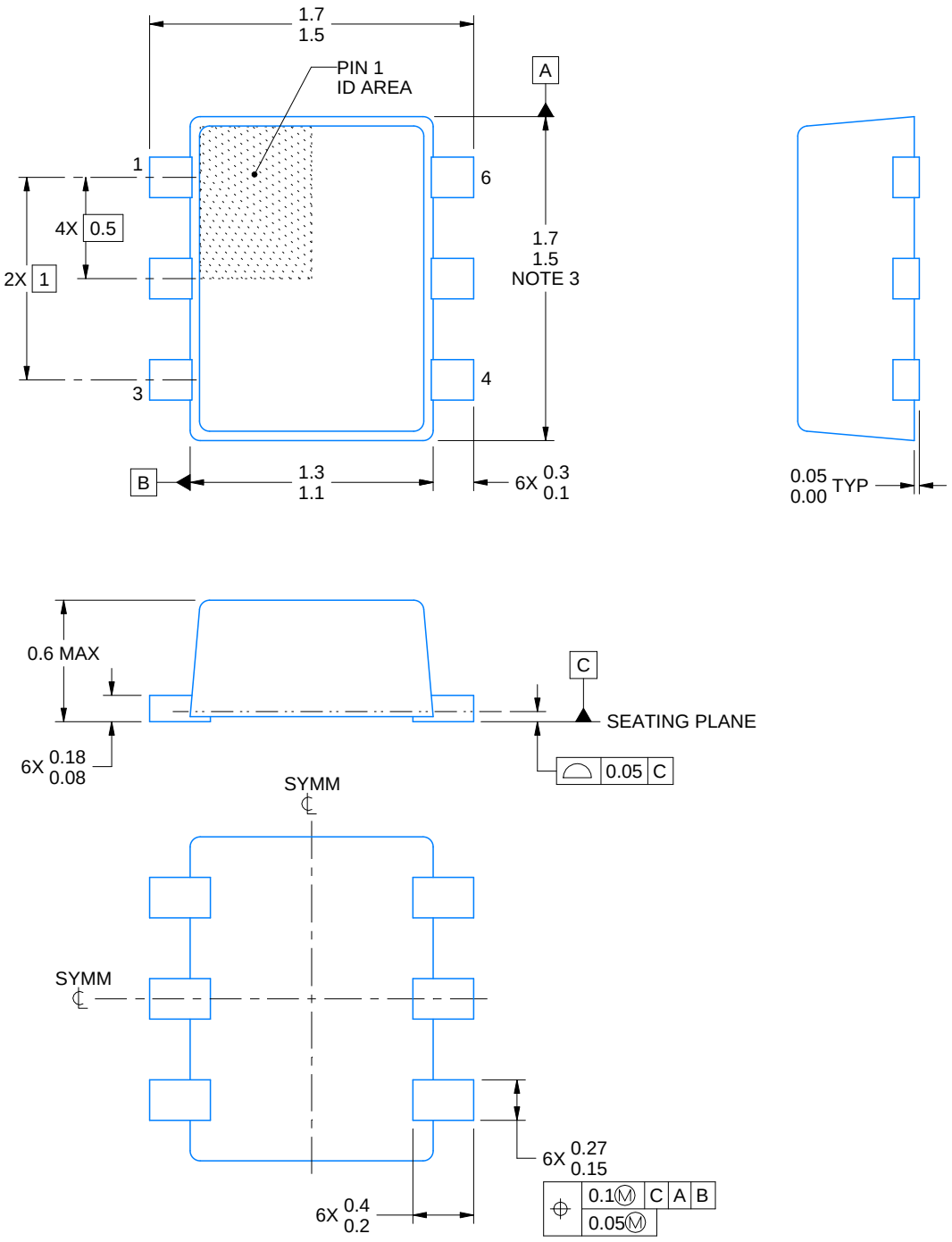
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DRL0006A

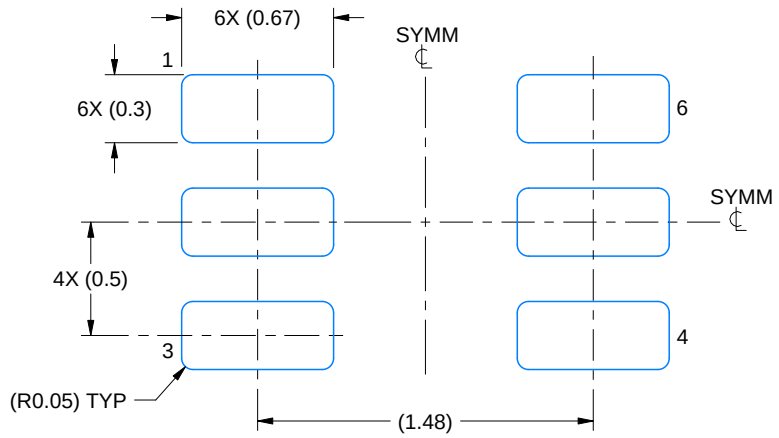
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

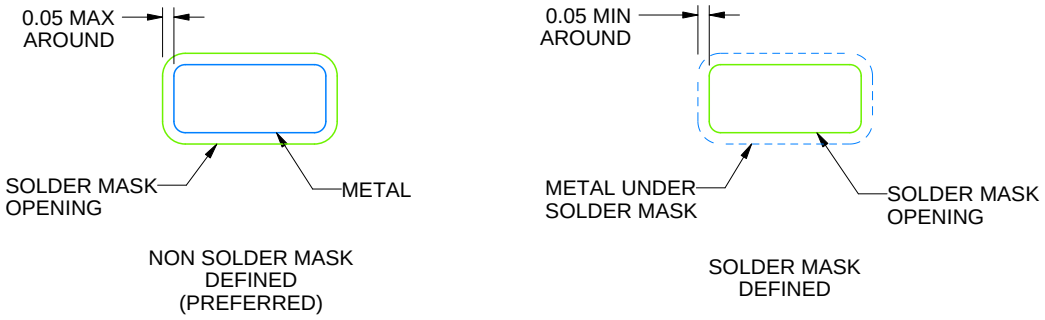


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

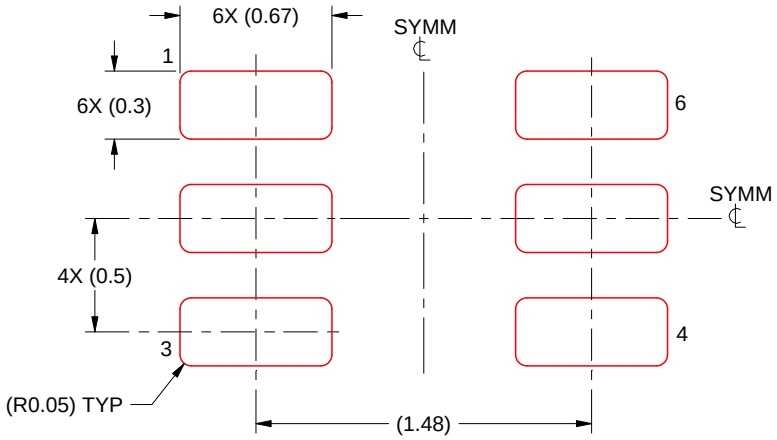
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

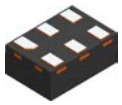
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

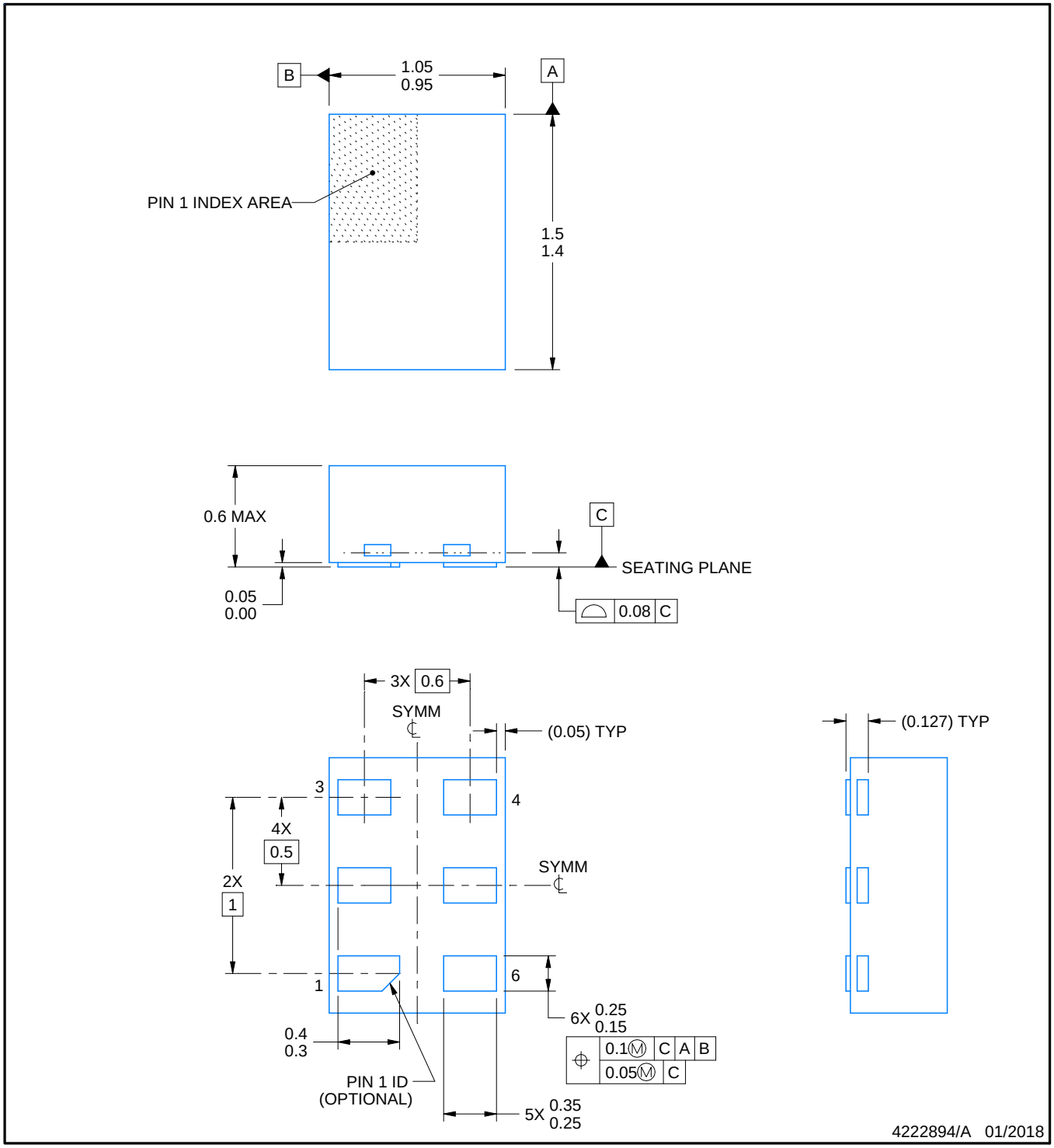
DRY0006A



PACKAGE OUTLINE

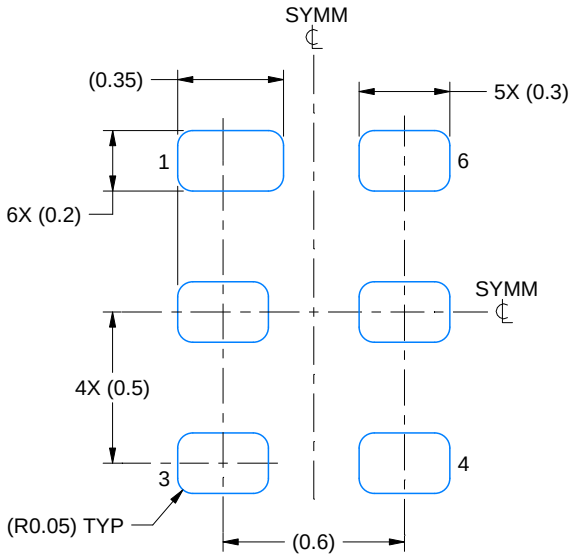
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

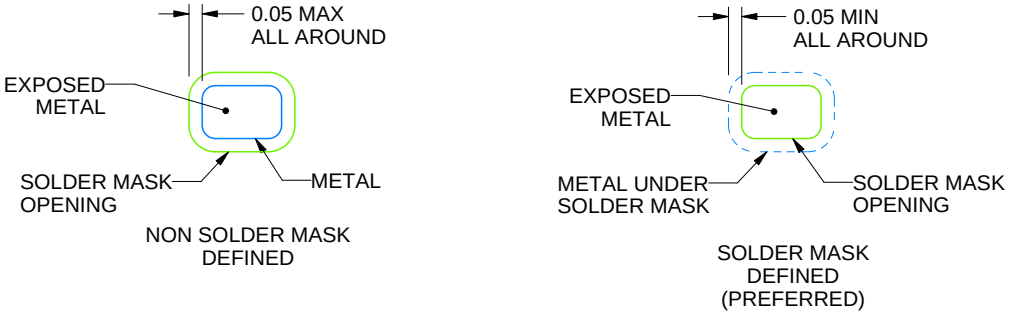


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

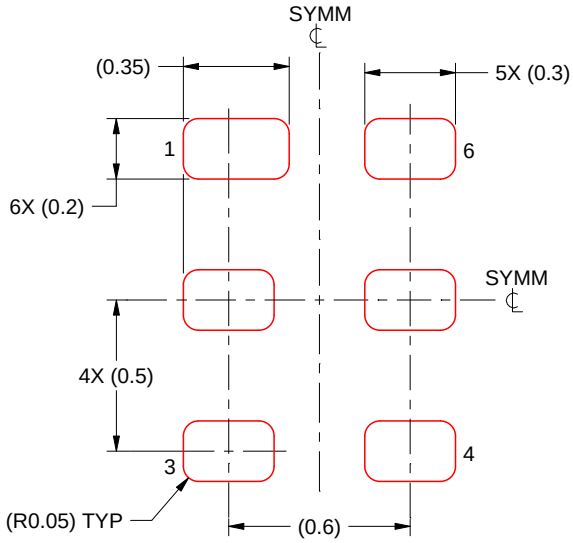
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

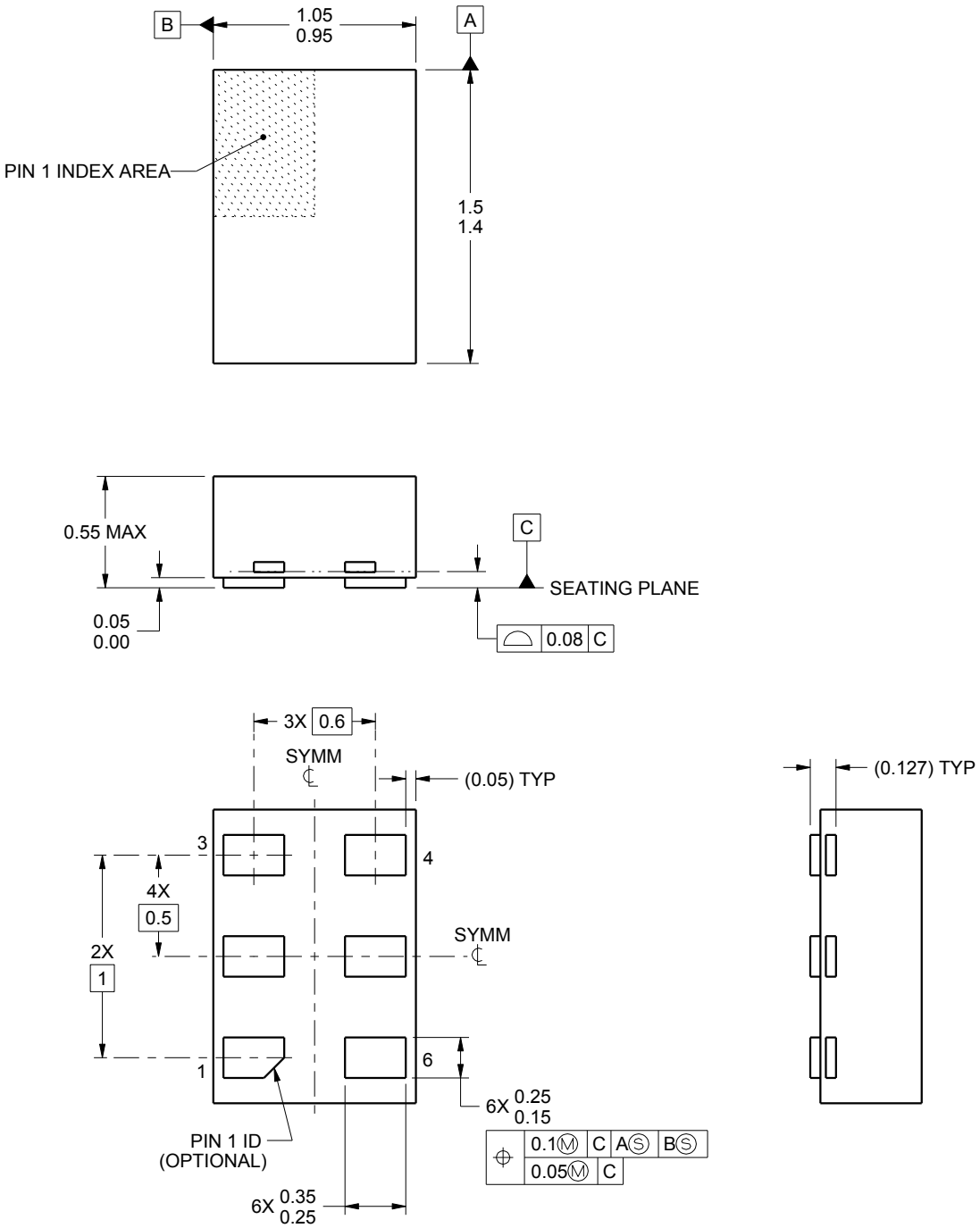
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRY0006B

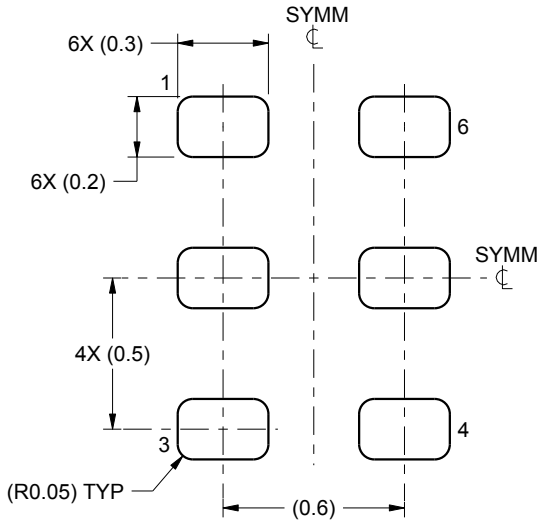
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

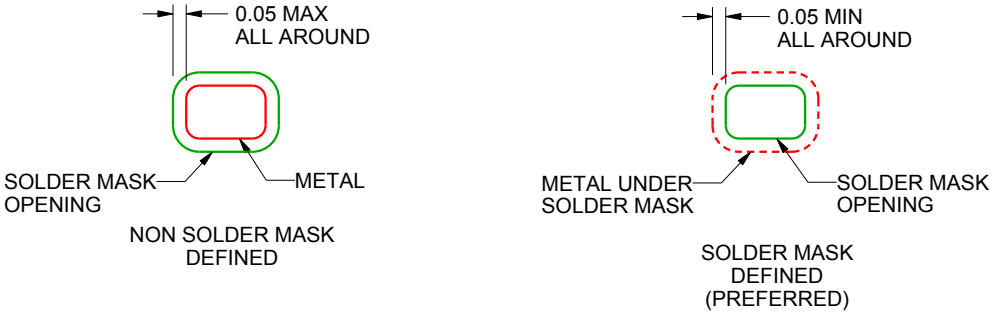


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

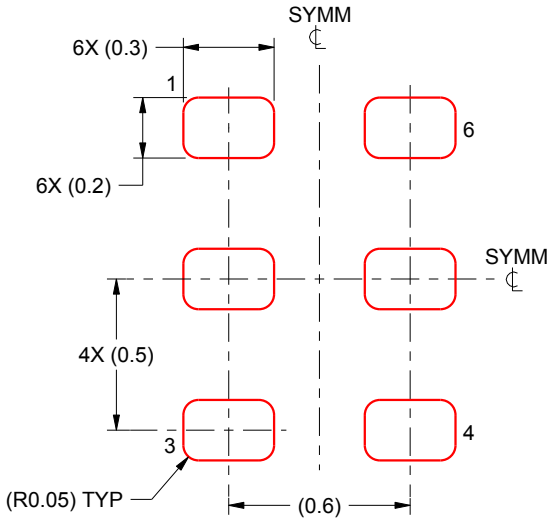
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

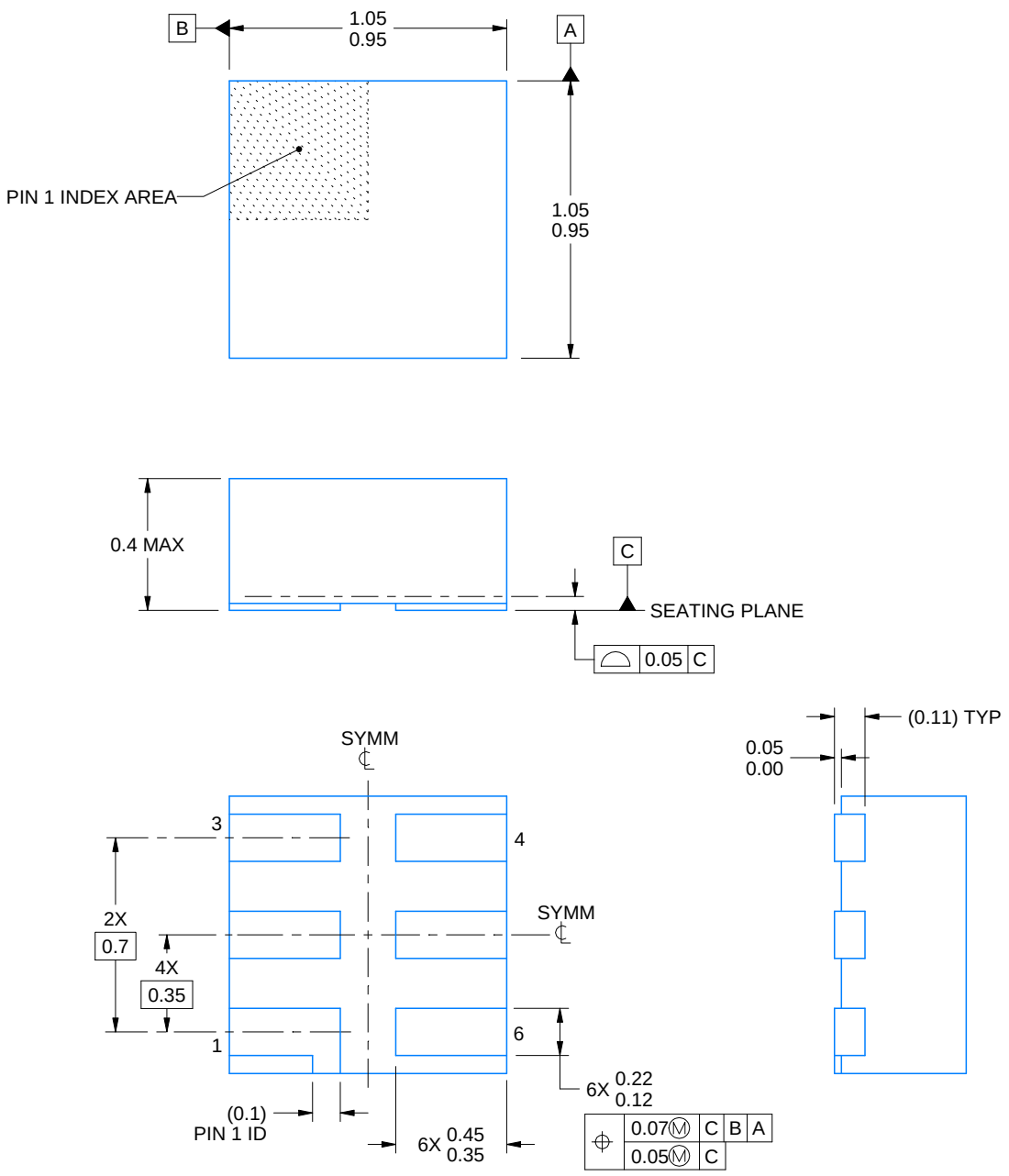
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

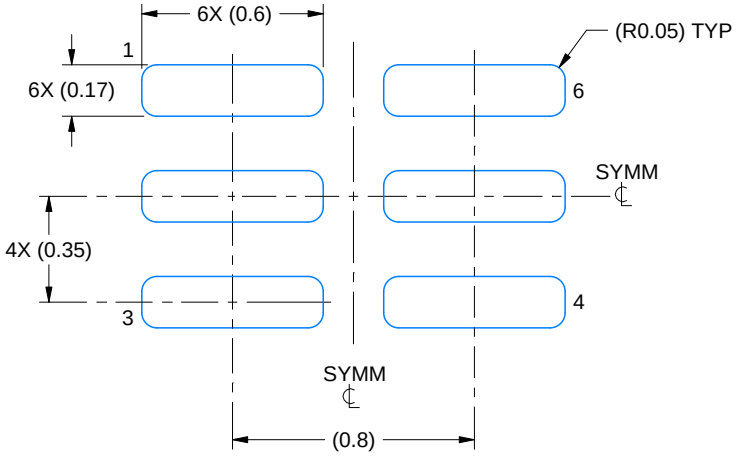
PLASTIC SMALL OUTLINE - NO LEAD



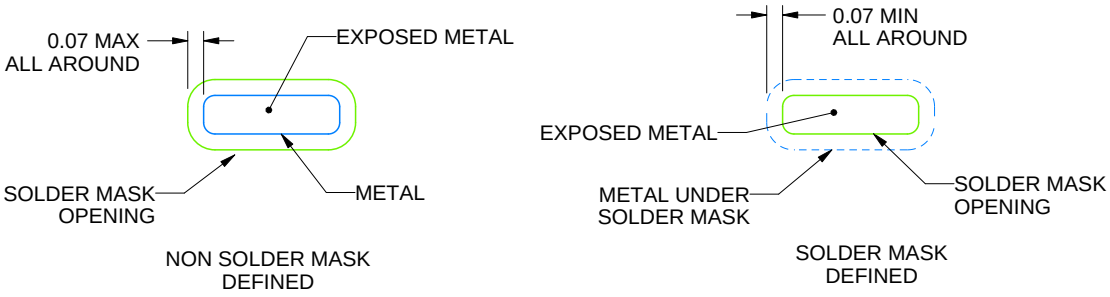
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

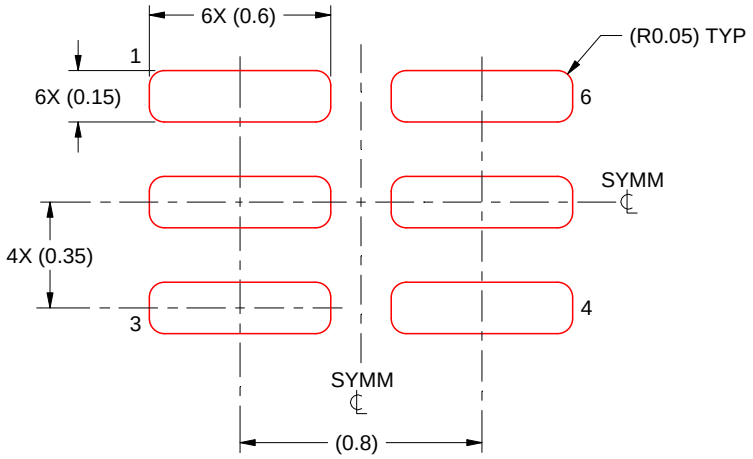
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

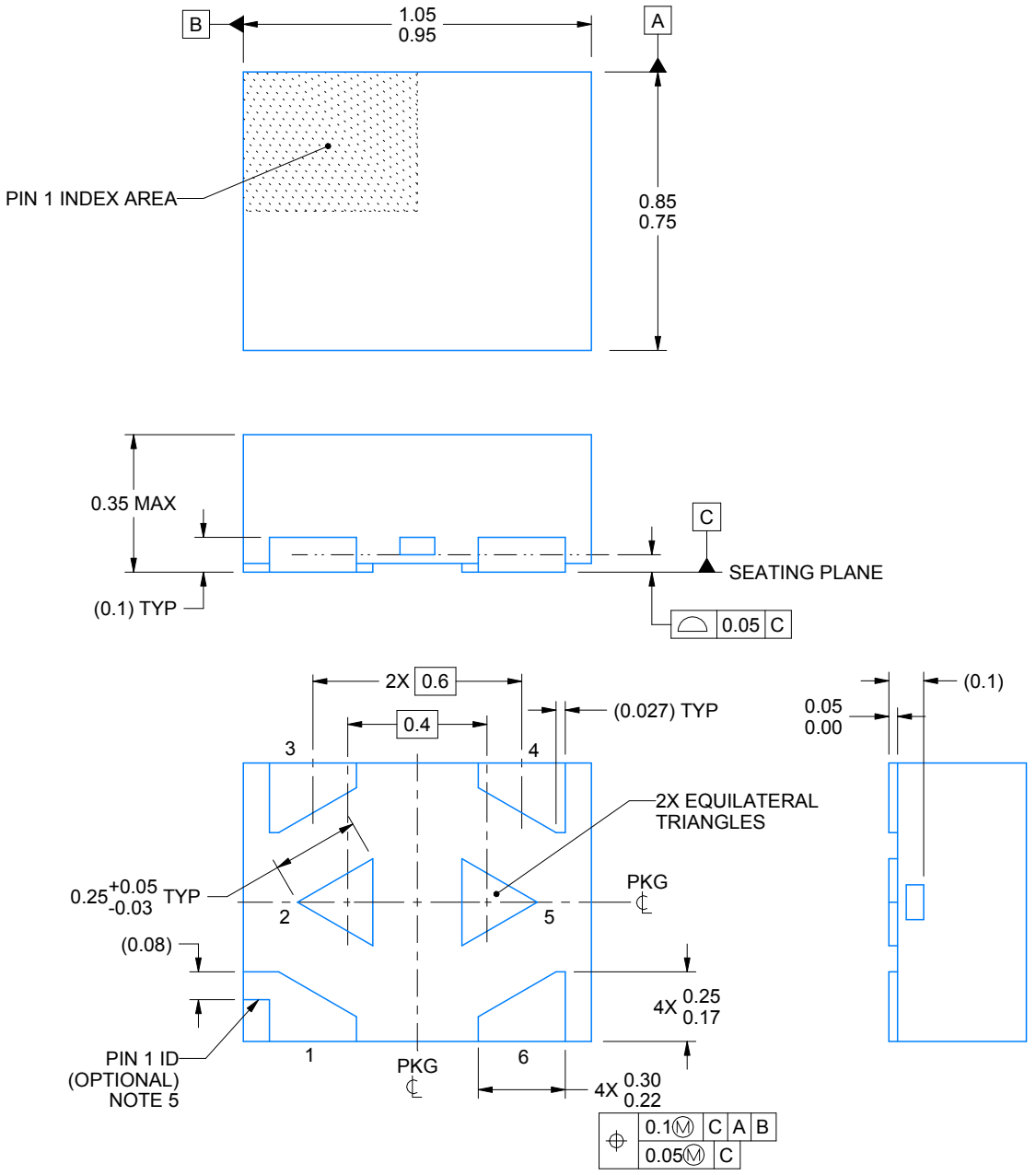
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DTB0006A

PACKAGE OUTLINE

X2SON - 0.35 mm max height

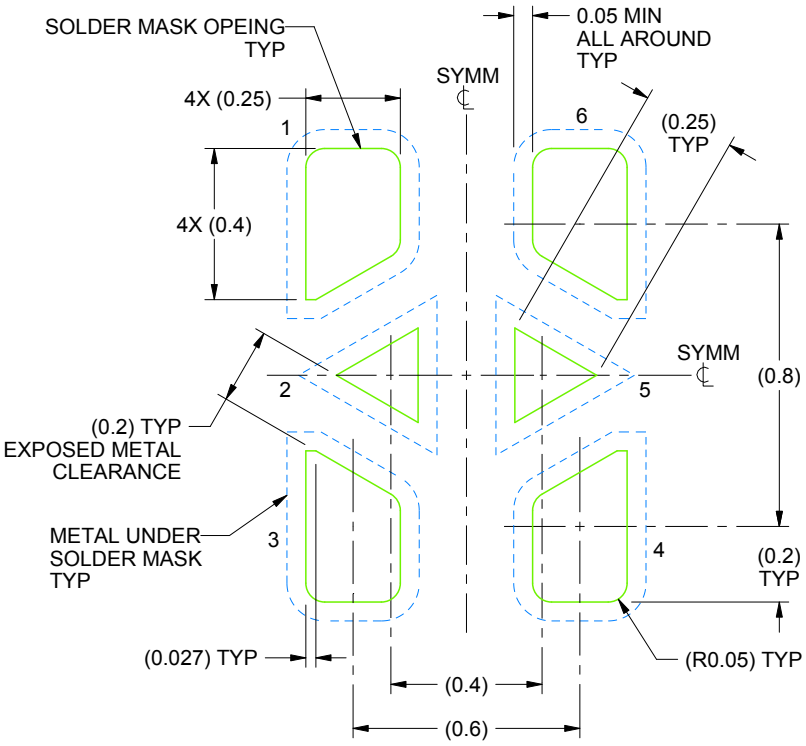
PLASTIC SMALL OUTLINE - NO LEAD



4223406/C 02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

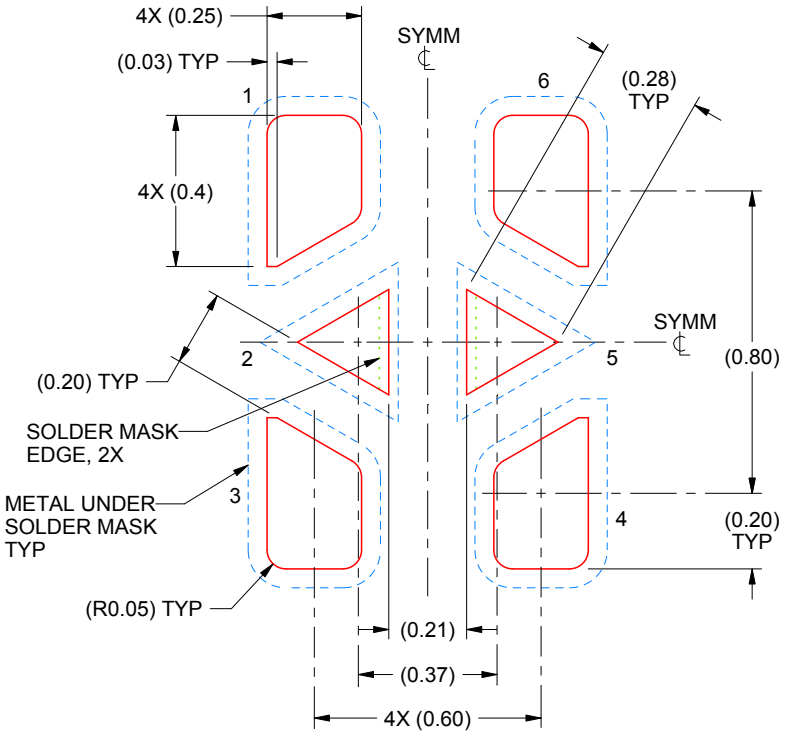


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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