



**MICROCHIP**

# **Platinum Rated 720W AC/DC Reference Design**

**Universal Single Phase Input, Single  
Phase Output**



# Agenda

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- **CSCI and ENERGY STAR Standards**
- **System Overview**
- **Hardware Information**
- **System Software**
- **Advanced Features**
- **Additional Resources**



# CSCI Efficiency Standards

## The Climate Saving Computing Initiative (CSCI) adds Platinum Efficiency standard as part of the ENERGY STAR specifications

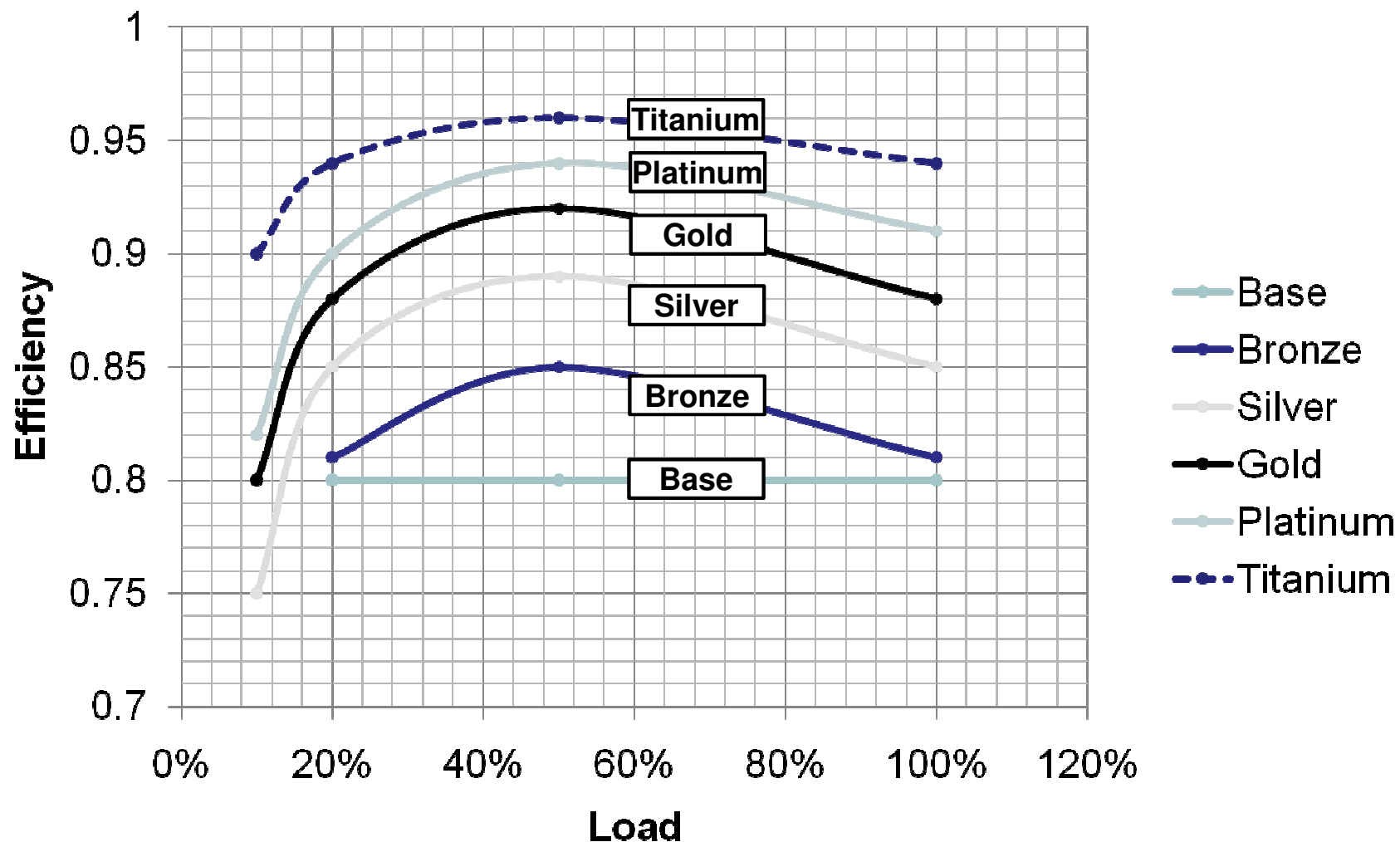
- Dedicated to blade and volume server applications
- 500-1,000W Single Phase 90-264V AC-Input, 12V Single DC-Output
- Specification defines minimum efficiencies and power factors for certain load conditions
- ENERGY STAR members have to meet Platinum Specification by July 2013



***Coming  
2014***

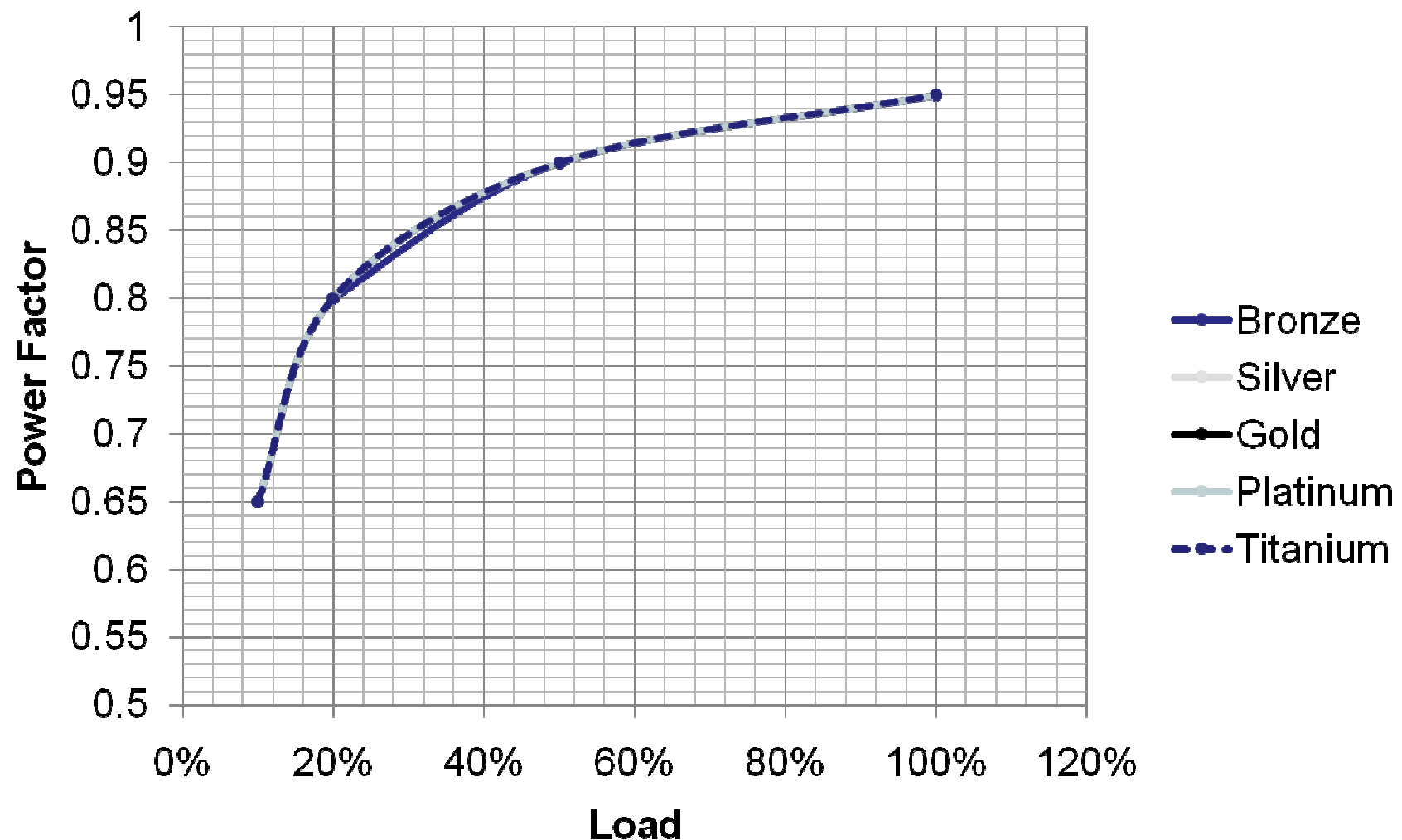


# CSCI Efficiency Levels





# CSCI Efficiency Levels





# Platinum-Rated AC/DC Reference Design

## Input:

- 90~264Vac, 45-65 Hz
- Active PFC (PF up to 0.99)

## Output:

- 12V DC / 60A (720W max)
- Load Regulation:  $\pm 1.5\%$
- Line Regulation:  $\pm 0.5\%$

## Efficiency:

- **Peak Efficiency:** 94.1%
- Meets ENERGY STAR CSCI Platinum Level

## Dimensions:

- 5U x 5U x 1U
- (222 x 222 x 44.45) mm





# Platinum-Rated AC/DC Reference Design

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## Special Features:

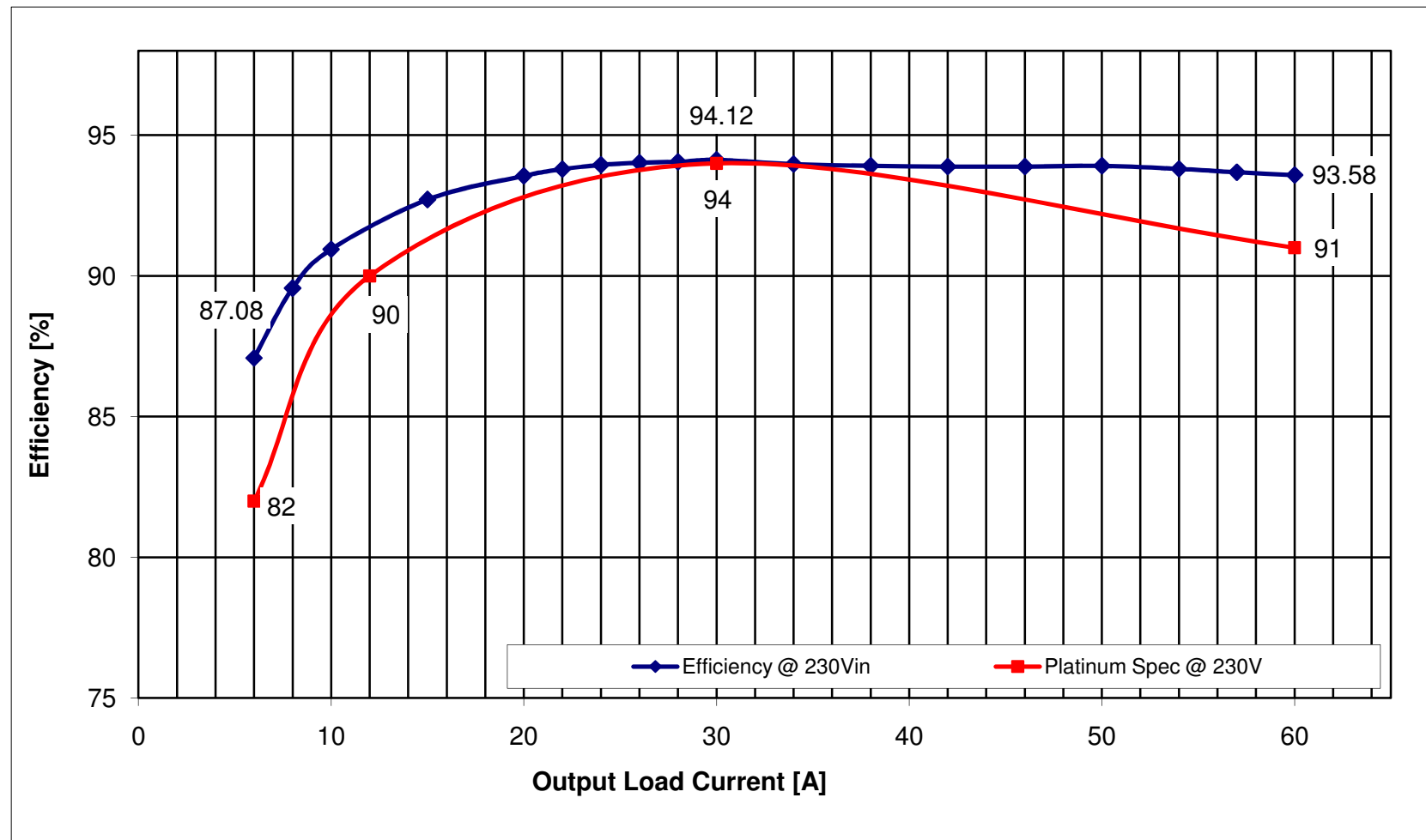
- Full digital control
- Enhanced system monitoring & fault handling
- Load share bus for N+1 Redundancy

## Efficiency Optimization:

- Switching Frequency Adaption
- Dynamic Bulk Voltage Adjustment
- Enhanced Sync Rectifier Control



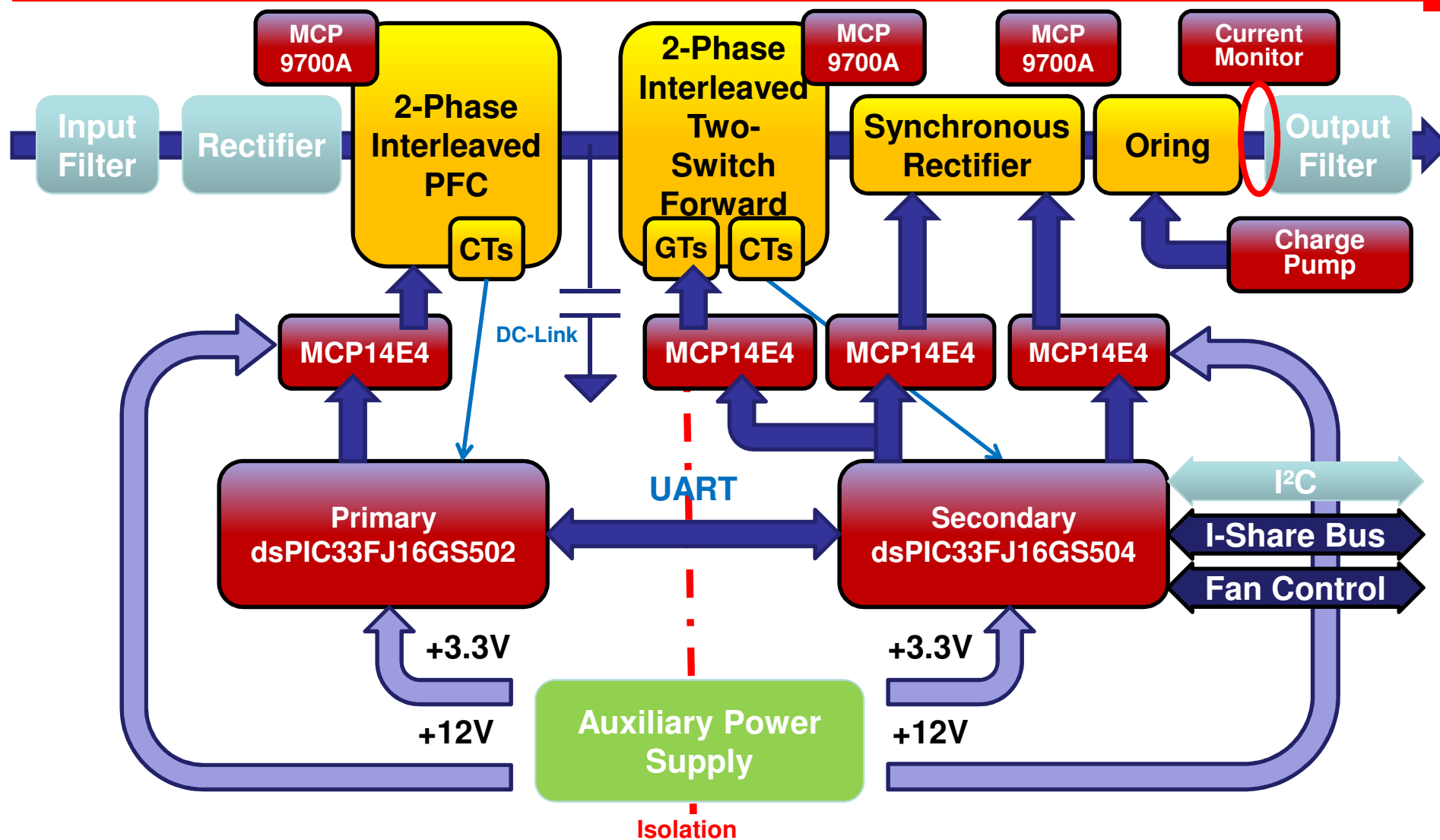
# Efficiency vs. Output Load





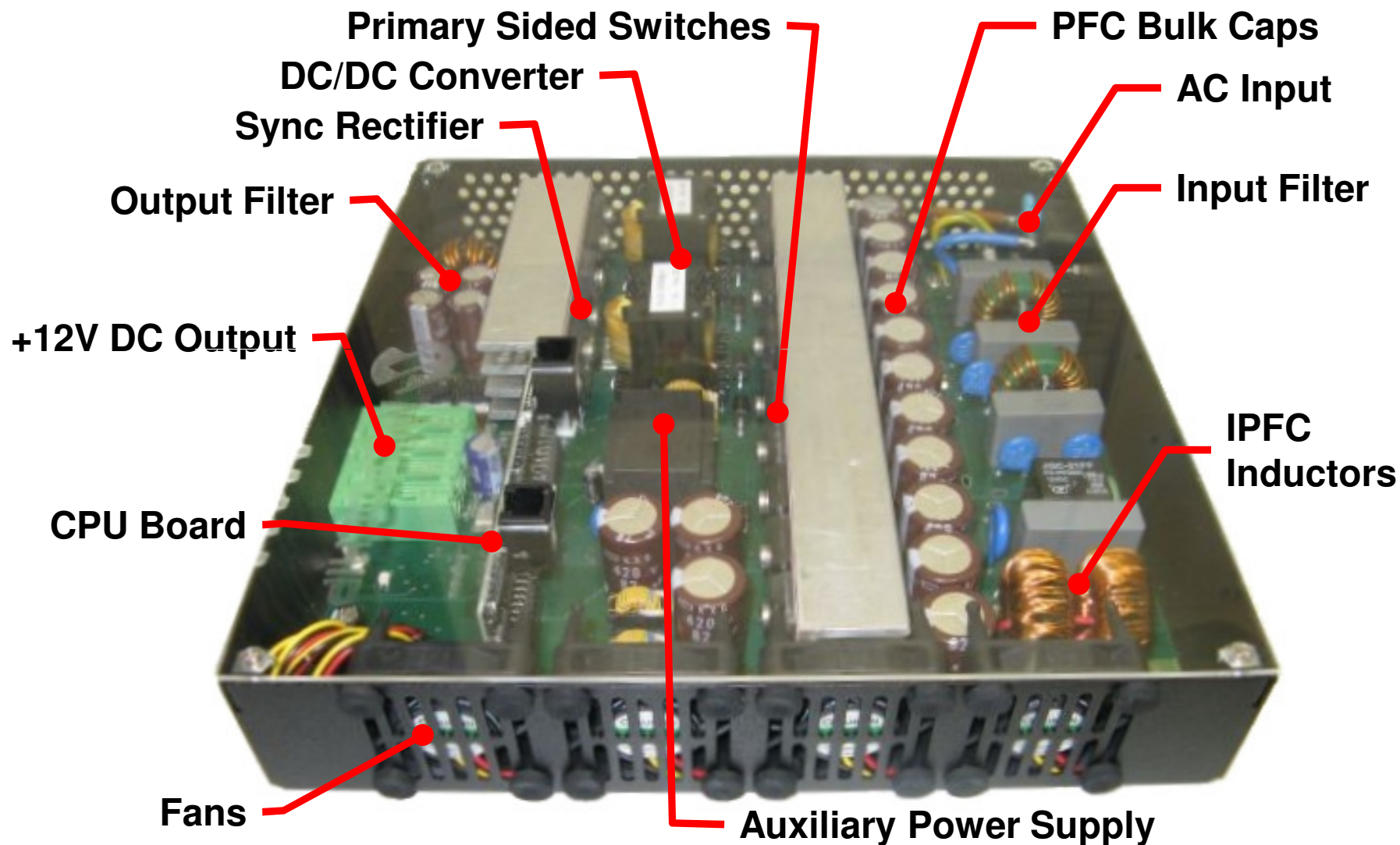


# High-Level Block Diagram



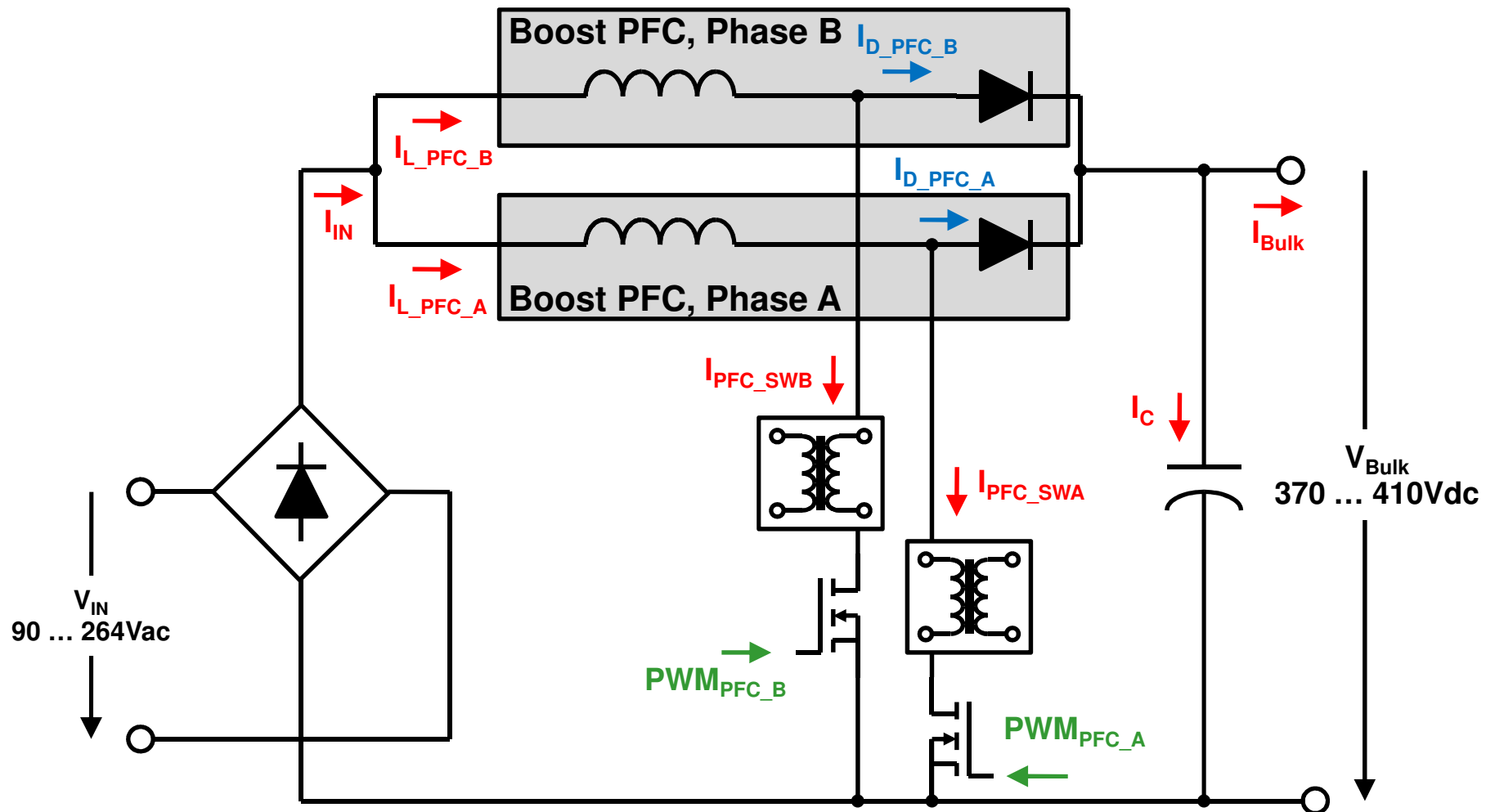


# Design Architecture



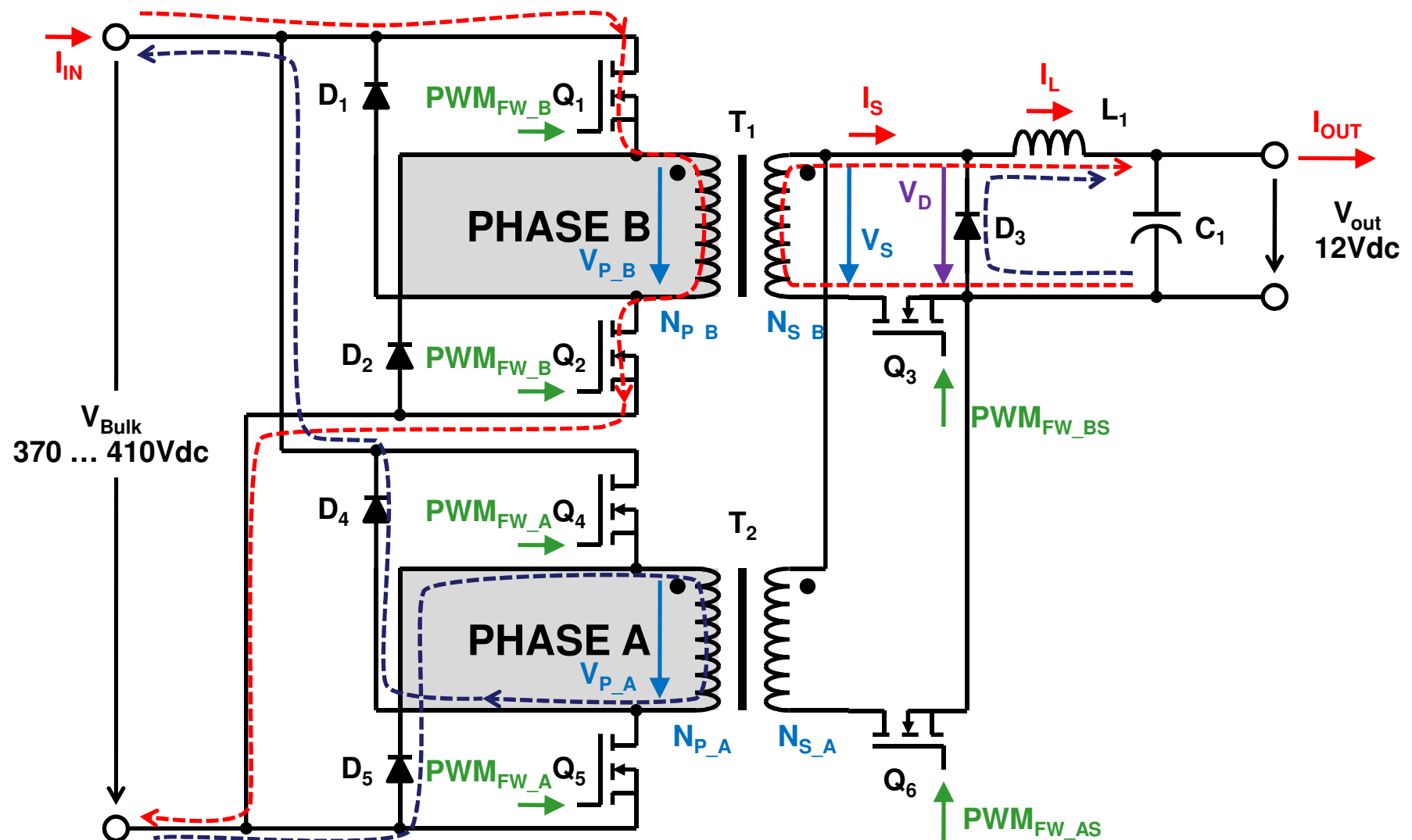


# Interleaved PFC Stage





# Interleaved 2-Switch Forward





# Software Overview

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**Two independent software projects**

- **Primary Side (PFC)**
- **Secondary Side (DC-DC)**

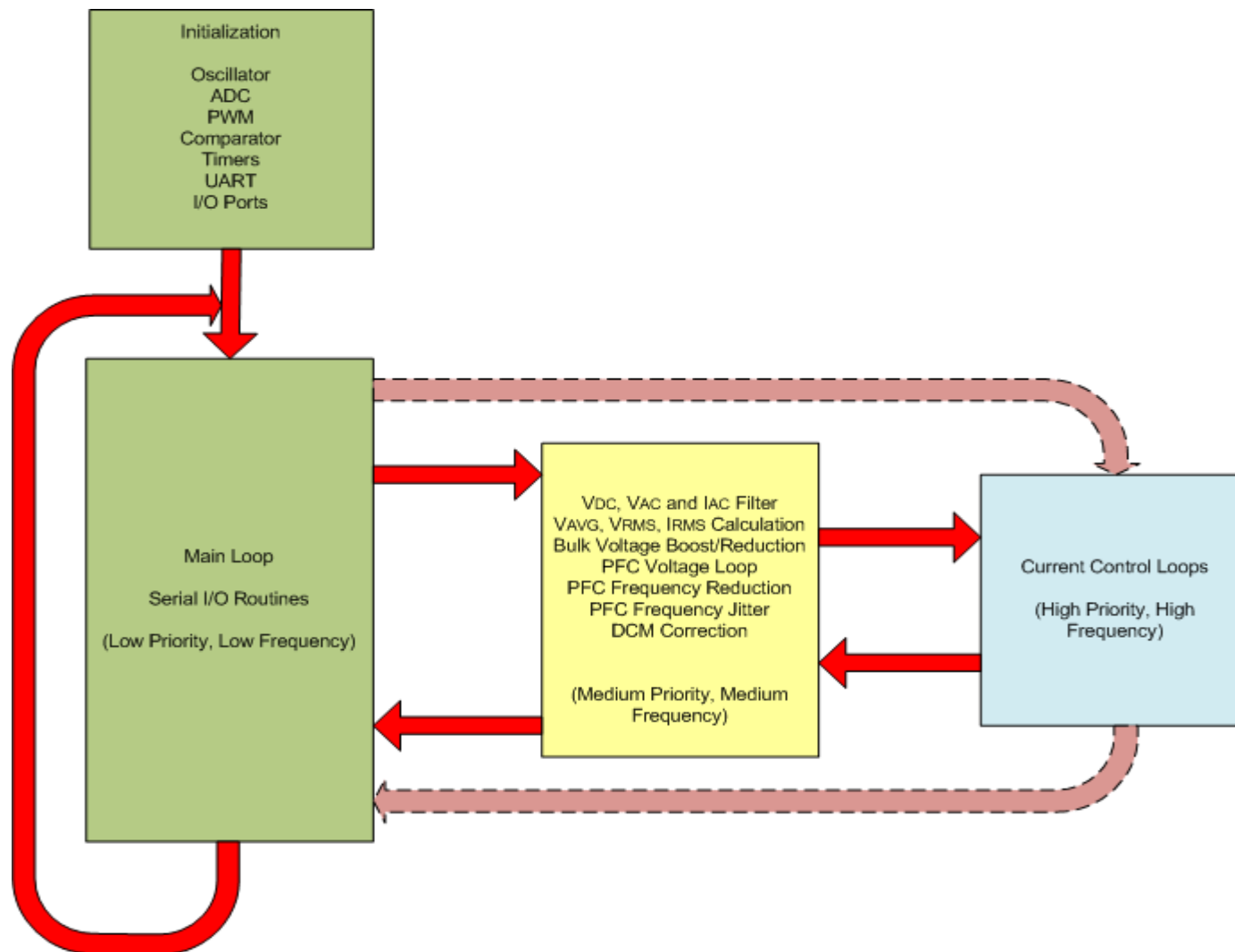
**Interrupt based priority scheme**

- **High Priority – Critical Power Control algorithms**
- **Medium priority – Advanced algorithms**
- **Low priority – Communications**

**UART Communication between primary and secondary  
for exchange of system information**



# System Software - Primary





# Primary Control Loop

## **Primary Side Control Loop consists of three sub-sections**

- Voltage Control Loop
- Current Control Loop
- Sine modulation of current and input feed-forward

## **Current Control Loops (x2)**

- High speed PI algorithm
- Executed in ADC ISR (Highest priority)
- Independent control loops for each interleaved phase

## **Sine Modulation**

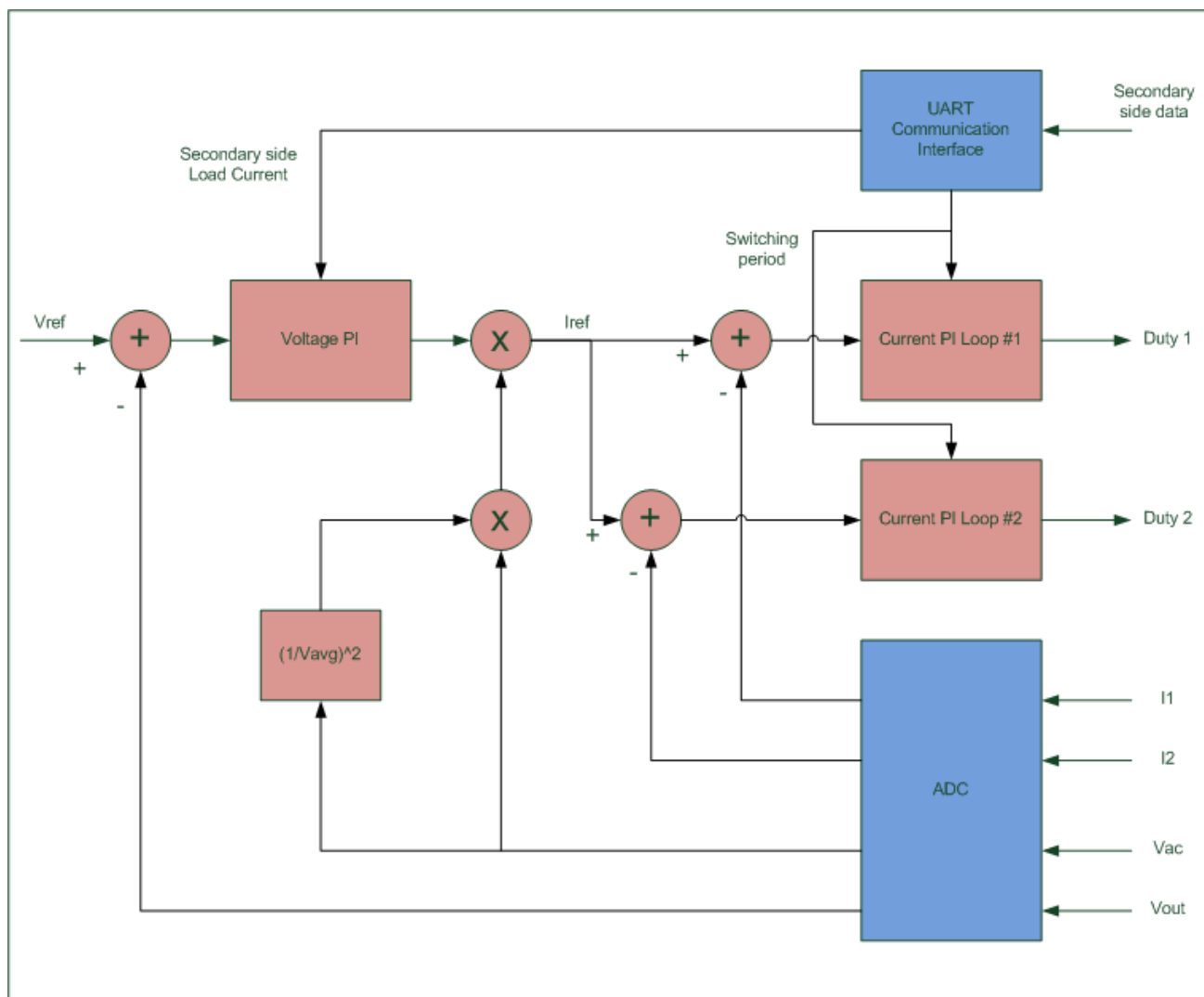
- Modulates output of voltage loop into a sinusoidal shape
- Adds input voltage feed-forward
- Executed in Timer2 ISR (Medium priority)

## **Voltage Loop**

- Controls output voltage using PI algorithm
- Executed in INT2 ISR (Medium priority) once every four Timer2 ISRs



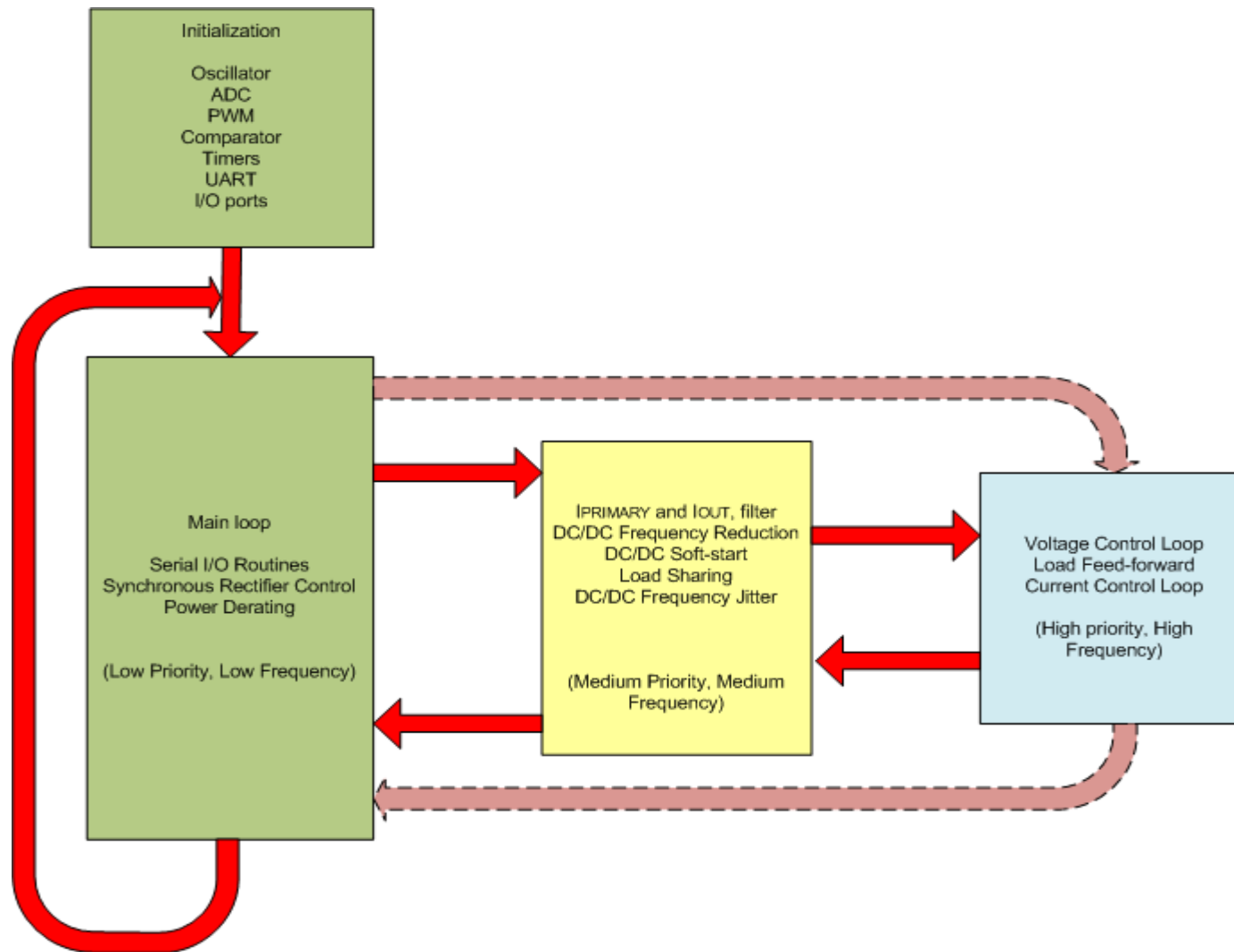
# Primary Control Loop







# System Software - Secondary





# Secondary Control Loop

**Secondary Side Control Loop consists of three subsections**

- Voltage Control Loop
- Current Control Loop
- Load Feed-forward

## **Current Control Loop**

- High speed PI algorithm
- Executed in every other PWM Special Event ISR (High priority)

## **Voltage Loop**

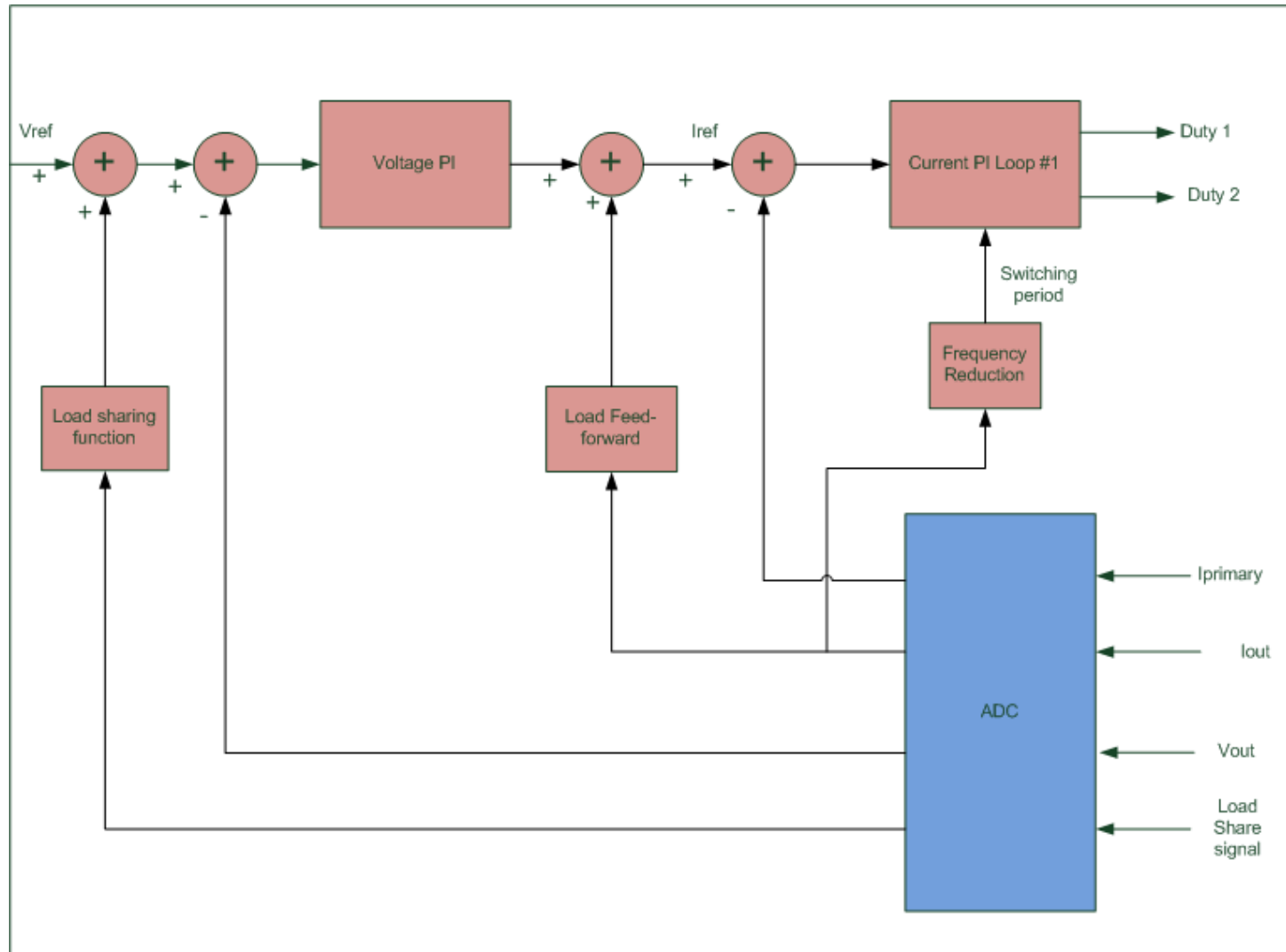
- High Speed PI algorithm
- Executed in every other PWM Special Event ISR (High priority)

## **Load Feed-Forward**

- Executed in every other PWM Special Event ISR (High priority)
- Improves response to load transients



# Secondary Control Loop





# Advanced Features

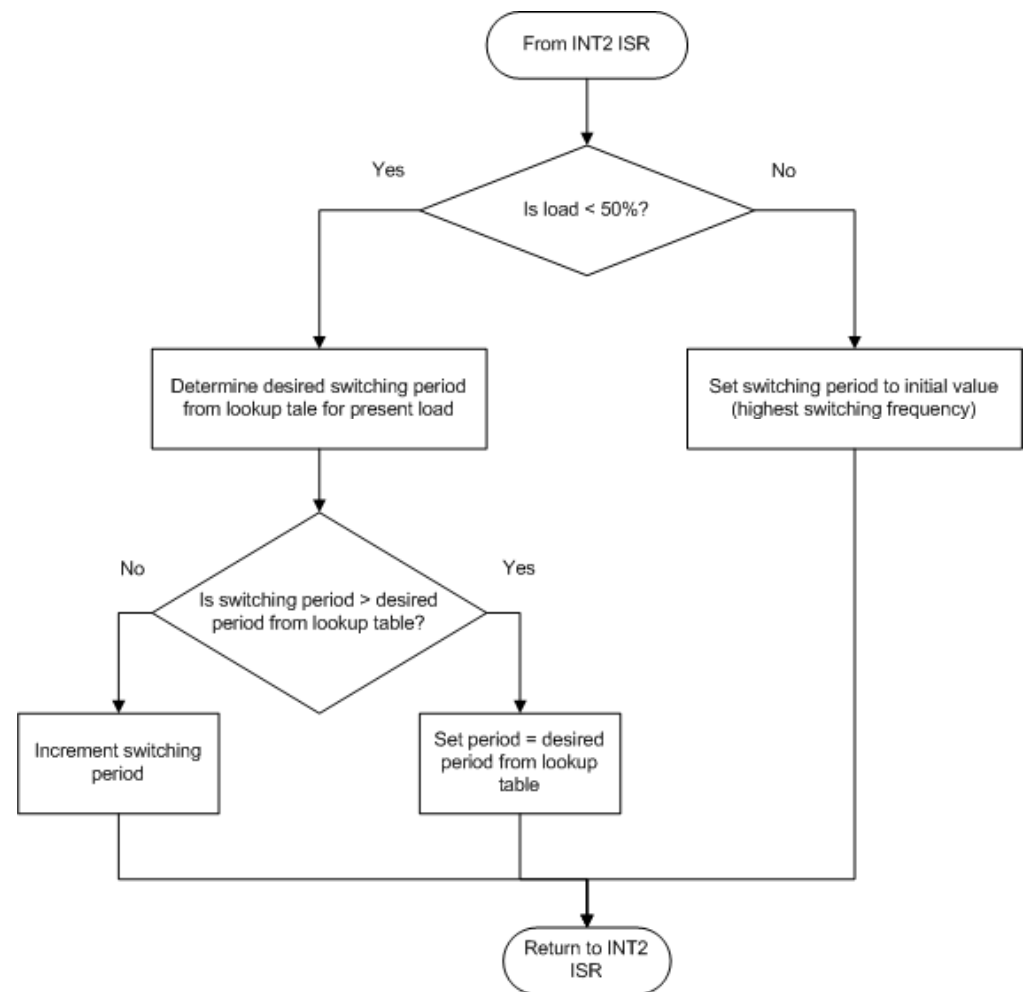
Algorithm	Primary	Secondary
Frequency Reduction	X	X
Frequency Jitter	X	X
DCM Correction	X	
Bulk Voltage Reduction/Boost	X	
Synchronous Rectifier Control		X
Power Derating		X
Load Sharing		X



# Frequency Reduction

- Improved efficiency at light loads
- Frequency is reduced gradually in small steps until optimum frequency is reached
- When a load transient is detected, frequency is instantly increased to maximum to maintain good response

PRIMARY SIDE	X
SECONDARY SIDE	X

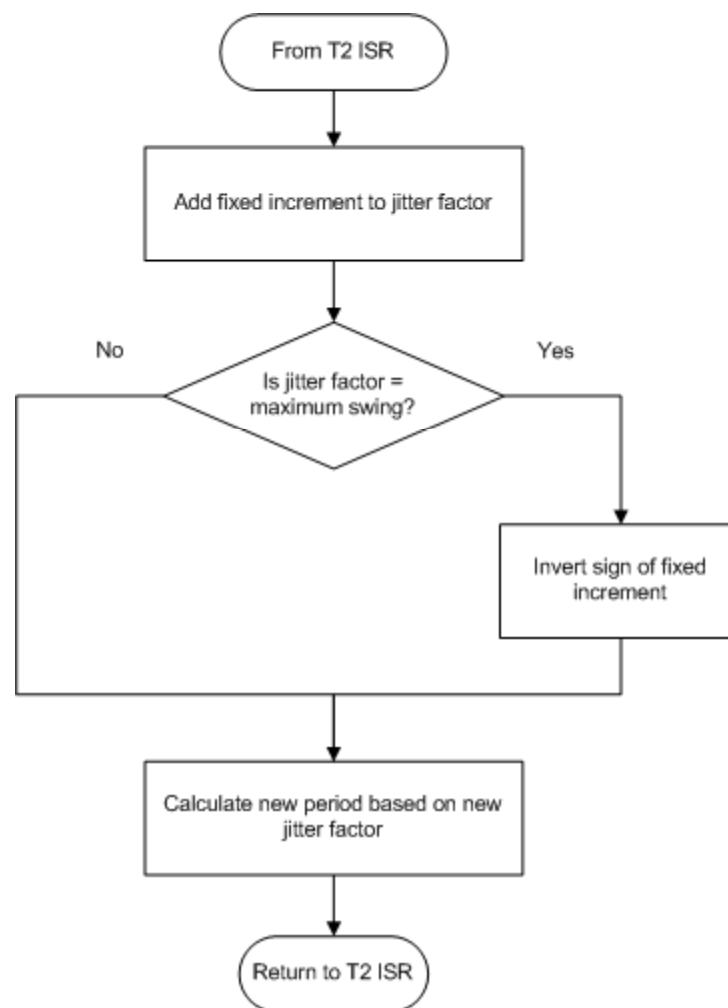




# Frequency Jitter

- Improves EMI performance of the system
- Jitter is applied to switching frequency at a slow rate after frequency reduction algorithm

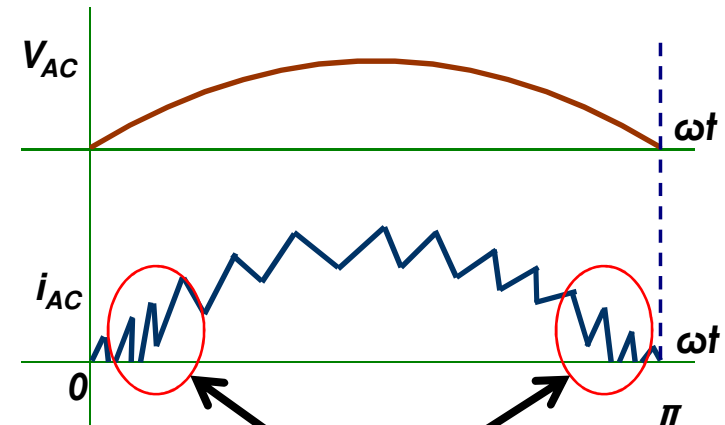
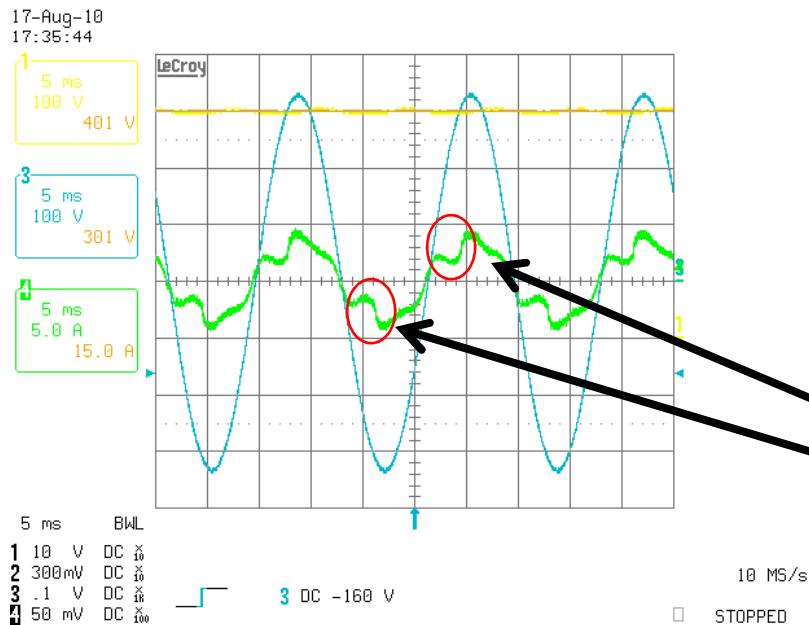
PRIMARY SIDE	X
SECONDARY SIDE	X





# PFC Discontinuous Conduction Mode (DCM)

- Transfer function becomes non-linear in DCM mode
- Control system can compensate for different operating modes



Transition between  
CCM and DCM modes

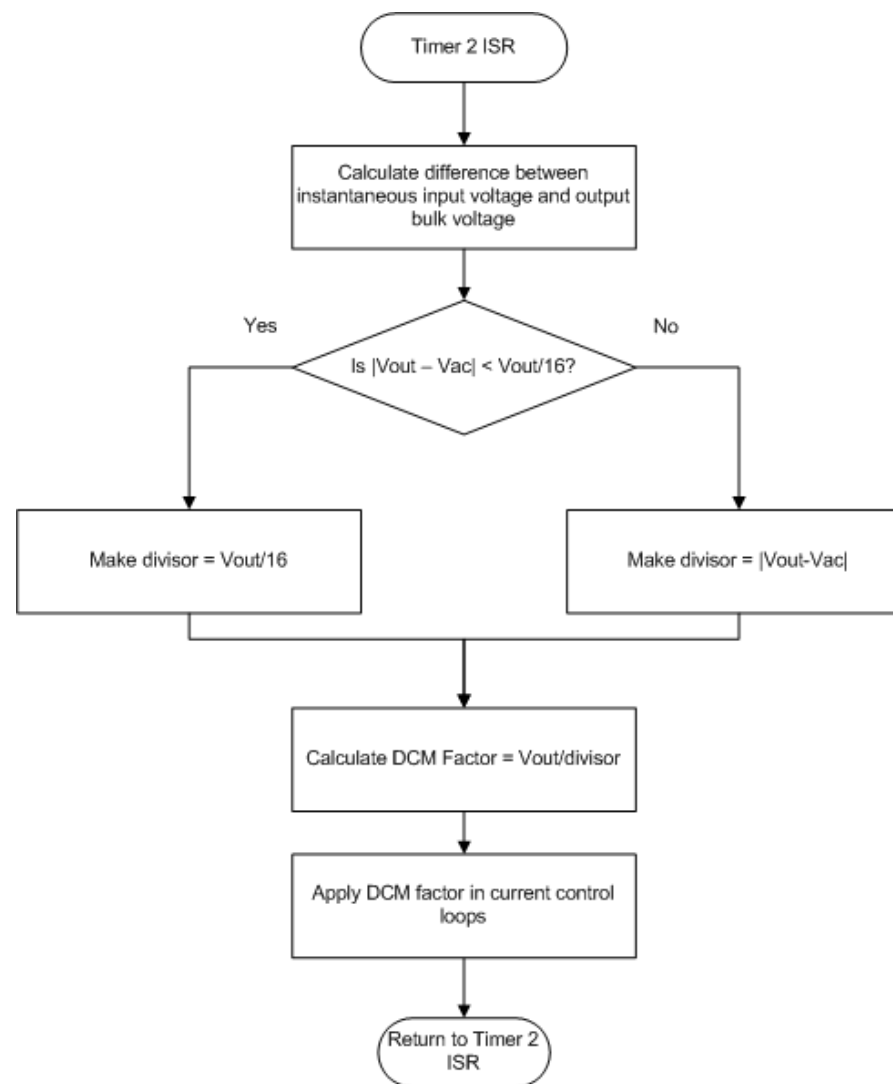
Worst Case:  
50-50% CCM and  
DCM operation



# DCM Correction

- Transition between CCM mode and DCM mode for PFC causes waveform distortion
- A correction factor is added to current control algorithm to improve PF and THD at light loads due to DCM-CCM transitions

PRIMARY SIDE	X
SECONDARY SIDE	



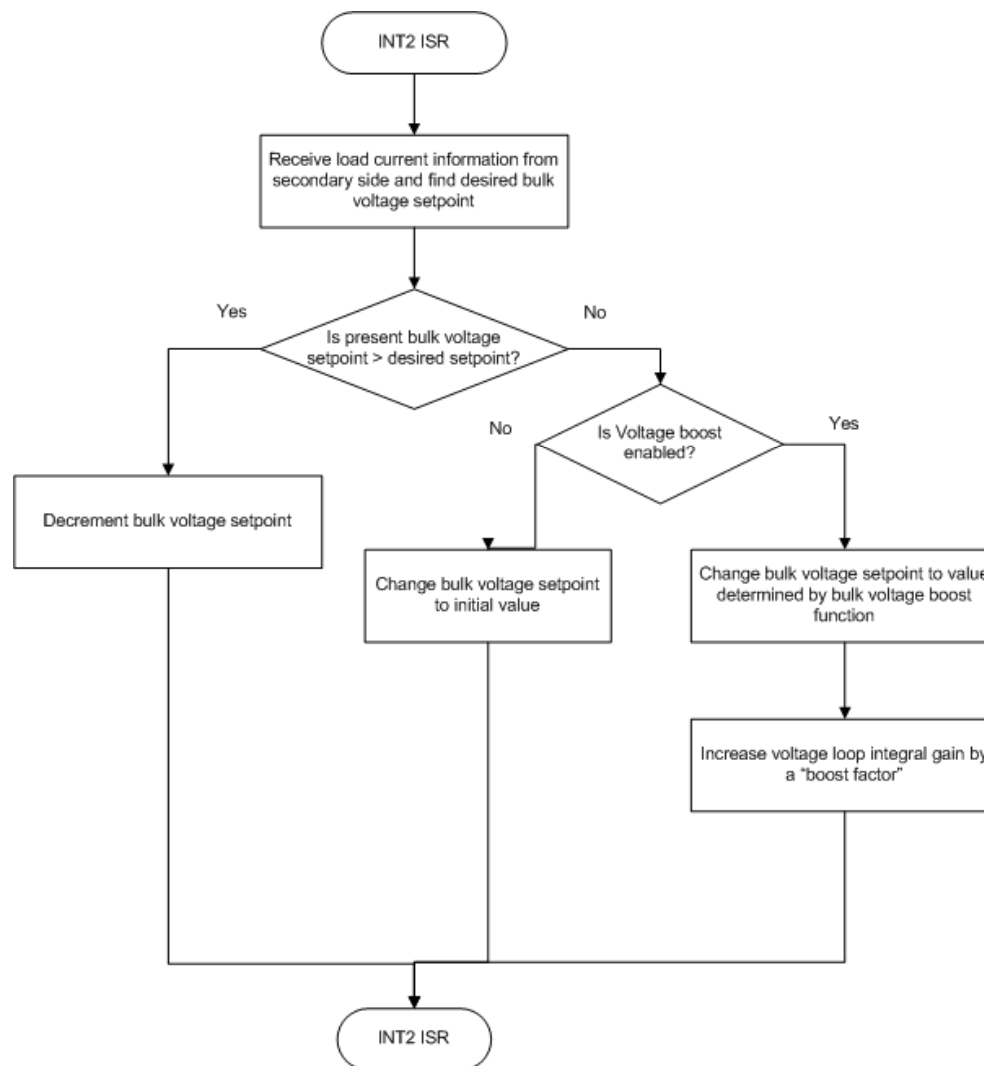




# Bulk Voltage Reduction/Boost

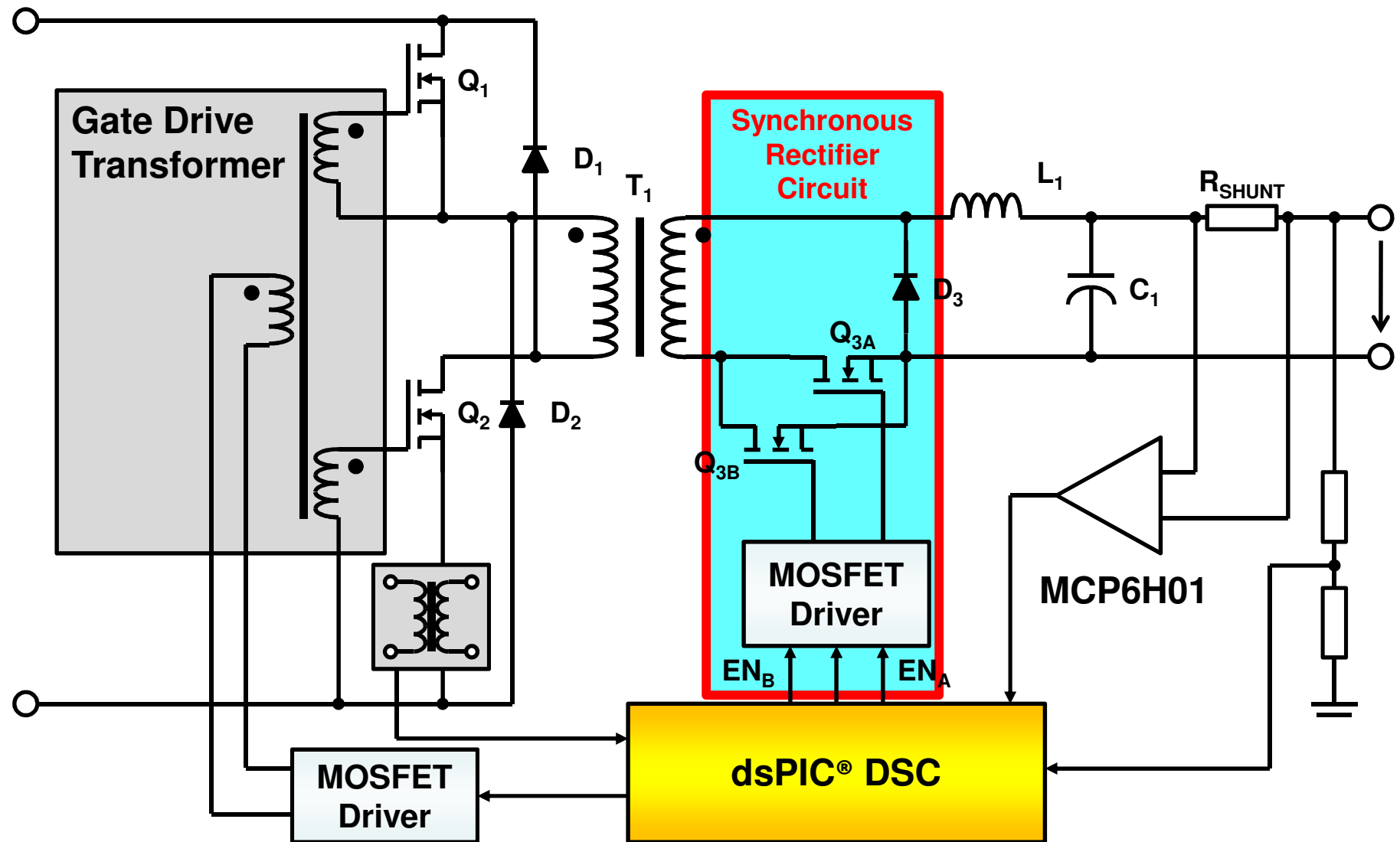
- PFC Output Bulk voltage is reduced to improve efficiency
- At light loads, a reduced bulk voltage can still allow the DC-DC
- Output Bulk Voltage is increased instantaneously in the event of a load transient to maintain good response

PRIMARY SIDE	X
SECONDARY SIDE	





# Synchronous Rectifier Control

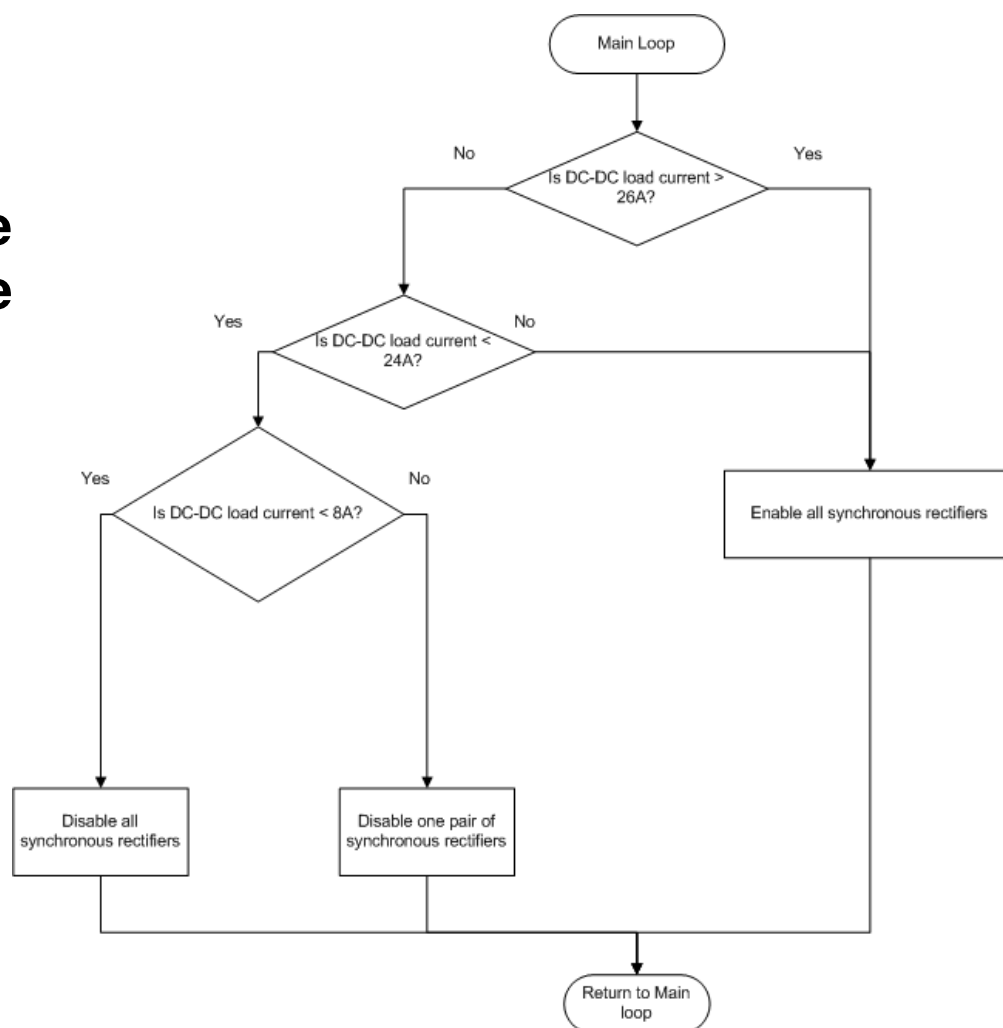




# Synchronous Rectifier Control

- The system implements two pairs of sync. rectifiers
- One or both pairs can be disabled at light loads to save switching losses and improve efficiency
  - $I_{out} > 26A$ , all ON
  - $8A < I_{out} < 24A$ , 1 pair ON
  - $I_{out} < 8A$ , both pairs OFF

PRIMARY SIDE	
SECONDARY SIDE	X

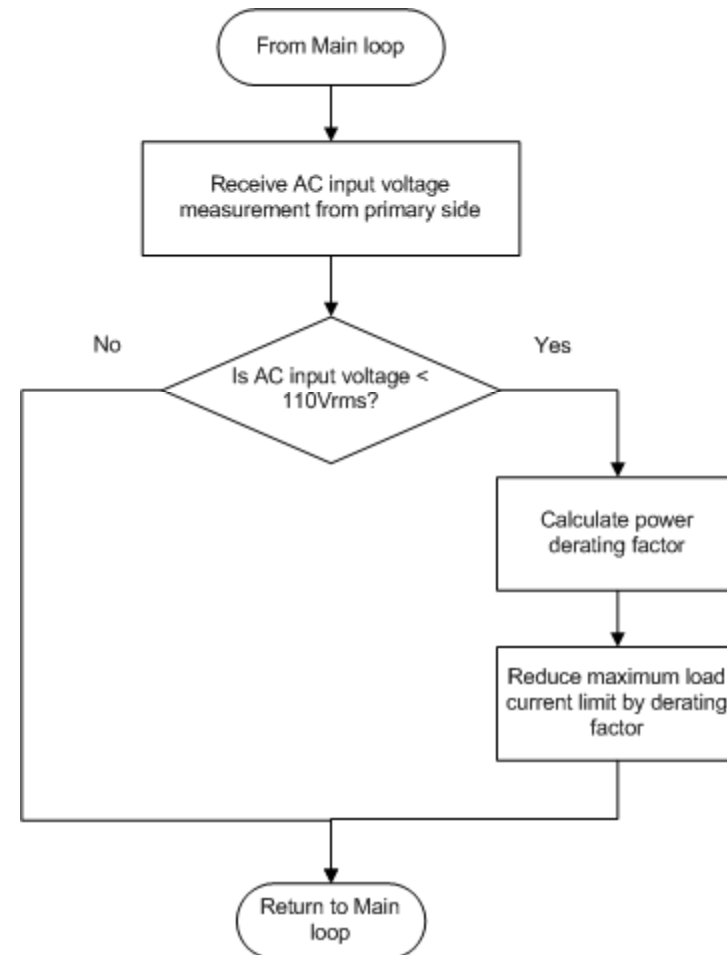




# Power De-rating

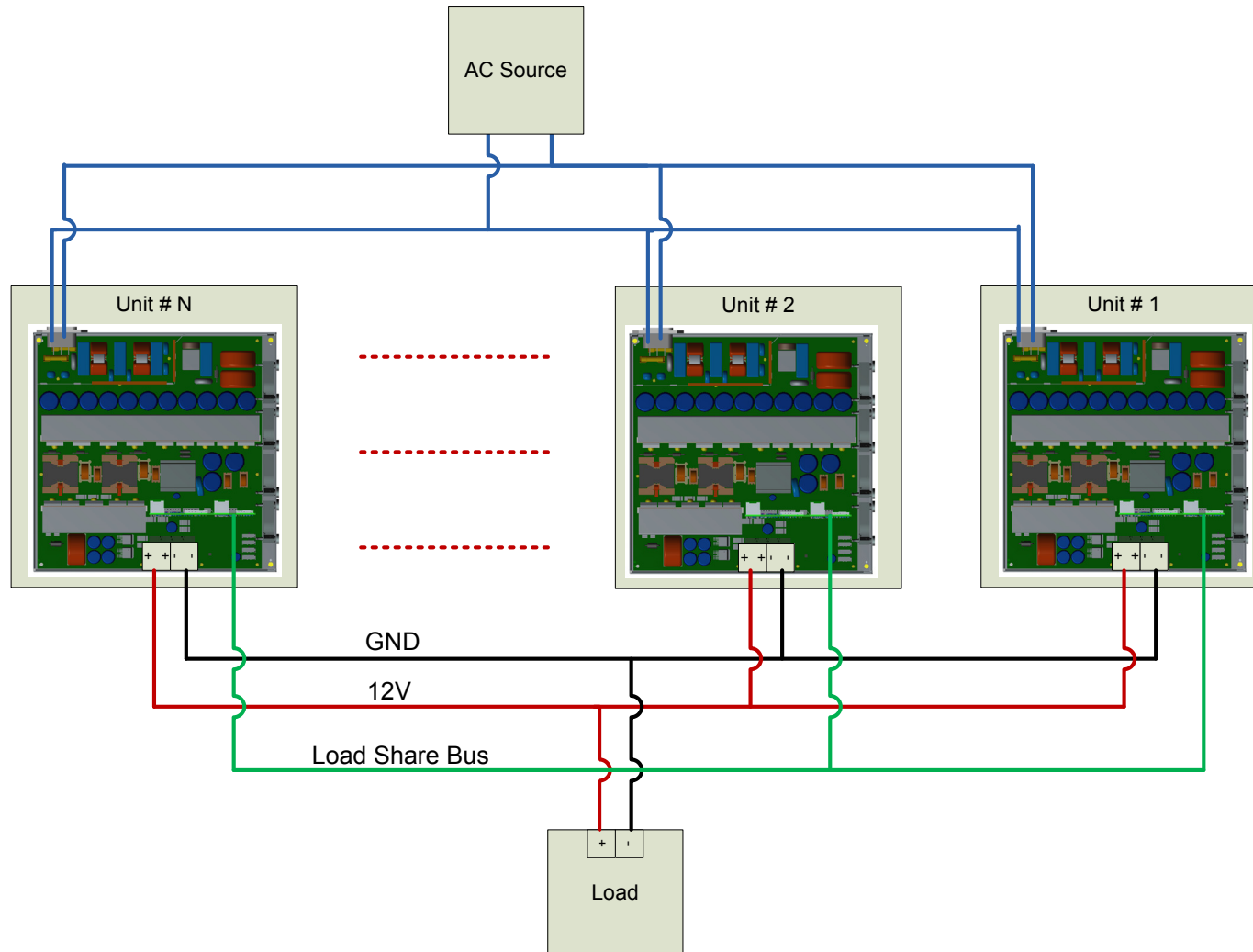
- AC Input voltage information is transmitted to secondary side
- If AC Input Voltage drops below  $110V_{rms}$ , maximum output power of the system is de-rated
- De-rating is achieved by modifying the output current limit by a de-rating factor
- De-rating factor is proportional to  $(110V_{rms} - V_{in\_rms})$

PRIMARY SIDE	
SECONDARY SIDE	X



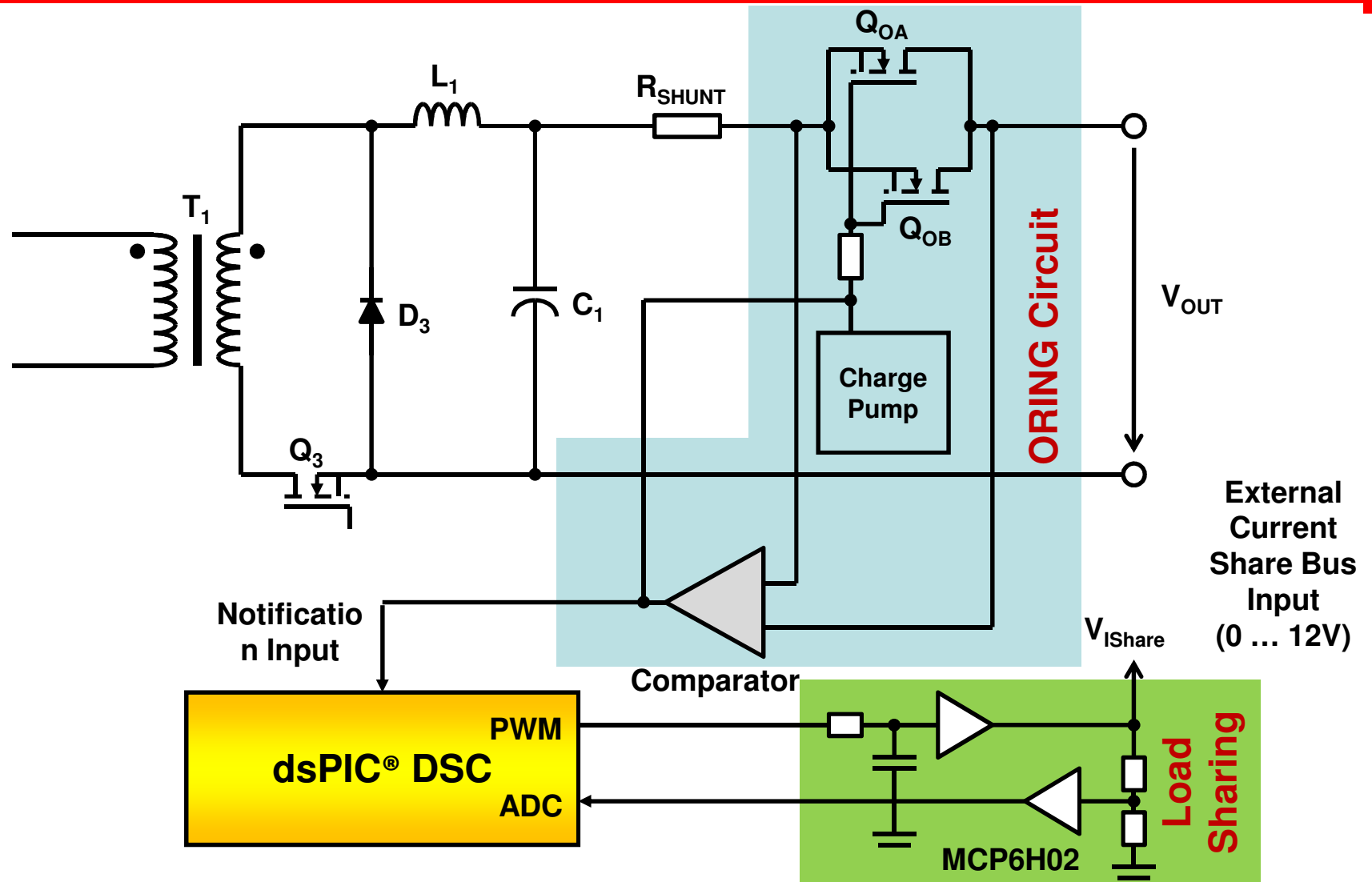


# Parallel Operation (N+1 Redundancy)





# ORing and Load Sharing

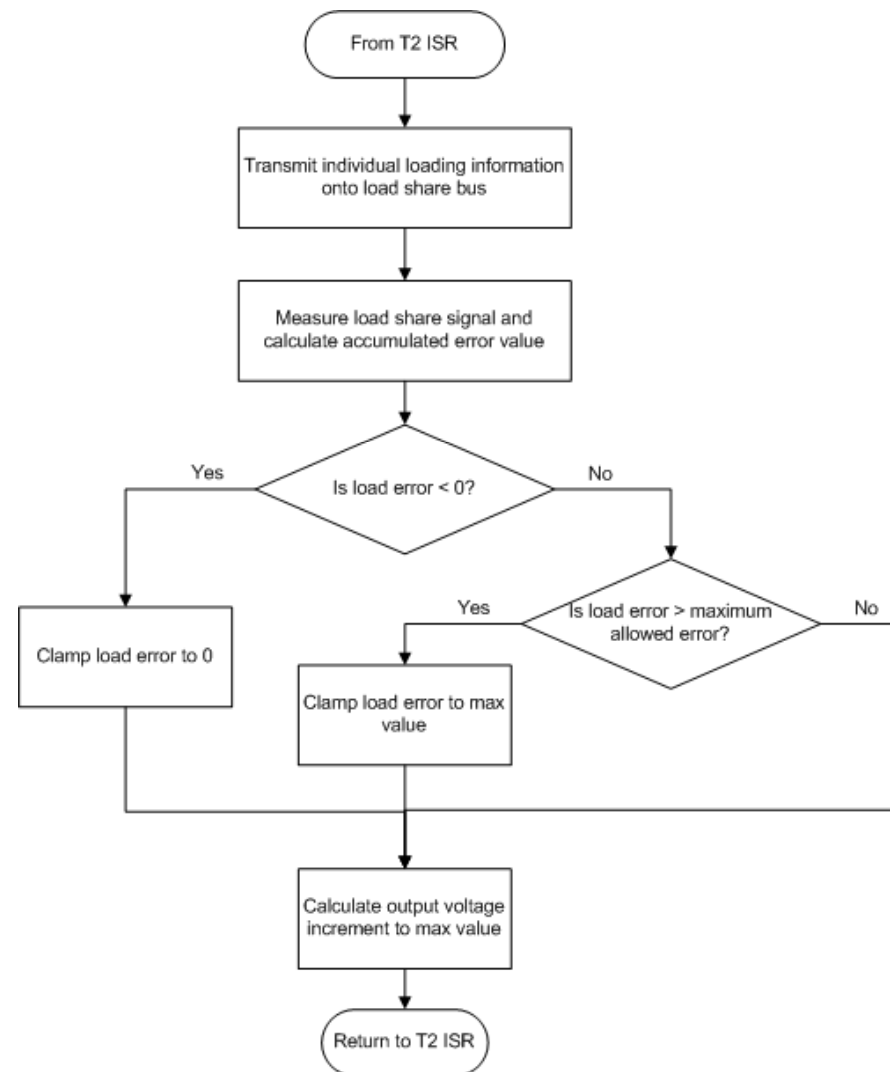




# ORing and Load Sharing

- System supports N+1 redundancy through OR-ing circuitry
- In addition to OR-ing circuit, the software implements load sharing through an analog load share bus
- Software adjusts the power level delivered by the system to balance the loading between different systems

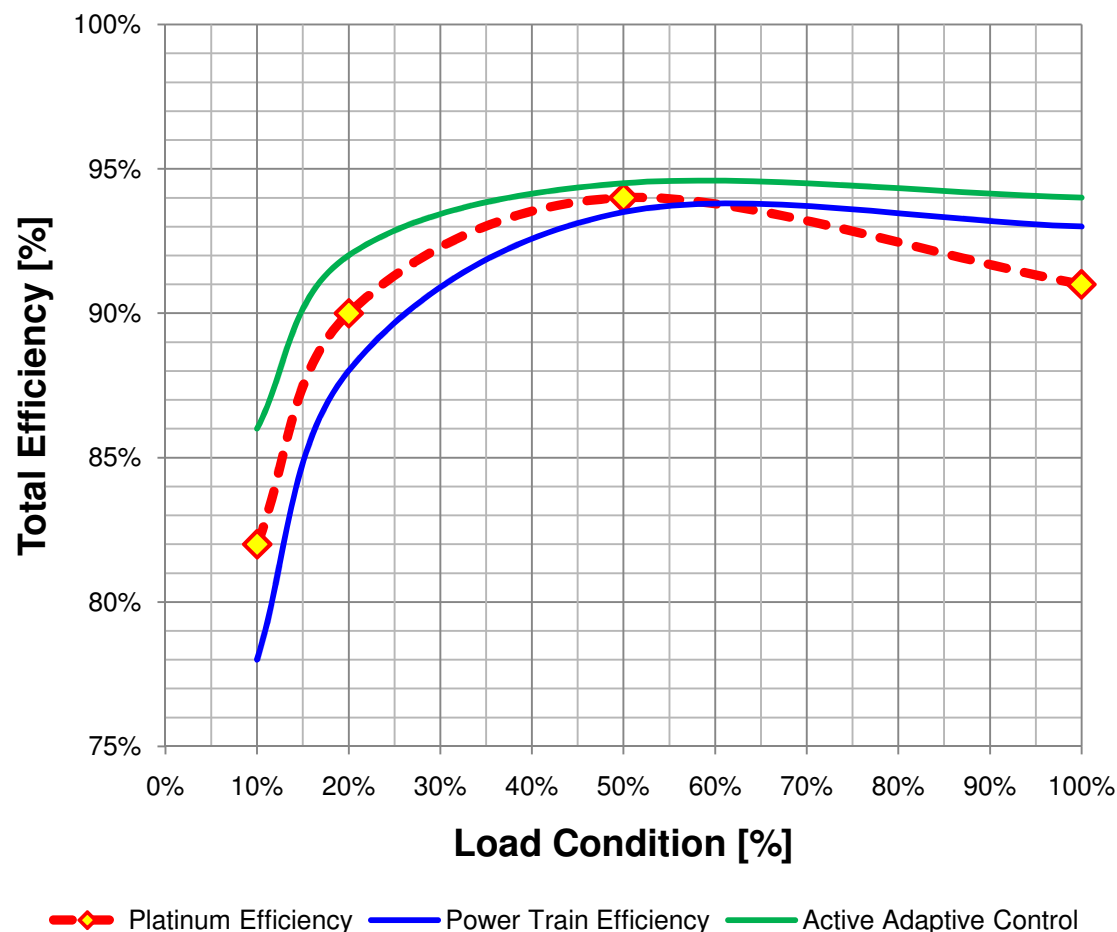
PRIMARY SIDE	
SECONDARY SIDE	X





# Efficiency Analysis

## Efficiency Level Optimization



### Test Conditions:

- 230Vac / 50Hz Input
- **Red:**  
CSCI Platinum Efficiency  
with given Reference  
Points
- **Blue:**  
Efficiency with no  
enhanced features enabled
- **Green:**  
Efficiency with enhanced  
features enabled





# Additional Resources

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- **Platinum-rated AC/DC Reference Design Application Note (DS-01421)**
- **Efficiency Measurement Guidelines document**
- **Demo Instructions Document**
- **Schematics, PCB and BOM**
- **Primary and Secondary Firmware**



**Thank You**