OA8600 (R6) Chip Specification

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Revision Log

Date	***Author***	***Version***	***Description***
01/31/20	Chin Tong	0.01	Initial Draft

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1 About This Document

1.1 Acronyms and Abbreviations

Acronyms/Abbreviations	Descriptions
AHB	AMBA Advanced High Performance Bus
AI	Audio Interface
AMBA	Advanced Microcontroller Bus Architecture
AXI	AMBA Advanced Extensible Interface
CB	Color Bar video self generation module (for testing purpose)
CPU	Central Processor Unit
CRP	Cryption module supporting AES/DES
D1	Refers to single pixel per clock cycle clock domain
D2	Refers to dual pixel per clock cycle clock domain (Horizontal grouping of 2 pixels)
D4	Refers to quad pixel per clock cycle clock domain (Horizontal grouping of 4 pixels)
DATAPATH	Refers to the video data path in the system
DCPC	Distortion Correction Perspective Correction
DDR (module)	DDR Controller
DM	Digital Mic Module
DMA (module)	DMA Controller
DVP	Digital Video Port
ECIF	Embedded Camera Interface
FB	Frame Buffer Controller
GIRSTAT	IR Statistic Module
GRFC	OVT Internal Bus
IAA	Image Arithmetic Accelerator
IDC	Image Data Convertor
IMG	(Still) Image Encoder
IOC	IO Controller Module
IRQ	Interrupt Controller
ISP	Image Signal Processor
ISP_V2	This refers to dual pixel per cycle clock domain (Vertical grouping of 2 pixels) in ISP processing and other video processing modules after ISP processing.
MBXCM	Mailbox between CPU and VPU
MD	Motion Detector
MERGER	Image Data Merger

Acronyms/Abbreviations	Descriptions
MIPICIF	MIPI Camera Interface
MIPIRX	MIPI RX Controller
MIPITX	MIPI TX Controller
MPU	Media Processor Unit
NAND	NAND Flash Controller
NPU	Neural Processing Unit
OSD	On Screen Display
PDCTRL	Power Down Controller Module
PTZ	Pan, Tilt, Zoom
RAWSCALER	Raw Scaler
Reg-Bus	OVT Internal 8-bit Register Access Bus
RGBIR	RGB IR Processor
RISC	Reduced Instruction Set Core This is used as a general term for CPU and MPU
SC	System Controller
SCRM	System Clock Reset Module
SCCBM	Serial Camera Control Bus Master
SCIF	Storage Card Interface
SCIO	Storage Card Input Output
SFB	Simple Frame Buffer Controller
SFC	Serial Flash Controller
SIF	Serial Interface
SRAM	SRAM Controller
STITCH	Stitch module
STITCH_BYP	Stitch Bypass module
STITCH_DVP	Stitch DVP module
UART	Universal Asynchronous Receiver Transmitter
USB®	Universal Serial Bus Device Controller
V2	Refers to dual pixel per clock cycle clock domain (Vertical grouping of 2 pixels), before ISP processing.
V2D2	V2 format (dual pixel per clock with vertical grouping of 2 pixels) to D2 format convertor (dual pixel per clock with horizontal grouping of 2 pixels) Related: V2D2<N> indicates the (N+1)th instance of V2D2 in the system. E.g. V2D21 indicates the 2nd instance of V2D2.
V4	Video Encoder Gen4
VFIFO	Video FIFO
VIF	Video Interfacer
YUVSCALER	YUV Scaler
AV1	AOMedia Video 11

1.2 Conventions

Type	Conventions
Register Name	The register name always have the module as the prefix. E.g. SC_GC0 register refers to a register in SC module.
Register Field representation	It is denoted as REGISTER_NAME.field_name. E.g. MD_CTRL_REG.frame_start

2 Overview & Target Application

3 Features

3.1 Embedded Micro-controllers

- Quad-Core ARM® Cortex® A32 (CPU)
  - 1GHz
  - L1 Cache: 32KB I-cache and 32KB D-cache
  - L2 Cache: 512KB
  - MMU, NEON acceleration and VFP
  - Support DVFS
- Main-BA22 (MPU)
  - 800MHz
  - 32KB I-cache and 32KB D-cache
- Always-On BA22 (AO_MCU)
  - 100MHz
  - 4KB I-cache and 4KB D-cache
- Dual boot (RTOS & Linux)
- Bootloader over-the-air upgrade CPU

3.2 Video Encoding Capability

Support triple video encoding in parallel with the following combination:

i. AV1 + HEVC + H264
ii. AV1 + dual-H264
iii. HEVC + dual H264.

The features of each video encoder are as follows:

- AV1 (Main Profile)
  - Single sensors: 8MP@30ps
  - Dual sensors: 4MP@30fps + 2MP@30fps
  - Multiple sensors: Total pixel rate not more than 2MP@90fps
  - Built-in 3D DNS
- V5 HEVC
  - Single sensor: 8MP@30ps
  - Dual sensors: 4MP@30fps + 2MP@30fps
  - Multiple sensors: Total pixel rate not more than 2MP@90fps
  - Built-in 3D DNS
- V4 H264 (BP/MP/HP)
  - Single sensors: 5MP@30fps
  - Dual steams or dual sensors: 4MP@30fps + 2MP@30fps
  - Multiple streams/sensors : Total pixel rate not more than 2MP@120fps
  - Built-in 3D DNS
  - Support both CBR/VBR bit rate control

3.3 Still Picture Encoding Capability

- Support still picture capture up to 16MP@ 30fps

3.4 Camera Interfaces

- 1 x MIPI RX (DPHY v1.2) supporting 1x4, or 2x2 lane configurations, with up to 2.5Gbps/lane.
- 1 x MIPI RX (DPHY v1.1) supporting 1x4, or 2x2 lane configurations, with up to 1.5Gbps/lane.
- Compliant to MIPI CSI v2.0

3.5 RGB-IR

- 1 x RGB-IR supporting up to dual-streams of 12MP@30fps
- 1 x RGB-IR supporting up to dual-streams of 5MP@30fps
- The two instances of RGB-IR can be used together to support up to quad-streams of 5MP@30fps
- Each RGB-IR instances supports:
  - RGB-IR 4x4 pattern, input RAW10.
  - Output Bayer (RAW10) and IR map.
  - Support binning (downsample to 1/4 original IR map) to reduce power
  - Normal Bayer after IR Removal

- BW for night vision
- Bayer for color night vision

3.6 Image Signal Processor

- Supports up to the following:
  - Total number of sensors input = 4
    - 3 external sensors
    - 1 pre-roll video input from external AO processor, or on-chip AO stage
  - Total number of streams (including HDR exposures of all sensors, and pre-roll video stream) = 10
  - Total input horizontal width (sum of horizontal width of all streams) = 18,560 pixels, equivalent to (1920 x 9) + 1280
  - Total output horizontal width for human vision (sum of horizontal width of all HDR-combined streams) = 9,344 pixels, equivalent to (2688 x 3) + 1280
  - Total output horizontal width for machine vision (sum of horizontal width of all HDR-combined streams) = 9,344 pixels, equivalent to (2688 x 3) + 1280
  - Total pixel rate = 720Mpixels/second (not including blanking)
- 16x16 zone lens shading correction and online color shading correction
- Color correction/adjustment, gamma correction and contrast adjustment
- On-the-fly RGB DPC
- Binning correction
- Video 2D/3D/3D-BiDir DNS
- Support EDR and up-to 4-exposure HDR
- Support PWL combined HDR input
- Enhanced color interpolation (RGB/RGBIR de-mosaic)

3.7 RAW Image Compression

- 3 x RAW Encoder
  - Support video compression for 720p@10fps
  - RAW domain compression, compression ratio ~x10
  - Visually loss-less compression
  - Auto/manual mode for compressed video to/from internal sram.
  - Bypass mode, store raw data to pre-roll buffer directly

3.8 RAW Image Decompression

- 1 x RAW Decoder
  - support decompression for 720p@10fps
  - HW decompress image
  - decompression can begin in MB lines

3.9 AO_Link

- 3 x AO_Link to transfer sensor image in low-power mode
- support frame by frame switch
- support 1 /2 /4 bits
- max speed up to 100MHz
- support DDR mode
- support cropping with granularity of 1 pixel.

3.10 Simple Image Signal Processor

- Simple CIP from RAW to YUV422 for Always-On sensor input
- AEC/AGC
- Video: up to 720p@10fps

3.11 HOGMD

- 1 x HOGMD Reference frame number can be 1~7.
- Support max resolution of 1280x720@30fps
- Build-in down-sample(up to x4 in both width & height) feature.

3.12 NPU

- 2048 MAC @ 600MHz
- 512KB Buffer
- Accelerate 2D-convolution and post-convolution operations such as BatchNorm, ReLu, bias-add, Sigmoid, tanh, max pool, avg pool, avg MFM and max MFM.
- Support weights decompression to allow compressed weights storage in DRAM.
- Support Depthwise 2D-convolution and fully connected layer convolution.
- Support multi-pass & sub-graph acceleration to reduce DDR bandwidth
- Support IR data format input for depth sensing CNN using structured lights
- Support EIS acceleration

3.13 Autoscaler

- Perform multiple scaling operations through link-list of commands stored in DDR
- Support yuv420/yuv422 DDR original image data format
- Support crop the original image from odd starting coordinates

3.14 IAA (Image Arithmetic Accelerator)

- Configurable as SAD accelerator for object tracking, or as warpaffine accelerator.
- For object tracking:
    - Support search object size is configurable,from 16x16 to 2048x2048 with step equal to 1

        - Support search center position is configurable
        - Support search range is configurable in both directions with step equal to 1
- For warpaffine:
    - Support warping image resolution up to 2048x2048
    - Support configuration for all the six parameters in transformation matrix
    - Support Y only or YUV422 or RGB image warping,each component will be processed individually
    - Support output statistic information for average and variance and pixel histogram for Y/Cb/Cr individually
    - Only support warping output 32x in both directions of horizontal and vertical for Y, and if YUV420,16x for Cb/Cr

3.15 Security

- Encryption and decryption (AES/DES/3DES, AES-192, AES-256)
- Support enhanced secure boot (RSA-based 2048-bit key, and/or ECC-based 256-bit key)
- Support ARM Trust-Zone
- Support privacy masking
- Support secure boot
    - Non-volatile storage of encryption key and signature
    - Secure 2 stage boot
    - Secure boot with firmware image authentication
    - Optional SHA3 hash engine
    - Deterministic pseudo-random number generator allowing seeding with user provided entropy
    - Secure JTAG allowing access only to authenticated users
    - Secure USB

3.16 DCPC and Stitching

- Dual DCPC, each with 128KB cache for Y, 64KB cache for UV
- Support bi-linear and bi-cubic for Luma interpolation
- Support enhanced (adaptive bi-cubicle) distortion and prospective correction up to:
    - Support single stream 8MP or triple stream 4MP@24fps.
- Support 8x8, 16x16 and 32x32 LUT
- Support stitching of 2xDCPC with 4096x2048 stitch output & stitch range: 128pixel (or 256pixels?)
- Support up to 4 images stitching.

3.17 Front and back scaling with PTZ

- 5 x Front scalers (RAWSCALE)
  - 1 x RAWSCALE before ISP supporting up to 3 streams with total input horizontal line-width of 8192 pixels
  - 2 x RAWSCALE before ISP supporting up to 3 streams with total input horizontal line-width of 5760 pixels
  - 1 x RAWSCALE before supporting up to 2 streams with total input horizontal line-width of 3840 pixels
  - 1 x RAWSCALE before RAW compression to DDR, supporting single stream with total input horizontal line-width of 1280pixels
  - Each RAWSCALE supports:
    - Scale video in RAW format (before ISP)
    - RAW image (from sensor & RGB-IR outputs) scales down before ISP
    - Down scale ratio of 3x, 2.5x, 2x, 1.67x, 1.5x, 1.33X. Small scale step between 1.33x and 1x is not supported.
    - Cropping to support PTZ
- 6 x Back scalers (YUVSCALER)
  - Scale video in YUV format (after ISP)
  - 3 x YUVSCALER supporting 3 x MV pipes from ISP, with horizontal resolutions up to 1920 pixels.
  - 3 x YUVSCALER supporting 3 parallel encoding paths, with horizontal resolutions up to 4096 pixels for 2 of the instances, and 4672 pixels for one of the instance.
  - Each YUVSCALER supports
    - 13-tap programmable polyphase filter for horizontal scaling
    - 5-tap programmable polyphase filter for vertical scaling
    - Support both bicubic and area mode scaling.
    - Support self-mastering
    - Support different scaling direction (up or down) for horizontal and vertical scaling
    - Scaling range is :
    - Input image size at X-Y direction needs to be modular of 4
    - Cropping to support PTZ
- 5 x Y-only SCALER
  - Each Y-only SCALER support resolutions up to 1280 pixels
- 1 x Auto scaler (AUTOSCALER)
  - Scale video in YUV format (after ISP)
  - Support linked-list jobs to allow multiple scaling jobs per SW interrupt.
  - Support self-mastering to fetch input images and upload scaled images to DDR
  - Support up to 8MP input (line-width=4096pixel).

- Support odd number scale_in/scale_out image width/height
- Down scaling range: 1/1024 to 1023/1024
- Up scaling range: 256/255 to 256/1

3.18 OSD

- A total of 4 OSD.
  - 1 x OSD after DCPC
  - 3 X OSD for each of 3 parallel encoding paths.
- Each OSD supports:
  - Pre-encoded OSD with 8 ROIs before and for video & still picture encoding Display OSD, including:
    - General OSD
      - 4 layers, each layer support only one color and one transparency
      - Maximum window size is 8192 (width) x 4096 (height)
    - RLC OSD
      - Use Run Length Coding
      - 4 layers, each layer supports 8 color and 5 transparency levels
      - Maximum window size is 4096 (Width) x 2048 (Height)
  - Two operation modes. One is with un-compressed patterns and the other one with compressed pattern after scaler. The compressed OSD will use compress pattern in DDR. During boot up, the DMA should transfer the pattern from flash to DDR.

3.19 DDR3, DDR3L, LP-DDR2, (LPDDR3)

- Support external DDR3(1.5V), DDR3L (1.35V), LPDDR3(1.2V) and LP-DDR2 (1.2V) DRAM with memory controller and DDR PHY built-in.
- 32 bit data interface with data rate up to 1866Mbps for DDR3, DDR3-L and LPDDR3
- 32 bit data interface with data rate up to 1066Mbps for LP-DDR2
- Support up to 2Gbit for DDR3(L), and up to 4Gbit for LPDDR2(3)
- Support LPDDR2 and LPDDR3 SiP
- Support Partial Array Self Refresh
- Support Write and Read Leveling

3.20 Display Output

- Support DVP 10-bit port YUV output for external VPU
- Support LCD-24bit port RGB output, with 4 x ARGB8888 alpha-blend windows, and up to 1080p@60Hz for external LCD panel
- Support MIPI TX
  - Compliant with DPHY version 1.2

- Support 4 lane output, up to 2.5Gbps per lane
- Supports both CSI (CSI version 2) and DSI (version 1.1)

3.21 Audio processing & Interfaces

- Full duplex audio Interface (up to 2 channels)
- 3 x digital MIC
- Support software based audio encoding algorithms
  - G.711, G.726, ADPCM, MP3, AAC
- Improved AEC & NR (MCU support)

3.22 Storage Device

- One SCIF host controller with built-in DLL to support up to SDR75 (single data rate 75MBps)
- One SCIO host controller support up to SDR50 (single data rate 50MBps)
- NAND flash support (8bits and 16bits) for both SLC and MLC (up to 8-bit BCH ECC capability). Support 35MBps for 8bits, 70MBps for 16bits

3.23 Peripherals

- USB 2.0 device.
- 3 x 4-wire SPI support master/slave mode operation (50MHz clock)
- 1 x serial flash master controller (SFC), at least 100MBps read rate (target up to 200MBps)
- 3 x serial interface controller (SIF) supporting master/slave mode operation (50MHz clock)
- GPIO
- 3 x PWM
- JTAG
- 3 x SCCB masters (up to 1MHz)
- 2 x Watchdog
- 5 x Timers
- 3 x UART (one 2-wire, two 4-wire)
- Crystal pad for main clock

3.24 On-Chip System Memories

- 128KB ROM
- 1.75MB SRAM

3.25 PLL

- Support input crystal as 6Mhz to 27Mhz and generated VCO up to 1.6Ghz, and post divider support

1/1.5/2/2.5/3/4/5/6/7/8/9/10

- System level PLL that provides system clock and most of the digital modules clocks, VCO output range: 1GHz~2GHz
- MIPI Tx clock that generated MIPI Tx serial clock, VCO range: 1.3GHz~2.6GHz
- USB device PLL
- DDR PHY, VCO output range: 600MHz~1.866GHz
- Analog voltage: 1.8v +/- 10%

3.26 DDR PHY

- Support external DDR3(1.5V), DDR3L (1.35V), LPDDR3(1.2V) and LP-DDR2 (1.2V) DRAM with memory controller and DDR PHY built-in.
- 32 bit data interface with data rate up to 1866Mbps for DDR3, DDR3-L and LPDDR3
- 32 bit data interface with data rate up to 1066Mbps for LP-DDR2
- Support up to 2x2Gbit for DDR3(L), and up to 8Gbit for LPDDR2(3)
- DDR PHY analog voltage range: 1.2V +/-5%, 1.35v+/-5%, 1.5v+/-5%
- Internal loop back BIST mode (both DQ and ADDR/CMD pins)
- Improve PHY scan coverage to > 90%
- Need to support power saving mode, in which DRAM and PHY only consume minimum power, and the content of DRAM should be kept.
- Support power down of PHY with DDRVDDQ still on, but DDRVDD is off. This is to support putting DRAM into self-refresh mode while AB1 is powered-down.
- Support CA training, Read-Leveling and Write-Leveling
- Include BIST for other analog circuitry if not covered by DQ and CA BIST (E.g. Training circuitry)
- Support Partial Array Self Refresh

3.27 MIPIRX PHY

- 1 x MIPI RX (DPHY v1.2) supporting 1x4, or 2x2 lane configurations, with up to 2.5Gbps/lane.
- 1 x MIPI RX (DPHY v1.1) supporting 1x4, or 2x2 lane configurations, with up to 1.5Gbps/lane.
- MIPI Rx IO voltage should be 1.8v +/- 10%

3.28 MIPITX PHY

- 2.5Gbps output speed, MIPI D-PHY
- Supports both CSI and DSI
- MIPI Tx can support 1x4, or 1x2 lanes
- Support LP write.
- MIPI TX analog voltage should be 1.8v +/- 10%

3.29 USB UTMI PHY

- UTMI compliant USB PHY support up to HS requirement (480Mbps)

3.30 Temperature Sensor

3.31 High Speed RC-OSC

- The output clock range is either 100MHz or 20MHz, software programmable.
- After power up, the oscillator will perform one time trimming to achieve the target frequency, using external 32KHz clock (always available) as reference.
- During run time, the clock speed might vary with the temperature and voltage supply. The variation should be within +/-12%.
- The digital logic will track the variation using external 32KHz clock and report the instantaneous frequency. The system will divide it by 2, as clock source of MCU and other blocks.

3.32 Low speed RC-OSC

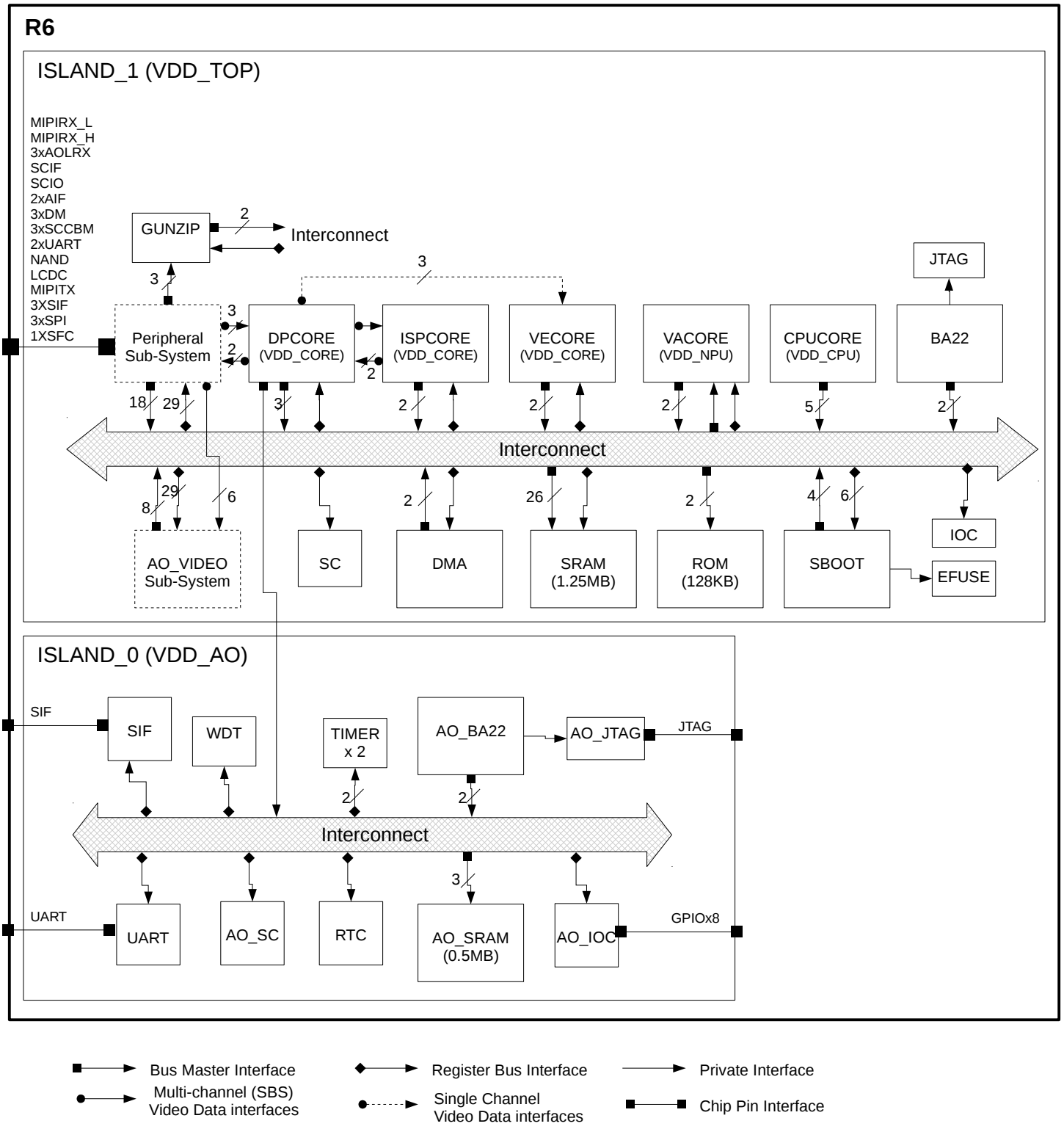
- The low speed OSC is to support external 32KHz crystal input and generate 32KHz clock to the digital logic, including RTC etc. At the same time, it should support external 32KHz clock input.

3.33 AO Link IO

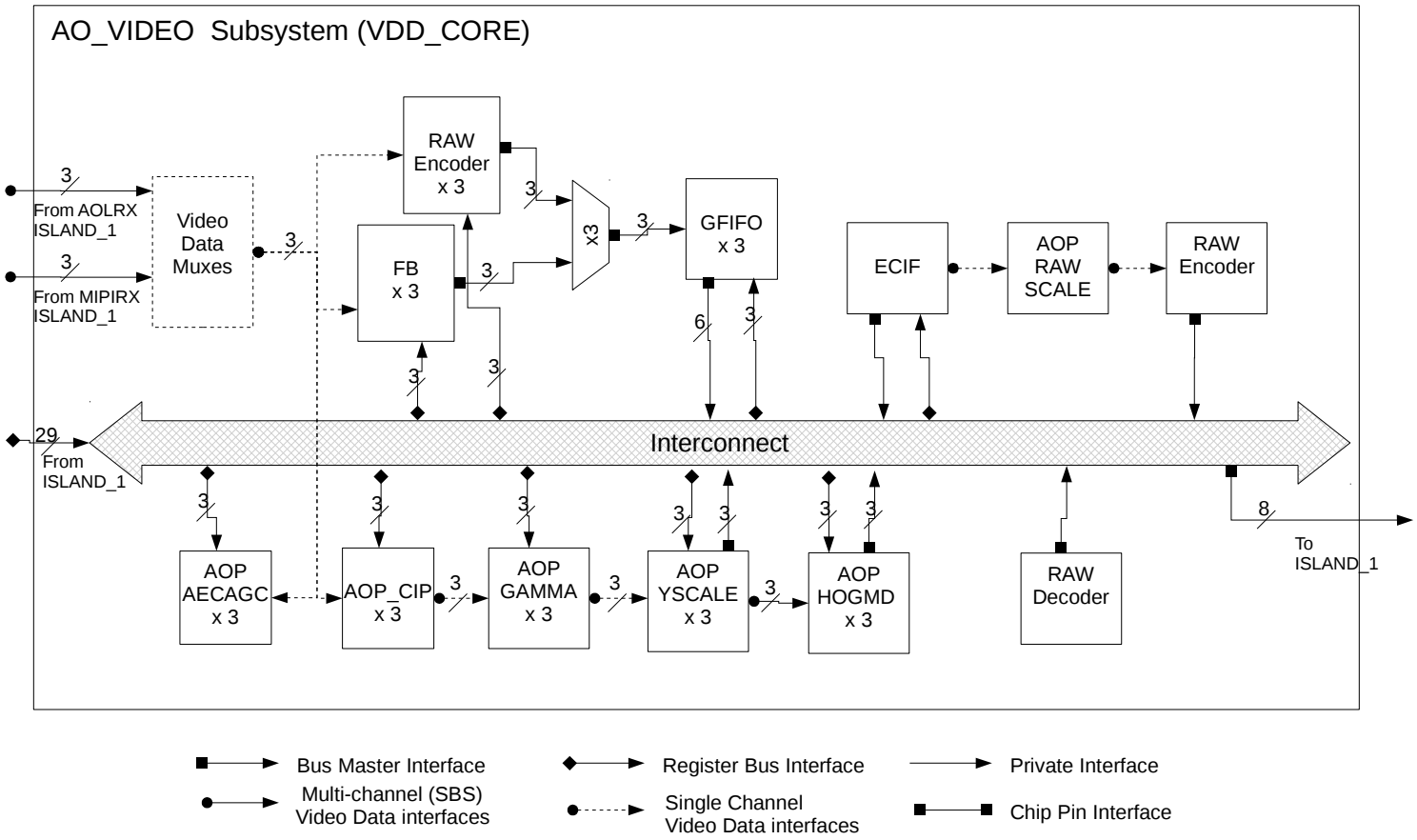
- 3 x AOL RX, support up to 100Mbps per lane input speed
- Support configuration as 1x2 and 1x4
- AO_Link I/O votlage is the same as image sensor in AO mode. The voltage range will be 0.6~1.0V.
- The speed requirement is to support below operation at 0.76V.
- Clock: 100MHz SDR mode and 50MHz DDR mode
- Data: 100Mbps which is equivalent to 50MHz DDR mode
- A special operating condition is that the CORE_VDD is supplied to the pad, but VDDIO is turned off. The design should have no leakage under this condition.

4 Block Diagram

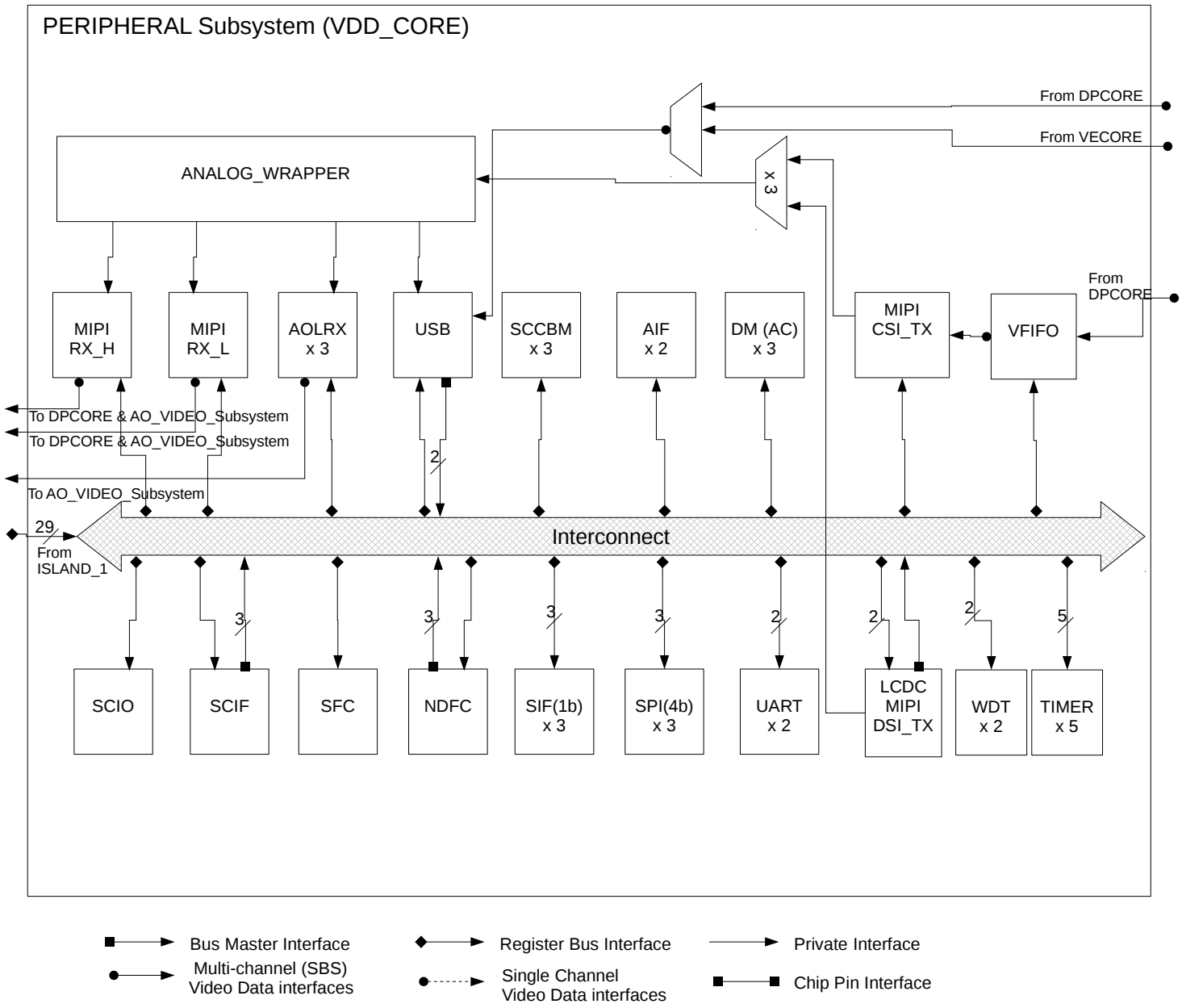
4.1 Top



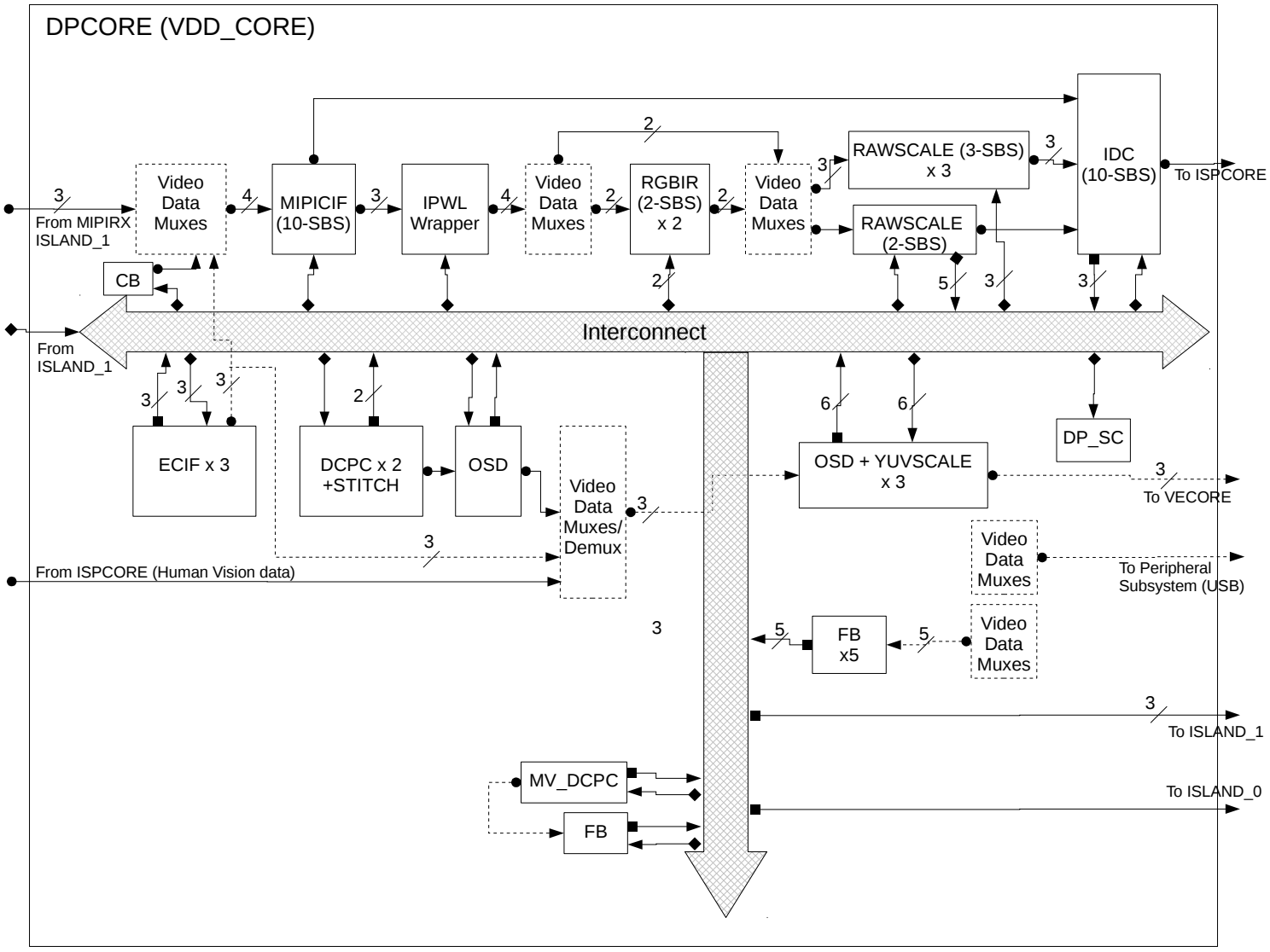
4.2 AOCORE


AO_VIDEO Subsystem (VDD_CORE)
From AOLRX ISLAND_1
From MIPIRX ISLAND_1
Video Data Muxes
RAW Encoder x 3
FB x 3
x3
GFIFO x 3
ECIF
AOP RAW SCALE
RAW Encoder
Interconnect
From ISLAND_1
AOP AECAGC x 3
AOP_CIP x 3
AOP GAMMA x 3
AOP YSCALE x 3
AOP HOGMD x 3
RAW Decoder
To ISLAND_1
Bus Master Interface
Register Bus Interface
Private Interface
Multi-channel (SBS) Video Data interfaces
Single Channel Video Data interfaces
Chip Pin Interface

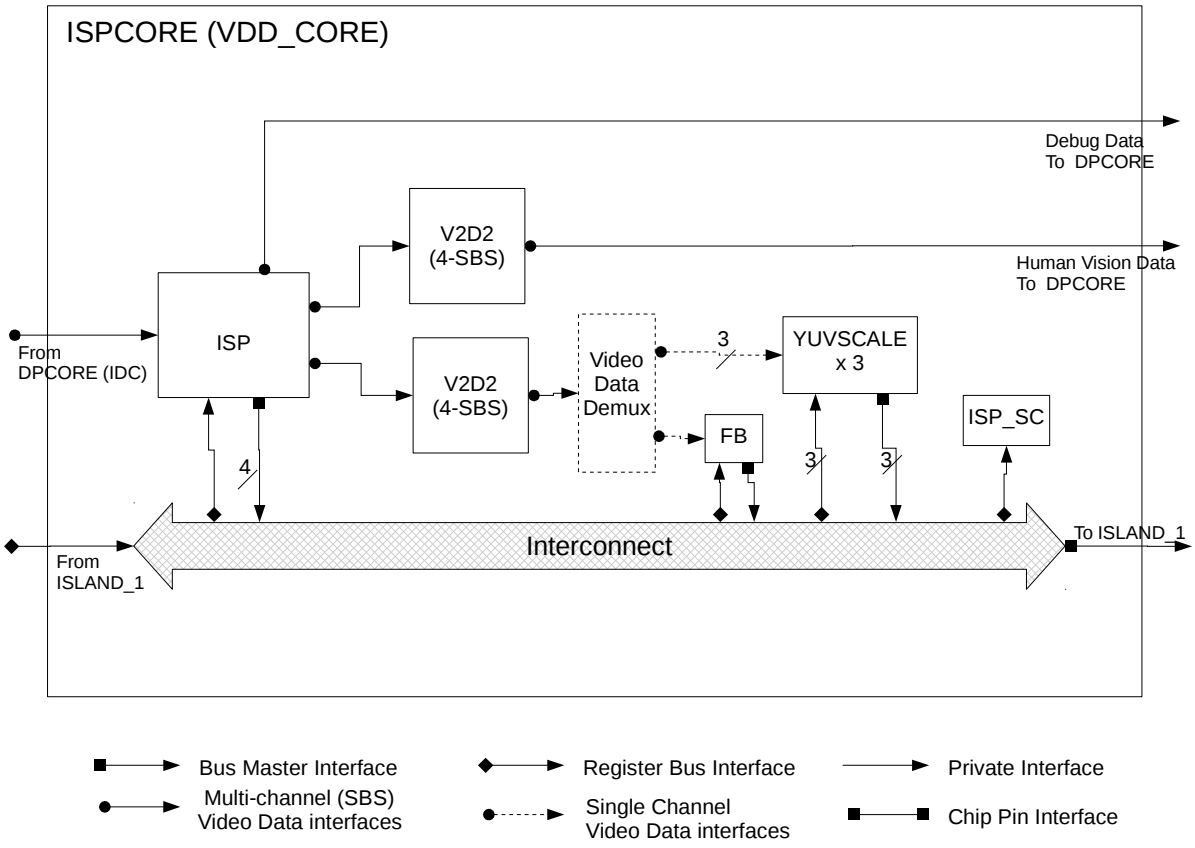
4.3 Peripheral Subsystem



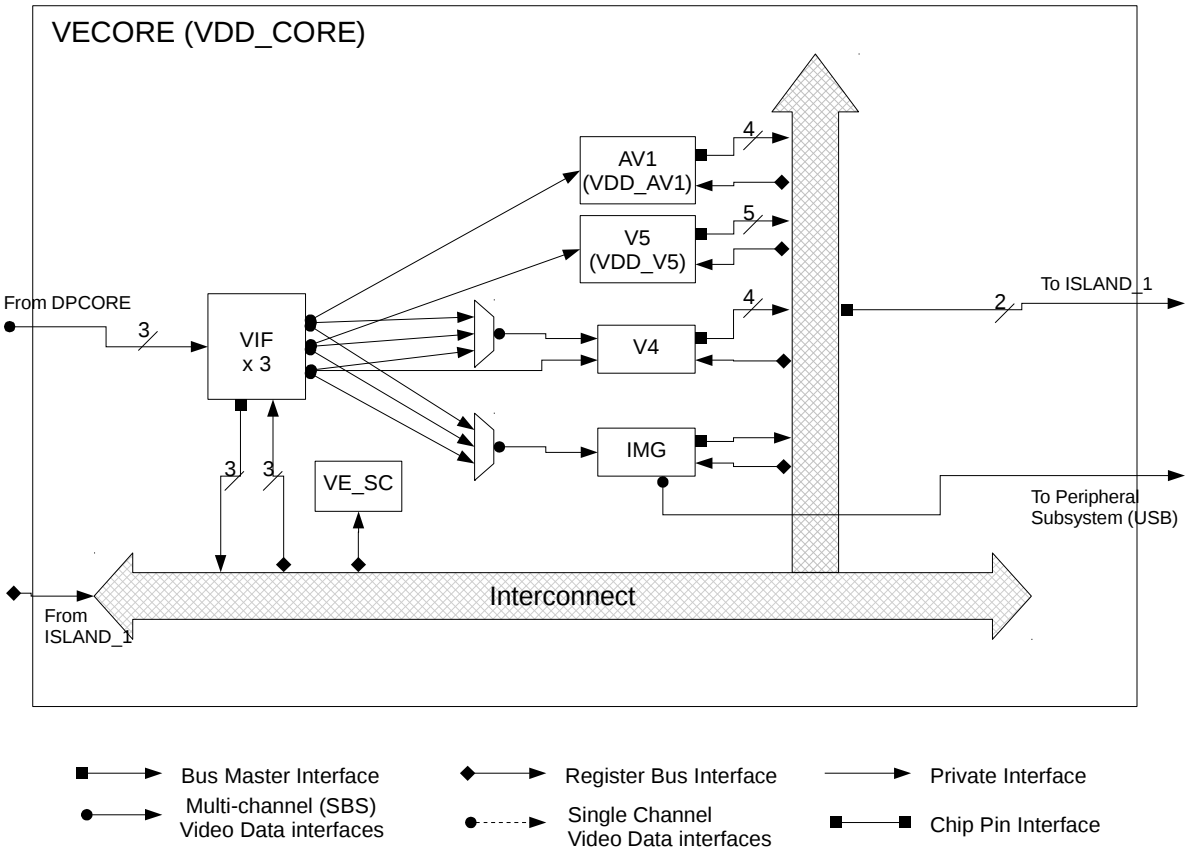
4.4 DPCORE


DPCORE (VDD_CORE)
From MIPIRX ISLAND_1
Video Data Muxes
MIPICIF (10-SBS)
IPWL Wrapper
Video Data Muxes
RGBIR (2-SBS) x 2
Video Data Muxes
RAWSCALE (3-SBS) x 3
RAWSCALE (2-SBS)
IDC (10-SBS)
To ISPCORE
CB
Interconnect
From ISLAND_1
ECIF x 3
DCPC x 2 +STITCH
OSD
Video Data Muxes/ Demux
From ISPCORE (Human Vision data)
OSD + YUVSCALE x 3
DP_SC
To VECORE
Video Data Muxes
To Peripheral Subsystem (USB)
FB x5
Video Data Muxes
To ISLAND_1
To ISLAND_0
MV_DCPC
FB
Bus Master Interface
Register Bus Interface
Private Interface
Multi-channel (SBS) Video Data interfaces
Single Channel Video Data interfaces
Chip Pin Interface

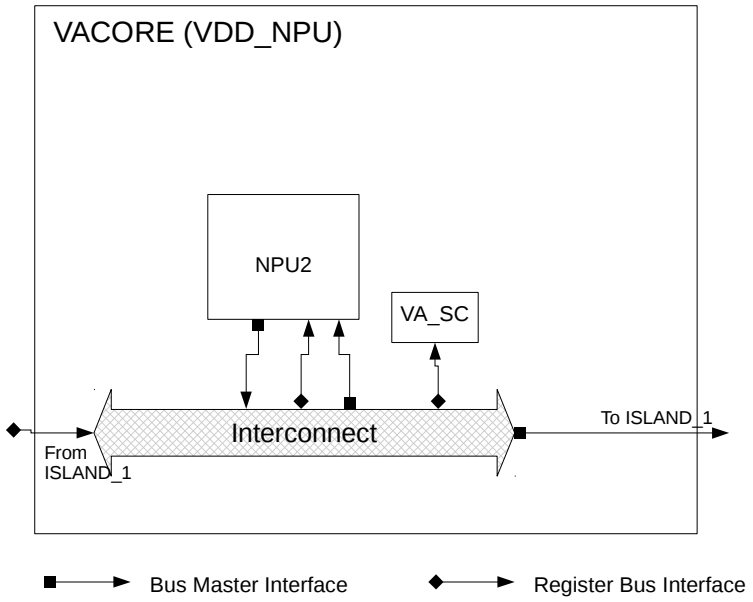
4.5 ISPCORE


ISPCORE (VDD_CORE)
Debug Data
To DPCORE
V2D2
(4-SBS)
Human Vision Data
To DPCORE
From
DPCORE (IDC)
ISP
V2D2
(4-SBS)
Video
Data
Demux
3
YUVSCALE
x 3
FB
ISP_SC
4
3
3
Interconnect
To ISLAND_1
From
ISLAND_1
Bus Master Interface
Multi-channel (SBS)
Video Data interfaces
Register Bus Interface
Single Channel
Video Data interfaces
Private Interface
Chip Pin Interface

4.6 VECORE


VECORE (VDD_CORE)
AV1
(VDD_AV1)
V5
(VDD_V5)
V4
IMG
VIF
x 3
VE_SC
From DPCORE
To ISLAND_1
To Peripheral
Subsystem (USB)
From
ISLAND_1
Interconnect
4
5
4
2
3
3
3
Bus Master Interface
Register Bus Interface
Private Interface
Multi-channel (SBS)
Video Data interfaces
Single Channel
Video Data interfaces
Chip Pin Interface

4.7 VACORE


VACORE (VDD_NPU)
NPU2
VA_SC
Interconnect
From
ISLAND_1
To ISLAND_1
Bus Master Interface
Register Bus Interface

5 Memory Map

5.1 System

Start Address	End Address	Size	Description
0x00000000	0x001FFFFF	-	Reserved
0x00200000	0xBFFFFFFF	3070 MB	MEM
0xC0000000	0xC00FFFFF	1 MB	CORE_PERIPHERAL
0xC0100000	0xE00FFFFF	512 MB	DP_CORE_PERIPHERAL
0xC0200000	0xC02047FF	18 KB	VA_CORE_PERIPHERAL
0xC0204800	0xC02FFFFF	-	Reserved
0xC0300000	0xC0310FFF	68 KB	VE_CORE_PERIPHERAL
0xC0311000	0xC03FFFFF	-	Reserved
0xC0400000	0xC0414FFF	84 KB	AO_CORE_PERIPHERAL
0xC0415000	0xC05FFFFF	-	Reserved
0xC0600000	0xE007FFFF	518656 KB	ISP_CORE_PERIPHERAL
0xE0080000	4294967295	-	Reserved

5.2 Memories

Start Address	End Address	Size	Description
0x00200000	0x003FFFFF	-	Reserved
0x00400000	0x0041FFFF	128 KB	BOOT ROM
0x00420000	0x005FFFFF	-	Reserved
0x00600000	0x0067FFFF	512 KB	AO_SRAM
0x00680000	0x007FFFFF	-	Reserved
0x00800000	0x0087FFFF	512 KB	NPU INTERNAL SRAM
0x00880000	0x0FFFFFFF	-	Reserved
0x10000000	0x101FFFFF	2 MB	SRAM
0x10200000	0x1FFFFFFF	-	Reserved
0x20000000	0x3FFFFFFF	512 MB	DDR DRAM
0x40000000	0x4FFFFFFF	-	Reserved
0x50000000	0x501FFFFF	2 MB	Alias to SRAM (only when Bootsel=0)
0x50200000	0x8FFFFFFF	-	Reserved
0x90000000	0x901FFFFF	2 MB	Alias to SRAM
0x90200000	0x9FFFFFFF	-	Reserved
0xA0000000	0xBFFFFFFF	512 MB	Alias to DDR DRAM

5.3 ISLAND_0 (AOCORE)

Start Address	End Address	Size	Description
0xC0400000	0xC0400FFF	4 KB	AO_SC_CTRL: Always On domain SC and PWR contrl
0xC0401000	0xC0401FFF	4 KB	AO_SCRM: Always on Clock and reset controller
0xC0402000	0xC0402FFF	4 KB	AO_IOC: Always On IO controller
0xC0403000	0xC0403FFF	4 KB	AO_SRAM_REG: Sram controller reg
0xC0404000	0xC0404FFF	4 KB	AO_SIF3: Serial Interface 3
0xC0405000	0xC0405FFF	4 KB	AO_BA22_IRQC: AO Ba22 irq controller
0xC0406000	0xC04063FF	1 KB	MBXAB_A: Mailbox between AO_BA and BA22 (AO_BA)
0xC0406400	0xC0406FFF	-	Reserved
0xC0407000	0xC04073FF	1 KB	MBXAB_B: Mailbox between AO_BA and BA22 (BA22)
0xC0407400	0xC0407FFF	-	Reserved
0xC0408000	0xC04083FF	1 KB	MBXAC_A: Mailbox between AO_BA and CPU (AO_BA)
0xC0408400	0xC0408FFF	-	Reserved
0xC0409000	0xC04093FF	1 KB	MBXAC_C: Mailbox between AO_BA and CPU (CPU)
0xC0409400	0xC040FFFF	-	Reserved
0xC0410000	0xC0410FFF	4 KB	RTC: Real Time Clock
0xC0411000	0xC0411FFF	4 KB	WDT_AO_BA: Watchdog Timer 2 (AO_BA22)
0xC0412000	0xC0412FFF	4 KB	TIMER5: Timer 5
0xC0413000	0xC0413FFF	4 KB	TIMER6: Timer 6
0xC0414000	0xC0414FFF	4 KB	UART1: Universal Asynchronous Receiver Transmitter 1

5.4 ISLAND_1 (TOP)

Start Address	End Address	Size	Description
0xC0000000	0xC0000FFF	4 KB	SCRM: System Clock Reset Module
0xC0001000	0xC0001FFF	4 KB	SC: System Controller
0xC0002000	0xC0002FFF	4 KB	IOC: IO Controller
0xC0003000	0xC0003FFF	4 KB	SRAM_REG: SRAM_REG (sramctrl_pd)
0xC0004000	0xC0004FFF	4 KB	DDR_REG: DDR_REG
0xC0005000	0xC0005FFF	4 KB	DDR_MERGE0: DDR merge control
0xC0006000	0xC0006FFF	4 KB	SRAM_MERGE: SRAM merge control
0xC0007000	0xC00073FF	1 KB	MBXCB_C: Mailbox between CPU and BA22 (CPU)
0xC0007400	0xC0007FFF	-	Reserved
0xC0008000	0xC00083FF	1 KB	MBXCB_B: Mailbox between CPU and BA22 (BA22)
0xC0008400	0xC0008FFF	-	Reserved
0xC0009000	0xC0009FFF	4 KB	IRQC_BA22: Interrupt Controller for BA22
0xC000A000	0xC000AFFF	4 KB	CRYPTION: Cryption
0xC000B000	0xC000BFFF	4 KB	SIGN: signature verify

Start Address	End Address	Size	Description
0xC000C000	0xC000CFFF	4 KB	OTP: otp_control
0xC000D000	0xC000DFFF	4 KB	SBOOT: sboot
0xC000E000	0xC000EFFF	4 KB	SJTAG: sjtag
0xC000F000	0xC000FFFF	4 KB	SHA: sha engine
0xC0010000	0xC0010FFF	4 KB	SFC: Serial Flash Controller
0xC0011000	0xC0011FFF	4 KB	SIF0: Serial Interface 0
0xC0012000	0xC0012FFF	4 KB	SIF1: Serial Interface 1
0xC0013000	0xC0013FFF	4 KB	SIF2: Serial Interface 2
0xC0014000	0xC0014FFF	4 KB	SPI1: SPI 1
0xC0015000	0xC0015FFF	4 KB	SPI2: SPI 2
0xC0016000	0xC0016FFF	4 KB	SPI3: SPI 3
0xC0017000	0xC0017FFF	4 KB	SPI4: SPI 4
0xC0018000	0xC0018FFF	4 KB	NAND: NAND Flash Controller
0xC0019000	0xC00193FF	1 KB	SCIF: Storage Card Interface
0xC0019400	0xC0019FFF	-	Reserved
0xC001A000	0xC001A3FF	1 KB	SCIO: Storage Card Interface Input output
0xC001A400	0xC001AFFF	-	Reserved
0xC001B000	0xC001BFFF	4 KB	GUNZIP_REG: GUNZIP register control
0xC001C000	0xC001CFFF	4 KB	DMA: DMA
0xC001D000	0xC001DFFF	4 KB	DDR_MERGE1: DDR merge control
0xC001E000	0xC001FFFF	-	Reserved
0xC0020000	0xC00203FF	1 KB	AIF0: Audio Interface 0
0xC0020400	0xC0020FFF	-	Reserved
0xC0021000	0xC00213FF	1 KB	AIF1: Audio Interface 1
0xC0021400	0xC0021FFF	-	Reserved
0xC0022000	0xC00223FF	1 KB	DM0: Digital Mic 0
0xC0022400	0xC0022FFF	-	Reserved
0xC0023000	0xC00233FF	1 KB	DM1: Digital Mic 1
0xC0023400	0xC0023FFF	-	Reserved
0xC0024000	0xC00243FF	1 KB	DM2: Digital Mic 2
0xC0024400	0xC0024FFF	-	Reserved
0xC0025000	0xC00253FF	1 KB	DM3: Digital Mic 3
0xC0025400	0xC0025FFF	-	Reserved
0xC0026000	0xC0026FFF	4 KB	MIPITX: MIPI CSI/DSI TX controller
0xC0027000	0xC0027FFF	4 KB	LCDC: LCD controller
0xC0028000	0xC0028FFF	4 KB	SCCBM0: Serial Camera Control Bus Master 0
0xC0029000	0xC0029FFF	4 KB	SCCBM1: Serial Camera Control Bus Master 1
0xC002A000	0xC002AFFF	4 KB	SCCBM2: Serial Camera Control Bus Master 2
0xC002B000	0xC002BFFF	4 KB	SCCBM3: Not used
0xC002C000	0xC002C3FF	1 KB	AO_HOGMD_0: Hogmd Always on 0
0xC002C400	0xC002CFFF	-	Reserved
0xC002D000	0xC002D3FF	1 KB	AO_HOGMD_1: Hogmd Always on 1
0xC002D400	0xC002DFFF	-	Reserved
0xC002E000	0xC002E3FF	1 KB	AO_HOGMD_2: Hogmd Always on 2
0xC002E400	0xC002EFFF	-	Reserved

Start Address	End Address	Size	Description
0xC002F000	0xC002F3FF	1 KB	AO_HOGMD_3: Not used
0xC002F400	0xC002FFFF	-	Reserved
0xC0030000	0xC0030FFF	4 KB	AO_ECIF0: AO Ecif
0xC0031000	0xC0031FFF	4 KB	AO_SFB0: AO Simple Frame Buffer Controller 0
0xC0032000	0xC0032FFF	4 KB	AO_SFB1: AO Simple Frame Buffer Controller 1
0xC0033000	0xC0033FFF	4 KB	AO_SFB2: AO Simple Frame Buffer Controller 2
0xC0034000	0xC0034FFF	4 KB	AO_SFB3: Not used
0xC0035000	0xC0035FFF	4 KB	AO_RAWSCL: AO D4 Rawscaler
0xC0036000	0xC003FFFF	-	Reserved
0xC0040000	0xC0040FFF	4 KB	UART0: Universal Asynchronous Receiver Transmitter 0
0xC0041000	0xC0041FFF	4 KB	UART2: Universal Asynchronous Receiver Transmitter 2
0xC0042000	0xC0042FFF	4 KB	PWM: PWM
0xC0043000	0xC0043FFF	4 KB	WDT_BA22: Watchdog Timer 0 (BA22)
0xC0044000	0xC0044FFF	4 KB	WDT_SYS: Watchdog Timer 1 (SYS)
0xC0045000	0xC0045FFF	4 KB	TIMER0: General Timer 0
0xC0046000	0xC0046FFF	4 KB	TIMER1: General Timer 1
0xC0047000	0xC0047FFF	4 KB	TIMER2: General Timer 2
0xC0048000	0xC0048FFF	4 KB	TIMER3: General Timer 3
0xC0049000	0xC0049FFF	4 KB	TIMER4: General Timer 4
0xC004A000	0xC004AFFF	4 KB	AO_RAW_ENC0: Raw encoder 0
0xC004B000	0xC004BFFF	4 KB	AO_RAW_ENC1: Raw encoder 1
0xC004C000	0xC004CFFF	4 KB	AO_RAW_ENC2: Raw encoder 2
0xC004D000	0xC004DFFF	4 KB	AO_RAW_ENC3: Not used
0xC004E000	0xC004EFFF	4 KB	AO_RAW_ENC4: Raw encoder 4
0xC004F000	0xC004FFFF	4 KB	AO_RAW_DEC: Raw Decoder
0xC0050000	0xC0050FFF	4 KB	MIPIRX_H: MIPI CSI RX Controller 2.5Gbps
0xC0051000	0xC0051FFF	4 KB	MIPIRX_L: MIPI CSI RX Controller 1.5Gbps
0xC0052000	0xC0052FFF	4 KB	VFIFO: Video FIFO
0xC0053000	0xC0053FFF	4 KB	DVP: Digital Video Port
0xC0054000	0xC0054FFF	4 KB	AOL_RX0: AOLink sensor interface 0
0xC0055000	0xC0055FFF	4 KB	AOL_RX1: AOLink sensor interface 1
0xC0056000	0xC0056FFF	4 KB	AOL_RX2: AOLink sensor interface 2
0xC0057000	0xC0057FFF	4 KB	AOL_RX3: Not used
0xC0058000	0xC0058FFF	4 KB	AO_YSCALER0: Y Scaler 0 (Y Dn scaler)
0xC0059000	0xC0059FFF	4 KB	AO_YSCALER1: Y Scaler 1 (Y Dn scaler)
0xC005A000	0xC005AFFF	4 KB	AO_YSCALER2: Y Scaler 2 (Y Dn scaler)
0xC005B000	0xC005BFFF	4 KB	AO_YSCALER3: Not used
0xC005C000	0xC005CFFF	4 KB	PDMA: PDMA for FPGA
0xC005D000	0xC005FFFF	-	Reserved
0xC0060000	0xC0060FFF	4 KB	AO_AECAGC0: simple isp0 aec/agc
0xC0061000	0xC0061FFF	4 KB	AO_AECAGC1: simple isp1 aec/agc
0xC0062000	0xC0062FFF	4 KB	AO_AECAGC2: simple isp2 aec/agc
0xC0063000	0xC0063FFF	4 KB	AO_AECAGC3: Not used
0xC0064000	0xC0064FFF	4 KB	AO_CIP0: simple isp0 cip
0xC0065000	0xC0065FFF	4 KB	AO_CIP1: simple isp1 cip

Start Address	End Address	Size	Description
0xC0066000	0xC0066FFF	4 KB	AO_CIP2: simple isp2 cip
0xC0067000	0xC0067FFF	4 KB	AO_CIP3: Not used
0xC0068000	0xC0068FFF	4 KB	AO_GAMMA0: simple isp0 gamma ctrl
0xC0069000	0xC0069FFF	4 KB	AO_GAMMA1: simple isp1 gamma ctrl
0xC006A000	0xC006AFFF	4 KB	AO_GAMMA2: simple isp2 gamma ctrl
0xC006B000	0xC006BFFF	4 KB	AO_GAMMA3: Not used
0xC006C000	0xC007FFFF	-	Reserved
0xC0080000	0xC008FFFF	64 KB	USBD: Universal Serial Bus Device Controller
0xC0090000	0xC00BFFFF	-	Reserved
0xC00C0000	0xC00FFFFF	256 KB	GIC400: GIC 400

5.5 ISLAND_1 (DPCORE)

Start Address	End Address	Size	Description
0xC0100000	0xC0100FFF	4 KB	DP_CTRL: DataPAth Controller
0xC0101000	0xC0101FFF	4 KB	DP_SCRM: DataPAth Clock and Reset Controller
0xC0102000	0xC0102FFF	4 KB	DP_DDR_MERGE0: DDR merge control
0xC0103000	0xC0103FFF	4 KB	DP_DDR_MERGE1: DDR merge control
0xC0104000	0xC0104FFF	4 KB	DP_SRAM_MERGE: SRAM merge control
0xC0105000	0xC0105FFF	4 KB	DP_AO_SRAM_MERGE: AO SRAM merge control
0xC0106000	0xC0106FFF	4 KB	ECIF0: Embedded Camera Interface 0
0xC0107000	0xC0107FFF	4 KB	ECIF1: Embedded Camera Interface 1
0xC0108000	0xC0108FFF	4 KB	ECIF2: Embedded Camera Interface 2
0xC0109000	0xC0109FFF	-	Reserved
0xC010A000	0xC010AFFF	4 KB	YUVSCALER0: YUV Scaler 0 (YUV Up/Dn scaler)
0xC010B000	0xC010BFFF	4 KB	YUVSCALER1: YUV Scaler 1 (YUV Up/Dn scaler)
0xC010C000	0xC010CFFF	4 KB	YUVSCALER2: YUV Scaler 2 (YUV Up/Dn scaler)
0xC010D000	0xC010DFFF	4 KB	SFB_MV: SFB to dump output of DCPC MV
0xC010E000	0xC010EFFF	4 KB	DCPC_MV: DCPC for Machine vision
0xC010F000	0xC0110FFF	-	Reserved
0xC0111000	0xC0111FFF	4 KB	SFB0: Simple Frame Buffer Controller 0
0xC0112000	0xC0112FFF	4 KB	SFB1: Simple Frame Buffer Controller 1
0xC0113000	0xC0113FFF	4 KB	SFB2: Simple Frame Buffer Controller 2
0xC0114000	0xC0114FFF	4 KB	SFB3: Simple Frame Buffer Controller 3
0xC0115000	0xC0115FFF	4 KB	SFB4: Simple Frame Buffer Controller 4
0xC0116000	0xC0116FFF	-	Reserved
0xC0117000	0xC0117FFF	4 KB	GIRSTAT0: IR statistic
0xC0118000	0xC0118FFF	4 KB	GIRSTAT1: IR statistic
0xC0119000	0xC0119FFF	4 KB	IDC: Image Data Convertor
0xC011A000	0xC011AFFF	4 KB	DCPC: Distortion Correction Perspective Correction
0xC011B000	0xC011BFFF	4 KB	IAA: IAA
0xC011C000	0xC011CFFF	4 KB	AUTOSCL: Auto Scaler

Start Address	End Address	Size	Description
0xC011D000	0xC011DFFF	4 KB	HOGMD: Motion Detector
0xC011E000	0xC011EFFF	4 KB	MIPICIF: MIPI Camera Interface
0xC011F000	0xC011FFFF	-	Reserved
0xC0120000	0xC0127FFF	32 KB	OSD0: On Screen Display 0
0xC0128000	0xC012FFFF	-	Reserved
0xC0130000	0xC0137FFF	32 KB	OSD1: On Screen Display 1
0xC0138000	0xC013FFFF	-	Reserved
0xC0140000	0xC0147FFF	32 KB	OSD2: On Screen Display 2
0xC0148000	0xC014FFFF	-	Reserved
0xC0150000	0xC0157FFF	32 KB	OSD3: On Screen Display 3
0xC0158000	0xC017FFFF	-	Reserved
0xC0180000	0xC0180FFF	4 KB	CB: Color Bar
0xC0181000	0xC0181FFF	4 KB	YSCALER0: Y Scaler 0 (Y Dn scaler)
0xC0182000	0xE00FFFFF	-	Reserved
0xE0100000	0xE01FFFFF	1 MB	RGBIR_RAWSCALE: RGBIR & RAWSCALER registers and internal Memory
0xE0200000	0xE00FFFFF	-	Reserved

5.6 ISLAND_1 (ISPCORE)

Start Address	End Address	Size	Description
0xC0600000	0xC0600FFF	4 KB	ISP_CTRL: ISP core control (include rawdns)
0xC0601000	0xC0601FFF	4 KB	ISP_SCRM: ISP Core Clock and reset controller
0xC0602000	0xC0602FFF	4 KB	ISP_DDR_MERGE: DDR merge control
0xC0603000	0xC0603FFF	-	Reserved
0xC0604000	0xC0604FFF	4 KB	YUVSCALER_MV0: YUV Scaler MV 0 (YUV Up/Dn scaler)
0xC0605000	0xC0605FFF	4 KB	YUVSCALER_MV1: YUV Scaler MV 1 (YUV Up/Dn scaler)
0xC0606000	0xC0606FFF	4 KB	YUVSCALER_MV2: YUV Scaler MV 2 (YUV Up/Dn scaler)
0xC0607000	0xC0607FFF	4 KB	YUVSCALER_MV3: not used
0xC0608000	0xC0608FFF	4 KB	SFB4_MV: SFB to dump output of ISP MV pipe 4
0xC0609000	0xDFFFFFFF	-	Reserved
0xE0000000	0xE00FFFFF	1 MB	ISP_REG: ISP registers & ISP internal Memory
0xE0100000	0xE007FFFF	-	Reserved

5.7 ISLAND_1 (VECORE)

Start Address	End Address	Size	Description
0xC0300000	0xC0300FFF	4 KB	VE_CTRL: VideoEncoder Controller
0xC0301000	0xC0301FFF	4 KB	VE_SCRM: VideoEncoder Clock and Reset Controller

Start Address	End Address	Size	Description
0xC0302000	0xC0302FFF	4 KB	VE_DDR_MERGE: DDR merge control
0xC0303000	0xC0303FFF	4 KB	VE_SRAM_MERGE: SRAM merge control
0xC0304000	0xC0305FFF	8 KB	V4: Video Encoder Gen4
0xC0306000	0xC0306FFF	4 KB	AV1: AV1 Video Encoder
0xC0307000	0xC0307FFF	4 KB	V5: Video Encoder Gen5
0xC0308000	0xC03083FF	1 KB	VIF0: Video Interfacer 0
0xC0308400	0xC0308FFF	-	Reserved
0xC0309000	0xC03093FF	1 KB	VIF1: Video Interfacer 1
0xC0309400	0xC0309FFF	-	Reserved
0xC030A000	0xC030A3FF	1 KB	VIF2: Video Interfacer 2
0xC030A400	0xC030FFFF	-	Reserved
0xC0310000	0xC0310FFF	4 KB	IMG: Image Encoder

5.8 ISLAND_1 (VACORE)

Start Address	End Address	Size	Description
0xC0200000	0xC0200FFF	4 KB	VA_CTRL: VideoAnalytics Controller
0xC0201000	0xC0201FFF	4 KB	VA_SCRM: VideoAnalytics Clock and Reset Controller
0xC0202000	0xC0202FFF	4 KB	VA_DDR_MERGE: DDR merge control
0xC0203000	0xC0203FFF	4 KB	VA_SRAM_MERGE: SRAM merge control
0xC0204000	0xC02043FF	1 KB	NPU: CNN Processor
0xC0204400	0xC02047FF	1 KB	NPU_SGA: CNN Processor (Sub Graph Accelerator)

6 Pin Table

6.1 Pin List

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
T8	RSTN	Reset negate	Digital	AO_VDDIO			Disabled				
D9	TEST_MODE	Test mode	Digital	AO_VDDIO			Disabled				
C16	BOOT_MODE0	Boot mode bit 0	Digital	AO_VDDIO			Disabled				
D16	BOOT_MODE1	Boot mode bit 1	Digital	AO_VDDIO			Disabled				
C15	BOOT_MODE2	Boot mode bit 2	Digital	AO_VDDIO			Disabled				
U9	GPIO0	GPIO 0	Digital	AO_VDDIO	HIGH	0	Enabled	High	Enabled	0	gpio

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
V9	GPIO1	GPIO 1	Digital	AO_VDDIO	HIGH	1	Enabled	High	Enabled	1	gpio
W9	GPIO2	GPIO 2	Digital	AO_VDDIO	HIGH	2	Enabled	High	Enabled	2	gpio
X9	GPIO3	GPIO 3	Digital	AO_VDDIO	HIGH	3	Enabled	High	Enabled	3	gpio
U10	GPIO4	GPIO 4	Digital	AO_VDDIO	HIGH	4	Enabled	High	Enabled	4	gpio
V10	GPIO5	GPIO 5	Digital	AO_VDDIO	HIGH	5	Enabled	High	Enabled	5	gpio
W10	GPIO6	GPIO 6	Digital	AO_VDDIO	HIGH	6	Enabled	High	Enabled	6	gpio
X10	GPIO7	GPIO 7	Digital	AO_VDDIO	HIGH	7	Enabled	High	Enabled	7	gpio
N10	UART1_TX	UART 1 TX data	Digital	AO_VDDIO	HIGH	8	Enabled	High	Enabled	8	gpio
N11	UART1_RX	UART 1 RX data	Digital	AO_VDDIO	HIGH	9	Enabled	High	Enabled	9	gpio
L7	CCLK	Sensor clock output	Digital	AO_VDDIO	HIGH	10	Enabled	High	Enabled	10	gpio
B15	JTAG_TCK	JTAG test clock	Digital	AO_VDDIO	HIGH	11	Enabled	High	Enabled	11	gpio
F12	JTAG_TMS	JTAG test mode select	Digital	AO_VDDIO	HIGH	12	Enabled	High	Enabled	12	gpio
A15	JTAG_TDI	JTAG serial input	Digital	AO_VDDIO	HIGH	13	Enabled	High	Enabled	13	gpio
E12	JTAG_TDO	JTAG serial output	Digital	AO_VDDIO	HIGH	14	Enabled	High	Enabled	14	gpio
U12	SIF3_MOSI	SIF 3 mosi	Digital	AO_VDDIO	HIGH	15	Enabled	High	Enabled	15	gpio
V12	SIF3_MISO	SIF 3 miso	Digital	AO_VDDIO	HIGH	16	Enabled	High	Enabled	16	gpio
W12	SIF3_CSN	SIF 3 Chip select negate	Digital	AO_VDDIO	HIGH	17	Enabled	High	Enabled	17	gpio
X12	SIF3_CLK	SIF 3 clock	Digital	AO_VDDIO	HIGH	18	Enabled	High	Enabled	18	gpio
W11	XI_32K	24MHz crystal input	Analog	AO_VDDIO							
X11	XO_32K	Crystal output	Analog	AO_VDDIO							
R6	AO_VDDIO		Power/Ground								
T6	AO_VDDIO		Power/Ground								
J9	VSS		Power/Gr								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
			ound								
M1	XI	24MHz crystal input	Analog								
N1	XO	Crystal output	Analog								
X13	LCD_CLK	LCD interface	Digital	LCD_VDDIO	HIGH	21	Enabled	High	Enabled	21	gpio
U14	LCD_VSYNC	LCD interface	Digital	LCD_VDDIO	HIGH	22	Enabled	High	Enabled	22	gpio
V14	LCD_HSYNC	LCD interface	Digital	LCD_VDDIO	HIGH	23	Enabled	High	Enabled	23	gpio
W14	LCD_DEN	LCD interface	Digital	LCD_VDDIO	HIGH	24	Enabled	High	Enabled	24	gpio
X14	LCD_DAT0	LCD interface	Digital	LCD_VDDIO	HIGH	25	Enabled	High	Enabled	25	gpio
U15	LCD_DAT1	LCD interface	Digital	LCD_VDDIO	HIGH	26	Enabled	High	Enabled	26	gpio
V15	LCD_DAT2	LCD interface	Digital	LCD_VDDIO	HIGH	27	Enabled	High	Enabled	27	gpio
W15	LCD_DAT3	LCD interface	Digital	LCD_VDDIO	HIGH	28	Enabled	High	Enabled	28	gpio
X15	LCD_DAT4	LCD interface	Digital	LCD_VDDIO	HIGH	29	Enabled	High	Enabled	29	gpio
U16	LCD_DAT5	LCD interface	Digital	LCD_VDDIO	HIGH	30	Enabled	High	Enabled	30	gpio
V16	LCD_DAT6	LCD interface	Digital	LCD_VDDIO	HIGH	31	Enabled	High	Enabled	31	gpio
W16	LCD_DAT7	LCD interface	Digital	LCD_VDDIO	HIGH	32	Enabled	High	Enabled	32	gpio
X16	LCD_DAT8	LCD interface	Digital	LCD_VDDIO	HIGH	33	Enabled	High	Enabled	33	gpio
U17	LCD_DAT9	LCD interface	Digital	LCD_VDDIO	HIGH	34	Enabled	High	Enabled	34	gpio
V17	LCD_DAT10	LCD interface	Digital	LCD_VDDIO	HIGH	35	Enabled	High	Enabled	35	gpio
W17	LCD_DAT11	LCD interface	Digital	LCD_VDDIO	HIGH	36	Enabled	High	Enabled	36	gpio
X17	LCD_DAT12	LCD interface	Digital	LCD_VDDIO	HIGH	37	Enabled	High	Enabled	37	gpio
U18	LCD_DAT13	LCD interface	Digital	LCD_VDDIO	HIGH	38	Enabled	High	Enabled	38	gpio
V18	LCD_DAT14	LCD interface	Digital	LCD_VDDIO	HIGH	39	Enabled	High	Enabled	39	gpio
W18	LCD_DAT15	LCD interface	Digital	LCD_VDDIO	HIGH	40	Enabled	High	Enabled	40	gpio

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
M7	UART0_TX	UART 0 TX data	Digital	LCD_VDDIO	HIGH	41	Enabled	High	Enabled	41	gpio
N7	UART0_RX	UART 0 RX data	Digital	LCD_VDDIO	HIGH	42	Enabled	High	Enabled	42	gpio
P7	UART0_CTS	UART 0 clear-to-send	Digital	LCD_VDDIO	HIGH	43	Enabled	High	Enabled	43	gpio
R7	UART0_RTS	UART 0 request-to-send	Digital	LCD_VDDIO	HIGH	44	Enabled	High	Enabled	44	gpio
U8	DM0_CLK	Digital mic 0 clk	Digital	LCD_VDDIO	HIGH	45	Enabled	High	Enabled	45	gpio
V8	DM0_DAT	Digital mic 0 data	Digital	LCD_VDDIO	HIGH	46	Enabled	High	Enabled	46	gpio
W8	DM1_CLK	Digital mic 1 clk	Digital	LCD_VDDIO	HIGH	47	Enabled	High	Enabled	47	gpio
X8	DM1_DAT	Digital mic 1 data	Digital	LCD_VDDIO	HIGH	48	Enabled	High	Enabled	48	gpio
H16	NAND_D0	NAND Data 0	Digital	NAND_VDDIO	HIGH	49	Enabled	High	Enabled	49	gpio
H15	NAND_D1	NAND Data 1	Digital	NAND_VDDIO	HIGH	50	Enabled	High	Enabled	50	gpio
J15	NAND_D2	NAND Data 2	Digital	NAND_VDDIO	HIGH	51	Enabled	High	Enabled	51	gpio
J16	NAND_D3	NAND Data 3	Digital	NAND_VDDIO	HIGH	52	Enabled	High	Enabled	52	gpio
L15	NAND_D4	NAND Data 4	Digital	NAND_VDDIO	HIGH	53	Enabled	High	Enabled	53	gpio
L16	NAND_D5	NAND Data 5	Digital	NAND_VDDIO	HIGH	54	Enabled	High	Enabled	54	gpio
M14	NAND_D6	NAND Data 6	Digital	NAND_VDDIO	HIGH	55	Enabled	High	Enabled	55	gpio
M13	NAND_D7	NAND Data 7	Digital	NAND_VDDIO	HIGH	56	Enabled	High	Enabled	56	gpio
H14	NAND_CS	NAND Chip select negate	Digital	NAND_VDDIO	HIGH	57	Enabled	High	Enabled	57	gpio
K15	NAND_ALE	NAND ALE	Digital	NAND_VDDIO	HIGH	58	Enabled	High	Enabled	58	gpio
M15	NAND_CLE	NAND CLE	Digital	NAND_VDDIO	HIGH	59	Enabled	High	Enabled	59	gpio
K16	NAND_WE	NAND Write Enable negate	Digital	NAND_VDDIO	HIGH	60	Enabled	High	Enabled	60	gpio
N14	NAND_RE	NAND Read Enable negate	Digital	NAND_VDDIO	HIGH	61	Enabled	High	Enabled	61	gpio
M16	NAND_RB	NAND Ready/Busy negate	Digital	NAND_VD	HIGH	62	Enabled	High	Enable	62	gpio

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
				DIO					d		
E11	SIF2_MOSI	SIF 2 mosi	Digital	NAND_VDDIO	HIGH	63	Enabled	High	Enabled	63	gpio
D11	SIF2_MISO	SIF 2 miso	Digital	NAND_VDDIO	HIGH	64	Enabled	High	Enabled	64	gpio
D10	SIF2_CSN	SIF 2 Chip select negate	Digital	NAND_VDDIO	HIGH	65	Enabled	High	Enabled	65	gpio
C11	SIF2_CLK	SIF 2 clock	Digital	NAND_VDDIO	HIGH	66	Enabled	High	Enabled	66	gpio
B13	SFC0_CSN	SFC chip select negate	Digital	PER_VDDIO	HIGH	67	Enabled	High	Enabled	67	gpio
B12	SFC0_CLK	SFC clock	Digital	PER_VDDIO	HIGH	68	Enabled	High	Enabled	68	gpio
A12	SFC0_DQ0	SFC master out/slave in 0	Digital	PER_VDDIO	HIGH	69	Enabled	High	Enabled	69	gpio
A13	SFC0_DQ1	SFC master out/slave in 1	Digital	PER_VDDIO	HIGH	70	Enabled	High	Enabled	70	gpio
C12	SFC0_DQ2	SFC master out/slave in 2	Digital	PER_VDDIO	HIGH	71	Enabled	High	Enabled	71	gpio
D12	SFC0_DQ3	SFC master out/slave in 3	Digital	PER_VDDIO	HIGH	72	Enabled	High	Enabled	72	gpio
G12	SFC0_DQ4	SFC master out/slave in 4	Digital	PER_VDDIO	HIGH	73	Enabled	High	Enabled	73	gpio
H12	SFC0_DQ5	SFC master out/slave in 5	Digital	PER_VDDIO	HIGH	74	Enabled	High	Enabled	74	gpio
J12	SFC0_DQ6	SFC master out/slave in 6	Digital	PER_VDDIO	HIGH	75	Enabled	High	Enabled	75	gpio
K12	SFC0_DQ7	SFC master out/slave in 7	Digital	PER_VDDIO	HIGH	76	Enabled	High	Enabled	76	gpio
F16	SCIO_DAT0	SCIO data 0	Digital	PER_VDDIO	HIGH	77	Enabled	High	Enabled	77	gpio
E16	SCIO_DAT1	SCIO data 1	Digital	PER_VDDIO	HIGH	78	Enabled	High	Enabled	78	gpio
F14	SCIO_DAT2	SCIO data 2	Digital	PER_VDDIO	HIGH	79	Enabled	High	Enabled	79	gpio
F15	SCIO_DAT3	SCIO data 3	Digital	PER_VDDIO	HIGH	80	Enabled	High	Enabled	80	gpio
E15	SCIO_CMD	SCIO command	Digital	PER_VDDIO	HIGH	81	Enabled	High	Enabled	81	gpio
F13	SCIO_CLK	SCIO clock	Digital	PER_VDDIO	HIGH	82	Enabled	High	Enabled	82	gpio
M10	SIF0_MOSI	SIF 0 mosi	Digital	PER_VDDIO	HIGH	83	Enabled	High	Enabled	83	gpio

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
M11	SIF0_MISO	SIF 0 miso	Digital	PER_VDDIO	HIGH	84	Enabled	High	Enabled	84	gpio
N9	SIF0_CSN	SIF 0 Chip select negate	Digital	PER_VDDIO	HIGH	85	Enabled	High	Enabled	85	gpio
L10	SIF0_CLK	SIF 0 clock	Digital	PER_VDDIO	HIGH	86	Enabled	High	Enabled	86	gpio
E13	AI_MCLK	I2S master clock for external audio codec	Digital	PER_VDDIO	HIGH	87	Enabled	High	Enabled	87	gpio
A14	AI_DI	I2S data input	Digital	PER_VDDIO	HIGH	88	Enabled	High	Enabled	88	gpio
B14	AI_DO	I2S data output	Digital	PER_VDDIO	HIGH	89	Enabled	High	Enabled	89	gpio
D13	AI_LR	I2S left/right channel select	Digital	PER_VDDIO	HIGH	90	Enabled	High	Enabled	90	gpio
E14	AI_CLK	I2S bit clock	Digital	PER_VDDIO	HIGH	91	Enabled	High	Enabled	91	gpio
A16	PWM0	PWM 0	Digital	PER_VDDIO	HIGH	92	Enabled	High	Enabled	92	gpio
B16	PWM1	PWM 1	Digital	PER_VDDIO	HIGH	93	Enabled	High	Enabled	93	gpio
F11	DEBUG	Reset Out negate	Digital	PER_VDDIO	HIGH	94	Enabled	High	Enabled	94	gpio
R2	SCIF_DAT0	SCIF controller data 0	Digital	SCIF_VDDIO	HIGH	95	Enabled	High	Enabled	95	gpio
R3	SCIF_DAT1	SCIF controller data 1	Digital	SCIF_VDDIO	HIGH	96	Enabled	High	Enabled	96	gpio
R1	SCIF_CMD	SCIF controller command	Digital	SCIF_VDDIO	HIGH	97	Enabled	High	Enabled	97	gpio
T1	SCIF_CLK	SCIF controller clock	Digital	SCIF_VDDIO	HIGH	98	Enabled	High	Enabled	98	gpio
T2	SCIF_DAT2	SCIF controller data 2	Digital	SCIF_VDDIO	HIGH	99	Enabled	High	Enabled	99	gpio
T3	SCIF_DAT3	SCIF controller data 3	Digital	SCIF_VDDIO	HIGH	100	Enabled	High	Enabled	100	gpio
T7	SCIF_CD	SCIF Controller CD	Digital	SCIF_VDDIO	HIGH	101	Enabled	High	Enabled	101	gpio
U1	SFC1_CSN	SPI1 chip select negate	Digital	COM_VDDIO	HIGH	102	Enabled	High	Enabled	102	gpio
V1	SFC1_CLK	SPI1 clock	Digital	COM_VDDIO	HIGH	103	Enabled	High	Enabled	103	gpio
W1	SFC1_DQ0	SPI1 master out/slave in 0	Digital	COM_VDDIO	HIGH	104	Enabled	High	Enabled	104	gpio
X1	SFC1_DQ1	SPI1 master out/slave in 1	Digital	COM_VDDI	HIGH	105	Enabled	High	Enable	105	gpio

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
				O					d		
U2	SFC1_DQ2	SPI1 master out/slave in 2	Digital	COM_VDDIO	HIGH	106	Enabled	High	Enabled	106	gpio
V2	SFC1_DQ3	SPI1 master out/slave in 3	Digital	COM_VDDIO	HIGH	107	Enabled	High	Enabled	107	gpio
W2	SFC2_CSN	SPI2 chip select negate	Digital	COM_VDDIO	HIGH	108	Enabled	High	Enabled	108	gpio
X2	SFC2_CLK	SPI2 clock	Digital	COM_VDDIO	HIGH	109	Enabled	High	Enabled	109	gpio
U3	SFC2_DQ0	SPI2 master out/slave in 0	Digital	COM_VDDIO	HIGH	110	Enabled	High	Enabled	110	gpio
V3	SFC2_DQ1	SPI2 master out/slave in 1	Digital	COM_VDDIO	HIGH	111	Enabled	High	Enabled	111	gpio
W3	SFC2_DQ2	SPI2 master out/slave in 2	Digital	COM_VDDIO	HIGH	112	Enabled	High	Enabled	112	gpio
X3	SFC2_DQ3	SPI2 master out/slave in 3	Digital	COM_VDDIO	HIGH	113	Enabled	High	Enabled	113	gpio
U4	SFC3_CSN	SPI3 chip select negate	Digital	COM_VDDIO	HIGH	114	Enabled	High	Enabled	114	gpio
V4	SFC3_CLK	SPI3 clock	Digital	COM_VDDIO	HIGH	115	Enabled	High	Enabled	115	gpio
W4	SFC3_DQ0	SPI3 master out/slave in 0	Digital	COM_VDDIO	HIGH	116	Enabled	High	Enabled	116	gpio
X4	SFC3_DQ1	SPI3 master out/slave in 1	Digital	COM_VDDIO	HIGH	117	Enabled	High	Enabled	117	gpio
U5	SFC3_DQ2	SPI3 master out/slave in 2	Digital	COM_VDDIO	HIGH	118	Enabled	High	Enabled	118	gpio
V5	SFC3_DQ3	SPI3 master out/slave in 3	Digital	COM_VDDIO	HIGH	119	Enabled	High	Enabled	119	gpio
G16	SCCBM0_DAT	SCCB master 0 data	Open-drain	VDDIO							
G15	SCCBM0_CLK	SCCB master 0 clock	Open-drain	VDDIO							
G14	SCCBM1_DAT	SCCB master 1 data	Open-drain	VDDIO							
G13	SCCBM1_CLK	SCCB master 1 clock	Open-drain	VDDIO							
U7	SCCBM2_DAT	SCCB master 2 data	Open-drain	VDDIO							
V7	SCCBM2_CLK	SCCB master 2 clock	Open-drain	VDDIO							
W7	SCCBM3_DAT	SCCB master 3 data	Open-drain	VDDIO							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
X7	SCCBM3_CLK	SCCB master 3 clock	Open-drain	VDDIO							
C10	DDR_DQ0	DDR data input/output bit 0	Analog	DDR_VDDQ							
A10	DDR_DQ1	DDR data input/output bit 1	Analog	DDR_VDDQ							
B10	DDR_DQ2	DDR data input/output bit 2	Analog	DDR_VDDQ							
C9	DDR_DQ3	DDR data input/output bit 3	Analog	DDR_VDDQ							
A9	DDR_DQ4	DDR data input/output bit 4	Analog	DDR_VDDQ							
B9	DDR_DQ5	DDR data input/output bit 5	Analog	DDR_VDDQ							
B8	DDR_DQ6	DDR data input/output bit 6	Analog	DDR_VDDQ							
A8	DDR_DQ7	DDR data input/output bit 7	Analog	DDR_VDDQ							
A2	DDR_DQ8	DDR data input/output bit 8	Analog	DDR_VDDQ							
B2	DDR_DQ9	DDR data input/output bit 9	Analog	DDR_VDDQ							
C2	DDR_DQ10	DDR data input/output bit 10	Analog	DDR_VDDQ							
C4	DDR_DQ11	DDR data input/output bit 11	Analog	DDR_VDDQ							
B3	DDR_DQ12	DDR data input/output bit 12	Analog	DDR_VDDQ							
A3	DDR_DQ13	DDR data input/output bit 13	Analog	DDR_VDDQ							
A4	DDR_DQ14	DDR data input/output bit 14	Analog	DDR_VDDQ							
B4	DDR_DQ15	DDR data input/output bit 15	Analog	DDR_VDDQ							
A20	DDR_DQ16	DDR data input/output bit 16	Analog	DDR_VDDQ							
B20	DDR_DQ17	DDR data input/output bit 17	Analog	DDR_VDDQ							
C20	DDR_DQ18	DDR data input/output bit 18	Analog	DDR_VDDQ							
D20	DDR_DQ19	DDR data input/output bit 19	Analog	DDR_VDDQ							
E20	DDR_DQ20	DDR data input/output bit 20	Analog	DDR_VDD							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
				Q							
F20	DDR_DQ21	DDR data input/output bit 21	Analog	DDR_VDDQ							
G20	DDR_DQ22	DDR data input/output bit 22	Analog	DDR_VDDQ							
H20	DDR_DQ23	DDR data input/output bit 23	Analog	DDR_VDDQ							
J20	DDR_DQ24	DDR data input/output bit 24	Analog	DDR_VDDQ							
K20	DDR_DQ25	DDR data input/output bit 25	Analog	DDR_VDDQ							
L20	DDR_DQ26	DDR data input/output bit 26	Analog	DDR_VDDQ							
M20	DDR_DQ27	DDR data input/output bit 27	Analog	DDR_VDDQ							
N20	DDR_DQ28	DDR data input/output bit 28	Analog	DDR_VDDQ							
P20	DDR_DQ29	DDR data input/output bit 29	Analog	DDR_VDDQ							
R20	DDR_DQ30	DDR data input/output bit 30	Analog	DDR_VDDQ							
T20	DDR_DQ31	DDR data input/output bit 31	Analog	DDR_VDDQ							
B7	DDR_DQSP0	DDR positive data strobe signal DQ[7:0]	Analog	DDR_VDDQ							
A7	DDR_DQSN0	DDR negative data strobe signal DQ[7:0]	Analog	DDR_VDDQ							
B5	DDR_DQSP1	DDR positive data strobe signal DQ[15:8]	Analog	DDR_VDDQ							
A5	DDR_DQSN1	DDR negative data strobe signal DQ[15:8]	Analog	DDR_VDDQ							
G5	DDR_DQSP2	DDR positive data strobe signal DQ[23:16]	Analog	DDR_VDDQ							
G6	DDR_DQSN2	DDR negative data strobe signal DQ[23:16]	Analog	DDR_VDDQ							
H5	DDR_DQSP3	DDR positive data strobe signal DQ[31:24]	Analog	DDR_VDDQ							
H6	DDR_DQSN3	DDR negative data strobe signal DQ[31:24]	Analog	DDR_VDDQ							
C7	DDR_DM0	DDR data mask signal 0	Analog	DDR_VDDQ							
B6	DDR_DM1	DDR data mask signal 1	Analog	DDR_VDDQ							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
J5	DDR_DM2	DDR data mask signal 2	Analog	DDR_VDDQ							
J6	DDR_DM3	DDR data mask signal 3	Analog	DDR_VDDQ							
B1	DDR_A0	DDR address bit 0	Analog	DDR_VDDQ							
C1	DDR_A1	DDR address bit 1	Analog	DDR_VDDQ							
D1	DDR_A2	DDR address bit 2	Analog	DDR_VDDQ							
D3	DDR_A3	DDR address bit 3	Analog	DDR_VDDQ							
D2	DDR_A4	DDR address bit 4	Analog	DDR_VDDQ							
J1	DDR_A5	DDR address bit 5	Analog	DDR_VDDQ							
K2	DDR_A6	DDR address bit 6	Analog	DDR_VDDQ							
K1	DDR_A7	DDR address bit 7	Analog	DDR_VDDQ							
K3	DDR_A8	DDR address bit 8	Analog	DDR_VDDQ							
L3	DDR_A9	DDR address bit 9	Analog	DDR_VDDQ							
E3	DDR_A10	DDR address bit 10	Analog	DDR_VDDQ							
E2	DDR_A11	DDR address bit 11	Analog	DDR_VDDQ							
E1	DDR_A12	DDR address bit 12	Analog	DDR_VDDQ							
E4	DDR_A13	DDR address bit 13	Analog	DDR_VDDQ							
H3	DDR_BA0	Bank address of DDR bit 0	Analog	DDR_VDDQ							
F2	DDR_BA1	Bank address of DDR bit 1	Analog	DDR_VDDQ							
J2	DDR_BA2	Bank address of DDR bit 2	Analog	DDR_VDDQ							
F1	DDR_CLKP	DDR positive edge clock	Analog	DDR_VDDQ							
G1	DDR_CLKN	DDR negative edge clock	Analog	DDR_VDDQ							
G4	DDR_CKE	DDR clock enable	Analog	DDR_VDD							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
				Q							
G2	DDR_CS	DDR chip select	Analog	DDR_VDDQ							
G3	DDR_RAS	DDR row address select	Analog	DDR_VDDQ							
H1	DDR_CAS	DDR column address select	Analog	DDR_VDDQ							
H2	DDR_WE	DDR write enable	Analog	DDR_VDDQ							
K4	DDR_RESETN	DDR reset negate	Analog	DDR_VDDQ							
H4	DDR_ODT	DDR on die resistor termination	Analog	DDR_VDDQ							
A1	DDR_ZQ	DDR resistor interface for calibration	Analog	DDR_VDDQ							
L2	DDR_VDDQ	DDR I/O pad power	Power/Ground								
D8	DDR_VDDQ	DDR I/O pad power	Power/Ground								
D5	DDR_VDDQ	DDR I/O pad power	Power/Ground								
B11	DDR_VDDQ	DDR I/O pad power	Power/Ground								
F4	DDR_VDDQ	DDR I/O pad power	Power/Ground								
J4	DDR_VDDQ	DDR I/O pad power	Power/Ground								
L1	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
C8	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
A11	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
C5	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
C3	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
F3	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
J3	DDR_VSSQ	DDR I/O pad ground	Power/Ground								
F5	DDR_VDD	DDR PHY power 0.9V	Power/Ground								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
E5	DDR_VDD	DDR PHY power 0.9V	Power/Ground								
M2	DU_VSS	DDR PHY Ground	Power/Ground								
M3	DU_VSS	DDR PHY Ground	Power/Ground								
D4	PLL_VDDA	DDR PLL Vdd	Power/Ground								
D6	DDR_DBG0	DDR debug signal 0	Analog	DDR_VDDQ							
D7	DDR_DBG1	DDR debug signal 1	Analog	DDR_VDDQ							
A6	DDR_VREFDQ01	DRAM IO reference voltage for LPDDR2 Data lane 0/1	Analog	DDR_VDDQ							
E7	DDR_VREFDQ23	DRAM IO reference voltage for LPDDR2 Data lane 2/3	Analog	DDR_VDDQ							
R9	MRXL0_DP	MIPI receiver 0 positive data	Analog	MIPIRX_VDDA							
T9	MRXL0_DN	MIPI receiver 0 negative data	Analog	MIPIRX_VDDA							
R10	MRXL1_DP	MIPI receiver 1 positive data	Analog	MIPIRX_VDDA							
T10	MRXL1_DN	MIPI receiver 1 negative data	Analog	MIPIRX_VDDA							
R12	MRXL2_DP	MIPI receiver 2 positive data	Analog	MIPIRX_VDDA							
T12	MRXL2_DN	MIPI receiver 2 negative data	Analog	MIPIRX_VDDA							
R13	MRXL3_DP	MIPI receiver 3 positive data	Analog	MIPIRX_VDDA							
T13	MRXL3_DN	MIPI receiver 3 negative data	Analog	MIPIRX_VDDA							
R11	MRXL0_CP	MIPI receiver 0 positive clock	Analog	MIPIRX_VDDA							
T11	MRXL0_CN	MIPI receiver 0 negative clock	Analog	MIPIRX_VDDA							
R14	MRXL1_CP	MIPI receiver 1 positive clock	Analog	MIPIRX_VDDA							
T14	MRXL1_CN	MIPI receiver 1 negative clock	Analog	MIPIRX_VDDA							
P11	MIPIRX_VDDA	MIPI receiver I/O pad power	Power/Ground								
N12	MIPIRX_VDD	MIPI receiver I/O pad power	Power/Gr								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
	A		ound								
P13	MIPIRX_VDD	MIPI receiver digital power	Power/Ground								
P12	MIPIRX_VSS	MIPI receiver I/O pad ground	Power/Ground								
P10	MIPIRX_VSS	MIPI receiver I/O pad ground	Power/Ground								
R15	MTX0_DP	MIPI transmitter 0 positive data	Analog	MIPITX_VDDA							
R16	MTX0_DN	MIPI transmitter 0 negative data	Analog	MIPITX_VDDA							
N15	MTX1_DP	MIPI transmitter 1 positive data	Analog	MIPITX_VDDA							
N16	MTX1_DN	MIPI transmitter 1 negative data	Analog	MIPITX_VDDA							
N17	MTX2_DP	MIPI transmitter 2 positive data	Analog	MIPITX_VDDA							
P17	MTX2_DN	MIPI transmitter 2 negative data	Analog	MIPITX_VDDA							
R17	MTX3_DP	MIPI transmitter 3 positive data	Analog	MIPITX_VDDA							
T17	MTX3_DN	MIPI transmitter 3 negative data	Analog	MIPITX_VDDA							
P15	MTX_CP	MIPI transmitter positive clock	Analog	MIPITX_VDDA							
P16	MTX_CN	MIPI transmitter negative clock	Analog	MIPITX_VDDA							
T15	MIPITX_VDDA	MIPI transmitter I/O pad power	Power/Ground								
P14	MIPITX_VDD	MIPI transmitter digital power	Power/Ground								
T16	MIPITX_VSS	MIPI transmitter ground	Power/Ground								
A17	MRXH0_DP	MIPI 2.5Gbps receiver 0 positive data	Analog	MIPIRX_VDDA							
B17	MRXH0_DN	MIPI 2.5Gbps receiver 0 negative data	Analog	MIPIRX_VDDA							
C17	MRXH1_DP	MIPI 2.5Gbps receiver 1 positive data	Analog	MIPIRX_VDDA							
D17	MRXH1_DN	MIPI 2.5Gbps receiver 1 negative data	Analog	MIPIRX_VDDA							
E17	MRXH2_DP	MIPI 2.5Gbps receiver 2 positive data	Analog	MIPIRX_VDDA							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
F17	MRXH2_DN	MIPI 2.5Gbps receiver 2 negative data	Analog	MIPIRX_VDDA							
G17	MRXH3_DP	MIPI 2.5Gbps receiver 3 positive data	Analog	MIPIRX_VDDA							
H17	MRXH3_DN	MIPI 2.5Gbps receiver 3 negative data	Analog	MIPIRX_VDDA							
J17	MRXH0_CP	MIPI 2.5Gbps receiver 0 positive clock	Analog	MIPIRX_VDDA							
K17	MRXH0_CN	MIPI 2.5Gbps receiver 0 negative clock	Analog	MIPIRX_VDDA							
L17	MRXH1_CP	MIPI 2.5Gbps receiver 1 positive clock	Analog	MIPIRX_VDDA							
M17	MRXH1_CN	MIPI 2.5Gbps receiver 1 negative clock	Analog	MIPIRX_VDDA							
M4	USBD_DP	USB device D+	Analog	USBD_VDDIO							
N4	USBD_DM	USB device D-	Analog	USBD_VDDIO							
N2	USBD_VDDIO	USB device I/O pad power	Power/Ground								
L5	USBD_VDD	USB device analog power	Power/Ground								
F6	DU_VSS	USB device I/O pad ground	Power/Ground								
E6	DU_VSS	USB device digital ground	Power/Ground								
N3	USBD_VDDA	Usb pll 1.8v	Power/Ground								
L4	USBD_REXT	Usb voltage ref	Analog	USBD_VDDIO							
A18	AOL0_CLK	Always on link for SNR 0	Analog	AOL_VDDIO							
B18	AOL0_DQ0	Always on link for SNR 0	Analog	AOL_VDDIO							
C18	AOL0_DQ1	Always on link for SNR 0	Analog	AOL_VDDIO							
D18	AOL0_DQ2	Always on link for SNR 0	Analog	AOL_VDDIO							
E18	AOL0_DQ3	Always on link for SNR 0	Analog	AOL_VDDIO							
F18	AOL1_CLK	Always on link for SNR 1	Analog	AOL_VDDIO							
G18	AOL1_DQ0	Always on link for SNR 1	Analog	AOL_VDDI							

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
				O							
H18	AOL1_DQ1	Always on link for SNR 1	Analog	AOL_VDDIO							
J18	AOL1_DQ2	Always on link for SNR 1	Analog	AOL_VDDIO							
K18	AOL1_DQ3	Always on link for SNR 1	Analog	AOL_VDDIO							
L18	AOL2_CLK	Always on link for SNR 2	Analog	AOL_VDDIO							
M18	AOL2_DQ0	Always on link for SNR 2	Analog	AOL_VDDIO							
N18	AOL2_DQ1	Always on link for SNR 2	Analog	AOL_VDDIO							
P18	AOL2_DQ2	Always on link for SNR 2	Analog	AOL_VDDIO							
R18	AOL2_DQ3	Always on link for SNR 2	Analog	AOL_VDDIO							
X18	AOL_SW_IN		Analog	AOL_VDDIO							
V19	AOL_SW_OUT		Analog	AOL_VDDIO							
W19	AOL_VDDIO		Power/Ground								
X19	AOL_VDDIO		Power/Ground								
C13	PER_VDDIO		Power/Ground								
D15	PER_VDDIO		Power/Ground								
P2	SCIF_VDDIO	1.8v/3.3v pad power	Power/Ground								
J14	NAND_VDDIO	1.8v/3.3v pad power	Power/Ground								
A19	COM_VDDIO	1.8v/3.3v pad power	Power/Ground								
K13	LCD_VDDIO	1.8v/3.3v pad power	Power/Ground								
B19	LCD_VDDIO	1.8v/3.3v pad power	Power/Ground								
P3	VREF1	VREF for bottom left corner digital IO Pin	Analog								
M8	VREF2	VREF for bottom left corner digital IO Pin	Analog								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
L14	VREF3	VREF for top right corner digital IO Pin	Analog								
D14	VREF4	VREF for top right corner digital IO Pin	Analog								
P9	EFUSE_VDDP		Power/Ground								
K8	CORE_VDD	PD domain, ACTIVE power,1.1v/0.9v	Power/Ground								
F9	CORE_VDD	PD domain, ACTIVE power,1.1v/0.9v	Power/Ground								
L6	VSS	digital core ground & all ESD ground	Power/Ground								
P8	VSS	digital core ground & all ESD ground	Power/Ground								
H10	VSS	digital core ground & all ESD ground	Power/Ground								
H8	VSS	digital core ground & all ESD ground	Power/Ground								
G9	VSS	digital core ground & all ESD ground	Power/Ground								
M6	VSS	digital core ground & all ESD ground	Power/Ground								
H9	VSS	digital core ground & all ESD ground	Power/Ground								
P5	VSS	digital core ground & all ESD ground	Power/Ground								
P1	VSS	digital core ground & all ESD ground	Power/Ground								
N6	VSS	digital core ground & all ESD ground	Power/Ground								
K6	VSS	digital core ground & all ESD ground	Power/Ground								
G8	VSS	digital core ground & all ESD ground	Power/Ground								
V13	VSS	digital core ground & all ESD ground	Power/Ground								
K14	VSS	digital core ground & all ESD ground	Power/Ground		0						
G10	VSS	SCIF pad ground	Power/Ground								
J8	VSS	NAND pad ground	Power/Ground								
W13	VSS	PER pad ground	Power/Gr								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
			ound								
J10	VSS	LCD pad ground	Power/Ground								
C14	VSS	COM pad ground	Power/Ground								
C6	DDR_ANA	Don't Connect	NC								
E10		Don't Connect	NC								
E8		Don't Connect	NC								
E9		Don't Connect	NC								
F10	CORE_VDD	Don't Connect	NC								
F7		Don't Connect	NC								
F8	CORE_VDD	Don't Connect	NC								
G11	CORE_VDD_VA	Don't Connect	NC								
G7	CORE_VDD_CPU	Don't Connect	NC								
H11	CORE_VDD_VA	Don't Connect	NC								
H13		Don't Connect	NC								
H7	CORE_VDD_CPU	Don't Connect	NC								
J11	CORE_VDD_VA	Don't Connect	NC								
J13		Don't Connect	NC								
J7	CORE_VDD_CPU	Don't Connect	NC								
K10	CORE_VDD_DP	Don't Connect	NC								
K11	CORE_VDD_VA	Don't Connect	NC								
K5		Don't Connect	NC								
K7	CORE_VDD_CPU	Don't Connect	NC								
K9	CORE_VDD_DP	Don't Connect	NC								
L11		Don't Connect	NC								
L12		Don't Connect	NC								
L13		Don't Connect	NC								
L19	CORE_VDD_AV1	Don't Connect	NC								
L8		Don't Connect	NC								
L9		Don't Connect	NC								
M12		Don't Connect	NC								

PIN	NAME	Description	Type	Power Rail	Drive Strength	Digital Pad Index	Default Pull Enable	Default Pull Direction	Default Input Enable	GPIO NUM	Default Selection
M19	CORE_VDD_AV1	Don't Connect	NC								
M5		Don't Connect	NC								
M9		Don't Connect	NC								
N13		Don't Connect	NC								
N19	CORE_VDD_V5	Don't Connect	NC								
N5		Don't Connect	NC								
N8		Don't Connect	NC								
P19	CORE_VDD_V5	Don't Connect	NC								
P4		Don't Connect	NC								
P6		Don't Connect	NC								
R4		Don't Connect	NC								
R5		Don't Connect	NC								
R8		Don't Connect	NC								
T18	AOL3_CLK	Don't Connect	NC								
T4		Don't Connect	NC								
T5		Don't Connect	NC								
U11	GPIO8	Don't Connect	NC								
U13		Don't Connect	NC								
U19	CORE_VDD_AO	Don't Connect	NC								
U20	AOL3_DQ0	Don't Connect	NC								
U6	SFC4_DQ0	Don't Connect	NC								
V11	GPIO9	Don't Connect	NC								
V20	AOL3_DQ1	Don't Connect	NC								
V6	SFC4_DQ1	Don't Connect	NC								
W20	AOL3_DQ2	Don't Connect	NC								
W5	SFC4_CSN	Don't Connect	NC								
W6	SFC4_DQ2	Don't Connect	NC								
X20	AOL3_DQ3	Don't Connect	NC								
X5	SFC4_CLK	Don't Connect	NC								
X6	SFC4_DQ3	Don't Connect	NC								

6.2 Pin Mux

PIN	NAME	MUX_SEL	MUX_SEL=0		MUX_SEL=1		MUX_SEL=2		MUX_SEL=3		MUX_SEL=4	
			FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL
T8	RSTN		rst_n									
D9	TEST_MODE		tm		tm		tm		tm		tm	
C16	BOOT_MODE0		boot_mode[0]		boot_mode[0]		boot_mode[0]		boot_mode[0]		boot_mode[0]	
D16	BOOT_MODE1		boot_mode[1]		boot_mode[1]		boot_mode[1]		boot_mode[1]		boot_mode[1]	
C15	BOOT_MODE2		boot_mode[2]		boot_mode[2]		boot_mode[2]		boot_mode[2]		boot_mode[2]	
U9	GPIO0		ao_gpio[0]	ao_gpio=0								
V9	GPIO1		ao_gpio[1]	ao_gpio=0								
W9	GPIO2		ao_gpio[2]	ao_gpio=0								
X9	GPIO3		ao_gpio[3]	ao_gpio=0								
U10	GPIO4		ao_gpio[4]	ao_gpio=0								
V10	GPIO5		ao_gpio[5]	ao_gpio=0								
W10	GPIO6		ao_gpio[6]	ao_gpio=0								
X10	GPIO7		ao_gpio[7]	ao_gpio=0								
N10	UART1_TX		uart1_tx									
N11	UART1_RX		uart1_rx	uart1=0								
L7	CCLK		snr_cclk									
B15	JTAG_TCK	r_jtag_sel_0	jtag_tclk	jtag=1					ao_jtag_tclk	ao_jtag=1	ba22_jtag_tclk	ba22_jtag=1
F12	JTAG_TMS	r_jtag_sel_1	jtag_tms	jtag=1					ao_jtag_tms	ao_jtag=1	ba22_jtag_tms	ba22_jtag=1
A15	JTAG_TDI	r_jtag_sel_2	jtag_tdi	jtag=1					ao_jtag_tdi	ao_jtag=1	ba22_jtag_tdi	ba22_jtag=1
E12	JTAG_TDO	r_jtag_sel_3	jtag_tdo	jtag=1					ao_jtag_tdo	ao_jtag=1	ba22_jtag_tdo	ba22_jtag=1
U12	SIF3_MOSI		sif3_mosi	sif3=0								
V12	SIF3_MISO		sif3_miso	sif3=0								
W12	SIF3_CSN		sif3_cs_n	sif3=0								
X12	SIF3_CLK		sif3_clk	sif3=0								
X13	LCD_CLK	r_lcd_dvp_sel_0	lcd_clk				dvp_clk					
U14	LCD_VSYNC	r_lcd_dvp_sel_1	lcd_vsync				dvp_vsync					
V14	LCD_HSYNC	r_lcd_dvp_sel_2	lcd_hsync				dvp_href					
W14	LCD_DEN	r_lcd_dvp_sel_3	lcd_den				dvp_hvalid					
X14	LCD_DAT0	r_lcd_dvp_sel_4	lcd_dat[0]				dvp_d[0]					
U15	LCD_DAT1	r_lcd_dvp_sel_5	lcd_dat[1]				dvp_d[1]					

PIN	NAME	MUX_SEL	MUX_SEL=0		MUX_SEL=1		MUX_SEL=2		MUX_SEL=3		MUX_SEL=4	
			FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL
V15	LCD_DAT2	r_lcd_dvp_sel_6	lcd_dat[2]				dvp_d[2]					
W15	LCD_DAT3	r_lcd_dvp_sel_7	lcd_dat[3]				dvp_d[3]					
X15	LCD_DAT4	r_lcd_dvp_sel_8	lcd_dat[4]				dvp_d[4]					
U16	LCD_DAT5	r_lcd_dvp_sel_9	lcd_dat[5]				dvp_d[5]					
V16	LCD_DAT6	r_lcd_dvp_sel_10	lcd_dat[6]				dvp_d[6]					
W16	LCD_DAT7	r_lcd_dvp_sel_11	lcd_dat[7]				dvp_d[7]					
X16	LCD_DAT8	r_lcd_dvp_sel_12	lcd_dat[8]		uart2_cts	uart2=1	dvp_d[8]		pvt8_clk			
U17	LCD_DAT9	r_lcd_dvp_sel_13	lcd_dat[9]		uart2_rts	uart2=1	dvp_d[9]		pvt9_clk			
V17	LCD_DAT10	r_lcd_uart_sel_0	lcd_dat[10]		uart2_tx	uart2=1			pvt10_clk			
W17	LCD_DAT11	r_lcd_uart_sel_1	lcd_dat[11]		uart2_rx	uart2=1			pvt11_clk			
X17	LCD_DAT12	r_lcd_sif1_sel_0	lcd_dat[12]		sif1_mosi	sif1=2			pvt12_clk			
U18	LCD_DAT13	r_lcd_sif1_sel_1	lcd_dat[13]		sif1_miso	sif1=2			pvt13_clk			
V18	LCD_DAT14	r_lcd_sif1_sel_2	lcd_dat[14]		sif1_cs_n	sif1=2						
W18	LCD_DAT15	r_lcd_sif1_sel_3	lcd_dat[15]		sif1_clk	sif1=2						
M7	UART0_TX	r_uart0_lcd_sel_0	uart0_tx		lcd_dat[16]		sif1_mosi	sif1=3				
N7	UART0_RX	r_uart0_lcd_sel_1	uart0_rx	uart0=1	lcd_dat[17]		sif1_miso	sif1=3				
P7	UART0_CTS	r_uart0_lcd_sel_2	uart0_cts	uart0=1	lcd_dat[18]		sif1_cs_n	sif1=3				
R7	UART0_RTS	r_uart0_lcd_sel_3	uart0_rts	uart0=1	lcd_dat[19]		sif1_clk	sif1=3				
U8	DM0_CLK	r_dm0_lcd_sel0	dm0_clk	dm0=1	lcd_dat[20]		uart0_tx					
V8	DM0_DAT	r_dm0_lcd_sel1	dm0_dat	dm0=1	lcd_dat[21]		uart0_rx	uart0=2				
W8	DM1_CLK	r_dm1_lcd_sel0	dm1_clk	dm1=1	lcd_dat[22]		uart0_cts	uart0=2				
X8	DM1_DAT	r_dm1_lcd_sel1	dm1_dat	dm1=1	lcd_dat[23]		uart0_rts	uart0=2				
H16	NAND_D0	r_nand_sel_0	nand_d[0]	nand=1	ddr_dbg_sig[0]				pvt0_clk			
H15	NAND_D1	r_nand_sel_1	nand_d[1]	nand=1	ddr_dbg_sig[1]				pvt1_clk			
J15	NAND_D2	r_nand_sel_2	nand_d[2]	nand=1	ddr_dbg_sig[2]				pvt2_clk			
J16	NAND_D3	r_nand_sel_3	nand_d[3]	nand=1	ddr_dbg_sig[3]				pvt3_clk			
L15	NAND_D4	r_nand_sel_4	nand_d[4]	nand=1	ddr_dbg_sig[4]				pvt4_clk			
L16	NAND_D5	r_nand_sel_5	nand_d[5]	nand=1	ddr_dbg_sig[5]				pvt5_clk			
M14	NAND_D6	r_nand_sel_6	nand_d[6]	nand=1	ddr_dbg_sig[6]				pvt6_clk			
M13	NAND_D7	r_nand_sel_7	nand_d[7]	nand=1	ddr_dbg_sig[7]				pvt7_clk			
H14	NAND_CS	r_nand_sel_8	nand_cs_n									
K15	NAND_ALE		nand_ale									
M15	NAND_CLE		nand_cle									
K16	NAND_WE		nand_we_n									
N14	NAND_RE		nand_re_n									

PIN	NAME	MUX_SEL	MUX_SEL=0		MUX_SEL=1		MUX_SEL=2		MUX_SEL=3		MUX_SEL=4	
			FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL
M16	NAND_RB		nand_rb_n	nandrb=1								
E11	SIF2_MOSI	r_sif2_uart2_sel_0	sif2_mosi	sif2=0	uart2_cts	uart2=2	mipirx_bist_flag		usb_clk_usable			
D11	SIF2_MISO	r_sif2_uart2_sel_1	sif2_miso	sif2=0	uart2_rts	uart2=2	mipirx25_bist_flag					
D10	SIF2_CSN	r_sif2_uart2_sel_2	sif2_cs_n	sif2=0	uart2_tx	uart2=2						
C11	SIF2_CLK	r_sif2_uart2_sel_3	sif2_clk	sif2=0	uart2_rx	uart2=2						
B13	SFC0_CSN		sfc_cs_n	sfc=0								
B12	SFC0_CLK		sfc_clk	sfc=0								
A12	SFC0_DQ0		sfc_mosi[0]	sfc=0								
A13	SFC0_DQ1		sfc_mosi[1]	sfc=0								
C12	SFC0_DQ2		sfc_mosi[2]	sfc=0								
D12	SFC0_DQ3		sfc_mosi[3]	sfc=0								
G12	SFC0_DQ4		sfc_mosi[4]	sfc=0								
H12	SFC0_DQ5		sfc_mosi[5]	sfc=0								
J12	SFC0_DQ6		sfc_mosi[6]	sfc=0								
K12	SFC0_DQ7		sfc_mosi[7]	sfc=0								
F16	SCIO_DAT0	r_scio_uart_sel0	scio_dat[0]	scio=0	uart2_cts	uart2=3						
E16	SCIO_DAT1	r_scio_uart_sel1	scio_dat[1]	scio=0	uart2_rts	uart2=3						
F14	SCIO_DAT2	r_scio_uart_sel2	scio_dat[2]	scio=0	uart2_tx	uart2=3						
F15	SCIO_DAT3	r_scio_uart_sel3	scio_dat[3]	scio=0	uart2_rx	uart2=3						
E15	SCIO_CMD		scio_cmd	scio=0								
F13	SCIO_CLK		scio_clk	scio=0								
M10	SIF0_MOSI	r_sif0_dm0_sel0	sif0_mosi	sif0=0			dm0_clk	dm0=2				
M11	SIF0_MISO	r_sif0_dm0_sel1	sif0_miso	sif0=0			dm0_dat	dm0=2				
N9	SIF0_CSN	r_sif0_dm1_sel2	sif0_cs_n	sif0=0			dm1_clk	dm1=2				
L10	SIF0_CLK	r_sif0_dm1_sel3	sif0_clk	sif0=0			dm1_dat	dm1=2				
E13	AI_MCLK		i2s_mclk	i2s=0								
A14	AI_DI	r_i2s_di_sel	i2s_di	i2s=0	uart0_tx		dm0_clk	dm0=3	sif1_mosi	sif1=4		
B14	AI_DO	r_i2s_do_sel	i2s_do	i2s=0	uart0_rx	uart0=2	dm0_dat	dm0=3	sif1_miso	sif1=4		
D13	AI_LR	r_i2s_lck_sel	i2s_lr	i2s=0	uart0_cts	uart0=2	dm1_clk	dm1=3	sif1_cs_n	sif1=4		
E14	AI_CLK	r_i2s_bck_sel	i2s_clk	i2s=0	uart0_rts	uart0=2	dm1_dat	dm1=3	sif1_clk	sif1=4		
A16	PWM0		pwm0									
B16	PWM1		pwm1									
F11	DEBUG		rst_out_n									
R2	SCIF_DAT0		scif_dat[0]	scif=0								

PIN	NAME	MUX_SEL	MUX_SEL=0		MUX_SEL=1		MUX_SEL=2		MUX_SEL=3		MUX_SEL=4	
			FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL	FUNC	INPUT_MUX_SEL
R3	SCIF_DAT1		scif_dat[1]	scif=0								
R1	SCIF_CMD		scif_cmd	scif=0								
T1	SCIF_CLK		scif_clk	scif=0								
T2	SCIF_DAT2		scif_dat[2]	scif=0								
T3	SCIF_DAT3		scif_dat[3]	scif=0								
T7	SCIF_CD		scif_cd	scif_cd=0								
U1	SFC1_CSN		spi1_cs_n	spi1=0								
V1	SFC1_CLK		spi1_clk	spi1=0								
W1	SFC1_DQ0		spi1_mosi[0]	spi1=0								
X1	SFC1_DQ1		spi1_mosi[1]	spi1=0								
U2	SFC1_DQ2		spi1_mosi[2]	spi1=0								
V2	SFC1_DQ3		spi1_mosi[3]	spi1=0								
W2	SFC2_CSN		spi2_cs_n	spi2=0								
X2	SFC2_CLK		spi2_clk	spi2=0								
U3	SFC2_DQ0	r_spi2_nand_sel_0	spi2_mosi[0]	spi2=0	nand_d[8]	nand16=1						
V3	SFC2_DQ1	r_spi2_nand_sel_1	spi2_mosi[1]	spi2=0	nand_d[9]	nand16=1						
W3	SFC2_DQ2	r_spi2_nand_sel_2	spi2_mosi[2]	spi2=0	nand_d[10]	nand16=1						
X3	SFC2_DQ3	r_spi2_nand_sel_3	spi2_mosi[3]	spi2=0	nand_d[11]	nand16=1						
U4	SFC3_CSN		spi3_cs_n	spi3=0								
V4	SFC3_CLK		spi3_clk	spi3=0								
W4	SFC3_DQ0	r_spi3_nand_sel_0	spi3_mosi[0]	spi3=0	nand_d[12]	nand16=1						
X4	SFC3_DQ1	r_spi3_nand_sel_1	spi3_mosi[1]	spi3=0	nand_d[13]	nand16=1						
U5	SFC3_DQ2	r_spi3_nand_sel_2	spi3_mosi[2]	spi3=0	nand_d[14]	nand16=1						
V5	SFC3_DQ3	r_spi3_nand_sel_3	spi3_mosi[3]	spi3=0	nand_d[15]	nand16=1						

7 IRQ MAP

- For the IRQ Map, each IRQ_ID maps directly to a interrupt register bit index in the IRQ Controller, in a running order. The highest pending IRQ_ID would be given by the IRQ Controller. There are 2 priority groups in the IRQ Controller (high and low), which SW can set for each IRQ_ID.

7.1 ISLAND_0 IRQ MAP

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
0	TIMER5	LEVEL	GENERIC	
1	TIMER6	LEVEL	GENERIC	
2	WDT_TO_AO_BA	LEVEL	GENERIC	Watchdog Timeout for AO_BA22
3	WDT_AO_BA	LEVEL	GENERIC	Watchdog IRQ for AO BA22
4	AO_GPIO	LEVEL	GENERIC	
5	MBOXAB	LEVEL	GENERIC	Mailbox IRQ to AO_BA. Triggered by BA22
6	MBOXAC	LEVEL	GENERIC	Mailbox IRQ to AO_BA. Triggered by CPU
7	UART1	LEVEL	GENERIC	
8	RTC	LEVEL	GENERIC	
9	SIF3	LEVEL	GENERIC	

7.2 ISLAND_1 IRQ MAP

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
0	WDT_TO_SYS	LEVEL	GENERIC	For System and A32. Using WDT1
1	WDT_SYS	LEVEL	GENERIC	For System and A32 . Using WDT1
2	WDT_TO_BA22	LEVEL	GENERIC	For BA22
3	WDT_BA22	LEVEL	GENERIC	For BA22
4	DMA	LEVEL	GENERIC	DMA
5	CRPYTION	LEVEL	GENERIC	
6	SJTAG	LEVEL	GENERIC	SJTAG irq
7	SBOOT_SHA	LEVEL	GENERIC	SBOOT sha fifo empty
8	SBOOT_SIGN	LEVEL	GENERIC	SBOOT Signature / SHA done
9	DDRC	LEVEL	GENERIC	DDRC
10	CORE_DDRC_MERGE0	LEVEL	bus_clk	
11	CORE_SRAM_MERGE	LEVEL	bus_clk	
12	TIMER0	LEVEL	GENERIC	
13	TIMER1	LEVEL	GENERIC	
14	TIMER2	LEVEL	GENERIC	
15	TIMER3	LEVEL	GENERIC	

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
16	TIMER4	LEVEL	GENERIC	
17	GPIO	LEVEL	GENERIC	
18	NAND	LEVEL	GENERIC	NAND Flash
19	SFC	LEVEL	GENERIC	Serial Flash Controller
20	SIF0	LEVEL	GENERIC	
21	SIF1	LEVEL	GENERIC	
22	SIF2	LEVEL	GENERIC	
23	UART0	LEVEL	GENERIC	UART Master (UART0)
24	UART1	LEVEL	GENERIC	UART Slave
25	UART2	LEVEL	GENERIC	
26	USB_RESUME	LEVEL	GENERIC	
27	USB_STA	LEVEL	GENERIC	USB_sta
28	USB_EP	LEVEL	GENERIC	USB_EP
29	USB_UDC	LEVEL	GENERIC	USB_udc
30	USB_SUSPEND	LEVEL	GENERIC	
31	UDC20_SETUP	EDGE	usb_app_clk	
32	IRQ_EARLY_SPD	EDGE	usb_app_clk	
33	IRQ_SPD	EDGE	bus_clk	
34	IRQ_USB	EDGE	usb_app_clk	
35	IRQ_USB_RESUME	EDGE	bus_clk	
36	SCCBM0	LEVEL	GENERIC	
37	SCCBM1	LEVEL	GENERIC	
38	SCCBM2	LEVEL	GENERIC	
39	SCCBM3	LEVEL	GENERIC	
40	GUNZIP	LEVEL	GENERIC	
41	SCIF	LEVEL	GENERIC	FSMC
42	SCIO	LEVEL	GENERIC	SDIO
43	SPI1	LEVEL	GENERIC	SFC 1
44	SPI2	LEVEL	GENERIC	SFC 2
45	SPI3	LEVEL	GENERIC	SFC 3
46	SPI4	LEVEL	GENERIC	Not used
47	A32MP_PMU0	LEVEL	GENERIC	A32MP PMU unit
48	A32MP_PMU1	LEVEL	GENERIC	
49	A32MP_PMU2	LEVEL	GENERIC	
50	A32MP_PMU3	LEVEL	GENERIC	
51	MBOXCB_C	LEVEL	GENERIC	Mailbox IRQ to CPU. Triggered by BA22
52	MBOXCB_B	LEVEL	GENERIC	Mailbox IRQ to BA22. Triggered by CPU
53	MBOXAB_A	LEVEL	GENERIC	Mailbox IRQ to BA22. Triggered by AO_BA22
54	MBOXAC_A	LEVEL	GENERIC	Mailbox IRQ to CPU. Triggered by AO_BA22
55	MIPITX_INT	LEVEL	GENERIC	
56	MIPIRXH	LEVEL	GENERIC	Mipirx H error
57	MIPIRXL	LEVEL	GENERIC	Mipirx L error
58	AI0	LEVEL	GENERIC	

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
59	AI1	LEVEL	GENERIC	
60	VFIFO_EOF	EDGE	vfifo_clk	
61	VFIFO_SOF	EDGE	vfifo_clk	
62	LCDC	LEVEL	GENERIC	LCD controller
63	AO_HOGMD_0	LEVEL	GENERIC	
64	AO_HOGMD_1	LEVEL	GENERIC	
65	AO_HOGMD_2	LEVEL	GENERIC	
66	AO_HOGMD_3	LEVEL	GENERIC	
67	AO_ECIF0	LEVEL	GENERIC	
68	AO_SFB0	LEVEL	GENERIC	
69	AO_SFB1	LEVEL	GENERIC	
70	AO_SFB2	LEVEL	GENERIC	
71	AO_SFB3	LEVEL	GENERIC	
72	AO_RAW_ENC0	LEVEL	GENERIC	
73	AO_RAW_ENC1	LEVEL	GENERIC	
74	AO_RAW_ENC2	LEVEL	GENERIC	
75	AO_RAW_ENC3	LEVEL	GENERIC	
76	AO_RAW_ENC4	LEVEL	GENERIC	
77	AO_RAW_DEC	LEVEL	GENERIC	
78	DVP	LEVEL	GENERIC	
79	AO_YSCALER0	LEVEL	GENERIC	
80	AO_YSCALER1	LEVEL	GENERIC	
81	AO_YSCALER2	LEVEL	GENERIC	
82	AO_YSCALER3	LEVEL	GENERIC	
83	AOL_RX0	LEVEL	GENERIC	
84	AOL_RX1	LEVEL	GENERIC	
85	AOL_RX2	LEVEL	GENERIC	
86	AOL_RX3	LEVEL	GENERIC	
87	CORE_DDRC_MERGE1	LEVEL	bus_clk	
88	DDRPLL_LOCK	LEVEL	GENERIC	
89	SIF3	LEVEL	GENERIC	
90	RTC	LEVEL	GENERIC	
91	AO_CIP0	LEVEL	GENERIC	
92	VA_DDRC_MERGE	LEVEL	va_bus_clk	
93	VA_SRAM_MERGE	LEVEL	va_bus_clk	
94	NPU	LEVEL	va_bus_clk	CNN
95	NPU_SGA	LEVEL	va_bus_clk	CNN SGA
96	ISP_DDRC_MERGE	LEVEL	isp_bus_clk	
97	ISP_PRE_0	LEVEL	isp_v2_clk	Pipe 0 pre (hist /lens_ol/awb/aec/line done), pre_pipe_stat done, all stat done
98	ISP_PRE_1	LEVEL	isp_v2_clk	Pipe 1
99	ISP_PRE_2	LEVEL	isp_v2_clk	Pipe 2
100	ISP_PRE_3	LEVEL	isp_v2_clk	Pipe 3
101	ISP_PRE_4	LEVEL	isp_v2_clk	Pipe 4
102	ISP_PRE_5	LEVEL	isp_v2_clk	Pipe 5

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
103	ISP_PRE_6	LEVEL	isp_v2_clk	Pipe 6
104	ISP_PRE_7	LEVEL	isp_v2_clk	Pipe 7
105	ISP_PRE_8	LEVEL	isp_v2_clk	Pipe 8
106	ISP_PRE_9	LEVEL	isp_v2_clk	Pipe 9
107	ISP_DMA	LEVEL	isp_bus_clk	ISP DMA done
108	ISP_POST_0	LEVEL	isp_v2_clk	Pipe 0 mid/post (sof/eof/log_y done)
109	ISP_POST_1	LEVEL	isp_v2_clk	
110	ISP_POST_2	LEVEL	isp_v2_clk	
111	ISP_POST_3	LEVEL	isp_v2_clk	
112	ISP_POST_4	LEVEL	isp_v2_clk	
113	ISP_POST_5	LEVEL	isp_v2_clk	
114	ISP_POST_6	LEVEL	isp_v2_clk	
115	ISP_POST_7	LEVEL	isp_v2_clk	
116	ISP_POST_8	LEVEL	isp_v2_clk	
117	ISP_POST_9	LEVEL	isp_v2_clk	
118	AO_CIP1	LEVEL	GENERIC	
119	VE_SRAM_MERGE	LEVEL	ve_bus_clk	
120	VE_DDRC_MERGE	LEVEL	ve_bus_clk	
121	AV1	LEVEL	ve_bus_clk	
122	V4	LEVEL	ve_bus_clk	
123	JPG	LEVEL	ve_bus_clk	
124	V5	LEVEL	ve_bus_clk	
125	VIF0	LEVEL	d2_clk	vif0 error
126	VIF1	LEVEL	d2_clk	vif1 error
127	VIF2	LEVEL	d2_clk	vif2 error
128	USB_JPG_DPSYNC_ERROR	EDGE	img_ref_clk	
129	DP_DDRC_MERGE0	LEVEL	dp_bus_clk	
130	DP_DDRC_MERGE1	LEVEL	dp_bus_clk	
131	DP_SRAM_MERGE	LEVEL	dp_bus_clk	
132	DP_AO_SRAM_MERGE	LEVEL	dp_bus_clk	
133	SYNC_DP_OVF	LEVEL	dp_bus_clk	SYNC_DP_OVF
134	IDC	LEVEL	dp_bus_clk	
135	YSCALE0_SOF	EDGE	d2_clk	
136	YSCALE0_EOF	EDGE	d2_clk	
137	DCPC	LEVEL	dp_bus_clk	
138	MIPICIF0	LEVEL	d4_clk	mipicif snr0
139	MIPICIF1	LEVEL	d4_clk	mipicif snr1
140	MIPICIF2	LEVEL	d4_clk	mipicif snr2
141	MIPICIF3	LEVEL	d4_clk	mipicif snr3
142	OSD0	LEVEL	dp_bus_clk	
143	OSD1	LEVEL	dp_bus_clk	
144	GIR0	LEVEL	dp_bus_clk	RGBIR G/IR statistic channel 0
145	GIR1	LEVEL	dp_bus_clk	RGBIR G/IR statistic channel 1
146	HOGMD	LEVEL	dp_bus_clk	

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
147	IAA	LEVEL	dp_bus_clk	IAA
148	AUTOSCL	LEVEL	dp_bus_clk	Auto Scaler
149	YUVSCALE0	LEVEL	dp_bus_clk	
150	YUVSCALE1	LEVEL	dp_bus_clk	
151	YUVSCALE2	LEVEL	dp_bus_clk	
152	OSD2	LEVEL	dp_bus_clk	
153	OSD3	LEVEL	dp_bus_clk	
154	ECIF0	LEVEL	dp_bus_clk	
155	ECIF1	LEVEL	dp_bus_clk	
156	ECIF2	LEVEL	dp_bus_clk	
157	SFB0	LEVEL	dp_bus_clk	Simple FB0 IRQ
158	SFB1	LEVEL	dp_bus_clk	Simple FB1 IRQ
159	SFB2	LEVEL	dp_bus_clk	Simple FB2 IRQ
160	SFB3	LEVEL	dp_bus_clk	Simple FB3 IRQ
161	SFB4	LEVEL	dp_bus_clk	Simple FB4 IRQ
162	DCPC_MV	LEVEL	dp_bus_clk	
163	SFB_MV	LEVEL	dp_bus_clk	
164	YSCALE0	LEVEL	dp_bus_clk	
165	MIPICIF4	LEVEL	d4_clk	mipicif snr3
166	CB_SOF	EDGE	d4_clk	
167	CB_EOF	EDGE	d4_clk	
168	DCPC_DVP_SOF	EDGE	d2_clk	
169	DCPC_DVP_EOF	EDGE	d2_clk	
170	OSD0_EOF	EDGE	d2_clk	
171	OSD0_SOF	EDGE	d2_clk	
172	OSD1_EOF	EDGE	d2_clk	
173	OSD1_SOF	EDGE	d2_clk	
174	ECIF0_SOF	EDGE	d2_clk	
175	ECIF0_EOF	EDGE	d2_clk	
176	ECIF1_SOF	EDGE	d2_clk	
177	ECIF1_EOF	EDGE	d2_clk	
178	ECIF2_SOF	EDGE	d2_clk	
179	ECIF2_EOF	EDGE	d2_clk	
180	YUVSCALE0_SOF	EDGE	d2_clk	
181	YUVSCALE0_EOF	EDGE	d2_clk	
182	YUVSCALE1_SOF	EDGE	d2_clk	
183	YUVSCALE1_EOF	EDGE	d2_clk	
184	YUVSCALE2_SOF	EDGE	d2_clk	
185	YUVSCALE2_EOF	EDGE	d2_clk	
186	OSD2_EOF	EDGE	d2_clk	
187	OSD2_SOF	EDGE	d2_clk	
188	OSD3_EOF	EDGE	d2_clk	
189	OSD3_SOF	EDGE	d2_clk	
190	RGBIR0_P0_EOF	EDGE	v2_clk	
191	RGBIR0_P1_EOF	EDGE	v2_clk	

IRQ_ID	IRQ_NAME	Type	Clk Domain	Description
192	RGBIR1_P0_EOF	EDGE	v2_clk	
193	RGBIR1_P1_EOF	EDGE	v2_clk	
194	RGBIR0_IN0_SOF	EDGE	v2_clk	
195	RGBIR0_IN1_SOF	EDGE	v2_clk	
196	RGBIR1_IN0_SOF	EDGE	v2_clk	
197	RGBIR1_IN1_SOF	EDGE	v2_clk	
198	RGBIR0_P0_DONE	EDGE	v2_clk	
199	RGBIR0_P1_DONE	EDGE	v2_clk	
200	RGBIR1_P0_DONE	EDGE	v2_clk	
201	RGBIR1_P1_DONE	EDGE	v2_clk	
202	RAWSCL0_IN0_SOF	EDGE	v2_clk	rawscaler0 in channel 0 sof
203	RAWSCL0_P0_EOF	EDGE	v2_clk	rawscaler0 in channel 0 eof
204	RAWSCL1_IN0_SOF	EDGE	v2_clk	rawscaler1 in channel 0 sof
205	RAWSCL1_P0_EOF	EDGE	v2_clk	rawscaler1 in channel 0 eof
206	RAWSCL2_IN0_SOF	EDGE	v2_clk	rawscaler2 in channel 0 sof
207	RAWSCL2_P0_EOF	EDGE	v2_clk	rawscaler2 in channel 0 eof
208	RAWSCL3_IN0_SOF	EDGE	v2_clk	rawscaler3 in channel 0 sof
209	RAWSCL3_P0_EOF	EDGE	v2_clk	rawscaler3 in channel 0 eof
210	YUVSCALE_MV0	LEVEL	isp_bus_clk	
211	YUVSCALE_MV1	LEVEL	isp_bus_clk	
212	YUVSCALE_MV2	LEVEL	isp_bus_clk	
213	YUVSCALE_MV3	LEVEL	isp_bus_clk	
214	SFB_MV4	LEVEL	isp_bus_clk	
215	AO_CIP2	LEVEL	GENERIC	
216	AO_CIP3	LEVEL	GENERIC	
217	AO_GAMMA0	LEVEL	GENERIC	
218	AO_GAMMA1	LEVEL	GENERIC	
219	AO_GAMMA2	LEVEL	GENERIC	
220	AO_GAMMA3	LEVEL	GENERIC	
221	AO_AECAGC0	LEVEL	GENERIC	
222	AO_AECAGC1	LEVEL	GENERIC	
223	AO_AECAGC2	LEVEL	GENERIC	
224	AO_AECAGC3	LEVEL	GENERIC	
225	AO_IOC	LEVEL	GENERIC	

8 System Boot

For all functional bootmodes, TEST_MODE pin needs to tie to LOW.

8.1 Boot Modes

BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	Boot Description
0	0	0	Boot from Serial NOR Flash (master mode)
0	0	1	Boot from SCIF
0	1	0	Boot from UART1
0	1	1	Boot from SIF2 (slave mode)
1	0	0	Boot from USB
1	0	1	Boot from NAND Flash
1	1	0	Boot from Serial NAND Flash
1	1	1	Reserved

8.2 Boot Up Time

Boot up time (power up to first frame encoded) should be less than 60ms.

8.3 Boot Flow

8.3.1 Main BA22

BA22 is always the first to be boot up upon powered-up. The boot sequence of main BA22 is as follows:

- BA22 reset vector (boot address) is 0x0001_FF00, which is remapped to BOOTROM region (0x0000_0000 to 0x0002_0000, 128KB)
- This boot vector can point to somewhere in the BOOTROM (e.g. 0X0000_2000)
- Write SRAM jump vectors at 0x1001_FF00 (or 0x9001_FF00). The jump vectors need to point to our executable in SRAM
- Change SC.BA22_BOOT_SEL to SRAM
- Trigger self-reset to BA22. Upon reset, BA22 would boot from 0x1001_FF00, and jump to executable.
- Default executable reserved region is 0x1000_0000 to 0x1006_1000.
- Note: 0x0000_0000 and 0x1000_0000 needs to be reserved for A32MP boot vectors, as A32MP can only boot from these 2 locations.

8.3.2 A32

After main BA22 is boot-up, A32 can be boot up as follows:

- Setup CPU clocks, using main BA22
- Download executable to SRAM or DDR, using main BA22
- Set A32 boot select in SC.CPU_BOOT_SEL (ROM, SRAM or DDR), using main BA22
- Release A32 reset (can be 1 core or multiple)
- A32 cores boot from 0x0 (remapped to ROM, SRAM, DDR according to boot select), then upon checking CPUIP, jump to their executable.

8.3.3 AO_BA22

After main BA22 is boot-up, AO_BA22 can be boot up as follows:

- Setup AO_BA22 clocks, using main BA22
- Download executable to AO_SRAM, using main BA22
- Release AO_BA22 reset
- AO_BA22 boot from 0x0067_FF00, then jump to executable

9 Power Domains

9.1 Power Up

a) There is no on-chip POR circuit. The reset is controlled by external through a pin, RESET.

b) During power up, only the reference clock is running in the chip. The boot ROM would based on IPL (initial program loading) to program the PLL to the desired the frequency.

9.2 Power Supplies

Power	Min (V)	Typ (V)	Max (V)	Description
VDD_AO	0.855	0.9	0.945	Digital circuit core power for ISLAND_0 domain
VDD_TOP	0.855	0.9	0.945	Digital circuit core power for ISLAND_1 domain
VDD_CORE	0.855	0.9	0.945	Digital circuit core power for CORE domain
VDD_CPU	0.855	0.9	0.945	Digital circuit core power for CPU domain
VDD_NPU	0.855	0.9	0.945	Digital circuit core power for NPU domain
VDD_AV1	0.855	0.9	0.945	Digital circuit core power for AV1 domain
VDD_V5	0.855	0.9	0.945	Digital circuit core power for V5 domain
DDR_DVDD	0.81	0.9	0.99	DDR circuit core power
CVDD_MIPIRX	0.81	0.9	0.99	MIPI RX circuit core power
CVDD_MIPITX	0.81	0.9	0.99	MIPI TX circuit core power
CVDD_USB	0.81	0.9	0.99	USB device circuit core power
DDR_VDDQ	1.425	1.5	1.575	DDR3IO power
	1.28	1.35	1.45	DDR3L IO power
	1.14	1.2	1.30	LPDDR2 IO power
PVDD_MIPIRX	1.62	1.8	1.98	MIPI RX analog circuit power
PVDD_MIPITX	1.62	1.8	1.98	MIPI TX analog circuit power
AVDD_USB	1.62	1.8	1.98	USB device analog circuit power
DDR_PLL_AVDD	1.62	1.8	1.98	DDR PLL analog circuit power
VREF1/VREF2	1.62	1.8	1.98	IO Reference Power
VDDA_AO	1.62	1.8	1.98	AO Domain Analog Power
VDDIO_AO	1.62 2.8	1.8 3.3	1.98 3.6	AO Domain IO pin power

VDDIO_AOLRX	0.72	0.76	0.8	AOLINK IO Power
VDDIO_SCIF	1.62 2.8	1.8 3.3	1.98 3.6	SCIF IO pin power
VDDIO_NAND	1.62 2.8	1.8 3.3	1.98 3.6	NAND flash, I2S and JTAG IO pin power
VDDIO_LCD	1.62 2.8	1.8 3.3	1.98 3.6	LCD and DVP output IO pin power
VDDIO_COM	1.62 2.8	1.8 3.3	1.98 3.6	SPI1, SPI2, and SPI3 IO pin power
VDDIO_PER	1.62 2.8	1.8 3.3	1.98 3.6	Peripheral IO pin power

9.3 Power Scheme

There are 5 different power modes:

- Stage 0 (Power Down)
- Stage 0.01 (Standby Mode for Instant On/Off)
- Stage 0.2 (Advanced 2nd Stage AO Video)
- Stage 0.3 (Stripping Full Operation)
- Stage 1.0 (Full Operation)

On power up, it would always be in Stage 0.2, as the main BA22 resides in VDD_TOP power domain, not in VDD_AO power domain.

9.3.1 Stage 0.01

In this mode, only ISLAND_0 is powered on, which should consume power of <1mW. It is entered from either Stage 0.2, Stage 0.3 or Stage 1.0 power mode. It exits to Stage 0.2 power mode, when it is woken up by external PIR/MCU, or external AOP processor (E.g. OA7600). It can also exit to Stage 0, power down mode.

9.3.2 Stage 0.2

In this mode, both ISLAND_0 and ISLAND_1 is powered on. But within ISLAND_1, the VDD_CORE remains shut-down. This stage is used to capture always-on video (pre-roll frames) from AOLRX or MIPIRX from sensors. It should consumes power of <15mW for 3 sensors x 720p@5fps using AOLRX. It can be entered from power-down mode, or Stage 0.01 when woken up by external PIR/MCU, or external AOP processor (E.g. OA7600). It can also be entered from Stage 1.0, to monitor for events. If events are detected, it would transit to Stage 0.3. Otherwise, it can either remain in this stage, or exit to Stage 0, power down.

9.3.3 Stage 0.3

In this mode, both ISLAND_0 and ISLAND_1 is powered on. Within ISLAND_1, the VDD_CORE is powered up

as well. But within the VDD_CORE domain, VDD_CPU, VDD_AV1, VDD_V5 and VDD_NPU remains powered off. The full ISP in the VDD_CORE domain is turned on to process the video frames from sensors, for more accurate event recognition. IMG is turned on to encode the videos during this stage. This stage is entered from Stage 0.2. If there are threat events, it would transit to Stage 1.0 for full operation. Otherwise, it can transit back to Stage 0.2 for more monitoring, or exit to Stage 0, power-down mode.

9.3.4 Stage 1.0

In this mode, both ISLAND_0 and ISLAND_1 is powered on. Within ISLAND_1, the VDD_CORE is powered up as well. And within the VDD_CORE domain, VDD_CPU is powered up as well. VDD_AV1, VDD_V5 and VDD_NPU can be powered on according to the use-case requirements. It is entered from Stage 0.3. When there are no more events, it can transits back to Stage 0.2, Stage 0.01 or exit to Stage 0, power-down mode.

10 Clock Domains

10.1 ISLAND_0 (AOCORE)

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ao_ba22_clk	120	24
ao_ba22_pm_clk	120	3
ao_bus_clk	120	24
ao_csram_clk	333	24
ao_ioc_bus_clk	120	0
ao_jtag_clk	120	30
ao_sram_ctrl_bus_clk	120	0
ao_sram_grfc_merge_clk	333	333
ao_sram_grfc_merge_div2_clk	167	166
ao_timer_ref_clk	120	24
ba22_jtag_clk	120	30
ba_irqc_bus_clk	120	0
bus_clk	200	200
cpu_jtag_clk	120	30
mbox_bus_clk	120	0
osc_clk	120	120
rtc_clk	24	1
rtc_bus_clk	120	0
sboot_jtag_clk	120	30
sif3_bus_clk	120	0
sif3_pad_clk	120	100
sif3_ref_clk	120	30
timer5_bus_clk	120	0
timer6_bus_clk	120	0
uart1_bus_clk	120	0
wdt_bus_clk	120	24
y_clk	120	120

10.2 ISLAND_1 (TOP)

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ac_clk	100	125
ac_bus_clk	200	0
ai0_ref_clk	100	0
ai1_ref_clk	100	0
ai_arbiter_ref_clk	100	0
ai_bus_clk	200	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ai_m_clk	100	24
ao_aecagc0_bus_clk	200	0
ao_aecagc0_d1_clk	100	0
ao_aecagc1_bus_clk	200	0
ao_aecagc1_d1_clk	100	0
ao_aecagc2_bus_clk	200	0
ao_aecagc2_d1_clk	100	0
ao_aecagc3_bus_clk	200	0
ao_aecagc3_d1_clk	100	0
ao_bus_clk	200	0
ao_cip0_bus_clk	200	0
ao_cip0_d1_clk	100	0
ao_cip1_bus_clk	200	0
ao_cip1_d1_clk	100	0
ao_cip2_bus_clk	200	0
ao_cip2_d1_clk	100	0
ao_cip3_bus_clk	200	0
ao_cip3_d1_clk	100	0
ao_d1_clk	100	12
ao_d2_clk	100	12
ao_d4_clk	100	12
ao_ecif_bus_clk	200	0
ao_ecif_fast_mem_clk	200	0
ao_fast_d1_clk	200	12
ao_fast_d4_clk	100	12
ao_fast_mem_clk	200	12
ao_gamma0_bus_clk	200	0
ao_gamma0_d1_clk	100	0
ao_gamma1_bus_clk	200	0
ao_gamma1_d1_clk	100	0
ao_gamma2_bus_clk	200	0
ao_gamma2_d1_clk	100	0
ao_gamma3_bus_clk	200	0
ao_gamma3_d1_clk	100	0
ao_md0_bus_clk	200	0
ao_md0_d2_clk	100	0
ao_md1_bus_clk	200	0
ao_md1_d2_clk	100	0
ao_md2_bus_clk	200	0
ao_md2_d2_clk	100	0
ao_md3_bus_clk	200	0
ao_md3_d2_clk	100	0
ao_mem_clk	200	12
ao_mem0_clk	200	0
ao_mem1_clk	200	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ao_mem2_clk	200	0
ao_mem3_clk	200	0
ao_raw_dec_bus_clk	200	0
ao_raw_dec_mem_clk	200	0
ao_raw_enc0_bus_clk	200	0
ao_raw_enc0_d1_clk	100	0
ao_raw_enc0_mem_clk	200	0
ao_raw_enc1_bus_clk	200	0
ao_raw_enc1_d1_clk	100	0
ao_raw_enc1_mem_clk	200	0
ao_raw_enc2_bus_clk	200	0
ao_raw_enc2_d1_clk	100	0
ao_raw_enc2_mem_clk	200	0
ao_raw_enc3_bus_clk	200	0
ao_raw_enc3_d1_clk	100	0
ao_raw_enc3_mem_clk	200	0
ao_raw_enc4_bus_clk	200	0
ao_rawscl_bus_clk	200	0
ao_sfb0_bus_clk	200	0
ao_sfb0_d1_clk	100	0
ao_sfb0_d2_clk	100	0
ao_sfb0_d4_clk	100	0
ao_sfb0_mem_clk	200	0
ao_sfb1_bus_clk	200	0
ao_sfb1_d1_clk	100	0
ao_sfb1_d2_clk	100	0
ao_sfb1_d4_clk	100	0
ao_sfb1_mem_clk	200	0
ao_sfb2_bus_clk	200	0
ao_sfb2_d1_clk	100	0
ao_sfb2_d2_clk	100	0
ao_sfb2_d4_clk	100	0
ao_sfb2_mem_clk	200	0
ao_sfb3_bus_clk	200	0
ao_sfb3_d1_clk	100	0
ao_sfb3_d2_clk	100	0
ao_sfb3_d4_clk	100	0
ao_sfb3_mem_clk	200	0
ao_sram_clk	333	24
ao_sram_cont_clk	333	24
ao_sram_div2_clk	167	12
ao_tst_clk	100	24
ao_y_clk	24	24
ao_yuvscl0_bus_clk	200	0
ao_yuvscl0_d2_clk	100	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ao_yuvscl1_bus_clk	200	0
ao_yuvscl1_d2_clk	100	0
ao_yuvscl2_bus_clk	200	0
ao_yuvscl2_d2_clk	100	0
ao_yuvscl3_bus_clk	200	0
ao_yuvscl3_d2_clk	100	0
aolrx0_bus_clk	200	0
aolrx0_d1_clk	100	0
aolrx0_phy_clk	100	100
aolrx1_bus_clk	200	0
aolrx1_d1_clk	100	0
aolrx1_phy_clk	100	100
aolrx2_bus_clk	200	0
aolrx2_d1_clk	100	0
aolrx2_phy_clk	100	100
aolrx3_bus_clk	200	0
aolrx3_d1_clk	100	0
autoscl_clk	400	12
av1_clk	330	12
ba22_clk	800	24
ba22_bus_clk	400	12
ba22_cont_clk	800	24
ba22_jtag_clk	30	30
ba22_pm_clk	400	12
bus_clk	200	24
cb_bus_clk	200	0
cpu_clk	1000	24
cpu_bus_clk	500	24
cpu_per_clk	500	12
crp_clk	400	24
crp_bus_clk	200	0
crp_ddr_clk	400	24
crp_sram_clk	400	24
d1_clk	860	24
d2_clk	430	12
d4_clk	430	12
dcpc_clk	500	12
ddr_clk	933	933
ddr_div2_clk	467	466
ddr_div2_c0_clk	467	466
ddr_div2_c1_clk	467	466
ddr_div2_dp_clk	467	466
ddr_div2_dp_cont_clk	467	466
ddr_div2_isp_clk	467	466
ddr_div2_isp_cont_clk	467	466

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ddr_div2_va_clk	467	466
ddr_div2_va_cont_clk	467	466
ddr_div2_ve_clk	467	466
ddr_div2_ve_cont_clk	467	466
ddr_div4_clk	234	233
ddr_div4_c0_clk	234	233
ddr_div4_c1_clk	234	233
ddr_div4_dp_clk	234	233
ddr_div4_isp_clk	234	233
ddr_div4_va_clk	234	233
ddr_div4_ve_clk	234	233
ddrc_bus_clk	200	24
dm0_ref_clk	100	0
dm1_ref_clk	100	0
dm2_ref_clk	100	0
dm3_ref_clk	100	0
dma_bus_clk	200	0
dma_mbus_clk	400	24
dp_bus_clk	200	0
dvp_bus_clk	200	0
dvp_vfifo_clk	300	0
ecif_clk	600	24
fb_clk	600	24
gunzip_bus_clk	200	0
gunzip_ref_clk	600	24
iaa_clk	400	12
idc_isp_v2_clk	430	12
img_ref_clk	400	24
img_vp_clk	400	24
ioc_bus_clk	200	24
irqc_ba22_bus_clk	200	0
isp_bus_clk	400	0
isp_dma_clk	400	0
isp_v2_clk	430	12
jtag_clk	30	30
mbus_clk	400	24
md_clk	334	24
mipirx00_d4_clk	430	0
mipirx01_d4_clk	430	0
mipirx0_d4_clk	430	0
mipirx10_d4_clk	430	0
mipirx11_d4_clk	430	0
mipirx1_d4_clk	430	0
mipirx25_s0_phy_clk	313	313
mipirx25_s1_phy_clk	313	313

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
mipirx25_s2_phy_clk	313	313
mipirx25_s3_phy_clk	313	313
mipirx_s0_phy_clk	300	187
mipirx_s1_phy_clk	300	187
mipirxh_bus_clk	200	0
mipirxl_bus_clk	200	0
mipitx_bus_clk	200	0
mipitx_p_clk	187	0
mipitx_s_clk	300	0
nand_bus_clk	200	0
nand_ref_clk	400	24
nand_s_clk	240	24
npu_clk	600	24
npu_grfc_clk	400	12
otp_clk	400	12
otp_bus_clk	200	0
pvt_y_clk	24	0
pwm_bus_clk	200	0
pwm_ref_clk	200	24
rom_clk	500	24
sboot_clk	400	12
sboot_bus_clk	200	0
sboot_jtag_clk	30	30
sboot_jtag_inv_clk	30	30
sccbm0_clk	120	12
sccbm0_bus_clk	200	0
sccbm1_clk	120	12
sccbm1_bus_clk	200	0
sccbm2_clk	120	12
sccbm2_bus_clk	200	0
sccbm3_clk	120	12
sccbm3_bus_clk	200	0
scif_bus_clk	200	0
scif_ref_clk	200	24
scio0_ref_clk	200	24
scio_bus_clk	200	0
sensor_clk	100	24
sfc_bus_clk	200	0
sfc_ref_clk	600	12
sif0_bus_clk	200	0
sif0_ref_clk	600	12
sif1_bus_clk	200	0
sif1_ref_clk	600	12
sif2_bus_clk	200	0
sif2_ref_clk	600	12

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
sign_bus_clk	200	0
sign_ddr_clk	400	12
sign_sram_clk	400	12
sjtag_bus_clk	200	0
spi1_bus_clk	200	0
spi1_ref_clk	600	12
spi2_bus_clk	200	0
spi2_ref_clk	600	12
spi3_bus_clk	200	0
spi3_ref_clk	600	12
spi4_bus_clk	200	0
spi4_ref_clk	600	12
sram_clk	400	24
sram_bus_clk	200	24
sram_c0_clk	400	24
sram_div2_clk	200	12
sram_div2_c0_clk	200	12
sram_div2_dp_clk	200	12
sram_div2_va_clk	200	12
sram_div2_ve_clk	200	12
sram_dp_clk	400	24
sram_dp_cont_clk	400	24
sram_va_clk	400	24
sram_va_cont_clk	400	24
sram_ve_clk	400	24
sram_ve_cont_clk	400	24
timer0_bus_clk	200	0
timer1_bus_clk	200	0
timer2_bus_clk	200	0
timer3_bus_clk	200	0
timer4_bus_clk	200	0
timer_ref_clk	200	24
uart0_bus_clk	200	0
uart1_bus_clk	200	0
uart2_bus_clk	200	0
usb_app_clk	120	120
usb_phy_clk	30	30
usb_ref_clk	125	24
usbd_bus_clk	200	0
usbd_per_bus_clk	200	0
v2_clk	430	12
v2d2_d2_clk	430	0
v4_clk	500	12
v5_clk	300	12
va_bus_clk	200	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ve_bus_clk	200	0
vfifo_clk	300	0
vfifo_bus_clk	200	0
vfifo_d2_clk	430	0
vif_d2_clk	430	0
wdt_bus_clk	200	24
y_clk	24	24

10.3 ISLAND_1 (DPCORE)

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ao_sram_grfc_merge_clk	333	333
ao_sram_grfc_merge_div2_clk	167	166
autoscl_clk	400	400
autoscl_bus_clk	200	0
bus_clk	200	200
cb_bus_clk	200	0
cb_d4_clk	430	0
d1_clk	720	720
d2_clk	430	430
d2_vfifo_clk	430	0
d2_vif0_clk	430	0
d2_vif1_clk	430	0
d2_vif2_clk	430	0
d4_clk	430	430
dbg_isp_d2_clk	430	0
dcpc0_clk	500	0
dcpc1_clk	500	0
dcpc_bus_clk	200	0
dcpc_d2_clk	430	0
dcpc_dvp_clk	500	0
dcpc_mv_clk	500	0
dcpc_mv_bus_clk	200	0
dcpc_mv_d2_clk	500	0
ddrc_grfc_merge_clk	467	467
ddrc_grfc_merge_div2_clk	234	233
dp_ao_sram_merge_bus_clk	200	0
dp_bus_clk	200	200
dp_ctrl_bus_clk	200	0
dp_ddrc_merge_bus_clk	200	0
dp_sram_merge_bus_clk	200	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
ecif0_bus_clk	200	0
ecif0_d2_clk	430	0
ecif0_mem_clk	600	0
ecif1_bus_clk	200	0
ecif1_d2_clk	430	0
ecif1_mem_clk	600	0
ecif2_bus_clk	200	0
ecif2_d2_clk	430	0
ecif2_mem_clk	600	0
ecif_fb_clk	600	0
gir0_bus_clk	200	0
gir0_v2_clk	430	0
gir1_bus_clk	200	0
gir1_v2_clk	430	0
iaa_clk	400	400
iaa_bus_clk	200	0
idc_bus_clk	200	0
idc_v2_clk	430	0
ipwl0_v2_clk	430	0
ipwl1_v2_clk	430	0
ipwl2_v2_clk	430	0
ipwl3_v2_clk	430	0
isp_d2_clk	430	430
isp_v2_clk	430	430
md_clk	334	334
md_bus_clk	200	0
md_d2_clk	430	0
mipicif0_d2_clk	430	0
mipicif0_d4_clk	430	0
mipicif0_rx_d4_clk	430	0
mipicif0_v2_clk	430	0
mipicif1_d2_clk	430	0
mipicif1_d4_clk	430	0
mipicif1_rx_d4_clk	430	0
mipicif1_v2_clk	430	0
mipicif2_d2_clk	430	0
mipicif2_d4_clk	430	0
mipicif2_rx_d4_clk	430	0
mipicif2_v2_clk	430	0
mipicif3_d2_clk	430	0
mipicif3_d4_clk	430	0
mipicif3_rx_d4_clk	430	0
mipicif3_v2_clk	430	0
mipicif4_d2_clk	430	0
mipicif4_d4_clk	430	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
mipicif4_v2_clk	430	0
mipicif_bus_clk	200	0
mipicif_d2_clk	430	0
mipicif_d4_clk	430	0
mipirxh_rx2_d4_clk	430	430
mipirxh_rx3_d4_clk	430	430
mipirxl_rx0_d4_clk	430	430
mipirxl_rx1_d4_clk	430	430
osd0_bus_clk	200	0
osd0_d2_clk	430	0
osd1_bus_clk	200	0
osd1_d2_clk	430	0
osd2_bus_clk	200	0
osd2_d2_clk	430	0
osd3_bus_clk	200	0
osd3_d2_clk	430	0
pvt_y_clk	24	0
rawscaler0_v2_clk	430	0
rawscaler1_v2_clk	430	0
rawscaler2_v2_clk	430	0
rawscaler3_v2_clk	430	0
rawscl0_bus_clk	200	0
rawscl1_bus_clk	200	0
rawscl2_bus_clk	200	0
rawscl3_bus_clk	200	0
rgbir0_bus_clk	200	0
rgbir0_d2_clk	430	0
rgbir0_d4_clk	430	0
rgbir0_v2_clk	430	0
rgbir1_bus_clk	200	0
rgbir1_d2_clk	430	0
rgbir1_d4_clk	430	0
rgbir1_v2_clk	430	0
rgbir_rawscl_bus_clk	200	0
sfb0_bus_clk	200	0
sfb0_dvp_clk	430	0
sfb0_mem_clk	600	0
sfb1_bus_clk	200	0
sfb1_dvp_clk	430	0
sfb1_mem_clk	600	0
sfb2_bus_clk	200	0
sfb2_dvp_clk	430	0
sfb2_mem_clk	600	0
sfb3_bus_clk	200	0
sfb3_dvp_clk	430	0

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
sfb3_mem_clk	600	0
sfb4_bus_clk	200	0
sfb4_dvp_clk	430	0
sfb4_mem_clk	600	0
sfb_d2_clk	430	0
sram_clk	400	400
sram_grfc_merge_clk	400	400
sram_grfc_merge_div2_clk	200	200
stitch_clk	500	0
stitch_byp_clk	500	0
usb_app_clk	120	120
usb_uvc_d1_clk	720	0
v2_clk	430	430
v2d20_d2_clk	430	0
v2d21_d2_clk	430	0
v2d22_d2_clk	430	0
v2d23_d2_clk	430	0
v2d24_d2_clk	430	0
v2d2_d2_clk	430	0
vfifo_d2_clk	430	0
vif0_d2_clk	430	0
vif1_d2_clk	430	0
vif2_d2_clk	430	0
y_clk	24	24
yscaler0_bus_clk	200	0
yscaler0_d2_clk	430	0
yuvscaler0_bus_clk	200	0
yuvscaler0_d2_clk	430	0
yuvscaler1_bus_clk	200	0
yuvscaler1_d2_clk	430	0
yuvscaler2_bus_clk	200	0
yuvscaler2_d2_clk	430	0

10.4 ISLAND_1 (ISPCORE)

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
bus_clk	200	200
dbg_isp_v2_clk	430	0
ddrc_grfc_merge_clk	467	467
ddrc_grfc_merge_div2_clk	234	233
idc_isp_v2_clk	430	430
isp_bus_clk	400	400

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
isp_ctrl_bus_clk	400	0
isp_dbg_d2_clk	430	0
isp_ddrc_merge_bus_clk	400	0
isp_dma_clk	400	0
isp_top_bus_clk	400	0
isp_v2_clk	430	430
pvt_y_clk	24	0
rawdns_isp_v2_clk	430	0
sfb_mv_bus_clk	400	0
sfb_mv_d2_clk	430	0
sfb_mv_mem_clk	467	0
v2d20_d2_clk	430	0
v2d20_isp_v2_clk	430	0
v2d21_d2_clk	430	0
v2d21_isp_v2_clk	430	0
v2d2x_d2_clk	430	430
y_clk	24	24
yuvscaler_mv0_bus_clk	400	0
yuvscaler_mv0_d2_clk	430	0
yuvscaler_mv1_bus_clk	400	0
yuvscaler_mv1_d2_clk	430	0
yuvscaler_mv2_bus_clk	400	0
yuvscaler_mv2_d2_clk	430	0
yuvscaler_mv3_bus_clk	400	0
yuvscaler_mv3_d2_clk	430	0

10.5 ISLAND_1 (VECORE)

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
av1_clk	330	330
av1_bus_clk	200	0
bus_clk	200	200
d2_clk	430	430
ddrc_grfc_merge_clk	467	467
ddrc_grfc_merge_div2_clk	234	233
img_bus_clk	200	0
img_ref_clk	400	400
img_vp_clk	400	400
pvt_y_clk	24	24
sram_grfc_merge_clk	400	400
sram_grfc_merge_div2_clk	200	200
usb_app_clk	120	120

Clk Name	Max Frequency (MHz)	Por Frequency (MHz)
v4_clk	500	500
v4_bus_clk	200	0
v5_clk	300	300
v5_bus_clk	200	0
ve_bus_clk	200	200
ve_ctrl_bus_clk	200	0
ve_ddrc_merge_bus_clk	200	0
ve_sram_merge_bus_clk	200	0
vif0_bus_clk	200	0
vif0_d2_clk	430	0
vif1_bus_clk	200	0
vif1_d2_clk	430	0
vif2_bus_clk	200	0
vif2_d2_clk	430	0
y_clk	24	24

10.6 ISLAND_1 (VACORE)

Rst Name	Rst input	Clk_sync	SCRM Control
bus_rst_n	sys_rst_n	bus_clk	
cpu_bus_rst_n	sys_rst_n	cpu_bus_clk	BIT2@0x70
ddrc_grfc_merge_div2_rst_n	sys_rst_n	ddrc_grfc_merge_div2_clk	BIT3@0x70
hw_rst_dp_rst_n	hw_rst_n	va_bus_clk	
npu_rst_n	sys_rst_n	npu_clk	BIT6@0x70
npu_bus_rst_n	sys_rst_n	npu_bus_clk	BIT7@0x70
npu_grfc_rst_n	sys_rst_n	npu_grfc_clk	
npu_grfc_sram_rst_n	sys_rst_n	npu_grfc_sram_clk	BIT14@0x70
npu_sga_rst_n	sys_rst_n	npu_sga_clk	BIT15@0x70
pvt_y_rst_n	hw_rst_n	pvt_y_clk	
sram_grfc_merge_div2_rst_n	sys_rst_n	sram_grfc_merge_div2_clk	BIT12@0x70
sys_rst_dp_rst_n	sys_rst_n	va_bus_clk	
va_bus_rst_n	sys_rst_n	va_bus_clk	
va_ctrl_bus_rst_n	sys_rst_n	va_ctrl_bus_clk	BIT10@0x70
va_ddrc_merge_bus_rst_n	sys_rst_n	va_ddrc_merge_bus_clk	BIT11@0x70
va_sram_merge_bus_rst_n	sys_rst_n	va_bus_clk	BIT13@0x70
y_rst_n	hw_rst_n	y_clk	

10.7 Clock Diagrams

The clock diagrams can be found at $HW/doc/spec/r6/sc/svg folder.

11 DFT Requirements (To Be Updated)

11.1 Pad loading from ATE Test

PAD loading supports maximum 50pf (TBD) for test machine at 1.7V~3.6V.

11.2 Package Simulation

Production team will validate the package design by simulation before taping out the product. RLC was extracted from package group and run simulation especially DDR PHY.

11.3 Scan Test

There would be 5 separate test modes for scan tests, to test NPU, V4, ISP and RGBIR and rest of the chip logic. The separation is based on chip physical design partitioning, and allows optimal scan chain length per hard-macro to optimize test time. Note that MPU and CPU core are physical partitions as well, but due to their smaller size, they are tested as part of chip-level sea-of-cell logic.

In each scan test mode, there are (TBD) compressed scan chains that can shift/capture at minimum of 24MHz. As there are multiple functional clock domains in the chip that are asynchronous to each other, multiple scan clocks are defined correspondingly. Due to pins availability limitation, not all function clock domains have its dedicated scan clock pin. There would be functional clock domains that need to share the same clock pins. The sharing would be such that there is no functional paths between the functional clock domains. For functional clock domains that talks to each other, using separate scan clocks allow adjustment of the scan clocks at ATPG/ATE level, to avoid race condition during the capture phase.

11.4 At-speed Test

At speed test along with scan test and just switch to functional cycle at speed. Its speed ranges from 24MHz to 800MHz-1GHz depends on the module speed.

11.5 Memory BIST

Memory Built-In-Self-Test (MBIST) logic will be inserted into the design by EDA tools for applying and observing patterns written into targeted memory, and the MBIST logic can be accessed via the JTAG macro controller. With this scheme, it allows for some level of scheduling and algorithm selection through program load and acquisition of diagnostic failure data.

BIST with repair is added because the total SRAM size is greater than 16Mb size, as required by TSMC redundancy free rules. eFuse would be used to store the repair information per chip.

To ensure no IR drop issue during memory BIST, the MBIST power consumption should be targeted to be 70% of functional power consumption.

11.6 PLL Test

The PLL clocks are divided down to a slow clock and output to pad for measurement in a functional test.

11.7 SD/SDIO Test

Support BIST internal and external loop-back testing for production test.

11.8 DDR PHY Test

DDR PHY will be tested in 2 ways. One is using the internal scan logic to test digital portion of DDR PHY. This would be a wrapped scan core (i.e. the scan test are encapsulated in the DDR PHY macro).

The other way is using BIST loopback to test it by comparing the read data pattern with the expected data pattern. In loopback test mode, the TX and RX are enabled at the same time. The writing data is fed back to the receiver, and the 90 degree shift for DQS is disabled. The command and address lines would be loop back to check the correctness as well.

~~The other is to use external DRAM device to test the read and write operation.~~

11.9 MIPI RX/TX PHY Test

MIPI RX and TX PHY are tested by doing external loopback and have TX generating PRBS pattern. Since there are 1x2 lanes TX and 2x2 lanes RX, one TX would fan out to two RX. It is important that the MIPI pins are NOT connected to test channels.

11.10 USB2.0 PHY Test

USB2.0 PHY is tested by two methods. The digital portion would be tested by scan logic, unwrapped (i.e. the scan tests are part of chip-level sea-of-cells logic). The other test is to perform internal BIST loopback. It is important that the USB DP/DM pins are NOT connected to test channels.

11.11 IDDQ/Pin-leakage Test

A functional pattern would be used to put the chip into reset and put all pins to tristate mode. This is to measure IDDQ and pin-leakage.

11.12 IDDA Test

A typical usecase functional pattern would be used for IDDA measurement.

11.13 Burn-in Test

To have high coverage in terms of the number of nodes switching between high and low during burn-in duration, and also to minimize the number of components and setup requirement for high-temperature burn-in board, on chip scan chains would be used to create the switching.

The board would provide 32kHz oscillator clock and the chip would generate a 1Hz output to be fed-back into the chip as scan clock, scan data input. The chip would output a 1 Hz toggling to drive external LED. The LED

blinking would then be used to indicate the chip is still alive during burn-in.

As scan and MBIST cannot be run concurrently, this method of burn-in requires 2 separates burn-in for memories and logic.

After the burn-in, the chips need to be moved to ATE for screening to check for damages. This would require socketed burn-in boards, which can be expensive.