

ToorCamp 2014

Secure Boot, Network Boot, Verified Boot, oh my

Vincent Zimmer

Usual disclaimer-

These foils and opinions are mine and not necessarily those of my employer

Agenda

History

UEFI Overview

Secure boot

Network boot

Coreboot

Verified boot

Building it

Testing it

Background

ToorCamp 2012

- Talked about UEFI Secure boot in 2012
- New features, new ecosystem
- Open core/closed platform

ToorCamp 2014

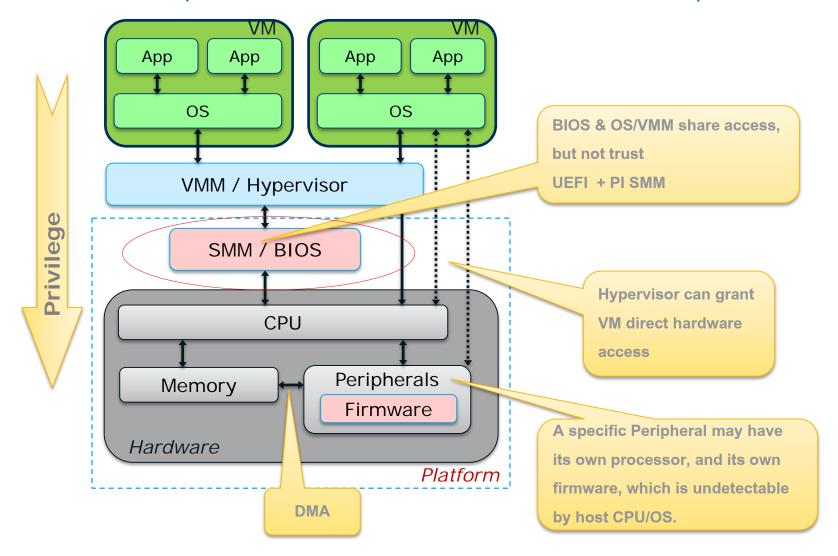
- Shipped several generations on UEFI
- More open platforms, ARM32/64 added, other fw

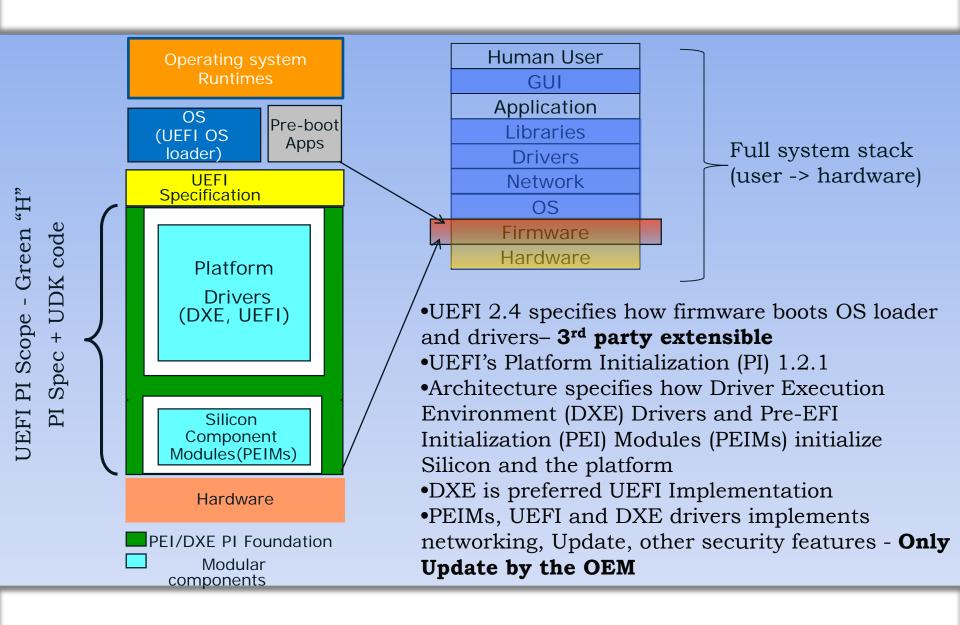
Challenge

More attacks, more defenses, more scale

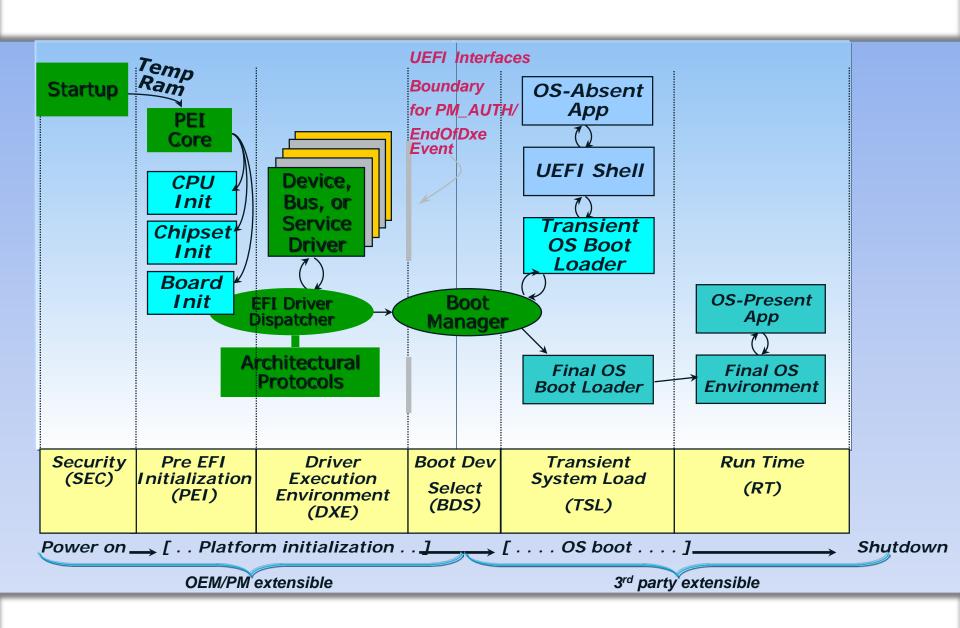
A reminder from the KGB school of cipher security: "You never attack the standard, you attack the implementation, including the process." - Grugq

Where are we (BIOS / UEFI firmware / Coreboot)?



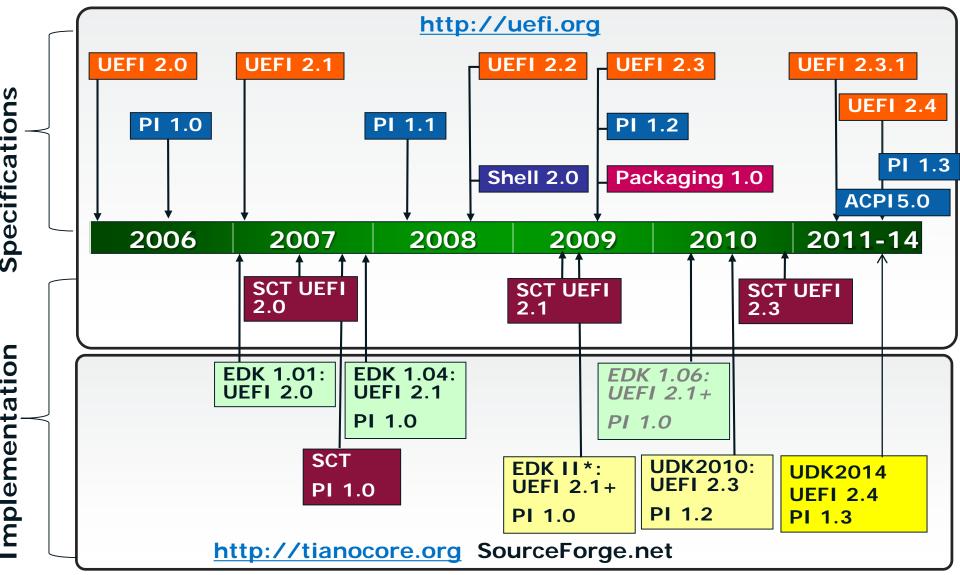


Stacking UEFI – Platform Initialization (PI)



Overall UEFI Boot Timeline

Specification & Tianocore.org Timeline



All products, dates, and programs are based on current expectations and subject to change without notice.

Industry BIOS Transition

Pre-2000

All Platforms BIOS were proprietary

2000

Intel invented the Extensible Firmware Interface (EFI) and provided sample implementation under free BSD terms

2004

tianocore.org, open source EFI community launched

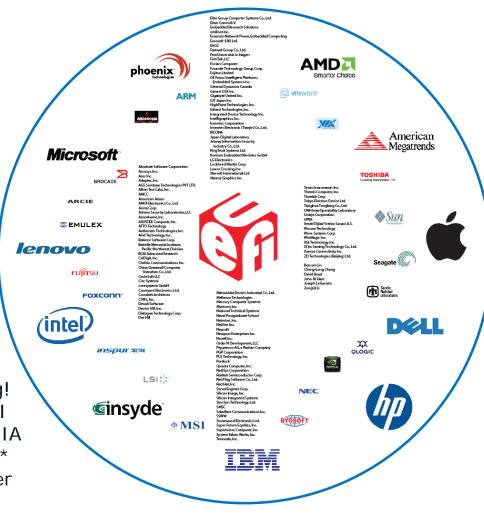
2005

Unified EFI (UEFI)

Industry forum, with 11 members, was formed to standardize FFI

2014

240 members and growing!
Major MNCs shipping; UEFI
platforms crossed most of IA
worldwide units; Microsoft*
UEFI x64 support in Server
2008, Vista* and Win7*;
RedHat* and SuSEI* OS
support. Mandatory for
Windows 8 client. ARM 32 and
64 bit support. ACPI added.



How to build UEFI? UDK2014

Industry Standards Compliance

• UEFI 2.0, UEFI 2.1, UEFI 2.2, UEFI 2.3, UEFI 2.4; PI 1.0, PI 1.1, PI 1.2, PI 1.3, ACPI 1.0-5.0

Extensible Foundation for Advanced Capabilities

- Pre-OS Security
- Rich Networking
- Manageability

Support for UEFI Packages

• Import/export modules source/binaries to many build systems

Maximize Re-use of Source Code **

- Platform Configuration Database (PCD) provides "knobs" for binaries
- ECP provides for reuse of EDK1117 (EDK I) modules
- · Improved modularity, library classes and instances
- · Optimize for size or speed

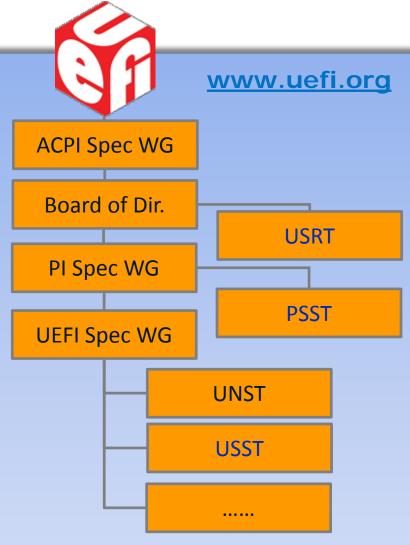
Multiple Development Environments and Tool Chains**

- Windows, Linux, OSX
- VS2003, VS2005, WinDDK, Intel, GCC

Fast and Flexible Build Infrastructure **

- 4X+ Build Performance Improvement (vs EDKI)
- Targeted Module Build Flexibility

Maximize the open source at www.tianocore.org



UNST

- UEFI Network Sub-Team
- Chaired by Vincent Zimmer (Intel)
- Responsible for evolving network boot wireless, IPV6, data center, including network security

USST

- **U**SWG **S**ecurity **S**ub-**t**eam
- Chaired by Vincent Zimmer (Intel)
- Responsible for all security related material and the team has been responsible for the added security infrastructure in the UEFI

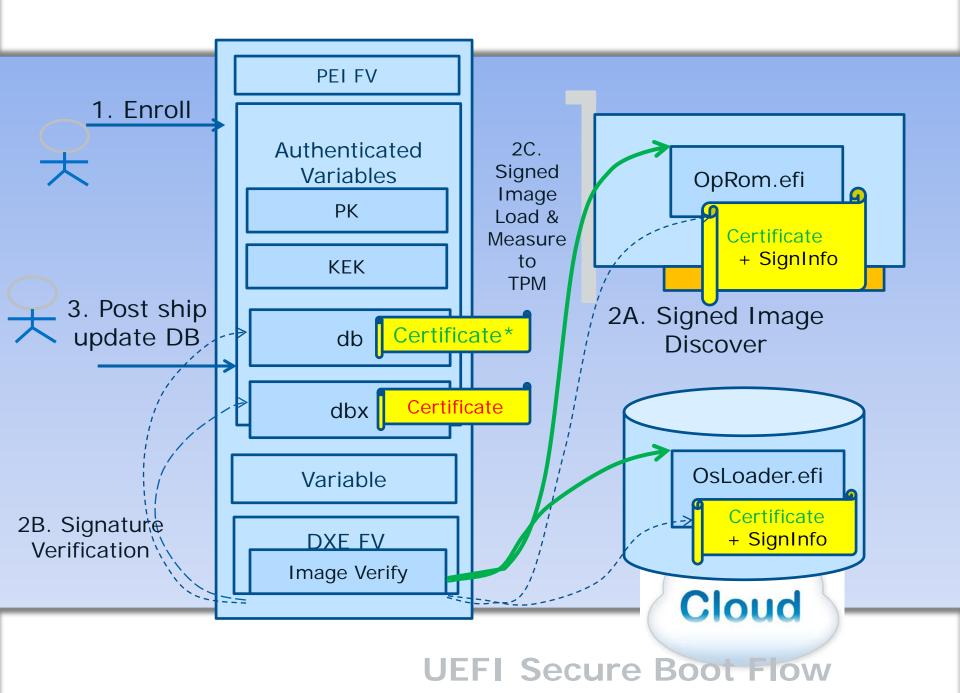
PSST

- PIWG Security Sub-team
- Chaired by Vincent Zimmer (Intel)
- Produce design guide(s) and security requirements, and identify architectural and implementation issues that cause the requirements not to be met.

Note: Engaged in firmware/boot

Related WG's of Trusted Computing Group (TCG), IETF, DMTF

Security Working Groups in UEFI



*Including UEFI CA

Network boot

What about networking in firmware?

- Rationale How to get to an OS (i.e., boot)
 - Provisioning/installation
 - Diskless client/server nodes
 - Recovery

Today's practice

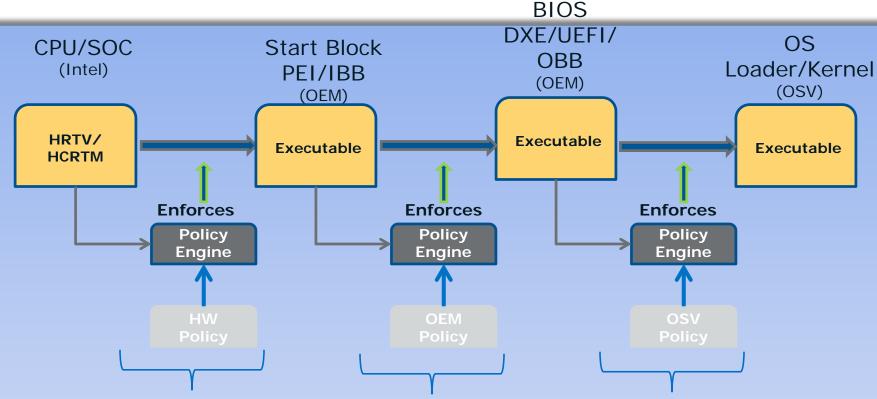
 Pxe2.1/Netboot6 using TFTP in standards, UEFI edk2 network pkg, ipxe, other - closed networks

Moving

• Boot from web-server, wireless,, the internet

Challenge

Credentialing, larger attack surface, complexity



Hardware Secure Boot, such as "Intel® Device Protection **Technology with Boot** Guard"

http://www.intel.com/content/dam/www/pu blic/us/en/documents/product-briefs/4thgen-core-family-mobile-brief.pdf

Figure 5 of http://www.uefidk.com/sites/default/files /resources/Platform_Security_Review_Intel Cisco White Paper.pdf

OEM PI Verification Using PI Signed Firmware Volumes

Vol 3, section 3.2.1.1 of PI 1.3 Specification or Custom internal chain

Maintenance (IPC to Sec, etc)

OEM UEFI 2.4 Secure Boot

Chapter 27.2 of The UEFI 2.4 Specification

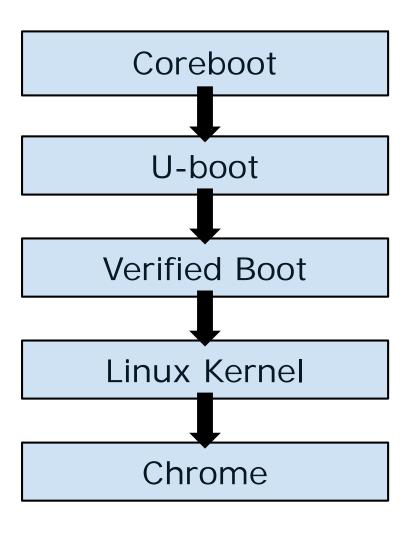
Different flavors of "Secure Boot"

Just UEFI/EDK2? Also Intel booting via Coreboot for Chromebooks

Open

- GPLv2
- Mostly written in C
- Kconfig and modified Kbuild
- High-level organization not too different from EFI
 - Well-defined boot phases
 - o Modular CPU, Chipset, Device support
- NOT a bootloader
 - Support for various payloads
 - o Payloads can boot Linux, DOS, Windows, etc

Basic Coreboot Boot Flow



Coreboot vs. UEFI

	Coreboot	EFI			
	Boot Block	SEC			
	ROM Stage	PEI			
	SI Reference Code				
	RAM Stage	DXE			
	Video Option ROM				
•	U-boot	BDS			
	Verified Boot				
	Linux Kernel				
	Chrome				

Firmware Support Package

Verified Boot - Firmware



- Root Of Trust is in read-only firmware
 - Reset vector must be in RO flash
 - Complicated by SPI Flash Descriptor and ME
- RO firmware can verify signed RW firmware
- Firmware verifies signed kernel from disk
- Reference implementation available
 - o chromiumos/platform/vboot_reference.git

Verified Boot - Overview

SPI Flash

Read-Only Firmware

Read-Write
Firmware
A

Read-Write
Firmware
B

Disk

Kernel Root FS **A** Kernel Root FS

B

Paths to openness

More platforms, more implementations

Intel FSP to build full platforms w/ Open Source IA firmware ecosystems

www.Coreboot.org

www.Tianocore.org

UEFI community at www.uefidk.com

Full platform sources for Intel Quark/Galileo, including feature rich UEFI build (1MByte image) and scaled down "TinyQuark"

Minnowl Atom

Intel® Firmware Support Package (FSP) Overview

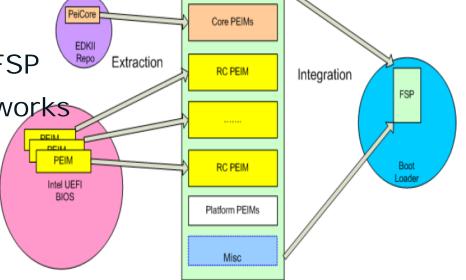
The Intel ® FSP provides processor & chipset initialization in a format that can easily be incorporated into many existing boot loader frameworks without exposing the Intellectual Property (IP) of Intel.

Distributed as single binary

Silicon PEIMs packaged into FSP

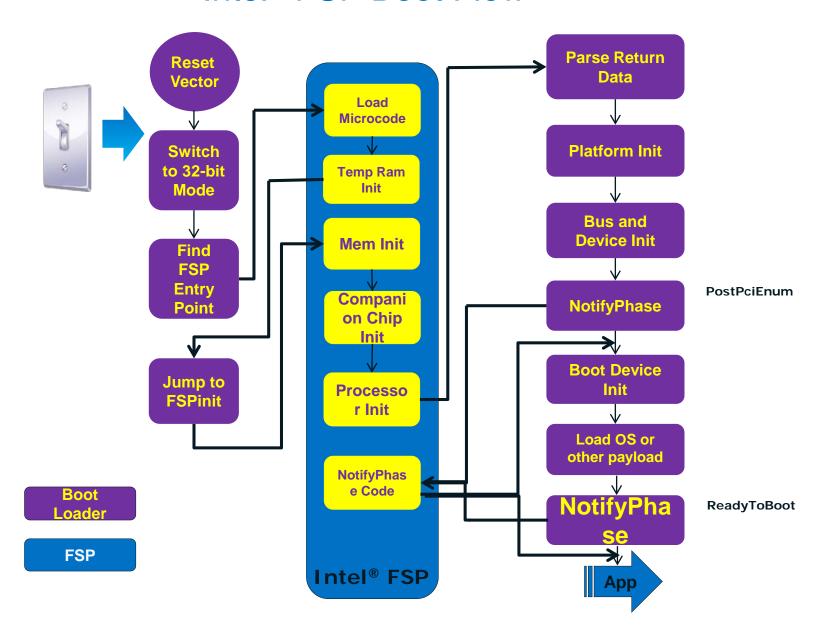
Plugs into existing f/w frameworks

Binary customization



More information at www.intel.com/fsp

Intel® FSP Boot Flow



What to build & defend - Rationale for a threat model

"My house is secure" is almost meaningless

 Against a burglar? Against a meteor strike? A thermonuclear device?

"My system is secure" is almost meaningless

Against what? To what extent?

Threat modeling is a process to define the goals and constraints of a (software) security solution

Translate user requirements to security requirements

We use threat modeling for firmware codebases

 We believe the process and findings are applicable to driver implementations as well as UEFI implementations in general

Defining, using a threat model

A Threat Model (TM) defines the security assertions and constraints for a product

- Assets: What we're protecting
- Threats: What we're protecting it against
- Mitigations: How we're protecting our Assets

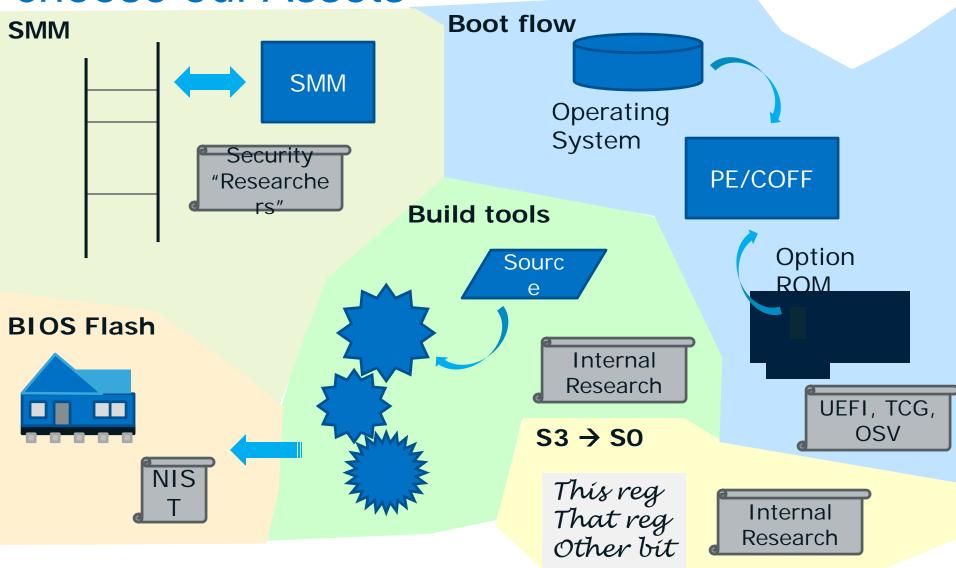
Use TM to narrow subsequent mitigation efforts

- Don't secure review, fuzz test all interfaces
- Select the ones that are critical

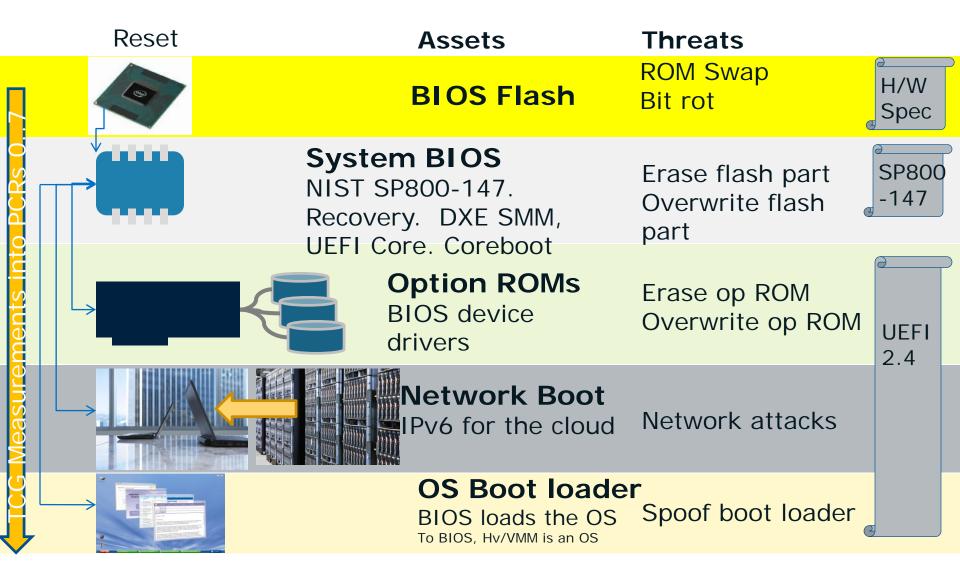
TM is part science, part art, part experience, part nuance, part preference

Few big assets vs lots of focused assets

We don't always get to choose our Assets



Technologies – putting it together

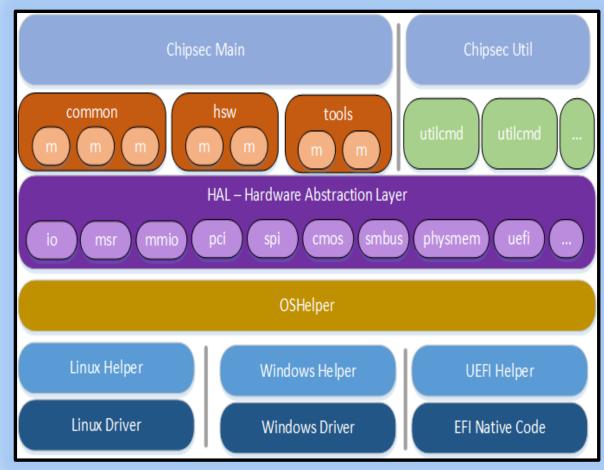


Different colors for different vendors

chipsec - Platform Security Assessment Framework

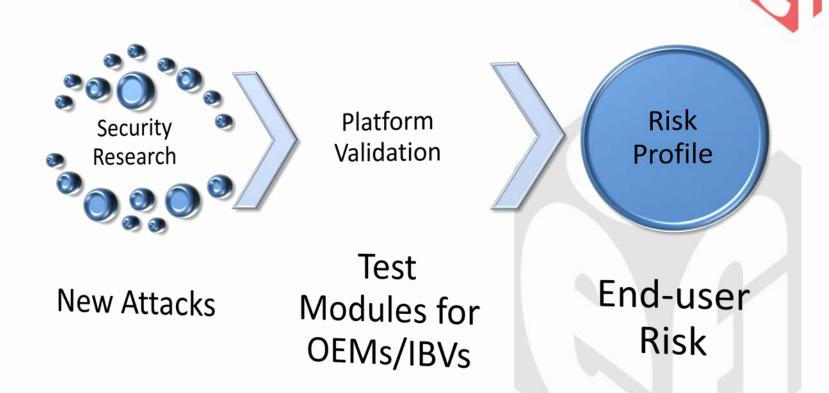


A single test designed to run in multiple environme nts



https://github.com/chipsec/chipsec

How do we raise the bar?



Empowering End-Users to Make a Risk Decision

Known Threats and CHIPSEC modules

Issue	CHIPSEC Module	Public Details	
SMRAM Locking	common.smm	CanSecWest 2006	
BIOS Keyboard Buffer Sanitization	common.bios_kbrd_buffer	<u>DEFCON 16</u> 2008	
SMRR Configuration	common.smrr	ITL 2009 CanSecWest 2009	
BIOS Protection	common.bios_wp	BlackHat USA 2009 CanSecWest 2013 Black Hat 2013 NoSuchCon 2013 Flashrom	
SPI Controller Locking	common.spi_lock	<u>Flashrom</u> <u>Copernicus</u>	
BIOS Interface Locking	common.bios_ts	PoC 2007	
Access Control for Secure Boot Keys	common.secureboot.keys	CanSecWest 2014	
Access Control for Secure Boot Variables	common.secureboot.variables	<u>HITB 2014</u>	

Example: BIOS Write

Protection

Black Hat USA 2013 "BIOS Security" - MITRE (Kovah, Butterworth, Kallenberg)

NoSuchCon 2013 "BIOS Chronomancy: Fixing the Static Root of Trust for Measurement" - MITRE (Kovah, Butterworth, Kallenberg)

Is BIOS correctly protected?



common.bios_wp

- [+] imported chipsec.modules.common.bios_wp
- [x][Module: BIOS Region Write Protection
- BIOS Control (BDF 0:31:0 + 0xDC) = 0x2A
- [05] SMM BWP = 1 (SMM BIOS Write Protection)
- [04] TSS = 0 (Top Swap Status)
- [01] BLE = 1 (BIOS Lock Enable)
- [00] BIOSWE = 0 (BIOS Write Enable)
- [+] BIOS region write protection is enabled (writes restricted to SMM)
- [*] BIOS Region: Base = 0x00500000, Limit = 0x00FFFFFF
- SPI Protected Ranges

PRx (offset)	Value	Base	Limit	WP?	RP?
PR0 (74) PR1 (78) PR2 (7C) PR3 (80) PR4 (84)	00000000 8FFF0F40 8EDF0EB1 8EB00EB0 8EAF0C00	0000000 00F40000 00EB1000 00EB0000	00000000 00FFF000 00EDF000 00EB0000 00EAF000	0 1 1 1	0 0 0 0

- [!] SPI protected ranges write-protect parts of BIOS region (other parts of BIOS can be modified)
- [+] PASSED: BIOS is write protected



Direct HW Access for Manual Testing Examples:

THE STATE OF THE S

```
chipsec_util msr 0x200
      chipsec util mem 0x0 0x41E 0x20
      chipsec util pci enumerate
      chipsec_util pci 0x0 0x1F 0x0 0xDC byte
      chipsec_util io 0x61 byte
      chipsec_util mmcfg 0 0x1F 0 0xDC 1 0x1
      chipsec_util cmos dump
      chipsec util ucode id
      chipsec_util smi 0x01 0xFF
      chipsec_util idt 0
      chipsec_util cpuid 1
      chipsec_util spi read 0x700000 0x100000
bios.bin
      chipsec_util decode spi.bin
      chipsec_util uefi var-list
```

• •

Forensics

Live system firmware analysis

chipsec_util spi info chipsec_util spi dump rom.bin chipsec_util spi read 0x700000 0x100000 bios.bin

chipsec_util uefi var-list chipsec_util uefi var-read db D719B2CB-3D3A-4596-A3BC-DAD00E67656F db.bin

Offline system firmware analysis

chipsec_util uefi keys PK.bin chipsec_util uefi nvram vss bios.bin chipsec_util uefi decode rom.bin chipsec_util decode rom.bin



Moving Forward

Test tools complement the SCT, but the community can do more!

Changing our development philosophy?

- "Testing shows the presence, not the absence of bugs" (Dijkstra, 1970)
- Better Living Through Tools? (Zimmer, 2013)

Getting code coverage closer to 100%?

- Internal Intel effort using <u>DDT</u> with EDK II
- Moving to <u>KLEE</u> (open source)

"Infrastructure for automatic code checking" (coreboot)

Automated system including KLEE, Splint, Frama-C

Summary

- Threats of firmware attacks & UEFI extensibility are real
- Address w/ open standards and open source
- Secure boot is here
- Platforms under attack
- More focus on implementation, less on feature
- Continue to open, open, open

For more information - UEFI Secure Boot

Intel Technology Journal, Volume 15, Issue 1, 2011, UEFI Today: Bootstrapping the Continuum, UEFI Networking and Pre-OS Security, page 80 at ITJ Secure Boot

Rosenbaum, Zimmer, "A Tour Beyond BIOS into UEFI Secure Boot," Intel Corporation, July 2012

http://sourceforge.net/projects/edk2/files/General%20Documentation/A_Tour_Beyond_B IOS_into_UEFI_Secure_Boot_White_Paper.pdf/download

UEFI 2.3.1 specification: Sections 7.2 (Variable Services) and

Sections 27.2 through 27.8 (Secure Boot) of the at www.uefi.org

Beyond BIOS: Developing with the Unified Extensible Firmware

Interface, 2nd Edition, Zimmer, et al, ISBN 13 978-1-934053-29-4,

Chapter 10 – Platform Security and Trust, http://www.intel.com/intelpress

"Hardening the Attack Surfaces," MSFT 2012 UEFI Plugfest

http://www.uefi.org/learning_center/UEFI_Plugfest_2012Q1_Microsoft_AttackSurface.pdf

"Building hardware-based security with a TPM" MSFT BUILD

http://channel9.msdn.com/Events/BUILD/BUILD2011/HW-462T

Lin, Oswald, Zimmer, "UEFI Secure Boot in Linux," Intel Developer Forum, San Francisco, September 11, 2013

https://intel.activeevents.com/sf13/connect/fileDownload/session/A25811835C1B657365 1FC73FB20D0F6C/SF13_STTS002_100.pdf

A Tale of One Software Bypass of Windows 8 Secure Boot by Andrew Furtak, Oleksandr Bazhaniuk and Yuriy Bulygin, Blackhat 2013

UEFI Industry Resources



www.uefi.org

UEFI Open Source



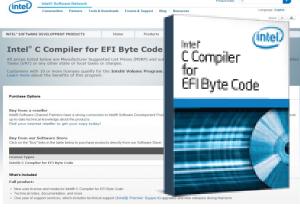
www.tianocore.org

Intel UEFI Resources



www.intel.com/UDK

Intel EBC Compiler



http://software.intel.com/en-us/articles/intel-c-compiler-for-efi-byte-code-purchase/

UEFI Books/ Collateral







www.intel.com/intelpress

http://www.intel.com/technology/itj/2011/v15i1/index.htm

ToorCamp

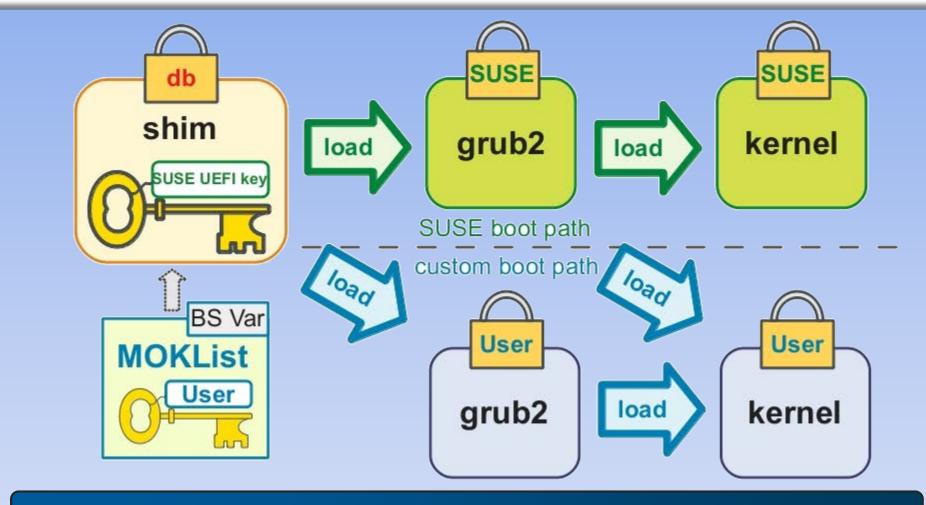
Thank You

Contact:

vincent.zimmer@gmail.com

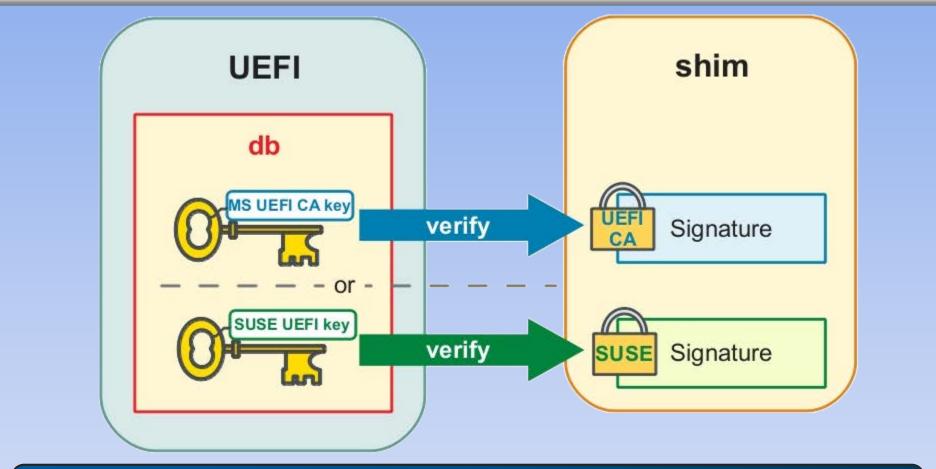
@vincentzimmer

BACKUP



Load the UEFI image as long as it is trusted

Linux Update – Multiple OS Boot with MOK



Either the UEFI CA key or SUSE key will let the shim boot with UEFI secure boot

RandomNumberGenerator

UEFI driver implementing the EFI_RNG_PROTOCOL from the UEFI2.4 specification TCG

PEI Modules & DXE drivers implementing Trusted Computing Group measured boot EFI_TCG_PROTOCOL and EFI_TREE_PROTOCOL from the TCG and Microsoft MSDN websites, respectively

UserIdentification

DXE drivers that support multi-factor user authentication Chapter 31 of the UEFI 2.4 specification

Library

DxeVerificationLib for "UEFI Secure Boot", chapter 27.2 of the UEFI 2.4 specification + other support libs

VariableAuthenticated

SMM and runtime DXE authenticated variable driver, chapter 7 of the UEFI2.4 specification

https://svn.code.sf.net/p/edk2/code/trunk/edk2/SecurityPkg UDK2014 SecurityPkg

Flash**



NIST SP800-147 says

- Lock code flash except for update before Exit Mfg Auth
- Signed update (>= RSA2048, SHA256)
- High quality signing servers
- Without back doors ("non-bypassability")

Threats

- PDOS Permanent Denial of Service
 - System into inefficient room heater
- Elevation of privilege
 - Owning the system at boot is an advantage to a virus

Known attacks

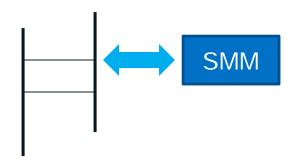
- CIH / Chernobyl 1999-2000
- Mebroni 2010

Mitigations include

- Reexamining flash protection methods use the best even if its new
- Using advanced techniques to locate and remove (un)intentional backdoors

** or tomorrow's equivalent NV storage

SMM



SMM is valuable because

- It's invisible to Anti Virus, etc
- SMM sees all of system RAM
- Not too different from PCI adapter device firmware

Threats

- Elevation
 - View secrets or own the system by subverting RAM

Known attacks

See e.g Duflot

Mitigations include

- Validate "external" / "untrusted" input
- Remove calls from inside SMM to outside SMM

Resume from S3

This reg That reg Other bit

ACPI says that we return the system to the S5→S0 configuration at S3→S0

• Must protect the data structures we record the cold boot config in

Threats

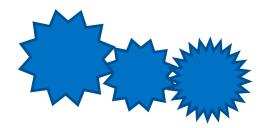
- Changing data structures could cause security settings to be incorrectly configured leaving S3
- Reopen the other assets' mitigated threats

No known attacks

Mitigations include

- Store data in SMM -or-
- Store hash of data structures and refuse to resume if the hashes don't compare

Tool chain



Tools create the resulting firmware

- Rely on third party tools and home grown tools
- Incorrect or attacked tools leave vulnerabilities

Threats

Disabled signing, for example

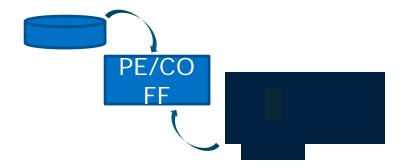
Known attacks

See e.g. Reflections on Trust, Ken Thompson**

Mitigation

- Difficult: For most tools, provided as source code
- Review for correct implementation
- Use static, dynamic code analysis tools
 - PyLint for Python, for example

Boot flow



Secure boot

- Authenticated variables
- Based on the fundamental Crypto being correct
- Correct location for config data

Threats

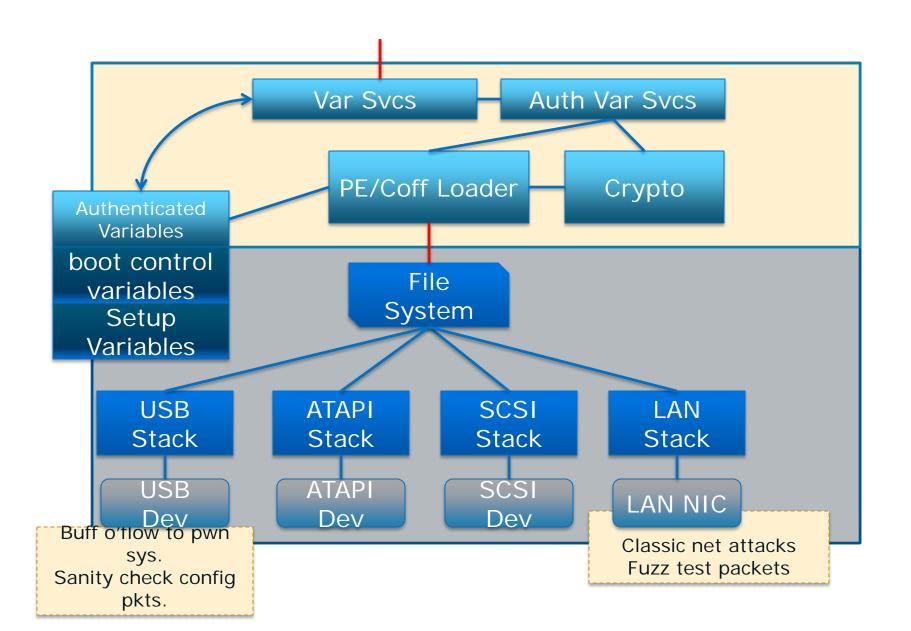
- Run unauthorized op roms, boot loaders
- PDOS systems with bad config variables

Known attacks

Mitigations include

- Sanity check config vars before use, use defaults
- Reviews, fuzz checking, third party reviews, etc.

TM to Modules: Boot flow



Assets or not?



Variable content sanity checking?

- If you randomly fill in your Setup variables, will your system still boot?
- Fit in as a part of boot flow

ACPI? We create it but don't protect it

TPM support? We fill in the PCRs but don't use them (today)

Quality ≠ Security

Analyze and Mark external Interfaces where input can be attacker controlled data, comment headers

```
/**
  Install child handles if the Handle supports GPT partition structure.
  Caution: This function may receive untrusted input.
  The GPT partition table is external input, so this routine
  will do basic validation for GPT partition table before install
  child handle for each GPT partition.
  @param[in] This
                         Calling context.
 @param[in] Handle
                         Parent Handle.
  @param[in] DevicePath Parent Device Path.
**/
EFI STATUS
PartitionInstallGptChildHandl
```

UDK2010 example:

http://edk2.svn.sourceforge.net/svnroot/edk2/trunk/edk2/MdeModulePkg/Universal/Disk/PartitionDxe/Gpt.c

Code Management