

The Wayback Machine - <https://web.archive.org/web/20120429172546/http://www.multicoreinfo.com:80/2011/04/uefi/>

- [Home](#)
- [about](#)
- [contact](#)
- [RSS](#)



- 

## • Categories

- [Academia News](#)
- [Applications](#)
- [Books](#)
- [Chip Tech](#)
- [Cloud Computing](#)
- [Embedded](#)
- [Events](#)
- [Future Tech](#)
- [Gaming](#)
- [GPU](#)
- [HPC](#)
- [Industry News](#)
- [Intel Press](#)
- [Jobs](#)
- [Memory](#)
- [Mobile](#)
- [MulticoreInfo](#)
- [Performance](#)
- [Press Release](#)
- [Processors](#)
- [Programming](#)
- [Related Topics](#)
- [Research](#)
- [Research Papers](#)
- [Storage](#)
- [Tools](#)
- [Whitepapers](#)

## • Popular Posts

- [Parallel Programming Tutorial Series - Part 9 - OpenCL](#)
- [Home page](#)
- [Parallel Programming Tutorial Series - Part 1 - Basics](#)
- [Parallel Programming Tutorial Series - Part 9 - OpenCL \(Updated\)](#)

- [Data Prefetching in the Era of Multicore Processors](#)

## • Archives

- [November 2011](#)
- [October 2011](#)
- [September 2011](#)
- [August 2011](#)
- [July 2011](#)
- [June 2011](#)
- [May 2011](#)
- [April 2011](#)
- [March 2011](#)
- [February 2011](#)
- [January 2011](#)
- [December 2010](#)
- [November 2010](#)
- [October 2010](#)
- [September 2010](#)
- [August 2010](#)
- [July 2010](#)
- [June 2010](#)
- [May 2010](#)
- [April 2010](#)
- [March 2010](#)
- [February 2010](#)
- [January 2010](#)
- [December 2009](#)
- [November 2009](#)
- [October 2009](#)
- [September 2009](#)
- [August 2009](#)
- [July 2009](#)
- [June 2009](#)
- [May 2009](#)
- [April 2009](#)
- [March 2009](#)
- [February 2009](#)
- [January 2009](#)
- [December 2008](#)
- [November 2008](#)
- [October 2008](#)
- [September 2008](#)
- [August 2008](#)
- [July 2008](#)
- [June 2008](#)
- [May 2008](#)
- [April 2008](#)



[Subscribe in a reader](#)

← [Tilera Releases Updated Development Tools for Manycore Processor Development](#) [Google Exacycle for Visiting Faculty Grant Program](#) →

# Intel Research: Manageability and the Intel Unified Extensible Firmware Interface

April 8th, 2011 · [No Comments](#)

*by Vincent Zimmer, Michael Rothman, and Suresh Marisetty*

## Abstract

RAS is a critical requirement for enterprise class servers, which includes high availability server platforms. System uptime is measured against the goal of “five nines,” which represents 99.999 percent availability. One of the key aims of manageability software is to help achieve this goal, by implementation functions like dynamic error detection, correction, hardware failure prediction, and the taking of corrective actions like replacing or turning off failing components before the failure actually happens. This article describes the enhanced Intel® architecture platform dynamic error handling framework, a system level error management infrastructure that is now an integral part of most industry standard server class operating systems.

[Full Story](#) [pdf]

ShareThis

[+ Share / Save](#)

**Tags:** [Embedded](#) · [Intel Press](#) · [MulticoreInfo](#)

Like what you're reading? [Come back](#) every day for multicore news, or subscribe to [RSS](#) updates.



Stumble It!

0 responses so far ↓

- There are no comments yet...Kick things off by filling out the form below.

You must [log in](#) to post a comment.

## • Search MulticoreInfo

To search, type and hit enter

- 

## • Featured Links

- [Multicore Books](#)
- [Multicore Related Blogs](#)
- [Multicore Research Papers](#)
- [Multicore Research Papers - 2009](#)
- [Multicore Research Papers - 2010](#)
- [Multicore Review 2009](#)
- [Whitepapers](#)

## • Featured Posts

- [\\* More Featured Posts \\*](#)
- [Multicore Papers at IPDPS 2010](#)
- [Multicore Review 2009](#)
- [Parallel Programming Tutorial Series](#)

## • Quick Links

- [“Multi-core Mania”: A Rebuttal](#)
- [\\* More Quick Links \\*](#)
- [A Poster on Fundamentals of HPC](#)
- [A Stimulus Package for HPC](#)
- [Adding Parallel Extensions to F#](#)
- [Data Flow Concurrency - let your data flow](#)
- [Down in the Weeds of Concurrency](#)
- [Getting a grip on cloud computing](#)
- [Handling Concurrency in Domain Models](#)
- [Heavyweights of the supercomputing world](#)
- [Intel touts 2GHz Atom](#)
- [Intel's Parallel Programming Talk #38](#)
- [Java Concurrency Bugs: Inconsistent Synchronization](#)
- [Linus Torvalds, Patterson and different views](#)
- [Multicore Intermediate](#)
- [Multicore Processor Simulator](#)
- [Multithreaded and Multicore Programming](#)
- [Multithreaded File I/O](#)
- [Programming languages for multicore computers](#)
- [RISC vs. CISC, multicore, SoC, and more](#)
- [Sea of cores: we're missing the ship](#)
- [The Power of “In Progress”](#)
- [Types for Concurrency](#)
- [What is Erlang-Style Concurrency?](#)

## • Headlines

- [Exascale computing seen in this decade](#)11.18
- [Mimicking the brain, in silicon](#)11.16
- [GPU technology key to exascale says Nvidia](#)11.16

- [Intel Shows 22nm 50-Core “Knights Corner” CPU](#)11.16
- [AMD Launches 16 Core Interlagos Opteron Servers, Targets HPC, Cloud Computing](#)11.16
- [ARM’s New GPUs to Step up Mobile War With NVIDIA, Imagination Tech.](#)11.16

© 2008–2020 [MulticoreInfo.com](#); [Sitemap](#)