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10.1 - An Efficient Asynchronous Batch Bayesian Optimization Approach for Analog Circuit Synthesis
Shuhan Zhang, Fan Yang, Dian Zhou, Xuan Zeng

10.2 - GUI-Enhanced Layout Generation of FFE SST TXs for Fast High-Speed Serial Link Design
Seungho Han, Sungyu Jeong, Chanho Kim, Hong-June Park, Byungsub Kim

10.3 - Bit Parallel 6T SRAM In-Memory Computing with Reconfigurable Bit-Precision
Kyeongho Lee, Jinho Jeong, SungSoo Cheon, Woong Choi, Jongsun Park

10.4 - Factored Radix-8 Systolic Array for Tensor Processing
Inayat Ullah, Kashif Inayat, Joon-Sung Yang, Jaeyong Chung

11.1 - StatSAT: A Boolean Satisfiability Based Attack on Logic-Locked Probabilistic Circuits
Ankit Mondal, Michael Zuzak, Ankur Srivastava

11.2 - DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY
Jianqi Chen, Monir Zaman, Yiorgos Makris, R. D. Shawn Blanton, Subhasish Mitra, Benjamin Carrion Schaefer

11.3 - RELIC-FUN: Logic Identification through Functional Signal Comparisons
James Geist, Travis Meade, Shaojie Zhang, Yier Jin

11.4 - Flashmark: Watermarking of NOR Flash Memories for Counterfeit Detection
Prawar Poudel, Biswajit Ray, Aleksandar Milenkovic

13.1 - AI Utopia or Dystopia: On Securing AI Platforms
Patrick Jauernig, Emmanuel Stapf, Ghada Dessouky, Nele Mentens, Ahmad-Reza Sadeghi

13.2 - Unified Architectural Support for Secure and Robust Deep Learning
Mojan Javaheripi, Huili Chen, Farinaz Koushanfar

13.3 - Developing Privacy-preserving AI Systems: The Lessons Learned
Fabian Boemer, Rosario Cammarota, Huili Chen, Siam Umar Hussain, Ahmad-Reza Sadeghi , Emmanuel Stapf , Farinaz Koushanfar

14.1 - Time-Division Multiplexing Based System-Level FPGA Routing for Logic Verification
Peng Zou, Zhifeng Lin, Xiao Shi, Yingjie Wu, Jianli Chen, Jun Yu, Yao-Wen Chang

14.2 - Symbolic Computer Algebra and SAT Based Information Forwarding for Fully Automatic Divider Verification
Christoph Scholl, Alexander Konrad

14.3 - A-QED Verification of Hardware Accelerators
Eshan Singh, Florian Lonsing, Saranyu Chattopadhyay, Max Strange, Peng Wei, Xiaofan Zhang, Yuan Zhou, Jason Cong, Deming Chen, Zhiru Zhang, Priyanka Raina, Clark Barrett, Subhasish Mitra

14.4 - Circuit Learning for Logic Regression on High Dimensional Boolean Space
Pei-Wei Chen, Yu-Ching Huang, Cheng-Lin Lee, Jie-Hong Roland Jiang

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15.1 - Enabling a B+-Tree-Based Data Management Scheme for Key-Value Store Over SMR-Based SSHD
Yu-Pei Liang, Tseng-Yi Chen, Ching-Ho Chi, Hsin-Wen Wei, Wei-kuan Shih

15.2 - S-CDA: A Smart Cloud Disk Allocation Approach in Cloud Block Storage System
Hua Wang, Yang Yang, Ping Huang, Yu Zhang, Ke Zhou, Mengling Tao, Bin Cheng

15.3 - Content Sifting Storage: Achieving Fast Read for Large-Scale Image Dataset Analysis
Yu Liu, Hong Jiang, Yangtao Wang, Ke Zhou, Yifei Liu, Li Liu

15.4 - Utilizing Direct Photocurrent Computation and 2D Kernel Scheduling to Improve In-Sensor-Processing Efficiency
Han Xu, Maimaiti Nazhamaiti, Yidong Liu, Fei Qiao, Qi Wei, Xinjun Liu, Huazhong Yang

16.1 - GENIEx: A Generalized Approach to Emulating Non-Idealities in Memristive X-bars Using Neural Networks
Indranil Chakraborty, Mustafa F. Ali, Dong Eun Kim, Aayush Ankit, Kaushik Roy

16.2 - Algorithm/Hardware Co-Design for In-Memory Neural Network Computing with Minimal Peripheral Circuit Overhead
Hyungjun Kim, Yulhwa Kim, Sungju Ryu, Jae-Joon Kim

16.3 - RaQu: An Automatic High-Utilization CNN Quantization and Mapping Framework for General-Purpose RRAM Accelerator
Songyun Qu, Bing Li, Ying Wang, Dawen Xu, Xiandong Zhao, Lei Zhang

16.4 - Accurate Inference with Inaccurate RRAM Devices: Statistical Data, Model Transfer, and On-line Adaptation
Gouranga Charan, Jubin Hazra, Karsten Beckmann, Xiaocong Du, Gokul Krishnan, Rajiv Joshi, Nathaniel Cady, Yu Cao

20.1 - FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization
Jiaqi Gu, Zheng Zhao, Chenghao Feng, Wuxi Li, Ray T. Chen, David Z. Pan

20.2 - T2FSNN: Deep Spiking Neural Networks with Time-To-First-Spike Coding
Seongsik Park, Seijoon Kim, Byunggook Na, Sungroh Yoon

20.3 - A 90nm 103.14 TOPS/W Binary-Weight Spiking Neural Network CMOS ASIC for Real-Time Object Classification
Po-Yao Chuang, Pai-Yu Tan, Cheng-Wen Wu, Juin-Ming Lu

20.4 - A Device Non-Ideality Resilient Approach for Mapping Neural Networks to Crossbar Arrays
Arman Kazemi, Cristobal Alessandri, Alan C. Seabaugh, Xiaobo Sharon Hu, Michael Niemier, Siddharth Joshi

21.1 - Stealing Your Data from Compressed Machine Learning Models
Nuo Xu, Qi Liu, Tao Liu, Zihao Liu, Xiaochen Guo, Wujie Wen

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21.2 - Imperceptible Misclassification Attack on Deep Learning Accelerator by Glitch Injection
Wenye Liu, Chip-Hong Chang, Fan Zhang, Xiaoxuan Lou

21.3 - Reverse-Engineering Deep Neural Networks Using Floating-Point Timing Side-Channels
Cheng Gongye, Yunsi Fei, Thomas Wahl

21.4 - TrojDRL: Evaluation of Backdoor Attacks on Deep Reinforcement Learning
Panagiota Kiourti, Kacper Wardega, Susmit Jha, Wenchao Li

23.1 - Computation on Sparse Neural Networks and its Implications for Future Hardware
Fei Sun, Minghai Qin, Tianyun Zhang, Liu Liu, Yen-Kuang Chen, Yuan Xie

23.2 - Efficient Synthesis of Compact Deep Neural Networks
Wenhan Xia, Hongxu Yin, Niraj Jha

23.3 - New Directions in Distributed Deep Learning: Bringing the Network at Forefront of IoT Design
Kartikeya Bhardwaj, Wei Chen , Radu Marculescu

24.1 - Analysis and Optimization of the Implicit Broadcasts in FPGA HLS to Improve Maximum Frequency
Licheng Guo, Jason Lau, Yuze Chi, Jie Wang, Cody Hao Yu, Zhe Chen, Zhiru Zhang, Jason Cong

24.1 - Analysis and Optimization of the Implicit Broadcasts in FPGA HLS to Improve Maximum Frequency
Licheng Guo, Jason Lau, Yuze Chi, Jie Wang, Cody Hao Yu, Zhe Chen, Zhiru Zhang, Jason Cong

24.2 - Time Multiplexing Via Circuit Folding
Po-Chun Chien, Jie-Hong Roland Jiang

24.3 - SAT-Sweeping Enhanced for Logic Synthesis
Luca Amarù, Felipe Marranghello, Eleonora Testa, Christopher Casares, Vinicius Possani, Jiong Luo, Patrick Vuillod, Alan Mishchenko, Giovanni De Micheli

24.4 - SFO: A Scalable Approach to Fanout-Bounded Logic Synthesis for Emerging Technologies
He-Teng Zhang, Jie-Hong Roland Jiang

25.1 - Input-Dependent Edge-Cloud Mapping of Recurrent Neural Networks Inference
Daniele Jahier Pagliari, Roberta Chiaro, Yukai Chen, Sara Vinco, Enrico Macii, Massimo Poncino

25.2 - RTMobile: Beyond Real-Time Mobile Acceleration of RNNs for Speech Recognition
Peiyan Dong, Siyue Wang, Wei Niu, Chengming Zhang, Sheng Lin, Zhengang Li, Yifan Gong, Bin Ren, Xue Lin, Dingwen Tao

25.3 - Seesaw: End-to-End Dynamic Sensing for IoT using Machine Learning
Vidushi Goyal, Valeria Bertacco, Reetu Das

25.4 - EMAP: A Cloud-Edge Hybrid Framework for EEG Monitoring and Cross-Correlation Based Real-Time Anomaly Prediction
Bharath Srinivas Prabakaran, Alberto García Jiménez, Germán Moltó Martínez, Muhammad Shafique

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26.1 - Clustering Approach for Solving Traveling Salesman Problems via Ising Model Based Solver
Akira Dan, Riu Shimizu, Takeshi Nishikawa, Song Bian, Takashi Sato

26.2 - Eliminating Redundant Computation in Noisy Quantum Computing Simulation
Gushu Li, Yufei Ding, Yuan Xie

26.3 - Transfer Learning-Based Microfluidic Design System for Customized Concentration Generation
Weiqing Ji, Tsung-Yi Ho, Hailong Yao

26.4 - Realistic Fault Models and Fault Simulation for Quantum Dot Quantum Circuits
Cheng-Yun Hsieh, Chen Hung Wu, Chen-Hung Wu, Chia-Hsien Huang, Hsi-Sheng Goan, James Chien-Mo Li

30.1 - BitPruner: Network Pruning for Bit-Serial Accelerators
Xiandong Zhao, Ying Wang, Cheng Liu, Cong Shi, Kaijie Tu, Lei Zhang

30.2 - CAP'NN: Class-Aware Personalized Neural Network Inference
Maedeh Hemmat, Joshua San Miguel, Azadeh Davoodi

30.3 - Learning to Quantize Deep Neural Networks: A Competitive-Collaborative Approach
Md Fahim Faysal Khan, Mohammad Mahdi Kamani, Vijaykrishnan Narayanan, Mehrdad Mahdavi

30.4 - ALF: Autoencoder-Based Low-Rank Filter-Sharing for Efficient Convolutional Neural Networks
Alexander Frickenstein, Manoj-Rohit Vemparala, Nael Fasfous, Laura Hauenschild, Christian Unger, Naveen-Shankar Nagaraja, Walter Stechele

30.5 - Algorithm-Hardware Co-Design of Adaptive Floating-Point Encodings for Resilient Deep Learning Inference
Thierry Tambe, En-Yu Yang, Zishen Wan, Yuntian Deng, Vijay Janapa Reddi, Alexander Rush, David Brooks, Gu-Yeon Wei

30.6 - Q-PIM: A Genetic Algorithm based Flexible DNN Quantization Method and Application to Processing-In-Memory Platform
Yun Long, Edward Lee, Daehyun Kim, Saibal Mukhopadhyay

31.1 - Reuse-Trap: Re-Purposing Cache Reuse Distance to Defend Against Side Channel Leakage
Hongyu Fang, Milos Doroslovacki, Guru Venkataramani

31.2 - Deep Learning Multi-Channel Fusion Attack Against Side-Channel Protected Hardware
Benjamin Hettwer, Daniel Fennes, Sebastien Leger, Jan Richter-Brockmann, Stefan Gehrer, Tim Güneysu

31.3 - Learning From A Big Brother - Mimicking Neural Networks in Profiled Side-channel Analysis
Daan van der Valk, Marina Krcek, Stjepan Picek, Shivam Bhasin

31.4 - From Homogeneous to Heterogeneous: Leveraging Deep Learning Based Power Analysis Across Devices
Fan Zhang, Bin Shao, Guorui Xu, Bolin Yang, Ziqi Yang, Zhan Qin, Kui Ren

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33.1 - Computational Methods for Biological Exploration
Louis K Scheffer

33.3 - Advancements in Model Checking Methods for System Biological Investigations
Bing Liu, Sara Safa

34.1 - A Cross-Layer Power and Timing Evaluation Method for Wide Voltage Scaling
Wenjie Fu, Leilei Jin, Ming Ling, Yu Zheng, Longxing Shi

34.2 - GRANNITE: Graph Neural Network Inference for Transferable Power Estimation
Yanqing Zhang, Haoxing Ren, Brucek Khailany

34.3 - VarSim: A Fast and Accurate Variability and Leakage Aware Thermal Simulator
Hameedah Sultan, Smruti Sarangi

34.4 - TYMER: A Yield-Based Performance Model for Timing-Speculation SRAM
Shan Shen, Liang Pang, Tianxiang Shao, Ming Ling, Xiao Shi, Longxing Shi

34.5 - Exploiting Zero Data to Reduce Register File and Execution Unit Dynamic Power Consumption in GPGPUs
Ahmad Radaideh, Paul Gratz

34.6 - TP-GNN: A Graph Neural Network Framework for Tier Partitioning in Monolithic 3D ICs
Yi-Chen Lu, Sai Surya Kiran Pentapati, Lingjun Zhu, Kambiz Samadi, Sung Kyu Lim

35.1 - COEXE: An Efficient Co-Execution Architecture for Real-Time Neural Network Services
Liu Chubo, Kenli Li, Mingcong Song, Jiechen Zhao, Keqin Li, Tao Li, Zihao Zeng

35.2 - TSN-Builder: Enabling Rapid Customization of Resource-Efficient Switches for Time-Sensitive Networking
Jinli Yan, Wei Quan, Xiangrui Yang, Wenwen Fu, Yue Jiang, Hui Yang, Zhigang Sun

35.3 - Predictable Memory-CPU Co-Scheduling with Support for Latency-Sensitive Tasks
Daniel Casini, Paolo Pazzaglia, Alessandro Biondi, Marco Di Natale, Giorgio Buttazzo

35.4 - Timing-Accurate General-Purpose I/O for Multi- and Many-Core Systems: Scheduling and Hardware Support
Shuai Zhao, Zhe Jiang, Xiaotian Dai, Iain Bate, Ibrahim Habli, Wanli Chang

35.5 - DPCP-p: A Distributed Locking Protocol for Parallel Real-Time Tasks
Maolin Yang, Zewei Chen, Xu Jiang, Nan Guan, Hang Lei

35.6 - On Computing Exact WCRT for DAG Task
Jinghao Sun, Feng Li, Nan Guan, Wentao Zhu, Minjie Xiang, Zhishan Guo, Wang Yi

36.1 - WET: Write Efficient Loop Tiling for Non-Volatile Main Memory
Mohammad Alshboul, James Tuck, Yan Solihin

36.2 - TCIM: Triangle Counting Acceleration With Processing-In-MRAM Architecture
Xueyan Wang, Jianlei Yang, Yinglin Zhao, Yingjie Qi, Meichen Liu, Xingzhou Cheng, Xiaotao Jia, Xiaoming Chen, Gang Qu, Weisheng ZHAO

36.3 - Towards State-Aware Computation in ReRAM Neural Networks
Yintao He, Ying Wang, Xiandong Zhao, Huawei Li, Xiaowei Li

36.4 - Robust Design of Large Area Flexible Electronics via Compressed Sensing
Leilai Shao, Ting Lei, Tsung-Ching Huang, Zhenan Bao, Tim Cheng

36.5 - Verification for Field-Coupled Nanocomputing Circuits
Marcel Walter, Robert Wille, Frank Sill Torres, Daniel Grosse, Rolf Drechsler

36.6 - Massively Parallel Approximate Simulation of Quantum Circuits
Igor Markov, Aneeqa Fatima, Sergei V. Isakov, Sergio Boixo

37.1 - WarningNet: A Deep Learning Platform for Early Warning of Task Failures under Input Perturbation for Reliable Autonomous Platforms
Minah Lee, Burhan Mudassar, Taesik Na, Saibal Mukhopadhyay

37.2 - Exploring Inherent Sensor Redundancy for Automotive Anomaly Detection
Tianjia He, Lin Zhang, Fanxin Kong, Asif Salekin

37.3 - PISCES: Power-Aware Implementation of SLAM by Customizing Efficient Sparse Algebra
Bahar Asgari, Ramyad Hadidi, Nima Shoghi Ghalehshahi, Hyesoon Kim

37.4 - Dadu-CD: Fast and Efficient Processing-in-Memory Accelerator for Collision Detection
Yuxin Yang, Xiaoming Chen, Yinhe Han

37.5 - Opportunistic Intermittent Control with Safety Guarantees for Autonomous Systems
Chao Huang, Shichao Xu, Zhilu Wang, Shuyue Lan, Wenchao Li, Qi Zhu

41.1 - GPNPU: Enabling Efficient Hardware-Based Direct Convolution with Multi-Precision Support in GPU Tensor Cores
Zhuoran Song, Jianfei Wang, Tianjian Li, Li Jiang, Jing Ke, Xiaoyao Liang, Naifeng Jing

41.2 - Tensor Virtualization Technique to Support Efficient Data Reorganization for CNN Accelerators
Donghyun Kang, Soonhoi Ha

41.3 - Balancing Efficiency and Flexibility for DNN Acceleration via Temporal GPU-Systolic Array Integration
Cong Guo, Yangjie Zhou, Jingwen Leng, Yuhao Zhu, Zidong Du, Quan Chen, Chao Li, Bin Yao, Minyi Guo

41.4 - SIEVE: Speculative Inference on the Edge with Versatile Exportation
Babak Zamirai, Salar Latifi, Pedram Zamirai, Scott Mahlke

42.1 - A Novel GPU Overdrive Fault Attack
Majid Sabbagh, Yunsi Fei, David Kaeli

42.2 - ROPAD: A Fully Digital Highly Predictive Ring Oscillator Probing Attempt Detector
Seyed Hamidreza Moghadas, Michael Pehl

42.3 - Runtime Trust Evaluation and Hardware Trojan Detection Using On-Chip EM Sensors
Jiaji He, Xiaolong Guo, Haocheng Ma, Yanjiang Liu, Yiqiang Zhao, Yier Jin

42.4 - DRAMDig: A Knowledge-Assisted Tool to Uncover DRAM Address Mapping
Minghua Wang, Zhi Zhang, Yueqiang Cheng, Surya Nepal

44.1 - Machine Learning Based Side Channel Attacks and Countermeasures
Dimitrios Serpanos, Shengqi Yang , Marilyn Wolf

44.3 - A 0.26% BER, Machine-Learning Resistant 1028 Challenge-Response PUF in 14nm CMOS Featuring Stability-Aware Adversarial Challenge Selection
Vikram Suresh, Raghavan Kumar, Sanu K. Mathew

45.1 - Learning Concise Models from Long Execution Traces
Natasha Yogananda Jeppu, Thomas Melham, Daniel Kroening, John O'Leary

45.2 - Machine Learning to Set Meta-Heuristic Specific Parameters for High-Level Synthesis Design Space Exploration
Zi Wang, Benjamin Carrion Schaefer

45.3 - A Machine Learning Approach for Reliability-Aware Application Mapping for Heterogeneous Multicores
Rafael B. Tonetto, Hiago M. G. de A. Rocha, Gabriel Nazar, Antonio Carlos Schneider Beck

45.4 - Exploration of Design Space and Runtime Optimization for Affective Computing in Machine Learning Empowered Ultra-Low Power SoC
Yijie Wei, Kofi Otseidu, Jie Gu

46.1 - The Best of Both Worlds: Combining CUDA Graph with an Image Processing DSL
Bo Qiao, M. Akif Özkan, Jürgen Teich, Frank Hannig

46.2 - DDOT: Data Driven Online Tuning for Energy Efficient Acceleration
Sotirios Xydis, Eleftherios Christoforidis, Dimitrios Soudris

46.3 - Efficient Multi-Grained Wear Leveling for Inodes of Persistent Memory File Systems
Chaoshu Yang, Duo Liu, Runyu Zhang, Xianzhang Chen, Shun Nie, Fengshun Wang, Qingfeng Zhuge, Edwin H.-M Sha

46.4 - ReTriple: Reduction of Redundant Rendering on Android Devices for Performance and Energy Optimizations
Xianfeng Li, Gengchao Li, Xiaole Cui

47.1 - CoinPurse: A Device-Assisted File System with Dual Interfaces
Zhe Yang, Youyou Lu, Erci Xu, Jiwu Shu

47.2 - LOFFS: A Low-Overhead File System for Large Flash Memory on Embedded Devices
Runyu Zhang, Duo Liu, Xianzhang Chen, Xiongxiong She, Chaoshu Yang, Yujuan Tan, Zhaoyan Shen, Zili Shao

47.3 - Layer RBER Variation Aware Read Performance Optimization for 3D Flash Memories
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47.4 - Access Characteristic Guided Partition for Read Performance Improvement on Solid State Drives
Yina Lv, Liang Shi, Qiao Li, Chun Jason Xue, Edwin Sha

51.1 - A Pragmatic Approach to On-Device Incremental Learning System with Selective Weight Updates
Jaekang Shin, Seungkyu Choi, Yeongjae Choi, Lee-Sup Kim

51.2 - SparseTrain: Exploiting Dataflow Sparsity for Efficient Convolutional Neural Networks Training
Pengcheng Dai, Jianlei Yang, Xucheng Ye, Xingzhou Cheng, Junyu Luo, Linghao Song, Yiran Chen, Weisheng ZHAO

51.3 - Tail: An Automated and Lightweight Gradient Compression Framework for Distributed Deep Learning
Jinrong Guo, Songlin Hu, Wang Wang, Chunrong Yao, Jizhong Han, Ruixuan Li, Yijun Lu

51.4 - Convergence-Aware Neural Network Training
Hyungjun OH, Yongseung Yu, Giha Ryu, Gunjoo Ahn, Youri Jeong, Yongjun Park, Jiwon Seo

52.1 - Pythia: Intellectual Property Verification in Zero-Knowledge
Dimitris Mouris, Nektarios Tsoutsos

52.2 - LoPher: SAT-Hardened Logic Embedding on Block Ciphers
Akashdeep Saha, Sayandeep Saha, Siddhartha Chowdhury, Debdeep Mukhopadhyay, Bhargab Bhattacharya

52.3 - AHEC: End-To-End Compiler Framework for Privacy-Preserving Machine Learning Acceleration
Huili Chen, Rosario Cammarota, Farinaz Koushanfar, Felipe Valencia, Francesco Regazzoni

52.4 - Compact Domain-Specific Co-Processor for Accelerating Module Lattice-Based KEM
Jose Maria Bermudo Mera, Furkan Turan, Angshuman Karmakar, Sujoy Sinha Roy, Ingrid Verbauwhede

54.0 - Invited Paper: Building End-to-end IoT Applications with QoS Guarantees
Arne Hamann, David Ginthoer, Dirk Ziegenbein, Selma Saidi, Christian Wietfeld, Anthony Rowe

55.1 - Towards Purposeful Design Space Exploration of Heterogeneous CGRAs: Clock Frequency Estimation
Dennis Leander Wolf, Christoph Spang, Christian Hochberger

55.2 - CL(R)Early: An Early-Stage DSE Methodology for Cross-Layer Reliability-Aware Heterogeneous Embedded Systems
Siva Satyendra Sahoo, Bharadwaj Veeravalli, Akash Kumar

55.3 - A Versatile and Flexible Chiplet-Based System Design for Heterogeneous Manycore Architectures
Hao Zheng, Ke Wang, Ahmed Louri

55.4 - Efficiently Exploiting Low Activity Factors to Accelerate RTL Simulation
Scott Beamer, David Donofrio

56.1 - Hardware-Assisted Service Live Migration in Resource-Limited Edge Computing Systems
Zhe Zhou, Xintong Li, Xiaoyang Wang, Zheng Liang, Guangyu Sun, Guojie Luo

56.2 - ApproxFPGAs: Embracing ASIC-Based Approximate Arithmetic Components for FPGA-Based Systems
Bharath Srinivas Prabakaran, Vojtech Mrazek, Zdenek Vasicek, Lukas Sekanina, Muhammad Shafique

56.3 - PEMACx: A Probabilistic Error Analysis Methodology for Adders with Cascaded Approximate Units
Muhammad Abdullah Hanif, Rehan Hafiz, Osman Hasan, Muhammad Shafique

56.4 - AdaSense: Adaptive Low-Power Sensing and Activity Recognition for Wearable Devices
Marina Neseem, Jon Nelson, Sherief Reda

57.1 - A Robust Exponential Integrator Method for Generic Nonlinear Circuit Simulation
Quan Chen

57.2 - Adjoint Transient Sensitivity Analysis for Objective Functions Associated to Many Time Points
Wenfei Hu, Zuochang Ye, Yan Wang

57.3 - MLParest: Machine Learning Based Parasitic Estimation for Custom Circuit Design
Brett Shook, Prateek Bhansali, Chandramouli Kashyap, Chirayu Amin, Siddhartha Joshi

57.4 - ParaGraph: Layout Parasitics and Device Parameter Prediction Using Graph Neural Networks
Haoxing Ren, George Kokai, Walker Turner, Ting Ku

58.1 - An Efficient EPIST Algorithm for Global Placement with Non-Integer Multiple-Height Cells
Jianli Chen, Zhipeng Huang, Ye Huang, Wenxing Zhu, Jun Yu, Yao-Wen Chang

58.2 - Hamiltonian Path Based Mixed-Cell-Height Legalization for Neighbor Diffusion Effect Mitigation
Jianli Chen, Ziran Zhu, Qinghai Liu, Yimin Zhang, Wenxing Zhu, Yao-Wen Chang

58.3 - TDP-ADMM: A Timing Driven Placement Approach for Superconductive Electronic Circuits Using Alternating Direction Method of Multipliers
Soheil Nazar Shahsavani, Massoud Pedram

58.4 - CUGR: Detailed-Routability-Driven 3D Global Routing with Probabilistic Resource Model
Jinwei Liu, Chak-Wa Pui, Fangzhou Wang, Evangeline Young

62.1 - HybridDNN: A Framework for High-Performance Hybrid DNN Accelerator Design and Implementation
Hanchen Ye, Xiaofan Zhang, Zhize Huang, Gengsheng Chen, Deming Chen

62.2 - EDD: Efficient Differentiable DNN Architecture and Implementation Co-Search for Embedded AI Solutions
Yuhong Li, Cong Hao, Xiaofan Zhang, Xinheng Liu, Yao Chen, Jinjun Xiong, Wen-mei Hwu, Deming Chen

62.3 - SCA: A Secure CNN Accelerator for Both Training and Inference
Lei Zhao, Youtao Zhang, Jun Yang

62.4 - Monitoring the Health of Emerging Neural Network Accelerators with Cost-Effective Concurrent Test
Qi Liu, Tao Liu, Zihao Liu, Wujie Wen, Chengmo Yang

62.5 - A History-Based Auto-Tuning Framework for Fast and High-Performance DNN Design on GPU
Jiandong Mu, Mengdi Wang, Lanbo Li, Jun Yang, Wei Lin, Wei Zhang

62.6 - DRMap: A Generic DRAM Data Mapping Policy for Energy-Efficient Processing of Convolutional Neural Networks
Rachmad Vidya Wicaksana Putra, Muhammad Abdullah Hanif, Muhammad Shafique

62.6 - DRMap: A Generic DRAM Data Mapping Policy for Energy-Efficient Processing of Convolutional Neural Networks
Rachmad Vidya Wicaksana Putra, Muhammad Abdullah Hanif, Muhammad Shafique

63.1 - Wafer Map Defect Patterns Classification Using Deep Selective Learning
Mohamed Baker Alawieh, Duane Boning, David Z. Pan

63.2 - HITTSFL: Design of a Cost-Effective HIS-Insensitive TNU-Tolerant and SET-Filtering Latch for Safety-Critical Applications
Aibin Yan, Xiangfeng Feng, Xiaohu Zhao, Hang Zhou, Jie Cui, Zuobin Ying, Patrick Girard, Xiaoqing Wen

63.3 - Exploring a Bayesian Optimization Framework Compatible with Digital Standard Flow for Soft-Error-Tolerant Circuit
Yan Li, Xiaoyoung Zeng, Zhengqi Gao, Liyu Lin, Jun Tao, Jun Han, Xu Cheng, Mehdi Tahoori, Xiaoyang Zeng

63.4 - DVFS-Based Scrubbing Scheduling for Reliability Maximization on Parallel Tasks in SRAM-based FPGAs
Rui Li, Heng Yu, Weixiong Jiang, Yajun Ha

63.5 - PAIR: Pin-Aligned In-DRAM ECC Architecture Using Expandability of Reed-Solomon Code
Sangmok Jeong, SeungYup Kang, Joon-Sung Yang

63.6 - Tier-Scrubbing: An Adaptive and Tiered Disk Scrubbing Scheme with Improved MTTD and Reduced Cost
Ji Zhang, Yuanzhang Wang, Yangtao Wang, Ke Zhou, Schelter Sebastian, Ping Huang, Bin Cheng, Yongguang Ji

65.2 - Software Defined Accelerators from Learning Tools Environment
Antonino Tumeo, Vito Giovanni Castellana, Marco Minutoli, Joseph Manzano, Vinay Amatya, David Brooks, Gu-Yeon Wei

65.3 - Creating an Agile Hardware Design Flow
Clark Barrett, Kayvon Fatahalian, Pat Hanrahan, Mark Horowitz, Priyanka Raina

65.4 - Chipyard: An Integrated SoC Research and Implementation Environment
John Wright, Colin Schmidt, Paul Rigge, Harrison Liew, Daniel Grubb, David Biancolin, Albert Magyar, Nathan Pemberton, Albert Ou, Howard Mao, Jerry Zhao, Abraham Gonzalez, Sagar Karandikar, Alon Amid, Jonathan Bachrach, Borivoje Nikolic, Krste Asanovic

66.1 - Kite: A Family of Heterogeneous Interposer Topologies Enabled via Accurate Interconnect Modeling
Srikant Bharadwaj, Jieming Yin, Brad Beckmann, Tushar Krishna

66.2 - CDRing: Reconfigurable Ring Architecture by Exploiting Cycle Decomposition of Torus Topology
Liang Wang, Leibo Liu, Xiaohang Wang, Jie Han, Chenchen Deng, Shaojun Wei

66.3 - ZENCO: Zero-bytes based ENCOding for Non-Volatile Buffers in On-Chip Interconnects
Khushboo Rani, Hemangee Kapoor

66.4 - Topological Structure and Physical Layout Codesign for Wavelength-Routed Optical Networks-on-Chip
Yu-Sheng Lu, Sheng-Jung Yu, Yao-Wen Chang

66.5 - Characterization and Applications of Spatial Variation Models for Silicon Microring-Based Optical Transceivers
Yuyang Wang, Jared Hulme, Peng Sun, Mudit Jain, M. Ashkan Seyedi, Marco Fiorentino, Raymond G. Beausoleil, Kwang-Ting Cheng

67.1 - R2D3: A Reliability Engine for 3D Parallel Systems
Javad Bagherzadeh, Aporva Amarnath, Jielun Tan, Subhankar Pal, Ronald Dreslinski

67.2 - Proactive Aging Mitigation in CGRAs through Utilization-Aware Allocation
Marcelo Brandalero, Bernardo Neuhaus Lignati, Antonio Carlos Schneider Beck, Muhammad Shafique, Michael Hübner

67.3 - TAEM: On-Chip Transfer-Aware Effective Loop Mapping for CGRAs
Mingyang Kou, Jiangyuan Gu, Shaojun Wei, Hailong Yao, Shouyi Yin

67.4 - Remote Atomic Extension (RAE) for Scalable High Performance Computing
Xi Wang, Brody Williams, John D. Leidel, Alan Ehret, Michel Kinsy, Yong Chen

67.5 - ATUNs: Modular and Scalable Support for Atomic Operations in a Shared Memory Multiprocessor
Andreas Kurth, Samuel Riedel, Florian Zaruba, Torsten Hoefler, Luca Benini

67.6 - BPU: A Blockchain Processing Unit for Accelerated Smart Contract Execution
Tao Lu, Lu Peng

68.1 - PIM-Assembler: A Processing-in-Memory Platform for Genome Assembly
Shaahin Angizi, Naima Ahmed Fahmi, Wei Zhang, Deliang Fan

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