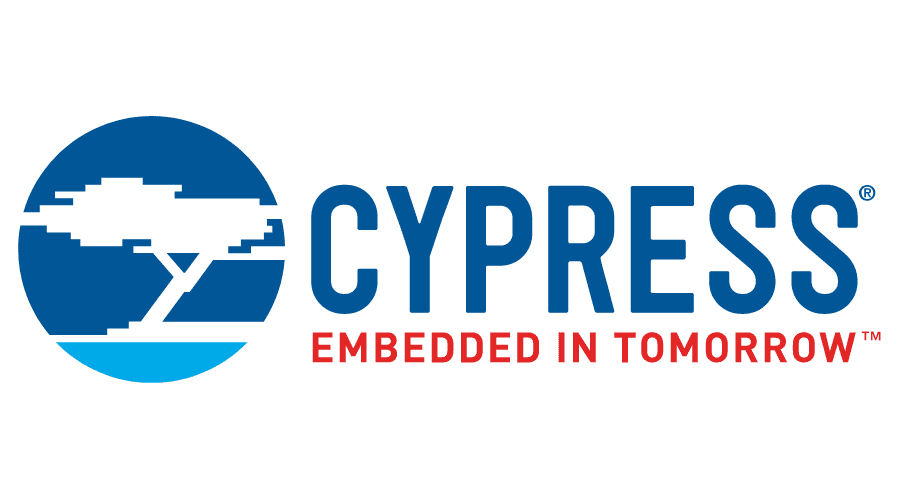
**CYPRESS**



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**CYPRESS Model**

**Manual**

**CYPRESS Model Manual**

Version \*B

**Author:** CYPRESS **Department:** Hardware Systems SEMICONDUCTOR Engineering

**Project:** CYPRESS Model Manual

**Document** Cypress Model Manual.docx **Name:**

**Last Changed:** 1/13/2022

**Distribution:** General Distribution

**Preface:** This document covers Verilog model simulation package

This document contains CYPRESS's technical specifications regarding the products described herein. This document may be revised by subsequent versions or modifications due to changes in technical specifications.

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# Document History

|  |  |
| --- | --- |
| **Version/Date** | **Modification** |
| \*\*: 02/27/2019 | Initial version |
| \*A: 01/13/2020 | Updated AC timing specs.  Fixed the latency issues  Fixed data mismatch at higher frequency  Fixed DPD and HSLEEP Entry Exit issue  Added Partial Refresh  Added Refresh Interval and variable latency feature  Added MPN based AC characteristics selection |
| \*B: 01/13/2022 | updated RWDS logic to check refresh\_pulse during CSNeg event. |

# Overview

The archive contains, model files for Cypress HyperRam Memory (Figure 1: Downloadable Package Contents).

These models support:

* Verilog behavioral simulation for 64Mb cypress’s HyperRam

* Timing-accurate simulation (including support for interconnect path delays)

* Built-in Timing checks

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Downloadable Self Extracting File | | | File  Manual | | ‐documentation (\*.pdf) | | |  | |  | | | Directory Models | | ‐model code (s27kl0642.v)  ‐test benches (HyperBusTestBench.v)  -controller code (hbram\_ctrl.v) | | |  | |  | | |

**Figure 1: Downloadable Package Contents**

The package contains all the necessary preload files, test benches and timing files to get started in your simulation environment.

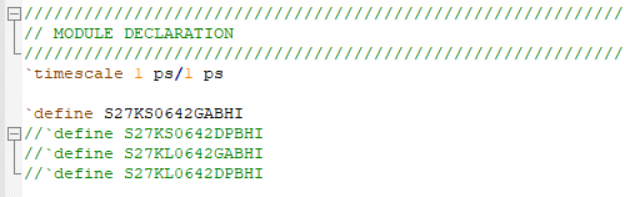
# Verilog – Model

## Required Files

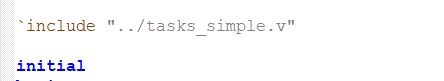
### Files for a Simple Verilog Behavioral Simulation

The model file s27kl0642.v is located in the model directory. It does not depend on other files and can be run as is in a behavioral Verilog simulation.

Depending upon device MPN requirement, user should enable the respective line, which select the AC timing parameters.



Depending on the file locations and project location, please modify the include file path for file “tasks\_simple.v” in “HyperBusTestBench\_simple.v”



## Compiling Model Files

### Compilation of Verilog Model Files

The file s27kl0642.v can be compiled as is. No further libraries need to be provided.

## Simulating Model Files

### Instantiation Template

s27kl0642 DUT (

.DQ7(DQ[7]) ,

.DQ6(DQ[6]) ,

.DQ5(DQ[5]) ,

.DQ4(DQ[4]) ,

.DQ3(DQ[3]) ,

.DQ2(DQ[2]) ,

.DQ1(DQ[1]) ,

.DQ0(DQ[0]) ,

.RWDS(RWDS) ,

.CSNeg(CS) ,

.CK(CK) ,

.CKn() ,

.RESET(dut\_reset)

);

**4 Support**

We appreciate your feedback or suggestions to ensure our models meet your needs. For contacting us, please use cypress forum