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IP Core	Dolby MS11 - (Advanced TSM Post	Notes Works only if few use cases in 40nm chips	Class of chip Chip Specific	72554	7278	7271	7268	72604B0	72604A0	7445S	7439	7250	7364 ☑	7366	7445	7344 ☑	7346 ✓	73465	7425	7231	7358		75525	7429	74295	7360 ☑	7362	73625	7563	75635	7435	7584	75845
	Processing) Dolby MS11 + 2nd Audio Decode Mixing - (AAC-HE 2.0 Channel, AAC- LC 2.0 Channel, MPEG-1 L1/L2/L3 2.0 Channel, Vorbis Audio, WMA 2.0 Channel)	eum uspa	Chip Specific			✓			✓		□						∠ .	N .		~				2		■			✓				
6 6 7	20 Channell Dolby MS12v1.3 - (AC4 (A specific Box mode and ARM officed required), Config A (A specific Box mode and ARM officed sequired), Config B, Config C, Config	Config B (DDP,AAC-HE) + DAPv2	Chip Specific	0	✓	☑			✓	≥	✓	✓	≥	✓	₩			0		-			-		0							0	-
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	stereo, MPEG4 stereo) MPEG Audio Descriptor		Chip Specific			<u> </u>		☑	2			2	<u> </u>		2	2	■		2		Ø			V		2		2	N N	- Z		2	
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	MALER Real Audio LBR iLBC		Chip Specific Chip Specific			V V	2	☑	V	V V		V	V			2	V	N N	V	✓	V	V V	Z	V	V V	V V	N N	2	\ \ \ \ \ \ \	2	2	2	<u> </u>
	ISAC SRS - (TruSurround, TruVolume)		Chip Specific Chip Specific			- M	2	2	2	2		✓	✓	2	2	2	✓	V		✓	✓	V	✓								2	2	Z
	Windows Media - (WMA (wLSF, QSF), WMA Pro) ATSC A/85 volume leveling		Chip Specific Chip Specific										2			2	✓					2			✓	Z	V	V	2	<u> </u>		Z	Ø
	Audio Decoder Fade effect Broadcom - (3D surround, AVL)		Chip Specific Chip Specific	H	H	<u> </u>	V	V	V	✓	V	V	V		V V	V	V	V	V	×	V	×	✓ ✓	V V	V	V	V	V V	N N N	7	2	<u> </u>	- W
			Chip Specific Chip Specific			☑	2		✓	V	2	2	Ø	<u> </u>	N N	2	~	V	N N	~	Ø	✓	✓			Z	N N	N	2	Z Z		Z	2
Audio Post Process	Clear Victice - (CV3) Dolby - (DDRE, DV-258, Prot.ogicil), bothyrough of the Community of t		All 28nm and 40nm										<u>□</u>	2			✓									☑				<u> </u>			
	Karaoke support - (Karaoke Decode processing, Karaoke Vocal processing)		Chip Specific				☑			✓		☑	☑			☑	✓			☑					☑	☑		☑	☑	$\overline{\mathbf{z}}$	☑	☑	☑
	PCM Mixing Ramping Mute		All 28nm and 40nm All 28nm and 40nm All 28nm and 40nm	V	V	✓	2	2	✓	V	V	2	~	V	2	Z Z	~		N		V			V	V	✓	V V	V				✓	
	SRC SRS - (SRS-TruVolume, SRS-TSHD)		All 28nm and 40nm Chip Specific Chip Specific			<u> </u>	V	Z Z	N	V	V	✓	∀	V	N N	2	V	\ \ \	N N	✓	<u> </u>	2	V	N		✓	KK	V	V	V	V	N N	
ŕ	AAC-HE AAC-LC		Chip Specific Chip Specific Chip Specific			V	V V	~	×	V V	V V V V V V V V V V V V V V V V V V V	~	V V	N	N	V	V V V	KK	N	× ×	Z Z		V V				KK		× ×	V V	N N N		
	AMR BTSC				<u> </u>												V					Z		V				N				V	
Audio Encoder E	DTS - (5.1) Enh AAC+ G.711/G.726		Chip Specific Chip Specific Chip Specific			2	2	2	2	2	<u> </u>	2	✓	2	2	Z Z	2	V V	N	2	2	2		V	Z Z	2	V	N N		✓	2	2	
	G.711/G.726 G.729 MPEG Layer3		Chip Specific					<u> </u>	<u> </u>	2	<u> </u>	2	2			2		V V	<u> </u>	2	2	2		V	✓	<u> </u>	V	N	<u> </u>	<u> </u>		<u> </u>	
	AAC-HE		Chip Specific Chip Specific Chip Specific Chip Specific Chip Specific	H	2	<u> </u>		1 2 2 2 2	<u> </u>	<u> </u>	V V	2	V	<u> </u>		<u> </u>	× × ×	V		> >	2	2	> > >	V	<u> </u>	V V	N N	2		<u> </u>		<u> </u>	
Audio Transcoder A	MP3 IEEE-1394 LPCM		Chip Specific Chip Specific	Ä			2	<u> </u>		<u> </u>			<u> </u>	Ø	<u> </u>		V	N N		V		2					<u> </u>	<u> </u>		<u> </u>			
Audio Transcoder (Pass-Through)	AAC-HE v1 (SBR) (Stereo/Mono) (16-48kbps)		Chip Specific	-	2	2	Ø	V		V	2	☑	Z	Ø		Ø	Ø.	V		V				Ø	V	Z	N	V	2	Z	Z		×
(Pass-Through) A	AAC-LC (Stereo/Mono) (16-320kbps) MP3 (Stereo/Mono) (32-320kbps)		Chip Specific Chip Specific		V	×	V	V	N N	KK	V V V V V V V V V V V V V V V V V V V	> >	\ \ \	N	N	KK	V V	KK	N	V	V	Z	N N	> >	Y Y	V	KK	N	N	y y	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V	V
	Trickmodes rates (0.5x to 2.0x) Decode to memory (for Android)		All 28nm and 40nm Chip Specific			☑	2		☑	Z Z	V V	<u>N</u>	Ø	~		<u> </u>	<i>V</i>	V	☑	2	2	V	✓	✓	✓	☑	V V	N	✓	Z		☑	<u> </u>
Audio System level features	6 NRT passthrough PCM input over I2S		Chip Specific Chip Specific Chip Specific													2	✓		2	Z	2	2		✓	Z Z	~	V						
i i	Compressed input over HDMI/SPDIF input		Chip Specific Chip Specific			✓	2	2	✓	Z	2	✓	✓	Ø	N	Z	✓		2	✓	2				<a>	Z	N N	N	V	2			✓
	Splicing support Player - UDP, RTP, RTSP, RTCP, HTTP, HLS, Limited DASH Player security - DTCP-IP, SSL/TLS, AFR		All 28nm and 40nm	V	2		Ø	<u> </u>		Ø		A	Ø	Ø		Z	V	N		Ø	Ø			Ø	V	Z	N	V		Z			Ø
	Player security - DTCP-IP, SSL/TLS, AES		All 28nm and 40nm	✓				☑		☑		☑	☑	✓		Z	☑	N		☑				✓	☑	☑	<u> </u>	✓	☑	≥		☑	☑
	Player - receiving from Home Server, from OTT/Cloud Server Player - IP clock recovery		All 28nm and 40nm All 28nm and 40nm	2		✓	2	2	✓	Z	2	✓	✓	Ø	2	Z	✓	✓	2	✓	2				<a>	Z	Z	2	✓	2	2	Z	✓
IPTV-BIP F	Player - IP clock recovery Player - IP record, playback and client/server side trick-modes Server - UDP, RTP, RTSP, HTTP, HLS, Limited DASH		All 28nm and 40nm	V		☑	☑	☑			V	☑	☑	N	N		$ \mathbf{v} $		N	≥	☑			☑	abla	☑	V			~		☑	✓
	Server - UDP, RTP, RTSP, HTTP, HLS, Limited DASH Server security - DTCP-IP, SSL/TLS, ACO		All 28nm and 40nm All 28nm and 40nm	2	✓	V		∅	V V	N N			V	✓	2	× ×	✓	V			✓			2		y V	KK	N N	V	N N	N N	V	N N
	Server - ASP offload		Chip Specific											-				П			- 0	0											
	SES SAT>IP 1.2 spec DTCP-IP implementation based on DTI & sner- 'DTCP V1 Rev 1.7 FD2		All 28nm and 40nm All 28nm and 40nm	V		Z	Z	2		V	2	2	Z			Z	V	N N	N N	~	V	2			<a>	~	N N	N N		V		V	~
	& DTCP V1SE IP Rev 1.4 EDS Option to run the library in HOST-						 	_														_	_	_									_
0	DTCP-IP implementation based on DTLA spec, 'DTCP V1 Rev 1.7 ED2 & DTCP V18 IP Rev 1.4 ED5 Option to run the library in HOST- only mode or SAGE mode (All chypto- operations and Confisiential information is handled on SAGE) Support for DTLA Format 3 & Format 5 Kersi.		All 28nm and 40nm All 28nm and 40nm		2	✓	2		✓	2			2				V	V		V				<a>		2			V	2		2	
DTCP-IP	Full Authentication support for both Source and Sink devices. (Restricted		All 28nm and 40nm				2				✓	Z	☑	2		■	✓			✓	☑		_	Z	Z	☑	☑		■	₩	☑	☑	
	Support for Nexus multi-process		All 28nm and 40nm	2								⊠	☑				☑			✓			2							Z			2
	mode Support for SRM update via other compliant devices Support for Additional Localization via RTT		All 28nm and 40nm	⊠	☑	☑	፟			⊻		⊠	☑		N		✓		N	⊠			☑	☑		☑			☑	V		☑	
	Support for Additional Localization via RTT PVR encryption - (3DES, AES, DES)		All 28nm and 40nm All 28nm and 40nm	✓			2	Z		2	✓	2	≥	2		 ☑	✓	V		✓			✓	2	V	 ✓	V	2	V	V			
	PVR tribypion - (3DES, AES, DES) PVR TSM Record - (AVC, MPEG2, MPEG4, MVC, SVC)		All 28nm and 40nm All 28nm and 40nm	V V	V V		V		V	N N	V	V	<u> </u>	V			×	V V V	N N	V	Ø		<u> </u>		V	Z Z	N N	2	V	<u> </u>	N N		
	MVC, SVC) STC rate based trickmode Timeshift - (AVC, MPEG2, MPEG4,		All 28nm and 40nm	Ø	☑			☑	☑	☑			✓	Ø	V	Ø	☑			Ø	Ø	☑					☑	☑		Ø	☑	2	✓
PVR N	Timeshift - (AVC, MPEG2, MPEG4, MVC, SVC) Trick mode - (AVC, Decoder		All 28nm and 40nm			☑							☑				☑			☑									☑	☑			
to E	trickmode, Display Queue Trickmode (DQT), DSDLA with audio, Fast Forward, HEVC, Host trickmode, Host trickmode wio index on MPEG- 2, MPEG2, MPEG4, MVC, playback, Rewind, Slow motion, Smooth 1x		All 28nm and 40nm					✓		☑				✓		☑				✓	⊌								☑				✓
1 !:	using muser, DVL, VFV)	Supported on 64 bit ARM systems. See datasheet	Chip Specific	2			■	2												-													
	32/64 mixed mode	See datasheet			_																												
	32/64 mixed mode AC3+ down-convert API to control audio output	See datasheet	All 28nm and 40nm All 28nm and 40nm	Ø		☑	✓		✓	N N	V	V	✓	V	N	2	V	N N	V	Z Z	2			2	V V	2	N N	N N	∀	Z Z	Z Z	2	2

IP Core	Feature	Notes	Class of chip	72554	7278	7271	7268	72604B0	72604A0	7445S	7439	7250	7364	7366	7445 7344	7346	73465	7425	7231	7358	7552	75525	429	74295 7360	7362	73625	7563 75635		7584 75845
	Audio Equalizer support	December on objection mode. See	All 28nm and 40nm																										
	Audio Primer for fast main/PIP audio swap	box mode PPT.	Chip Specific												0 0									0 0					
	Auto Volume Level Callback for display changes		All 28nm and 40nm All 28nm and 40nm	- W	- E	✓	- E		- Z	V	W	<u> </u>	✓	<u> </u>		- E	<u> </u>	V	<u> </u>	[2]	▼	<u> </u>	Ø		✓	V		<u> </u>	
	Display VBI functions		All 28nm and 40nm			Ž	- Z		Z	- Z	- Z	Ž	Z	2			2	V			Ž			V V		2	Z Z	2	
	Explicit PIP window support	Depends on chip/box mode. See box mode PDF	Chip Specific																										
NaClient Multinoscope	HDCP Revocation list HDMI input encoding supporting (included rework of resclient hidmi input api)		All 28nm and 40nm		☑					☑		☑	☑												☑		2 2		2
library	HDMI input encoding supporting (included rework of rectient hdmi		All 28nm and 40nm											✓				$\overline{\mathbf{v}}$			⊠	☑	☑		☑				
	input api) Macrovision	+	All 28nm and 40nm	2		V			V	Z								$\overline{\mathbf{v}}$				⊠	Ø		☑				
	Main/PIP video swap	Depends on chip/box mode. See box mode PDF	Chip Specific																										0 0
	MS12	1	All 28nm and 40nm								2	Z						Z		2	Z			Z Z		2			
	NRT (non-real-time) transcode	All chips with VCE . See datasheet.	Chip Specific																										
	Nxserver external app mode		All 28nm and 40nm			✓		✓		✓		✓	✓	2				$\overline{\mathbf{v}}$			☑	☑	Ø	V V	✓		Z Z		
	Per-output audio volume control		All 28nm and 40nm All 28nm and 40nm	- Z	✓	☑		<u>⊠</u>			<u>⊠</u>	⊠		2				<u> </u>		⊠	⊠				<u></u>	<u> </u>		<u> </u>	
	Picture quality adjustments PIP mosaic	Depends on chip/box mode. See box mode PDF	Chip Specific																					0 0			0 0		0 0
	SCMS for SPDIF	Dox mode PUF	All 28nm and 40nm			- M	100	- E	- E	- E	100	- E	- E	- E		- 10	- E	- E	- E	- E	- FI	- E	8		- E	- E		- E	
	Thermal Monitor		All 28nm and 40nm							2		× ×	2					₹			Ø		Ø	V V			Z Z		
	Video-as-graphics	Por Moto descriptor	All 28nm and 40nm All 28nm and 40nm Chip Specific		- I	<u> </u>	V	<u> </u>		☑	E2	<u> </u>						<u> </u>					Ø		<u> </u>				
BRCM Demo Application	High Dynamic Range application	Box Mode dependent	Chip Specific			Ž	- 2		Ž		Ö	ä	<u> </u>	Ö				ä		ö	ä		ă		l ii	- 6		ä	<u> </u>
	DolbyVision - (5, 8.1, 8.2, 8.3, 8.4,	Box Mode dependent	Chip Specific			$\overline{\mathbf{v}}$									0 0												0 0		0 0
Hinh Dynamic Ranne	8.5, 9) HDR10/HLG/SDR (Pass-through and Conversion)	d Box Mode dependent	Chip Specific		☑	☑	■	☑	V						0 0									0 0			0 0		0 0
High Dynamic Range (HDR)	HDR10/HLG/SDR (Pass-through		Chip Specific		_	-	 	-	-				2							0	0			0 0		0	0 0	_	0 0
	only) Technicolor HDR Prime - (v1.4)	Roy Mode descriptors	Chip Specific								- N						0			0	Н	-			H H			0	
	CableCARD stack - (Basic,	For 7278, only support 3158 legacy OOB	Chip Specific		2				-	- M	2									0	-	-			0	-	0 0	□ □	0 0
	CableCARD stack - (Basic, Basic+DSG, Basic+DSG+OOB) DOCSIS Firentend - (DSG, dual band WFI, E-Router, LNA control, OOB, RMAGNUM, SNMP, VOIP, WIFI (2.4	regacy OOB						_		1																-			
1	WIFI, E-Router, LNA control, OOB, RMACNIM SNMP VOIP MISS 22.4	I	Chip Specific				✓						l					$\overline{\mathbf{v}}$					✓						
1	GHz)) DSG Client Controller DSG Clients	1		1									1						1 1								- 1		
Cable FE	DSG Client Controller, DSG Clients DVB-C - (fast channel scan, tuning)	_		R		+ 8		H 8-			- M	<u> </u>	-							R	R						+ + =		
1	FrontEnd Power Management	Supported for 3384/33843 but not	All 28nm and 40nm																	0									
	OCAP Host MIB/SNMP	3383	All 28nm and 40nm	1	1 0	+ -		1 0					l i			+ +			+ + +		- -	-	_		- i			+ 11	1 1 1
1	QAM Tuning	7584 platform, only supports	Chip Specific	-	0	-		0		- Z						1 5		<u> </u>		0	0				0	0	0 0		
	Discounty 2.6	docsis2.0 40nm host based only	All 28nm and 40nm	-					■			- ✓						2			2					2			
1	Playready 3.x Widevine		28nm Only All 28nm and 40nm	✓	V	✓	V	V	✓	✓	Ø	✓	Z.	✓				0							Ó				
1	Widevine	40nm host based only 40nm host based only	All 28nm and 40nm			- Z														Ø		Z				<u> </u>		2	
1	DTCP-IP	40nm host based only 40nm host based only	All 28nm and 40nm All 28nm and 40nm		✓	<u> </u>	>			<u> </u>			2						5			Ø							
	HDCP 2.2		28nm Only			✓		☑	✓				Z	2														8	
SAGE	SVP 2.6	secure graphics New SoC with HDR Static DTU Available Secure HDMI Rx AV FW auth get API	28nm Only	_								_ ⊠	-		rid .					0									<u> </u>
1	SVP 2.7	Static DTU Available Secure HDMI Rv	1	✓	$\overline{\mathbf{v}}$	✓	✓		☑	☑	☑		✓	✓															0 0
1	one	AV FW auth get API	28nm Only 28nm Only	-			✓									1												+	_ _
	TZ based Audio		Chin Sperific									<u> </u>		- M	<u> </u>			-		H	- 1		н	- 	- 1	-	- 		*
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	SAGE Unified Image Format	Non Real Time	Chip Specific Chip Specific		- I	- 8		- 8				- 8					- 8				8		8						8 8
	Operation Modes	Real Time	Chip Specific		V	- 6				1 5		H					H	Ž		Н		- 6	Н			- 6			
	A/V Sync		Chip Specific Chip Specific		V									Ø				✓		8			ă l					Ž.	
	Software Extensible Mux Support	Audio Codecs: AAC-HE. AAC-LE	Chip Specific				+ -			+ -		Ш						~		Ш	ш		ш						
	MP4 File Mux : Codecs	Audio Codecs: AAC HE, AAC LE Video Codecs: H264/AVC, MPEG4Part2	Chip Specific								☑			✓															
	MP4 File Mux : Features	MPEG4Part2 Features: Progressive Download, Single Audio, Single Video Audio Codecs: AAC-HE, AAC-LE,	Chip Specific		☑													✓						0 0			0 0	2	0 0
		Audio Codecs: AAC-HE, AAC-LE,			_			_		+						_					_		_						
	TS Stream Mux: Codecs	Video Codecs: H284/AVC,	Chip Specific								₩.			⊠				\checkmark											
		AC3, LPCM, MP3, MPEG2 Video Codecs: H284AVC, MPEG2, MPEG4Part2, H265/HEVC		1																									
		Audio PES packing	Chip Specific		V						V		-			0		~											
		video/audio PIDs Initial PTS configurable in NRT	Chip Specific		☑													☑											
		Initial PTS configurable in NRT mode	Chip Specific															$\overline{\mathbf{v}}$									0 0		0 0
		Multiple Audio PIDs	Chip Specific											Ø				☑										2	
		PCR generation Per segment PTS insertion	Chip Specific Chip Specific	-	- V	+ +	+ +	- H		+ +	V	+ +		V		-		V V	-	-	+		H	- 	- $+$ $ +$		- H - H -	V V	
	TS Stream Mux: Features	PES stream of VBI User Data Pass Through (ETSI en 300 472 and SCTE 127)	Chip Specific		_						_			_									_					_	
		and SCTE 127)			☑						☑			☑				☑						0 0				☑	
		Single MCPB Channel Mode Single Video PID	Chip Specific Chip Specific		<u>⊠</u>		+			 	<u> </u>												<u>-</u>						
		System Data Insertion (e.g.	Chip Specific		□			-		-	2			2						0	0					0	0 0	□ □	0 0
1		TTS 4-byte timestamp (Binary)		-		+ -	1 -	10		+ -	- E	<u> </u>	+ -			+ -			+ +		-	 	_	- 1 - 1	-		 		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1		TTS 4-byte timestamp (MOD300)	Chip Specific Chip Specific		Z	ŏ		ŏ	ă			ă					ŏ	V					Ô					Z	
		H264/AVC MPEG2		-	✓	+ -	+	H B		+ -	W		-					V		8			H	+ + -			+ + -	E2	
1	Codore	MPEG4Part2	Chip Specific Chip Specific								Ö	_ =		Ö			<u> </u>	<u> </u>		ŏ	ä	<u> </u>	ă.		ŏ	- 6		2	
1		VP8 H265/HEVC	Chip Specific				1 8	1 8		1 -		- 8	+ =			1 8		-		8	8				- 8	-8		- 8	
1		VP9	Chip Specific Chip Specific	 	Z	+ =	1 -	 		+ =	H	 	1 -		 	1 8	H	- 1	 	H	H		H		H			1 5	
	Bit Rates	CBR	Chip Specific													1 0	<u> </u>	<u> </u>											
1		VBR Bit Rate	Chip Specific Chip Specific	 	 ✓	+ +	+ +	+ +	+ +	+ +	- E2	 H	+ +	✓		+ 8	H H	<u> </u>	+ + +	H	H	++	H	+ + +	$\vdash \vdash \vdash$	-	+ + -	Ø	
1	Dynamic Settings	Frame Rate GOP Structure	Chip Specific		V			Lŏ				L ö					ŏ	2		ŏ	ă		ō.	ă l ă	ŏ	ŏ			
Transcode	, ,	GOP Structure	Chip Specific Chip Specific							1 -			H =			1 2		<u> </u>		8									H - H
		7.5	Chip Specific	-		- 5	1 6	1 8		1 5	5	H	1 5					<u> </u>		ä			ä			- 6			
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1	Communication Communication	15	Chip Specific Chip Specific Chip Specific	_ ŏ				L ö			Ø	_ ö		2			ŭ			ŏ	ŏ		ă.		ŏ	ŏ			
1	Frame Rate Conversion (analog equivalent also supported)	20	Chip Specific											2															
1		25	Chip Specific Chip Specific	 	- Z	+ +	+ +	 H	+ +	+ +	[Z]	 H	+ +			+ #	H	<u> </u>	+ + +	H	+		H	 	H	-	 		
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	GOP Structure		Chip Specific Chip Specific Chip Specific	_ ŏ	Ø	l ö		l ö	Ĭ			ŏ					ŏ	ŏ		ŏ	ŏ	ŏ	ō		ŏ	ŏ		Ö	
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	GOP Structure Max Resolution	1280x720 1920x1080	Chip Specific						ŭ																				
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	Max Resolution Scan Type	1280x720 1920x1080 Progressive Interfaced HRD	Chip Specific Chip Specific Chip Specific Chip Specific		V V						Z Z			Ø Ø		1 8		2											
	Max Resolution	1280x720 1920x1080 Progressive Interlaced HRD Segment Mode	Chip Specific		>						V V V V V V V V V V V V V V V V V V V			V V				> > >											
	Max Resolution Scan Type Rate Control	Progressive Interfaced HRD Segment Mode 3D Data (ARIB spec STD-832)	Chip Specific								\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \							> > > > > > > > > > > > > > > > > > >											
	Max Resolution Scan Type	Preset Lutinous 1280x720 1920x1080 Progressive Interfaced HRD Segment Mode 3D Data (ARIB spec STD-832) AFD Data Bar Data	Chip Specific								\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \							>											
	Max Resolution Scan Type Rate Control	Preset Lutinous 1280x720 1920x1080 Progressive Interfaced HRD Segment Mode 3D Data (ARIB spec STD-832) AFD Data Bar Data	Chip Specific								\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \							>											
	Max Resolution Scan Type Rate Control	Progressive Interfaced HRD Segment Mode 3D Data (ARIB spec STD-832)	Chip Specific								\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \							X											
	Max Resolution Scan Type Rate Control	Prests Lottlewin 1280/C/20 1520/c/1050 Progressive Intertaced HRD Segment Mode 3D Data (ARIB spec STD-832) AFD Data Bar Data Closed Captoning LASS MPEGG for ATSC)	Chip Specific								N N N N N N N N N N N N N N N N N N N																	V V V V V V V V V V V V V V V V V V V	
	Max Resolution Scan Type Rate Control	Prests Lottlewin 1280/C/20 1520/c/1050 Progressive Intertaced HRD Segment Mode 3D Data (ARIB spec STD-832) AFD Data Bar Data Closed Captoning LASS MPEGG for ATSC)	Chip Specific								\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \																		

IP Core	Feature	Notes	Class of chip	72554	7278	7271	7268	72604B0	72604A0	7445S	7439	7250	7364	7366	7445	7344	7346	73465	7425	7231	7358	7552	75525	7429	74295	7360	7362	73625	7563	75635	7435	7584	75845
	Closed Caption User Data: Service	CEA608 (line 21 analog CC)	Chip Specific		V									N					V														
	Standards	CEA708 (DTVCC)	Chip Specific		N						V			V	N				K												N		
	Low Delay Mode	Fast Channel Change (aka Adaptive Low Delay)	Chip Specific								☑			☑																			
	Aspect Ratio Conversion		Chip Specific		V									₩.					✓														
	Video and Crashins Composition		Chin Specific		FF2						FP2			FF2	FF2				FF2												192		