

JUSTIN COPPOLA

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EDUCATION

University of Florida

Gainesville, FL

Bachelor of Science in Electrical Engineering / GPA: 3.30

May 2025

- **Awards/Honors:** 2022 Dean's List, Order of the Eastern Star scholarship recipient, Mensa Society
- **Relevant Coursework:** Machine Learning Applications, SoC Design, Reconfigurable Computing, Microprocessor Applications, Digital Logic and Computer Systems, Hardware Security and Trust

TECHNICAL SKILLS

Programming & Coding: SystemVerilog, Verilog, VHDL, Python, C, C++, Assembly, MATLAB, HTML

Tools & Environments: Vivado, ModelSim, Verdi, Quartus, Cadence, Git, Linux (CLI), MATLAB, LTSpice, Altium

Hardware Design: RTL Design, FPGA Development, Testbench Creation, Assertions, Design Verification, UVM

Software & Scripting: REST APIs, OAuth Authentication, Linux Automation, Bash/Python Scripting

PROFESSIONAL EXPERIENCE

Intel Corporation

Hillsboro, OR

Front-End RTL Design Engineering Intern

May 2024 – August 2024

- Spearheaded the design of a new RTL sub-IP bridging debug and functional control interfaces for next-generation CPU designs by reverse engineering legacy systems, enabling migration to industry-standard DFT tools
- Developed a comprehensive SystemVerilog testbench suite with in-line assertions, automated simulation flows using Linux shell scripting and verification via Vivado and Verdi environments to enhance RTL validation
- Independently rebuilt critical IP tooling, replacing outdated Perl scripts with Python workflows used for parsing IP RDL metadata into user-friendly CSVs, enhancing internal IP deliverables across Intel business units
- Delivered a fully validated and documented RTL IP solution that accelerated internal testing cycles, reduced validation runtime and enabled adoption of industry-standard DFT tools across multiple product lines

L3Harris Technologies

Palm Bay, FL

Electrical Digital Design Engineering Intern

May 2023 – August 2023

- Conducted comprehensive FPGA timing verification for a wideband processing card's SPI communication between the primary FPGA and peripheral devices, ensuring reliable satellite communication after launch
- Simulated and optimized multilayer PCB signal integrity, mitigating reflection and overshoot and completed advanced FPGA verification training specializing in testbench creation and clock domain crossing techniques

Element Solutions | MacDermid Alpha Electronics Solutions

Johns Creek, GA

Research and Development – Electrical Engineering Intern

May 2022 – August 2022

- Updated and enhanced technical datasheets through ASTM and MIL-STD quality control experiments on semiconductor and circuit card manufacturing materials, driving greater customer confidence and product sales
- Identified potential performance improvements that informed next-generation R&D product initiatives

PROJECTS

MIPS Processor (32-bit CPU) | VHDL, FPGA Prototyping

Spring 2023

- Designed a fully functional 32-bit MIPS processor supporting arithmetic, memory access and branching operations, verified with exhaustive VHDL testbenches and deployed onto FPGA hardware
- Leveraged ModelSim tools for functional verification and optimization of the datapath for minimal latency

Autonomous Car SoC System | SystemVerilog, Python, OpenCV

Spring 2024

- Led SoC design and integration for an autonomous car, developing an image processing pipeline in Python with OpenCV for lane detection and SystemVerilog-based motor control logic, enabling real-time vehicle navigation
- Translated processed sensor input into autonomous motor control actions through state machines

Pong Game on FPGA (Pynq-Z2 Board) | SystemVerilog, HDMI Video Output

Spring 2024

- Built a fully playable Pong game using SystemVerilog featuring ball movement, collision detection, paddle control and real-time scoring updates displayed over HDMI using timing synchronization for seamless input
- Fostered efficient collaboration and communication with design group through git and Microsoft teams

LEADERSHIP AND INVOLVEMENT

Theta Tau Professional Engineering Organization

Gainesville, FL

Leadership Chairman

December 2021- Present

- Organized high-visibility engineering organization events focused on risk management, inclusivity and professional development and mentored successive leadership cohorts ensuring continued success