JUSTIN COPPOLA

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EDUCATION

University of Florida **Gainesville, FL**
Bachelor of Science in Electrical Engineering | GPA: 3.30 *May 2025*

- **Awards/Honors:** 2022 Dean's List, Order of the Eastern Star scholarship recipient, Mensa Society
- **Relevant Coursework:** Machine Learning Applications, SoC Design, Reconfigurable Computing, Microprocessor Applications, CAD for Hardware Security Validation, Hardware Security and Trust

TECHNICAL SKILLS

Programming & Coding: SystemVerilog, Verilog, VHDL, Python, C, C++, Assembly, MATLAB**,** HTML
Tools & Environments: Vivado, ModelSim, Verdi, Quartus, Cadence, Git, Linux (CLI), MATLAB, LTSpice, Altium
Hardware Design: RTL Design, FPGA Development, Testbench Creation, Assertions, Design Verification, UVM, TCL
Software & Scripting: REST APIs, Linux Automation, Bash/Python Scripting

PROFESSIONAL EXPERIENCE

Intel Corporation **Hillsboro, OR**
Front-End RTL Design Engineering Intern *May 2024 – August 2024*

- Led the design of a new RTL sub-IP bridging debug and functional control interfaces for next-generation CPU designs by reverse engineering legacy systems to enable migration to new industry-standard DFT tools
- Developed a comprehensive SystemVerilog testbench which leveraged assertions and Linux shell scripts for simulation and verification via Vivado and Verdi tools such as linting, CDC analysis, and static design checks
- Rebuilt critical IP tools in Python to replace outdated Perl scripts used in parsing my team's RDL metadata into user-friendly CSVs to improve clarity of deliverables to other Intel IP teams, greatly expediting design processes
- Delivered a fully validated and documented RTL IP solution that accelerated internal testing cycles, reduced validation runtime and enabled adoption of industry-standard DFT tools across multiple product lines

L3Harris Technologies **Palm Bay, FL**
Electrical Digital Design Engineering Intern *May 2023 – August 2023*

- Conducted comprehensive FPGA timing verification for a wideband processing card's SPI communication between the primary FPGA and peripheral devices to ensure reliable satellite communication after launch
- Completed FPGA verification training specializing in testbench creation and clock domain crossing techniques
- Simulated and optimized multilayer PCB signal integrity, mitigating reflection and overshoot

Element Solutions | MacDermid Alpha Electronics Solutions **Johns Creek, GA**
Electrical Engineering Intern *May 2022 – August 2022*

- Updated and enhanced technical datasheets through ASTM and MIL-STD quality control experiments on semiconductor and circuit card manufacturing materials to drive greater customer confidence and product sales
- Identified potential performance improvements that informed next-generation R&D product initiatives

PROJECTS

MIPS Processor (32-bit CPU) | VHDL, FPGA Prototyping *Spring 2023*

- Designed a fully functional 32-bit MIPS processor supporting arithmetic, memory access and branching operations, verified with exhaustive VHDL testbenches and deployed onto FPGA hardware
- Leveraged ModelSim tools for functional verification and optimization of the datapath for minimal latency

Autonomous Car SoC System | SystemVerilog, Python, OpenCV *Spring 2024*

- Led SoC design and integration for an autonomous car by developing an image processing pipeline in Python with OpenCV for lane detection and SystemVerilog motor control logic to enable real-time vehicle navigation
- Translated processed sensor input into autonomous motor control actions through state machines

Pong Game on FPGA (Pynq-Z2 Board) | SystemVerilog, HDMI Video Output *Spring 2024*

- Built a fully playable Pong game using SystemVerilog featuring ball movement, collision detection, paddle control and real-time scoring updates displayed over HDMI using timing synchronization for seamless input
- Fostered efficient collaboration and communication with design group through git and Microsoft teams

LEADERSHIP AND INVOLVEMENT

Theta Tau Professional Engineering Organization **Gainesville, FL**
Leadership Chairman *December 2021- Present*

- Organized high-visibility engineering fraternal events focused on risk management, inclusivity, professional development and mentored future leadership colleagues ensuring continued success