Assignment 1 – Introduction to Computer Systems
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s3855159

Task 1 – Number Systems.

a) Convert student number to binary (S3855159)

Equation	Quotient	Remainder
3855159/2	1927579	1
1927579/2	963789	1
963789/2	481894	1
481894/2	240947	0
240947/2	120473	1
120473/2	60236	1
60236/2	30118	0
30118/2	15059	0
15059/2	7529	1
7529/2	3764	1
3764/2	1882	0
1882/2	941	0
941/2	470	1
470/2	235	0
235/2	117	1
117/2	58	1
58/2	29	0
29/2	14	1
14/2	7	0
7/2	3	1
3/2	1	1
1/2	0	1
Answer = 1110101101001100110111_2		

b)

    a. Convert binary string of RMIT student number to octal.

       001 110 101 101 001 100 110 111_2

        1   6 5   5   1   4   6   7 _8

    b. And hexadecimal.

       0011 1010 1101 0011 0011 0111_2

        3   A   D   3   3   7 _16

c) Convert student number to base 13.

Equation	Quotient	Remainder(Decimal)	Remainder(Base 13)
3855159/13	296550	9	9
296550/13	22811	7	7
22811/13	1754	9	9
1754/13	134	12	C
134/13	10	4	4
10/13	0	10	A
Answer: A4C979_13			

d)

    a. Add 39_10 to student number. Convert to base 13.

       3855159 + 39 = 3855198

Equation	Quotient	Remainder(Decimal)	Remainder(Base 13)
3855198/13	296553	9	9
296553/13	22811	10	A
22811/13	1754	9	9
1754/13	134	12	C
134/13	10	4	4
10/13	0	10	A
Answer: A4C9A9_13			

    b. Why was this easy?

       Because after the second digit, the rest of the digits were the same as the first conversion. The only digit that has changed is the second (7 to A).

e) Add together two base 26 numbers.

		P = 16		16		P
C = 2	+	E = 5	=	7	Base 26	G
O = 15		E = 5		20		T
Answer = CO_26 + PEE_26 = PGT_26						

Task 2 – Binary Addition and Subtraction.

a) Convert A_10 and B_10 to 4-bit binary, add together and state whether answer is valid to 4-bit binary.

Value	Decimal	Binary
A	10	1010
B	11	1011

Carry	1		1		
		1	0	1	0
+		1	0	1	1
=		0	1	0	1

This is not a valid equation while adding two binary numbers using only four bits as the answer is 21, the highest value that can be represented is 15, and the final carried value is lost.

b) Convert A_10 and B_10 to 6-bit binary. Using two's compliment show how to:

a. Subtract the two binary numbers A + (-B).

A = 10 = 001 010
B = 11 = 001 011

Find two's compliment of B.
B   = 001 011
1's = 110 100
2's = 110 101

Subtract B from A.
  001 010
+ 110 101
= 111 111

b. Translate the binary result back to decimal.

X   = 111 111
1's = 000 000
2's = 000 001
X   = -1_10

Task 3 - Bitwise Operations.

a) Set bit 0, bit 7 and leave the rest untouched.

```
A     = XXXX XXXX
O     = OR
M     = 1000 0001
A     = 1XXX XXX1
```

b) Make sure that bit 1 and bit 6 are reset, and all others are set.

```
A     = XXXX XXXX
O1    = AND
M1    = 1011 1101
A1    = X0XX XX0X
O2    = OR
M2    = 1011 1101
A2    = 1011 1101
```

c) Toggle the values of the middle four bits and set the 2 bits on each side.

```
A     = XXXX XXXX
O1    = XOR
M1    = 0001 1000
A     = XXX/X /XXXX
O2    = OR
M2    = 0010 0100
A     = XX1/X /X1XX
```

Task 4 – Logic Circuits and Truth Tables.

Write down the equivalent logic expression.

   /(/((A.B).(A.C))^(B+/C))

a) Write a truth table that shows the final outputs for A, B and C.

A	B	C	/C	A.B	A.C	B+/C	(A.B).(A.C)	/(A.B).(A.C)	/(A.B).(A.C)^(B+/C)	/(/(A.B).(A.C)^(B+/C))
0	0	0	1	0	0	1	0	1	0	1
0	0	1	0	0	0	0	0	1	1	0
0	1	0	1	0	0	1	0	1	0	1
0	1	1	0	0	0	1	0	1	0	1
1	0	0	1	0	0	1	0	1	0	1
1	0	1	0	0	1	0	0	1	1	0
1	1	0	1	1	0	1	0	1	0	1
1	1	1	0	1	1	1	1	0	1	0

a) Write down the equivalent logical expression.

   (/A.B)+/C

b) Write a truth table that shows the final outputs for A,B and C.

A	B	C	/A	/C	/A.B	(/A.B)+/C
0	0	0	1	1	0	1
0	0	1	1	0	0	0
0	1	0	1	1	1	1
0	1	1	1	0	1	1
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	0	0	0	0

b) Are the two expressions equivalent?

   Yes, the two expressions give the same output. They are equivalent expressions.

Task 5 – Pipelining.

Question 1.

  a)

    i) For each processor, how many clock ticks does it take to fill the pipeline?
1. Stages * clock ticks per stage = 8 * 3 = 24.
2. Stages * clock ticks per stage = 20 * 1 = 20.

    ii) How many instructions can be executed for each processor in 30 clock cycles?

It depends on the number of pipelines that the processor can handle, and the stage at which execution occurs.

1. If an instruction requires all 8 steps to execute then 3 instructions can be executed. If we assume that stage 5 (clock tick 13, 14 and 15) and 6 (clock tick 16, 17 and 18) are comparable to the store stage in a 4-stage pipeline, then 5 instructions can be executed.
2. If an instruction requires all 20 steps to execute then 1 instruction can be executed. If we assume that stage 11, 12, 13, 14 and 15 are comparable to the store stage in a 4-stage pipeline, then 16 instructions could be executed.

  b) Describe four disadvantages of a deeply pipelined processor.
1. Can suffer from bad instruction latency.
2. Prone to stalling bubbles due to incorrect branch predictions.
3. Performance decrease when processing high-level instructions.
4. The more pipelining is used in a processor the more complex and expensive it is to produce.

Question 2.

A	F	D	E	Flushed					
B		F	D	Flushed	Bubble				
C			F	Flushed	Bubble	Bubble			
D				F	D	E	S		
E					F	D	E	S	
F						F	D	E	S
G							F	D	E
H								F	D
I									F

Task 6 – CPU Architecture.

1. Compare and contrast multithreading and multiprocessing.

   - Multiprocessing refers to adding multiple cores to a processor to perform instructions in parallel on separate cores.
   - Multithreading refers to performing multiple instructions on one core by utilizing space or "gaps" in instruction pipelines to execute two instructions on the same pipeline.

2. Explain how threads are used by the CPU to process tasks by describing a modern example.

   A modern of example is the Intel Hyperthreading technology used in modern CPU's like the Core i7-9750. The CPU itself has six cores but is described to have 12 "logical" cores because each core can process two threads at a time. When one thread of a core is required to stop processing because it is waiting on data to be received from memory, the other thread can continue to execute distinct from the other. Under the right circumstances, hyperthreading allows CPU cores to perform to tasks, simultaneously (Intel, Viewed 14th January 2021, Para 11). This minimizes the likelihood of long processing times and greatly improves the efficiency and speed of each CPU core.

3. What is a circumstance in which SMT cannot offer any advantage, or even cause a performance decrease?

   SMT involves complex programming and relies on support from the application that it is attempting to execute instructions for. Therefore, if an application does not provide support for multithreading, for example in a legacy program being utilized on a modern CPU, or on a program that has not been written to support SMT, performance can suffer, and even cause the program to terminate. To take advantage of multithreading, it requires implementation at the software level (Konsyse Staff, 2020, para 12).

Task 7 – Memory.

a) What are the maximum clock speeds for GDDR5 memory, and GDDR6?

GDDR5 = 2002 MHz (NVIDIA GeForce GTX 1060 6GB)
GDDR6 = 1875 MHz (NVIDIA GeForce RTX 3060)
(Tech Power Up, viewed 14th January 2021).

b) What is the current maximum throughput available for GDDR5 and GDDR6?

GDDR5 = 40 – 256 GB/s (AMD Radeon RX 580)
GDDR6 = 112 – 936.2GB/s (NVIDIA GeForce RTX 3090)
(Tech Power Up, viewed 14th January 2021).

c)

1. Find the bus sizes for GDDR5 6400 MHz and GDDR6.

GDDR5 = The maximum bus size for GDDR5 is 256-bit (256/32 = 8 bus channels).
GDDR6 = The maximum bus size for GDDR6 is 384-bit (384/32= 12 bus channels).
(Tech Power Up, viewed 14th January 2021).

2. Explain why the sizes are quite different.

As GPU architecture improves, they require better memory bandwidth to take advantage of the large amount of data that they need to transfer to and from memory. In answer to this, GDDR6 memory developers have introduced additional data buses to allow more data to be transferred to memory and prevent loss of performance due to memory bottlenecks.

d)

1. Explain the difference between GDDR6 and HBM.

GDDR memory relies on fast clock rates between the GPU in relatively smaller sizes of data and utilizes multiple 32-bit buses. HBM memory, though, uses high bandwidth so that it can transfer large amounts of data with a slower clock-rate over a single 1024-bit bus. HBM memory is most suited to systems that send a lot of data relatively slowly i.e., artificial intelligence or autonomous vehicles (Frank Ferro, May 9 2018)

2. What is the size of the HBM bus? Does this give HBM an advantage?

HBM memory buses are 1024-bits in size. This does not necessarily give HBM an advantage as both systems are suited to different workloads. For example: gaming requires a lot of very small instructions to render large, complex 3D graphics so it is most common to use GDDR memory, whereas an autonomous vehicle sends large packets of data at a slower rate, making HBM memory more appropriate.

Task 8 – Hamming and SECDED Code.

a) Determine the maximum number of data bits that can be protected.

Maximum protectable bits = 2^p >= m + p + 1.

p = 4.

2^4 = 16.

A maximum of 16 bits can be protected using 4 hamming bits.

b) A SECDED encoded character has been retrieved, with the hexadecimal value of 51A_16.

1. Was there an error in transmission?

Yes, there was an error in transmission. P1 needed a 1 to produce an even amount of 1's in it's row, indicating an error. P1 and P4 also required a 1 to be added to them both to be in parity. An error can be identified, though, by looking only at P0 and noticing that it is not in parity.

2. If there was an error, either correct it or explain why it could not be corrected.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
D12	P5	D11	D10	D9	D8	D7	D6	D5	P4	D4	D3	D2	P3	D1	P2	P1	P0	
0		1	0	1	0	0	0	1		1	0	1		0				D
0		1	0	1	0	0	0	1		1	0	1		0			**1**	PO
0		1		1		0		1		1		1		0		**1**		P1
		1	0			0	0			1	0			0	**0**			P2
		1	0	1	0					1	0	1	**0**					P3
		1	0	1	0	0	0	1	**1**									P4
0	**0**																	P5

PO	Error.	1
P1	Error.	1
P2	No Error.	0
P3	No Error.	0
P4	Error.	1
P5	No Error.	0
01001 = 9. Error is on row 9.		

Solution:

If the values on column 9 are flipped, that gives 0101 0000 1010_2 = 50A_16.

Advanced Questions.

Question 9.2 – Logic Simplification using Karnaugh Maps and Boolean Algebra.

a) Show how to use the K-Map to simplify the logic expression of circuit 1 in question 4.
/(/(A.B).(A.C)^(B./C))

A	B	C	/(ABAC)^(B+/C)	X1^X2	F	/F
0	0	0	/(0000)^(0+1)	1^1	0	1
0	0	1	/(0001)^(0+0)	1^0	1	0
0	1	0	/(0100)^(1+1)	1^1	0	1
0	1	1	/(0101)^(1+0)	1^1	0	1
1	0	0	/(1010)^(0+1)	1^1	0	1
1	0	1	/(1011)^(0+0)	1^0	1	0
1	1	0	/(1110)^(1+1)	1^1	0	1
1	1	1	/(1111)^(1+0)	0^1	1	0

BC A	00	01	11	10
0	1	0	1	1
1	1	0	0	1

F = /A+(B/C)

b) Show how to use Boolean algebra to simplify the expression.
/(/(A.B)(A.C)^(B/C))
/((/A+/B+/A+/C)^(B/C))
/((/A+/B+/C)^(B./C))
/A+(B./C)

c) Compare the above two simplification methods and discuss which is better.

Both methods have their own set of benefits, depending on the requirements when performing the simplification. The K-Map was better in this circumstance though, as it allows us to see the function of all possible inputs and the expression can be simplified without requiring knowledge of common Boolean algebra rules. Though the algebra looks shorter, it requires a substantial amount more knowledge from the user.

d) What are the limitations of K-Maps?

Though K-Maps are extremely useful when there are only a few variables, they begin to be very difficult to visualize when 5 or more variables are used. The cells in the map number too high, and it becomes difficult to make sense of the position of the variables. They also cannot be used to perform computer reduction and are mostly relevant for humans performing Boolean algebra.

References.

- Intel.com, *What is Hyperthreading*, Intel, Viewed 14th January 2021,
  < https://www.intel.com/content/www/us/en/gaming/resources/hyper-threading.html>
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