Delay Signal Generator with 150ps-Resolution and 100ps RMS Jitter

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***Abstract*—At the Budker Institute of Nuclear Physics, special devices called Time Interval Generators and Delayed Signal Generators are used to synchronize the Accelerator complex systems. In Time Interval Generators, the basic delay principle is simple counters in Field-Programmable Gate Array from a 100 MHz quartz oscillator. Whereas in Delayed Signal Generators, the counters of Field-Programmable Gate Array are supplemented by a special analog circuit. This circuit consists of special charging circuit, high-speed comparator with low leakage current and capacitor. The method using this circuit improves the delay setting resolution to 150 ps and addresses delay instability due to the random phase of the trigger signal with respect to the main clock frequency by taking into account the arrival time of the delayed signal relative to the clock frequency. At the end of signal generation, this time is "added" to the delayed signal. Using this method, it is possible to delay signals with 150 ps resolution, Root Mean Square jitter of about 100 ps, and a maximum delay in the current configuration of up to 10 µs. The RMS jitter measurements were taken from four channels at different delays using an eye-diagram on an oscilloscope with at least 10k measurements. The results showed no jitter change over the range of operating delays up to 10us.**

Keywords—digital to time converter, time to digital converter, DTC, TDC, TDC-DTC, signal generation, signal delay methods, synchronization, synchronization of large acceleration devices, accelerator complex preparation, diagnostic devices, delayed pulse generators, time interval generators, FPGA, analog circuit design, circuit design, delay instability, eye-diagram measurement, RMS Jitter, jitter reduction, fast comparator, integration capacitor

I. INTRODUCTION

In the field of synchronization of large acceleration devices, there are many methods for delaying signals, each of which has its own features, accuracy and limitations. The paper [1] discusses various approaches including Time to Digital (TDC) - Digital to Time (DTC) Converters implemented using embedded Field-Programmable Gate Array (FPGA) hardware blocks. Notable among them are Vernier delay line using phase-locked-loops (PLL), tapped-delay-line and register known as time coding line [2], DTC based on look-up tables (LUTs). It is also possible to realize TDC using dynamic reconfiguration [3]. The most modern TDC-DTCs are developed on the basis of specialized integrated circuits and are able to achieve resolutions up to 1 ps [4], [5], [6], [7].

However, in this article we will focus on the signal delay method developed at the Institute of Nuclear Physics (INP) and actively used since the 1980s. First, let us briefly review the history of developments at INP.

In the 1980s, a wide range of CAMAC (Computer Automated Measurement and Control) modules was developed at the INP. Representing CAMAC crate controllers with the INP computer command system - "ODRENOK" based on Odra-1300 computers [8], [9] allowed solving almost all tasks of automation of the particle Accelerators. Over time, these devices became obsolete, and the lack of components made maintenance difficult. The solution to this problem was the development of a new series of devices in the VME (VersaModule Eurocard bus) standard using Experimental Physics and Industrial Control System (EPICS) software [10]. But this did not affect the devices we will describe below.

The INP uses two type synchronization devices of Accelerators: Delayed Pulse Generators (DSG) and Time Interval Generators (TIG). These devices play a key role in synchronizing the precision-intensive particle injection triggering systems and preparing the complex for injection.

The delay of the DSG is adjustable from 100ns to 10µs with a resolution of 150psec. These generators serve for triggering kickers during the injection of particles in the accelerator, start devices for diagnostics of fast processes, etc. One module has 2 channels with common triggering and is made in CAMAC standard.

In TIG, the delay is adjustable with a resolution of 100 ns, the jitter is 10 ns, and the delay is adjustable from 150 ns up to a few seconds. These devices are used to trigger "slow" elements: pulse deflector magnets, charge line kickers, etc.

The basic principle of delay generation in TIG - simple counters of pulses from the quartz oscillator (100 MHz). In the DSG, the clock counters are supplemented with a special analog delay, which allows to increase the resolution up to 150psec and exclude delay instability at random phase of the start relative to the phase of the clock frequency.

In spite of sufficient accuracy, obsolescence and increasing requirements for ease of operation and setup require the development of new devices. Hence the task to develop a device that will have the functionality of both TIG and DSG. Since the principle of operation of TIG is simple enough and can be combined with DSG, so this article will deal only with DSG.

II. DSG DESIGN

To achieve high delay accuracy, it's crucial to account for the fact that the start signal may arrive at any point in time relative to the clock pulses. To address this uncertainty, a method utilizing a special charging circuit with an integrating capacitor and a comparator is employed, as illustrated in Fig.

1. This method enables us to offset the uncertainty of the signal delay relative to the clock frequency and introduce an analog delay by setting an initial voltage across the capacitor, which we will refer to as UrefA.

The rising edge of Start signal triggers the charging of a particular capacitor with a known charging current and its voltage starts to increase from UrefA. The FPGA logic tracks the startup on the rising edge and falling edge of the clock signal. Once both conditions are met, the capacitor charge is interrupted on the falling edge of the clock pulse and the capacitor charge is kept constant thereafter.The capacitor charge time varies randomly from 0.5 to 1.5 periods of the clock frequency (see Fig. 1).

The internal FPGA counters are then switched on and count the settable number of N pulses. After the counting is completed, the capacitor charging current is switched on again at the falling edge of the last clock pulse. When its voltage reaches the constant voltage UrefB, an output delayed pulse is generated. Obviously, the total device delay is determined only by the capacitor charge time from UrefA to UrefB and the number of counts N.

The UrefA voltage in the device is regulated from UrefAmin to UrefAmax from the 8-bit Digital to Analog Converter (DAC). The difference of these values dV = UrefAmax - UrefAmin is equal to the capacitor charge voltage over 1 clock period. By adjusting the number N and changing the value of dV, it is possible to change continuously the delay of the device with the resolution T_{clk}/256 of the clock period, where T_{clk} is the clock period.

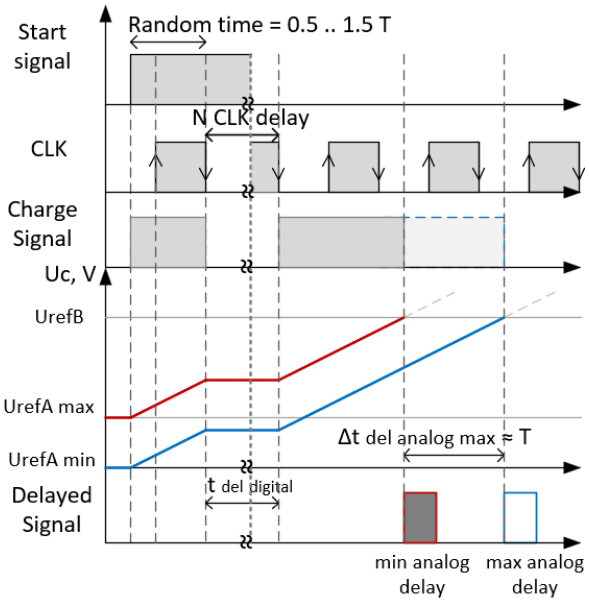

Fig. 1. Method for addressing uncertainty with minimum (UrefA max) and maximum (UrefA min) analog delay.

The regulation is done by setting the initial voltage (UrefA) on the capacitor before the start pulse arrives. This method provides sufficient accuracy for accelerator injection systems at the NRC. The total delay is calculated from the minimum device delay $t_{min\ time}$ (or dead time), the digital delay $t_{del\ digital}$, and the analogue delay $t_{del\ analog}$.

$$t_{delay} = t_{\min time} + t_{del\ digital} + t_{del\ analog},$$

or

$$t_{delay} = t_{\min time} + N_d \times clk + N_a \times Resolution_a,$$

where, N_d – Number of digital delay; N_a – number written to the DAC; $Resolution_a$ – analog resolution of the device

$$Resolution_a = \frac{\Delta t\ del\ analog\ max}{N_{a\ max}}.$$

The minimum and maximum range of the output signal generation relative to the clock frequency is determined by the Duty Cycle (DC) of the clock frequency. Accordingly, the minimum variation of the generated signal with respect to the clock frequency is $T_{clk} \times (1 + DC)$ and the maximum variation is $T_{clk} \times DC$ For simplicity in the Fig. 1 and 2 DC = 0.5. The minimum and maximum achievable voltage across the capacitor at first charge also depends on DC: $U_{c\ first\ charge\ min} = (1 + DC) \times U_{c\ 1\ Tclk}$; $U_{c\ first\ charge\ max} = DC \times U_{c\ 1\ Tclk}$. $U_{c\ 1\ Tclk}$ – is the voltage to which the capacitor will be charged at the selected current during one period T_{clk}.

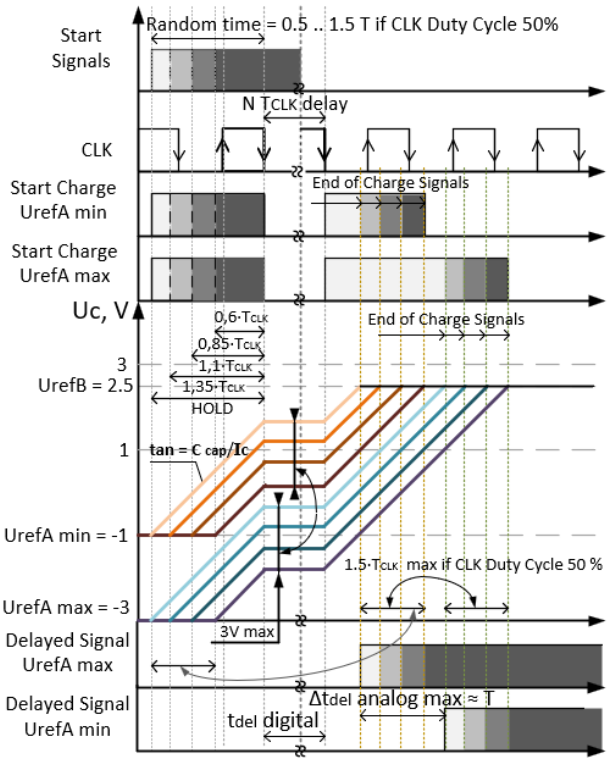

Fig. 2. Charge signal on capacitor, 2 specific cases of delay uncertainty addressing, with minimum (UrefA min = -1V) and maximum analog delay (UrefA max = -3V) at different phase of the start signal.

Fig. 2 shows an ideal representation of the signals, which does not take into account the speed of the comparator and the FPGA. Therefore, in the real case, the capacitor voltage will rise above UrefB until a delayed signal arrives at the FPGA.

Fig. 3 shows the electrical circuit diagram of one channel of the GZI. The frequency of clock pulses is chosen equal to 25 MHz. The current Ic, charging capacitor C3, flows through transistor VT2. This current is regulated by resistor R1=100 Ohm. The calculated value of the current is 25mA. We calculate the nominal value of capacitor C3 under the condition that during the period of clock frequency T_{clk} (40ns) the capacitor is charged by dV = 2V.

$$C_3 = I_c \times T_{clk}/dV = 500\ pF.$$

A value of 510 pF selected.

As shown above, the adjustment resolution is 40ns/256 = 0.15nsec. Let's calculate the voltage change on the capacitor when the delay is changed by 0.15ns. If a 2V change in the voltage on C3 corresponds to a 40 ns delay change, then from the proportion for 0.15ns, the voltage on C3 will change by 7.8mV.

Due to the need to hold the voltage on the capacitor for a long time (tmax = 10 μs), to implement this method it is necessary to use elements with low leakage currents in the charging circuit C3. For the selected fast comparator KP597CA1 (analogue of Am685), the leakage current of the non-inverting input at the voltage from -3 to 3V and at the voltage at the inverting input +3.5V does not exceed 20 nA. The total leakage current of transistor VT1 and switch VT4 also does not exceed this value.

Let's calculate the voltage drift on capacitor C3 from the leakage current $I_{leakage}$ =40 nA for the time t_{max} = 10 us.

$$dV1 = \frac{I_{leakage} \times t_{max}}{C_3} = \frac{40 \cdot 10^{-9} \times 10 \cdot 10^{-6}}{510 \times 10^{-12}} = 0.8\ mV,$$

which is much less than dV1=7.5mV found above.

The initial voltage on capacitor C3 is set via the voltage setting circuit UrefA, coming from the DAC DD1 and the charge switch. This allows the voltage to be adjusted during operation of the device, thereby changing the value of the analogue delay. UrefA can be varied between -3 and -1 V. The duration of the first charge of capacitor C3 is randomly varied from 0.5 to 1.5 T_{clk}. This corresponds to a voltage change of 1 to 3V. Thus, the maximum voltage on C3 after the first charge (UrefAmax = -1V) is 2V. The voltage UrefB is adjusted so that at maximum UrefA, after the first charge, the voltage across the capacitor is always 0.5V below UrefB. This is to ensure that from any set UrefA and the first charge pulse (0.5-1.5T duration), there is still a voltage margin for charging after the counters are triggered. The UrefB signal is taken from the emitter of transistor VT3 and is set to be +2.5V.

In static mode the switch VT4 is open and capacitor C3 is charged to voltage UrefA. On the rising edge of the start pulse, the switch opens and then the charging current through VT2 is switched on. Because the range of voltage change over one period T_{clk} and UrefA coincide and are equal to 2V, the continuity of the delay setting is achieved. The voltage at the second input of the comparator is set via the UrefB setting circuitry and can be changed to adjust between 2V and 3V.

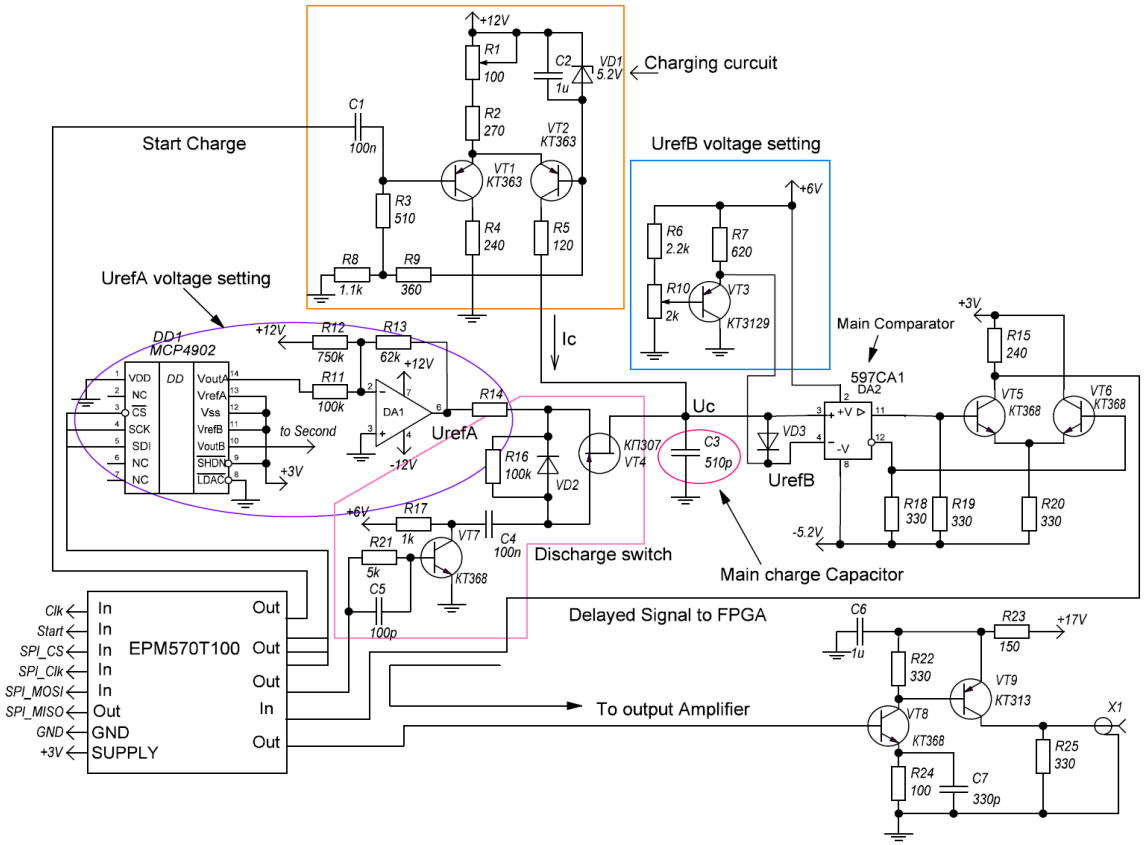

Fig. 3. electrical circuit diagram of one DSG channel.

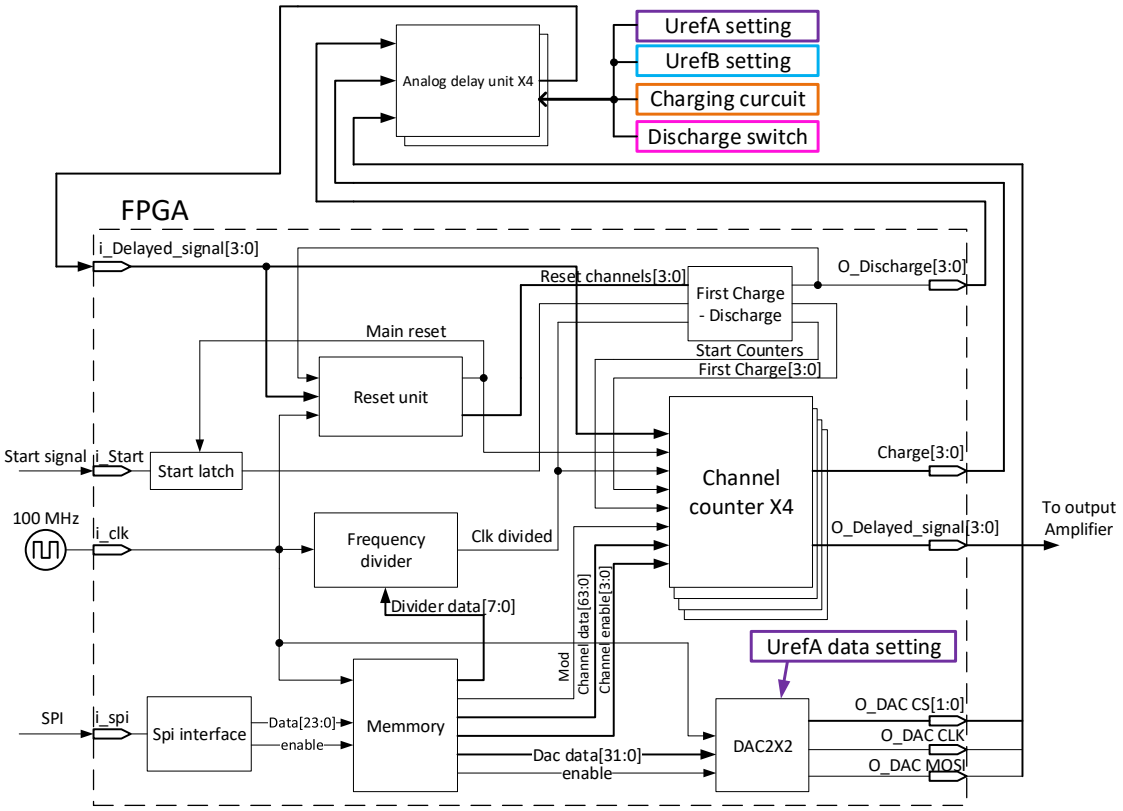

Fig. 4. Functional diagram of the device.

The functional diagram of the DSG device is shown in Fig. 4. The internal logic of the FPGA is divided into 7 blocks. The memory stores all the data for counters, DAC, frequency divider, operating mode and clocking resolution of the channel. The frequency divider works as a simple counter, generating the clock frequency for clocking the counters, first charge and discharge block. The reset block generates individual reset signals for the discharge switches of each channel and a general reset. This is to ensure that at any set delay the channels have time to prepare for the next Start signal. Otherwise, the dependence of analogue delay on frequency increases. The total resource utilization in FPGA MAXII EPM570 for this implementation is 446 Logic Elements (LE) out of the 570 available [11].

III. EXPRIMENTAL

Jitter was evaluated using an eye-diagram on a Keysight Infinium oscilloscope with 10k measurements at room temperature (T = 20 C). The measurements showed a steady increase in jitter and spread between edge pulses as the delay increased. At delays as low as 10 µs rms, the jitter was less than 150 ps with a maximum signal spread of 350 ps or less. No significant dependence of jitter on analog delay on operating range was observed. Table 1 shows the measured jitter values on the channels at different delays.

It should be noted that the high jitter of channel 4 is caused by a large variation of parameters of the charging circuit transistors VT1 and VT2, which leads to resonance at high frequencies. Since in this method these transistors are the main source of jitter compared to the rest of the circuit elements, their selection is very important. It should be noted that all measurements of jitter with delays higher than 10us exceed the design operating range.

TABLE I. JITTER MEASUREMENTS OF RISING EDGE DELAYED SIGNAL

Channel, RMS jitter ps		***Ch 1***	***Ch 2***	***Ch 3***	***Ch 4***
Digital delay	**Analog delay**				
0	0	89	78	84	170
0	40 ns	94	77	83	146
10 us	0	94	76	N/A[a]	N/A[a]
10 us	40 ns	107	78	84	164
40 us	40 ns	101	N/A[a]	N/A[a]	N/A[a]
2.6 ms	40 ns	111	82	84	164

[a] N/A – Not Available (Not Measured)

Fig. 5 illustrates oscilloscope readings of the capacitor voltage under minimum digital and maximum analogue delay conditions, with charge pulse signals in accumulation mode. The delayed signal was captured from the comparator output. Due to significant interference from the charge start pulses, these readings were obtained separately.

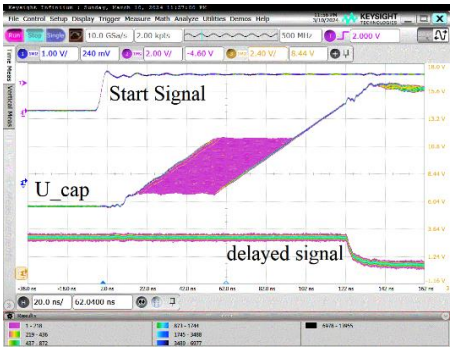

Fig. 5. Oscillograms of the capacitor voltage at minimum digital analog delay with the Start Charge signals in the accumulation mode. The delayed signal is taken from the stage of transistors VT5 and VT6.

Fig. 6. Oscillogram of the discharge signal in relation to the voltage on the capacitor.

Following are the oscillograms with the minimum, maximum designed delay and delay outside the operating range of the best and worst channel from the amplifiers' outputs. Since the TIG requires large delays, 16-bit counters are used, which allows us to set delay for milliseconds despite the use of DSG. At operating frequency 25MHz and 16-bit counters, it gives us digital delay of 2.621 milliseconds. This allows us to see how the circuit responds at delays much greater than the calculated maximum delays for the required precision.

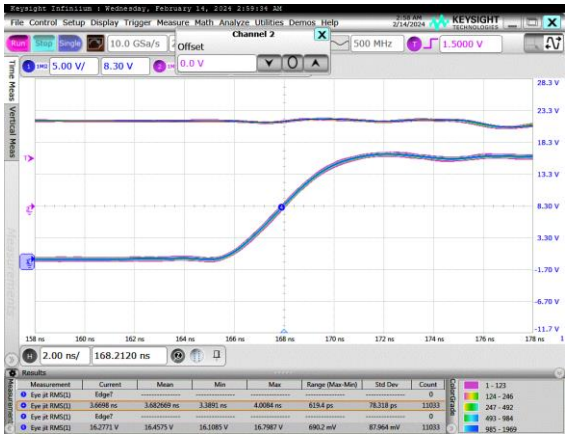

Fig. 7. Delayed signal of Channel 2 at minimum delay (≈168ns).

Fig. 8. Delayed signal of Channel 2 at maximum operating delay (≈10us).

Fig. 9. Delayed signal of Channel 2 at ≈2.6ms (far beyond the operating range).

Fig. 10. Delayed signal of Channel 4 at minimum delay (≈162ns).

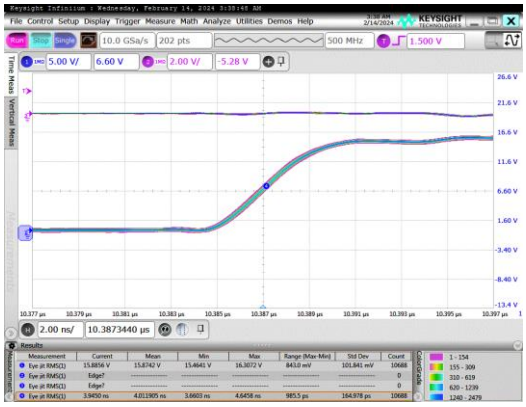

Fig. 11. Delayed signal of Channel 4 at maximum operating delay (≈10us).

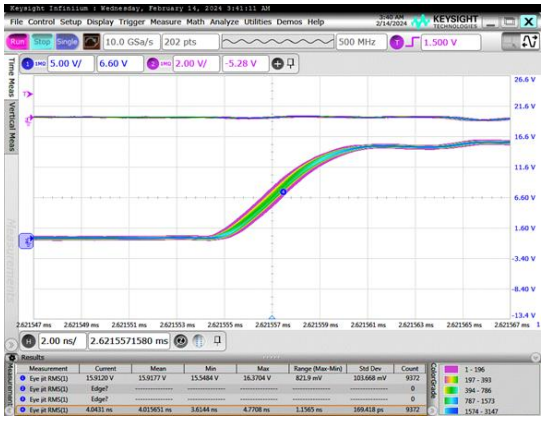

Fig. 12. Delayed signal of Channel 4 at maximum delay (far beyond the operating range).

Fig. 13. Test equipment PCB board with CPLD EPM570T100 in the centre and 4 analog delay channels with comparator KP597CA1.

IV. Conclusion

During the development of the device, we verified that using a charging circuit with a comparator it is possible to delay signals with rms jitter up to 100 ps, 150 ps resolution for a time from 170 ns to 10 us, which is sufficient for kicker triggering and particle injection of the accelerators of the INP. The results were taken at room temperature with a sample of 10k measurements for each channel at a trigger frequency of 200 Hz. No significant dependence of jitter on analog delay on operating range was observed. To increase stability and maximize delay, high precision quartz oscillators with stability above 10e-6 are required. The main elements contributing jitter to the signal are the external charging circuit transistors VT1, VT2 and the output amplifier. Therefore, by proper selection of components for low jitter, applying filtering techniques to remove noise, and optimizing the circuit layout it is possible to significantly reduce jitter.

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