HUANG XUE
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OBJECTIVE

Seeking an IT/Network administrator position.

SUMMARY OF QUALIFICATIONS

- More than 15 years of experience in IC design, familiar with every steps of a successful chip design, strong hands-on skills in hardware, software, programming, and network administration.
- Programming languages: MS VB, C/C++, Linux gcc/g++, Matlab, verilog/VHDL, system Verilog, OVM/UVM, Cshell, Perl, Python.
- Experience in Solaris/UNIX, linux, windows NT/Windows 7/8/10, and Mac OS. Familiar with C programming and scripts on Windows/Linux/Unix operation system. Setup and installation of different OS(windows+linxu+unix+andriod), network connection, database management and maintenance.
- Setup and administration of mail server, VPN server, virtual machine, firewall, router and IP forward on different platforms and equipment.
- Work experience in FPGA verification, and RTL /circuit simulations/debug.
- Full knowledge of i8051/MIPS-X/MIPS24Kc X86 CPU structure, ISA, compiler, software and hardware verification/debug environment.
- ARM series CPU and AHB/AXI bus transactions, mobile multimedia application processor structure.
- LCD design: color space conversion, multi-channel and mixed format video input, POP and PIP.
- Linux/Solaris NFS network management, workspace sharing and EDA tools setup/maintenance.
- Strong background in signal processing, Video/Audio codec, and hardware implementation. Experience in H264/265 video codec, BT1120 input/output interface design, ISP function and image processing algorithms.
- Setup/configuration of network storage, iSCSI, SSD. Full knowledge of variety of interface: PCIe, SATA, USB3.0, NVMe, M.2, DDR2/3/4 etc.

EDUCATION

Study and research experience for Ph.D. in Tsinghua University, Beijing, China, 1993-1997.
Thesis: "Research on Low bit-rate Speech codec design".
MSEE, Harbin Institute of Technology, Harbin, China, 5/1990
Conducted research at Northeast Microelectronics Institute, Shenyang city, China, 3/1990
Studied at Xidian University, Xian city, China, 9/1987 - 9/1988
BSEE, Hebei University of Technology, Tianjin city, China, 7/1987

PROFESSIONAL EXPERIENCE

----- 7/2013 – 1/2019 Marvell Semiconductor, Inc. (Santa Clara, CA 95054)
Senior SOC Design/verification Engineer

- System integration and verification for SSD controller chips. UVM verification for AXI, DMA data transfer and coverage debug;
- ARM Core CPU integration, full coverage regression test, interrupt controller design;
- Silicon test and ATE test pattern generation, debug.

----- 10/2010 – 3/2013 Techwell/Intersil , Inc. (Milpitas, CA 95035)
Senior SOC Design/verification Engineer

- Whole chip synthesis, STA timing closure, and formal/verilog verification for a PCI-e based surveillance chip. Succeeded with one-time tape-out, and move smooth into mass-production;
- Privacy mask module design, including c-model prototype and verilog HDL implementation;
- ISP function verification, and SPI OSD simulation.
- SOC with Serdes and MAC IPs, knowlege of networking protocols, layer 2 and layer 3.

----- 10/2007 – 10/2010 Nemochips Inc /ApusOne Technology, Inc. (Fremont, CA 94538)
SOC Verification Manager, Project data/network administrator

- Map100/Map150 projects and database management, top level integration and verification;
- Whole chip synthesis and timing check, power analysis;

- ARM926(300Mhz) and ARM626(800Mhz) based SOC design, integration and verification;
- LCD module design and verification: including writing c model for full function test, implementation of multi-channel DMA input, color space convert, scaling filter, POP/PIP, etc. Finished full-chip Altera FPGA emulation;
- Linux/Solaris NFS network setup and management, Linux server installation, project data storage maintenance/backup, EDA tools setup/update.
- Router and VPN setup, remote site database access/backup and network management.

----- 11/2006 - 10/2007 Magnum Semiconductor Inc. (Milpitas, CA 95035)

Senior Design Engineer, Hardware Group

- Mips24kc core configuration, rom/dram boot setup;
- Multi CPU interface design and AHB-OCP bridge verification;
- Av-link interface debug and test vector generation;
- Verification for H264 De-blocking design.

----- 5/2001 - 10/2006 ESS Technology, Inc. (Fremont, CA 94538)

Project Lead, Video Hardware Group

- Worked on RTL design of RISC CPU interface, multi-cpu bus arbiter, interrupts/timers, clock generator, and sdram bus interface;
- Perform whole chip logic comparison between gate netlist and RTL using Verplex/Formality;
- For couple of chips, run logic synthesis, sdf annotated post-layout simulations, timing check, system debug and ECO;
- Wrote test patterns and performed simulation for Uart/Atapi/PCI/USB_OTG/LPC/SPI blocks
- Integrated 8051 as microcontroller for DVD servo, migrate 8051compiler to test environment and created testbench to test SDRAM access, multi-CPU interactive talk and debug port interface;
- Responsible for Video/Audio data stream simulation and various interface debug;
- Worked on bisted memory compilation and simulation, DFT and scan chain debug;
- Complete MIPS24kc OCP bus to ddr memory controller interface design, and worked out HW/SW integrated verification environment, wrote patterns for cache, TLB and scratch pad test;
- Other duties, including project management and environment/scripts setup.

----- **9/1999 - 5/2001** Weishi Electronic Company, Shanghai, China

SOC ***Design Manager,***

- Designed and performed simulations for MIPS CPU;
- Designed 1394 Firewire interface.

----- 8/1997 - 8/1999 Xiamen Microelectronic Integration Technology R&D Center, Xiamen, China

Chief Engineer,

- Wrote a multi-media player for a LED display using VB;
- HDL design and simulation for a Motorola 16-bit compatible MCU;
- Completed FPGA board design and verification for a game controlling IC.

Referral:

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