To Whom It May Concern,

I am a highly motivated, seasoned veteran of high performance, scientific, and technical computing architectures, with a detailed understanding of the x86\_64 CPU micro-architecture. Throughout my career I have constantly worked on improving my understanding of how software application design, as well as hardware systems design impact how well customer codes scale, and what to do when performance bottlenecks are encountered.

I have worked in this industry for more than 20 years, and spent the majority of my career as an individual contributor on product engineering teams, working in fast-paced high-pressure environments always focused on how to maximize value for the customer and shareholder alike. I have been in specific situations involving customer emergencies, where account managers have come to me to salvage high-profile corporate accounts. I recall one such occasion when a high-profile customer was threatening to take their business elsewhere if we couldn’t make our demo system function as advertised. After spending a couple of days correcting the configuration, I successfully demonstrated the system capabilities to the customer and single-handedly saved the account.

My background is primarily in HPC solution design in a technical pre-sales role supporting global field sales teams. This work included the deployment of large parallel systems, and training of onsite personnel following the deployment phase. Specific to my role at Cray; I have personally deployed every CX1000 system in the field, all of which are still in service to date.

As you will note from my resume, I have worked for fortune 100 companies such as Intel Corporation, where I spent 8 years as a Sr. Performance Analyst reporting to Software Performance Lab, and 4 years as a Product Line Manager reporting to EPSD, managing the HPC motherboard product line.

I was one of two engineers at Intel who co-developed the half-u (0.5U) server motherboard form-factor, now used in most blade server systems. I am extremely well versed in system performance analysis, tuning and optimization of the entire solution stack for variety of business applications.

Thank you for your consideration of my candidacy. I look forward to hearing from you.

Sincerely,

Paul J. Del Vecchio

408-334-6074

pdelvecc@outlook.com

Paul Del Vecchio 814 Saint Elizabeth Dr. San Jose CA 95126 408-334-6074 [pdelvecc@outlook.com](mailto:pdelvecc@outlook.com)

**Skill-Set Summary:**

* Expert in performance analysis, tuning and optimization of n-tier architecture solutions including performance benchmarking and generation of industry standard benchmark results for publication into the public domain.
* Extensive experience in technical pre-sales engineering (solution architecture) across multiple NTOS platforms including dedicated and virtualized scenarios supporting account teams across all market verticals and GEOS.
* Over 10 years’ experience conceptualizing, deploying and sustaining n-tier systems on the following NTOS platforms: Windows Server, RHEL, SuSE, CentOS, Ubuntu Server including traditional Unix operating systems
* Vast experience with the top virtual software platforms including VMWare ESX, V-Switch, Workstation, Fusion and Player, as well as Oracle Virtualbox and Microsoft Hyper-V hosting OSX, Windows and Linux desktop clients.

**Work Experience:**

**6/2018 – 6/2019 Sr. Pre-Sales Engineer   
Exxact Corporation, Fremont CA**

* Work with sales teams and account managers to define a technically sound product solution tailored to each customer and ensure it resolves their specific business problem.
* Generate product quotations, ensuring they are both inline with the customer request and technically sound.
* Work to setup, run and measure performance benchmarks against Exxact’s product portfolio for publication on the company website.
* Update the company confluence pages with technical content generated from performance benchmark experiments.
* Work with product marketing to generate product photos and videos to be posted online for public consumption.

**4/2017 – 11/2017 Sr. HPC Systems Analyst  
U.S. Government D.O.E. National Laboratory**

* The exact nature of work performed for this position is still classified D.O.E. Confidential.

**6/2012 – 2/2017 Sr. Technical Marketing Engineer / Solutions Architect   
Cisco Systems, San Jose CA**

* Define the technical requirements and solution criteria required for Cisco’s UCS HPC Product Portfolio
* Generate the technical content and program elements required to provide the global field sales organization with the necessary knowledge and skills required to win HPC business across multiple verticals and segments.
* Work directly with OSV/ISV partners to improve HPC software solution functionality and performance as applicable to enable UCS as a viable and sustainable technical and scientific computing solution architecture.
* Train customers and authorized re-seller channel partners on HPC systems deployment and maintenance.
* Define the requirements for new future Cisco HPC products based on the latest UCS compute and Nexus 10GbE and 40GbE switch solutions.
* Define a competitive and compelling Go-To-Market strategy for Cisco to win in the broader HPC market.

**1/2010 – 6/2012 Sr. Solutions Architect / Pre-Sales Engineer  
Cray Inc., Seattle WA**

* Architect HPC compute cluster solutions for new and existing Cray customers.
* Design, plan and deploy compute cluster systems for Cray’s worldwide consumer base.
* Consult to Cray sales personnel and customers on HPC system design, including overall required compute performance, high-speed network interconnect topology and centralized storage infrastructure.
* Work directly with Cray’s OSV/ISV partners to improve HPC software solution functionality and performance.
* Train customers and authorized re-seller channel partners on Cray systems deployment and maintenance.
* Work with OEM partners to define requirements for new Cray HPC products, including characteristics for mechanical, electrical and thermal design features as well as validation engineering and quality assurance.

**2/2007 – 1/2010 Sr. Sales Manager / Business Development Manager  
Supermicro Computer, San Jose CA**

* Develop new direct business through lead generation, relationships, customer engagement and follow up.
* Open new accounts, determine customer technical requirements and enterprise computing usage model.
* Assist new accounts with evaluation of Supermicro enterprise server technology and orchestrate all logistics.
* Proactively manage all accounts in portfolio, staying engaged with the customer and their operational status.
* Deliver quarterly forecasts for all accounts and update according to actual customer demand before month end.
* Work with all team members on account technical requirements and provide guidance as appropriate.
* Hold regular road-map review meetings with all customers.
* Process confidentiality and other account paperwork as needed with signature from legal, finance and accounting.
* Enter all leads into online sales generation tool and update on a monthly basis.

**6/2004 – 2/2007 HPC Team Lead, Sr. Technical Marketing Engineer  
Intel Corporation, Hillsboro OR**

* Product TME Team Lead for EPSD Uni-Processor and High Performance Computing (HPC) server platforms.
* Direct marketing interface into the server board engineering teams.
* Drive server board/system design and feature definition utilizing direct customer feedback, target market segment requirements, current competitive landscape and several other factors.
* Represent the highest point of the customer support hierarchy and “last-stop” escalation support.
* Act as the customer pre-sales consulting arm of EPSD, for the Intel field sales organization.
* Oversee all program engagements with Intel’s ISV/OSV partners to enable these systems as early as possible to include in product compatibility and validation matrices for launch.
* Engage market vertical ISV partners in early competitive benchmarking activities to expose performance regressions in HW and SW for corrective feedback into development teams.
* Develop and maintain internal and external platform “seed” programs with multiple geo customers for early product adoption and promotion.
* Generate the bulk of technical marketing and technical specification collateral for owned products.
* Assist product marketing engineers with technical support for any and all product marketing needs ncluding trade-show demo creation and execution.

**8/2000 – 6/2004 Sr. Performance Analyst - Microsoft On-Site Contingent  
Intel Corporation, Redmond WA**

* Manage the Seattle Performance Lab and the Seattle CME fiscal budget.
* Manage all lab operations including client and server benchmark systems, IP network infrastructure, Storage Area Network, KVM/IP console solution and all tape backup systems.
* Collect and analyze data from various client and server workloads for performance tuning and optimization of the Microsoft.NET managed runtime.
* Mentor less experienced engineers in data collection and analysis techniques and the performance tuning disciplines.
* Proactively manage the Seattle CME fiscal budget and all purchasing responsibilities for the group.
* Assist all project teams with enabling and sustaining, data collection, analysis, data presentation and training.

**8/1995 – 8/2000 Sr. Performance Analyst, Software Performance Lab  
 Intel Corporation, Hillsboro OR**

* Work with Independent Software Vendors (ISV’s) to ensure optimal performance of their software applications running on Intel’s latest 32bit architecture platforms.
* Engage in a formal process to study then reproduce (in detail) their N-tier architecture solutions
* Reproduce ISV client-server environments including: LAN/WAN network infrastructure, web-server or web-farm front-end (web e-commerce or other web-server solution), back-end (typically a heterogeneous database solution) and Middle-ware (the ISV application of focus).
* Work directly with ISV architects to stress the application through either homegrown or off-the-shelf regression suites.
* Analyze and root-cause performance issues either in the system, application or micro-architecture levels.
* Repeat experiments to continue drilling down until all sizable performance problems have been resolved.
* Deliver a white paper documenting all lab experiments, data and results following the engagement, some which were published in the form of a joint press release.

**Education:**

* 1981 Graduate, Monta Vista High School, Cupertino CA.
* Sonar Theory, Anti-Submarine Warfare Training Center, San Diego CA
* Basic Electricity and Electronics, Anti-Submarine Warfare Training Center, San Diego CA
* Digital Electronics Training, Anti-Submarine Warfare Training Center, San Diego CA
* Sonar Supervisor, Submarine Training Center Pacific, Pearl Harbor HI
* AN/SQQ-89V1 Operation/Maintenance, Anti-Submarine Warfare Training Center, San Diego CA

**Professional Training & Certifications:**

* Intel Cluster Ready, Intel Cluster Checker, Runtime and Toolkit Suite
* Microsoft Certified Systems Engineer, Windows 2000 (MCSE)
* EMC Fiber-Channel Storage Systems Maintenance, Austin TX
* Microsoft SQL Server, SQL Performance Tuning and Optimization, Austin TX
* Microsoft SQL Server, SQL Administration, Austin TX

**References:**

* Jason Choy PhD. Salesforce.com, VP Datacenter Technology  
  212-622-6285 [jason.k.choy@salesforce.com](mailto:jason.k.choy@salesforce.com)
* Ted Barragy PhD. CGG Veritas, Senior Architect, Seismic/Reservoir Systems  
  512-314-0396 [ted.barragy@yahoo.com](mailto:ted.barragy@yahoo.com)
* Grant Mader eSignal.com, Sr. VP Network Operations  
  510-266-6000 [gmader@mail.esignal.com](mailto:gmader@mail.esignal.com)
* Brenda Culbertson Intel Corporation, Sr. Manager, Server Chipsets  
  503-712-9795 [brenda.e.culbertson@intel.com](mailto:brenda.e.culbertson@intel.com)