AXI PMOD 4.3” TFT

Introduction

This user guide describes the Cospan Design AXI PMOD TFT interface Intellectual Property. This IP interfaces directly with the Cospan Design PMOD TFT. The core encodes 24-bit RGB data into the appropriate signals to drive the PMOD TFT.

Features

- Interfaces with standard Vivado IP Cores
  - AXI Lite Slave (for control/configuration)

    - Video IO (for streaming video)
- Display video: 480x272 @ 60FPS

Diagram/schematic

<Picture of the core in a schematic form (The first should be simple, optionally there could be a second)>

<It might be good to put a small picture at the top near the Title

Specification

Details describing the interface (Does it have an AXI bus?) If it's a video device does it have frequency of operation?

Pin Map

Name	Description	Direction/Bus	Range
clk	Main core clock	input	NA
rst	Main core reset	input	NA
video_clk	RGB Video Reset	input	NA
video_rst	RGB Video Reset	input	NA
CONTROL_AXI	AXI Lite Interface	Aximm (slave)	NA
VIDEO_IN	Video IO bus	Video_io (slave)	NA
PMOD_CTR	LCD Pmod Ctr Interface	Pmod Interface	NA
PMOD_DAT	LCD Pmod Data Interface	Pmod Interface	NA

Software Configuration

Register Set

Control

Low level configuration and control bits

Name	Description	R/W	Bit Range
Enable	Enable the core	R/W	[0]
Command Mode	Switch to command mode	R/W	[2]
Reset	Reset driver (user must manually clear)	R/W	[4]
Command Write	When in command mode, write register or data	R/W	[5]
Command Read	When in command mode, read a register value	R/W	[6]
Command Parameter	When in command mode, set to send data, clear to send register	R/W	[7]
Write Override	Take direct control over the ‘Write’ signal to the driver	R/W	[8]
Chip Select	Set the Chip select of the driver chip	R/W	[9]
Enable Tearing	Enable the Tearing detector when writing video	R/W	[10]

Status

Status of the core (Currently Nothing is defined)

Control Data

When communicated with the LCD driver this value is used to specify which register to write or read to/from or it contains the data to write to the register or the data read from the register.

This is used with the ‘CONTROL’ register.

When ‘Command Write’ is set and the ‘Command Parameter’ is cleared the value within this register will set the register the user will read or write to in a consecutive command.

When ‘Command Write’ is set and ‘Command Parameter’ is set the value within this register will be set within the register address specified by a previous ‘Command Write’ (within ‘Command Parameter’ set)

Note: The driver internal register pointer will increment enabling consecutive register write

When ‘Command Read’ is set the value of the register specified by ‘Command Write’ will be returned.

Pixel Count

Total number of pixels that will be written to the TFT

Width * Height: Normally this will be set with 480 * 272 = 130,560

Version

Version of the core, standard version information in the format of:

Name	Description	R/W	Bit Range
Major Version	Major version of the core	R	31:28
Minor Version	Minor version of the core	R	27:20
Revision	Revision	R	19:16

Core Configuration

The core needs to be configured through the AXI Lite slave interface before it will start displaying video.

- Physically reset the driver
- Perform soft LCD driver reset
- Enable the LCD enable using the driver GPIO
- Configure the PLL
- Configure the driver to work with the specific LCD
- Enable Tearing
- Enable the Backlight

Demo Pointer

<Pointer to a project that demonstrates the core>