Assignment - 20BCE10503

1) Zero address

```
LOAD D
PUSH D
PUSH E
PUSH F
MUL
PUSH G
PUSH H
MUL
ADD
SUB
PUSH B
PUSH C
MUL
PUSH A
ADD
DIV
POP X
```

One address

```
LOAD D
MUL F
STORE Y
LOAD G
MUL H
SUB Y
ADD
STORE Z
LOAD B
MUL C
ADD A
DIV Z
STORE X.
```

One address

```
AC ← E
AC ← AC * F
Y ← AC
AC ← G
AC ← AC * H
ACC ← AC + D
Z ← AC
AC ← AC + C
AC ← AC + A
AC ← AC / Z
X ← AC
```

2) No of bits in tag

-) No of bits in physical size

=) 128kb

=) 2^{17} bytes

=) 17 bits

No of bits in block offset

=) Block size

=) 256 bytes

=) 2^8 bytes

=) 8 bits

No of bits in line number.

=) Cache size / line size

=) 16kb / 256 bytes

=) 2^{14} bytes / 2^8 bytes

=) 2^6 lines.

=) 6 bits

No of bits in tag

=> 17 - (6 + 8)

=> 17 - 14

=> 3 bits

size of main memory

=> No of bits in physical address = 26 bits

=> 2^{26} bytes

=> 64 mb

No of bits in block offset

=> 2^{10} byte

= 10 bits

=> Line number

= 9 bits

=> physical address

=> 7 + 9 + 10

=> 26 bits.

5) 4, 7, 6, 1, 7, 6, 1, 2, 7, 2