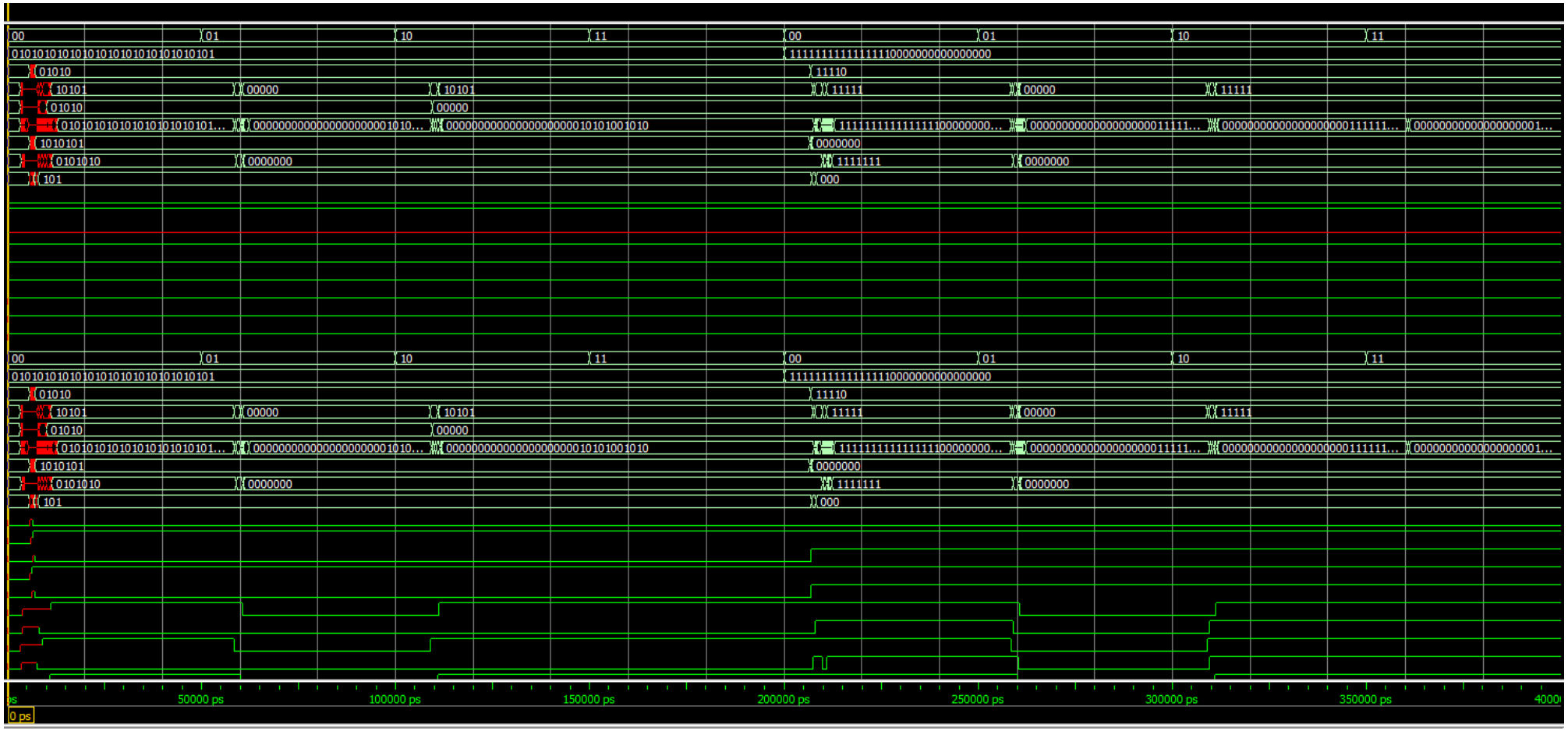
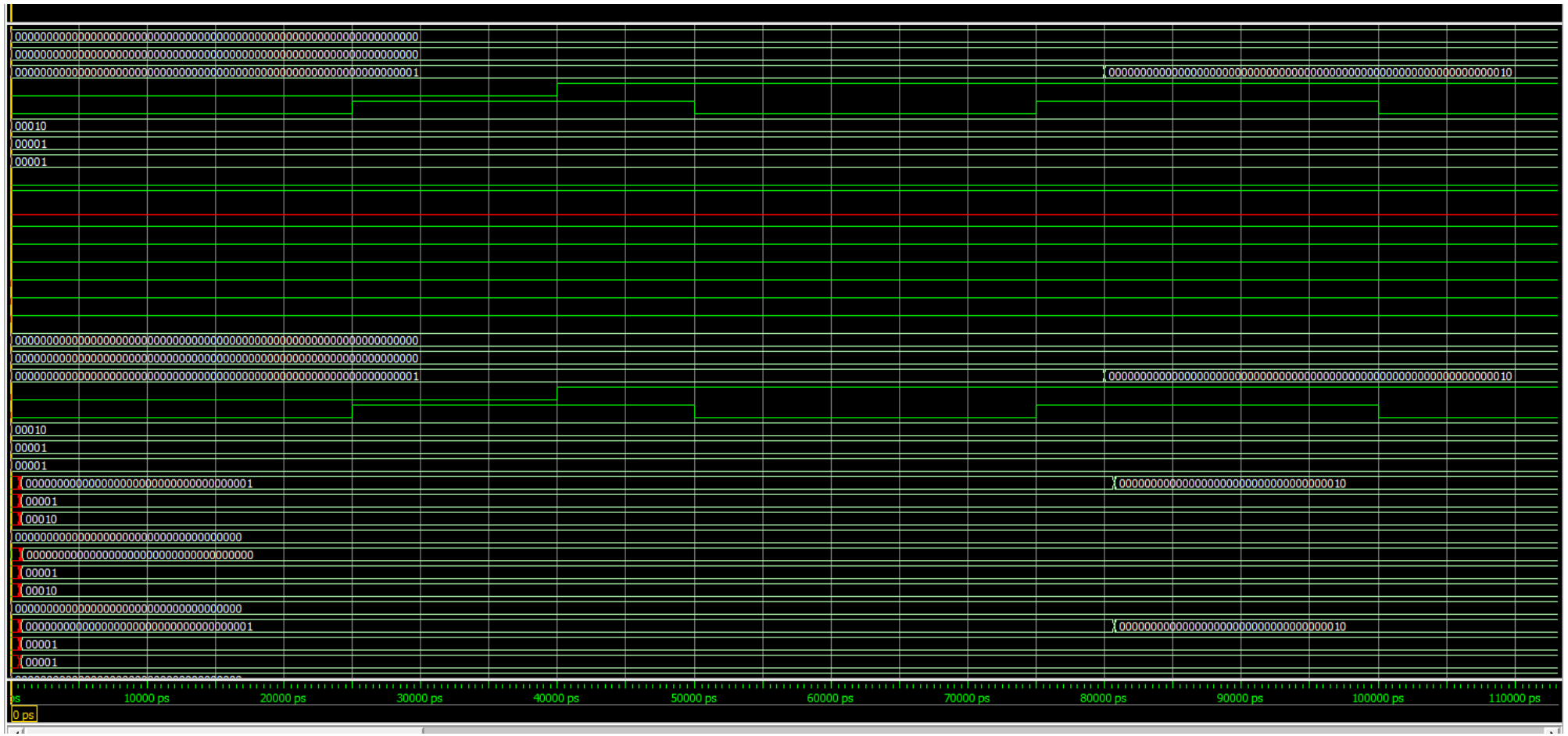
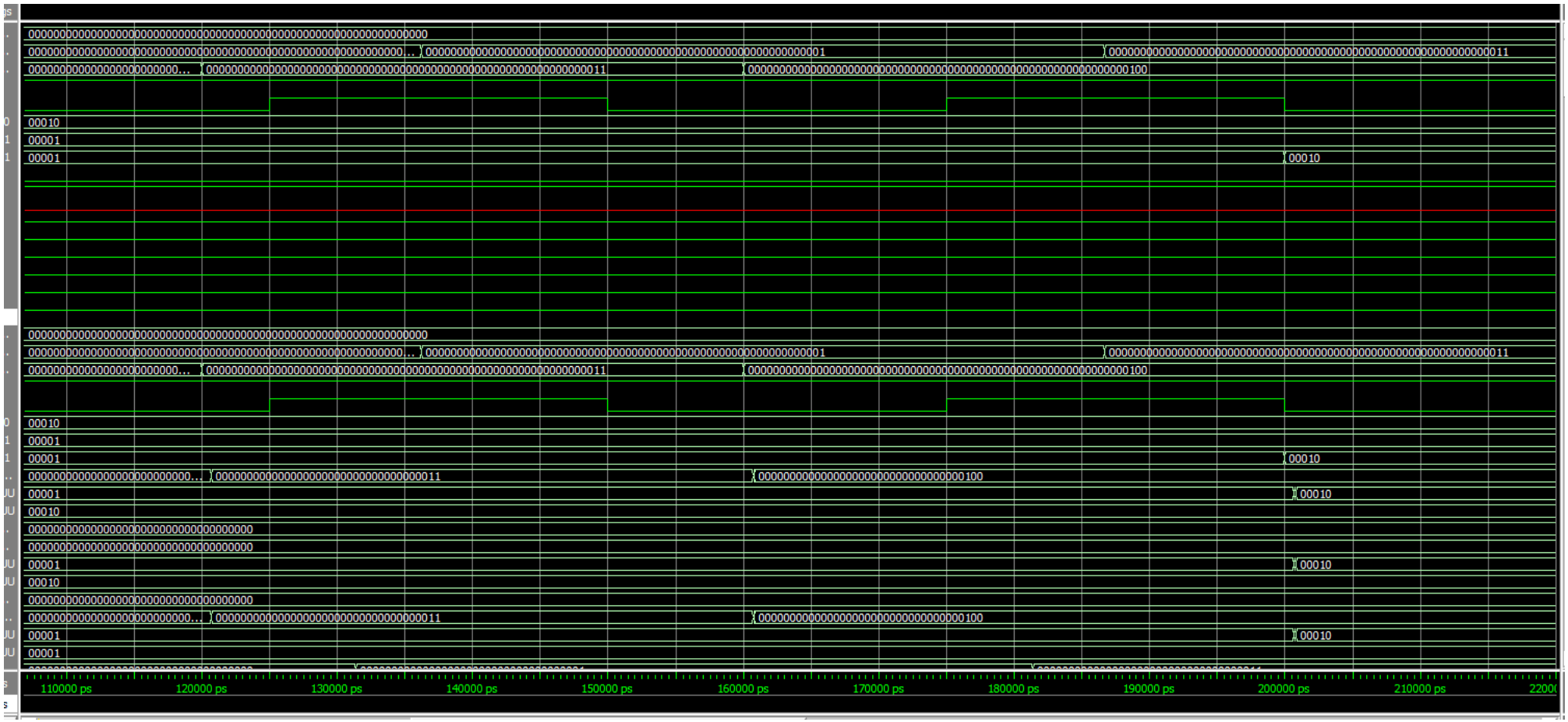
Delay time for each test is included in the tb code

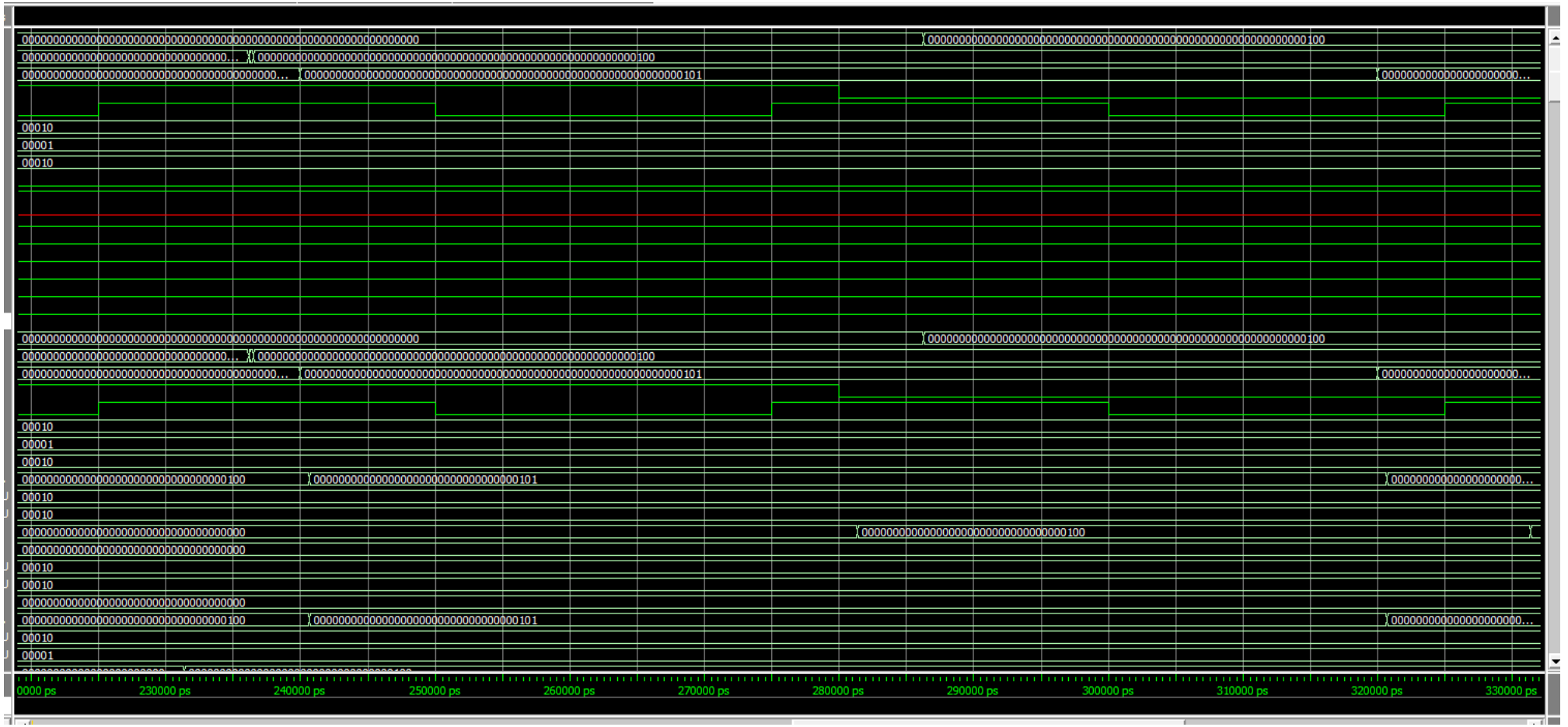
Assignment3 decoder

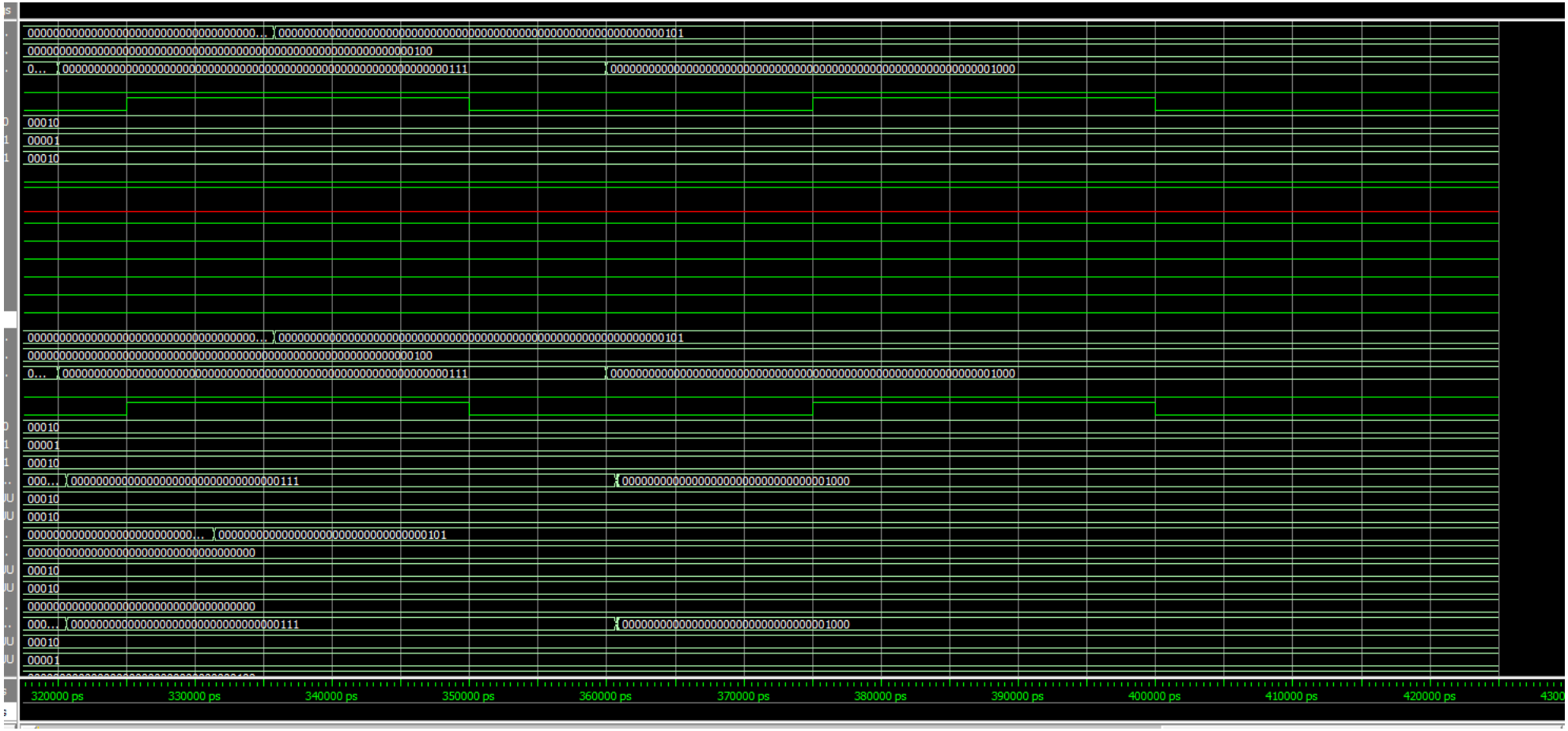


Assignment3 register, worst case delay : 26674ps frequency = 37 mhz (1/period) period = worst case delay? Do we need set up and hold here, it seems maybe negligible….

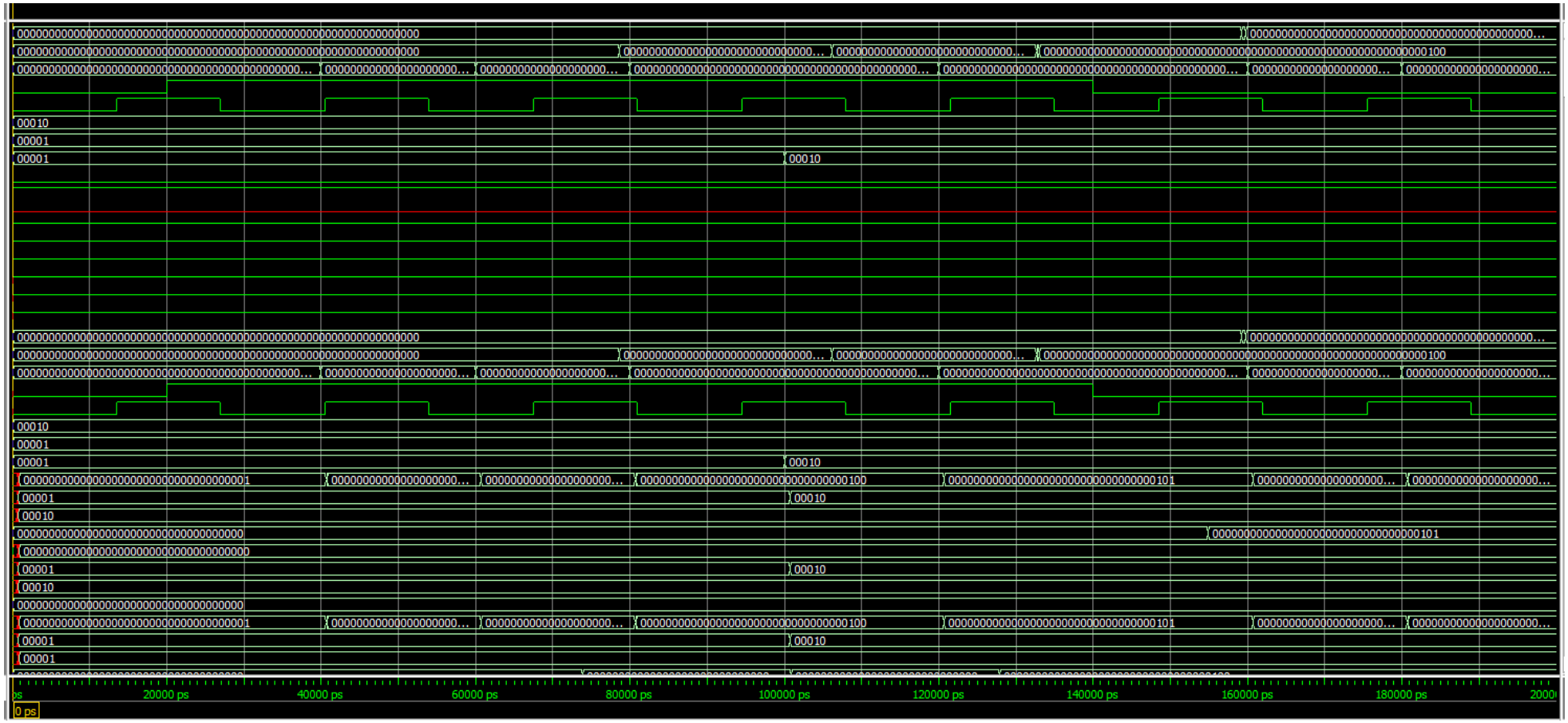



00010
00001
00001
00010
00010
00001
00001
00010
00001
00010
00010
00001
00010
00001
00001
00010
110000 ps
120000 ps
130000 ps
140000 ps
150000 ps
160000 ps
170000 ps
180000 ps
190000 ps
200000 ps
210000 ps

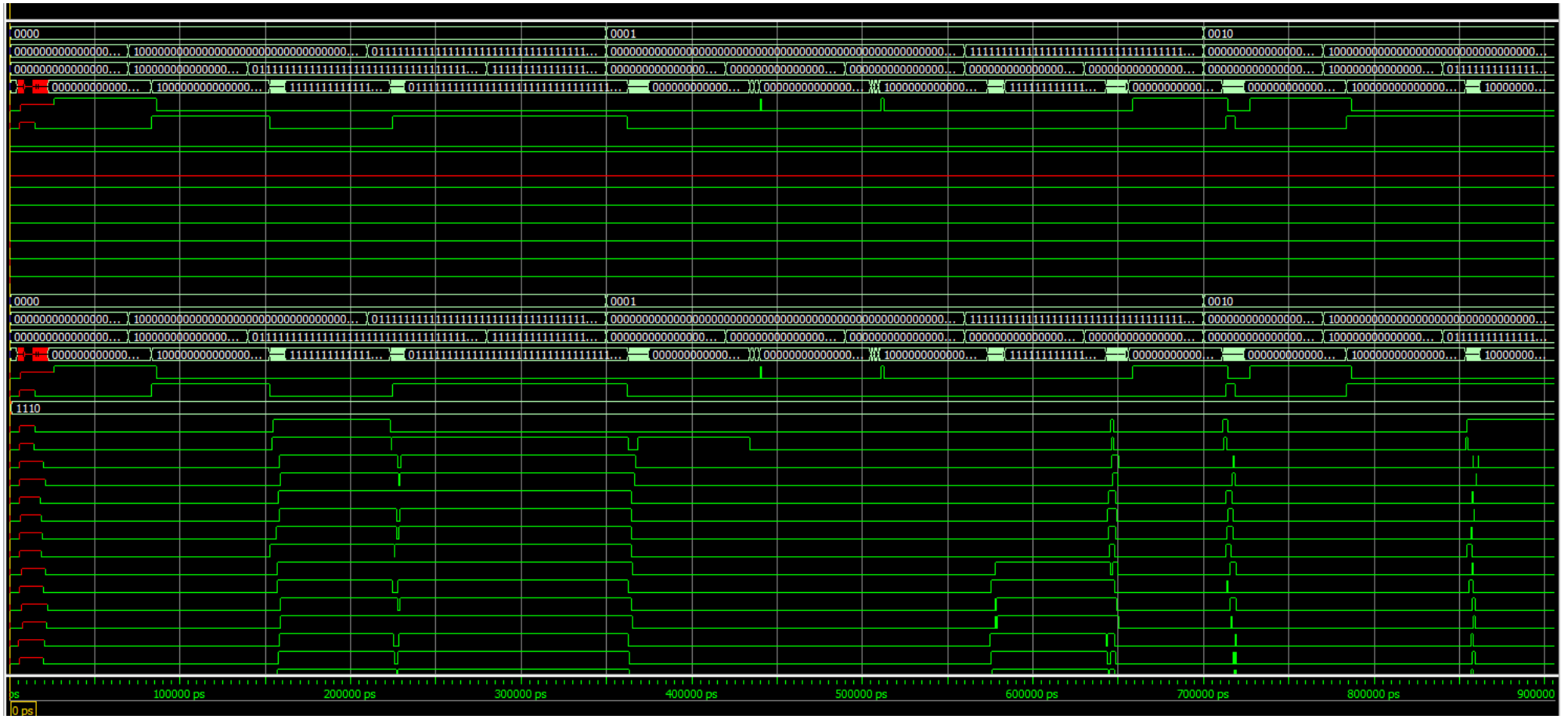

00010
00001
00010
00010
00001
00010
00010
00010
00010
00001
0000 ps
230000 ps
240000 ps
250000 ps
260000 ps
270000 ps
280000 ps
290000 ps
300000 ps
310000 ps
320000 ps
330000 ps

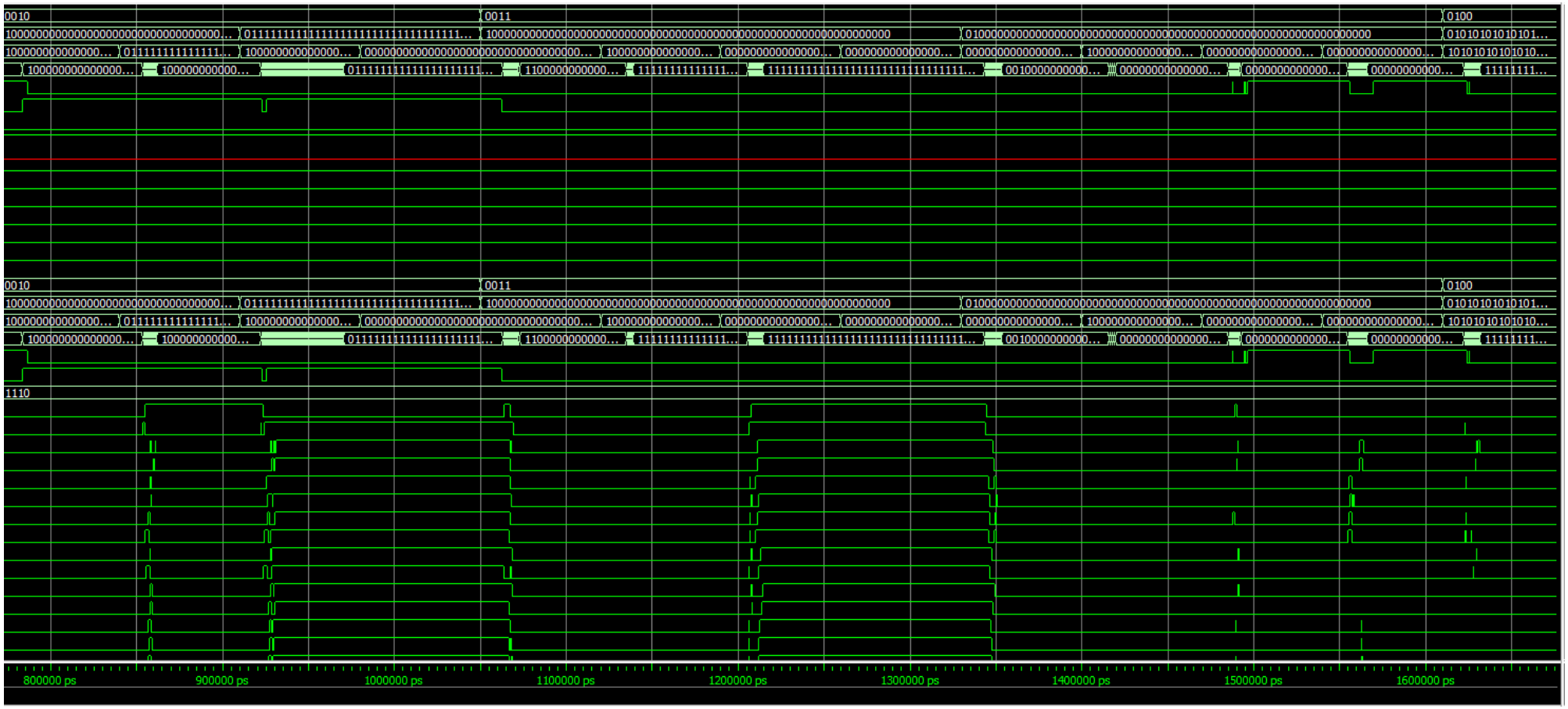


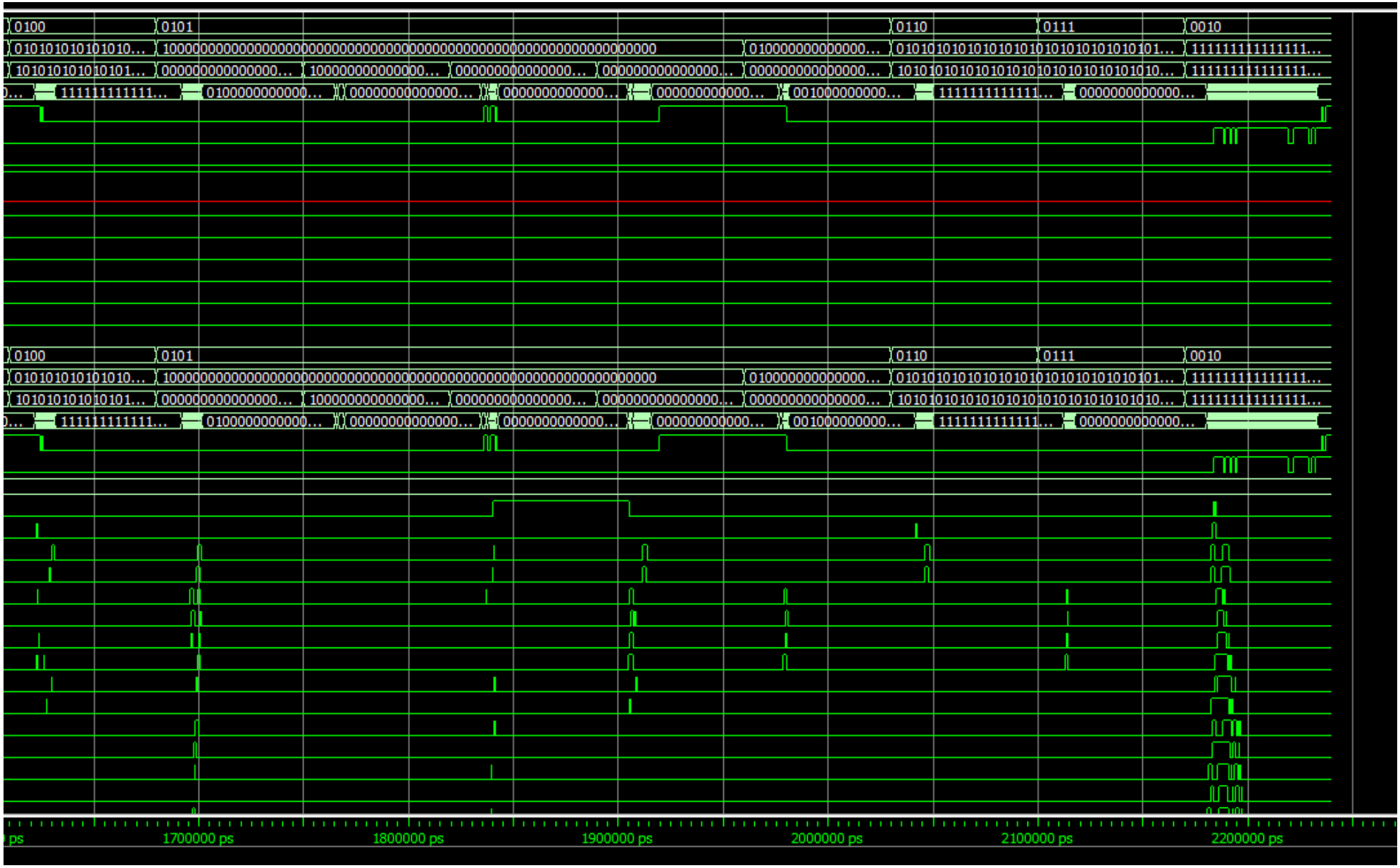
Increased frequency:



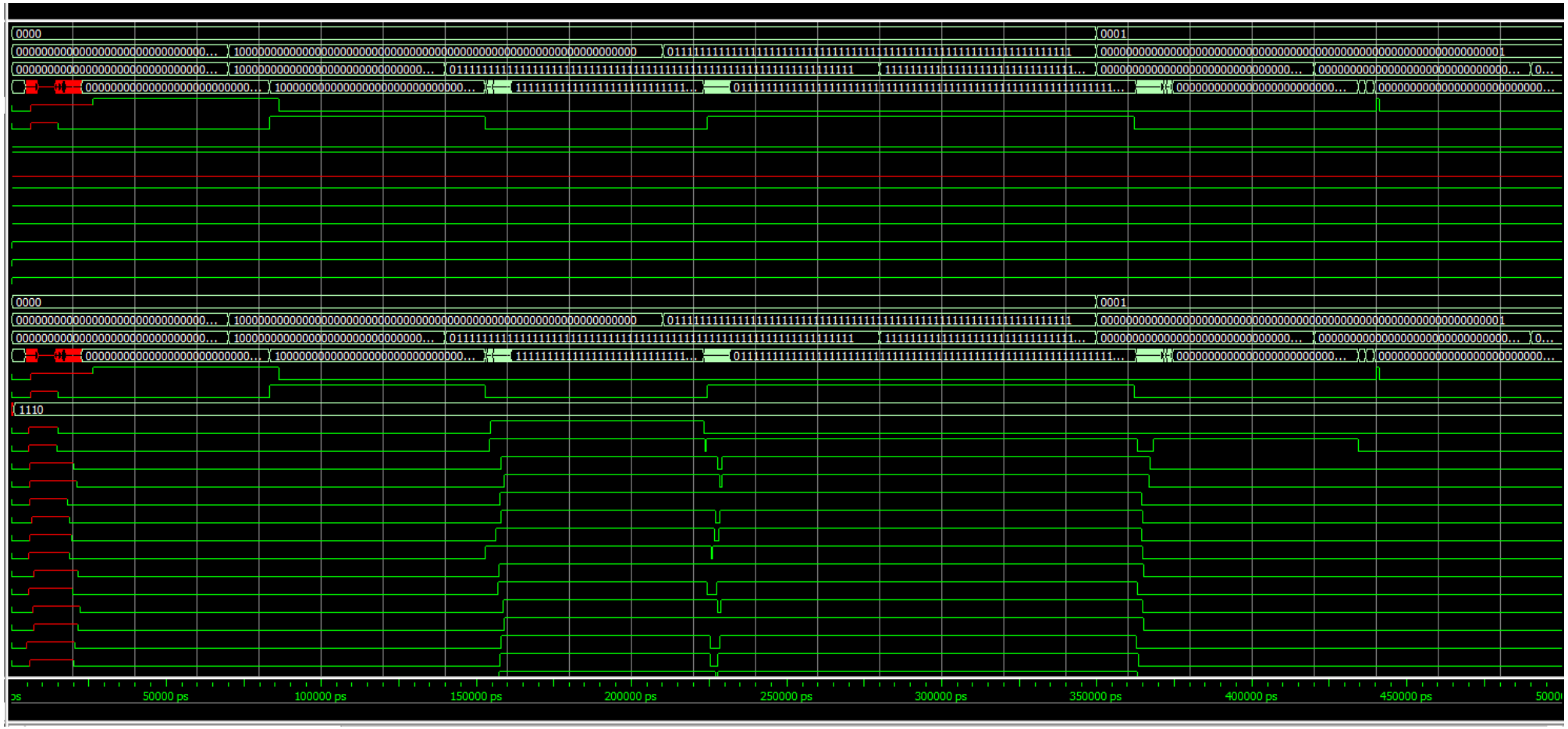
Assignment2 ALU_64 incorrect (the outputs were correct but my assert statements I put the incorrect result for right shifts)

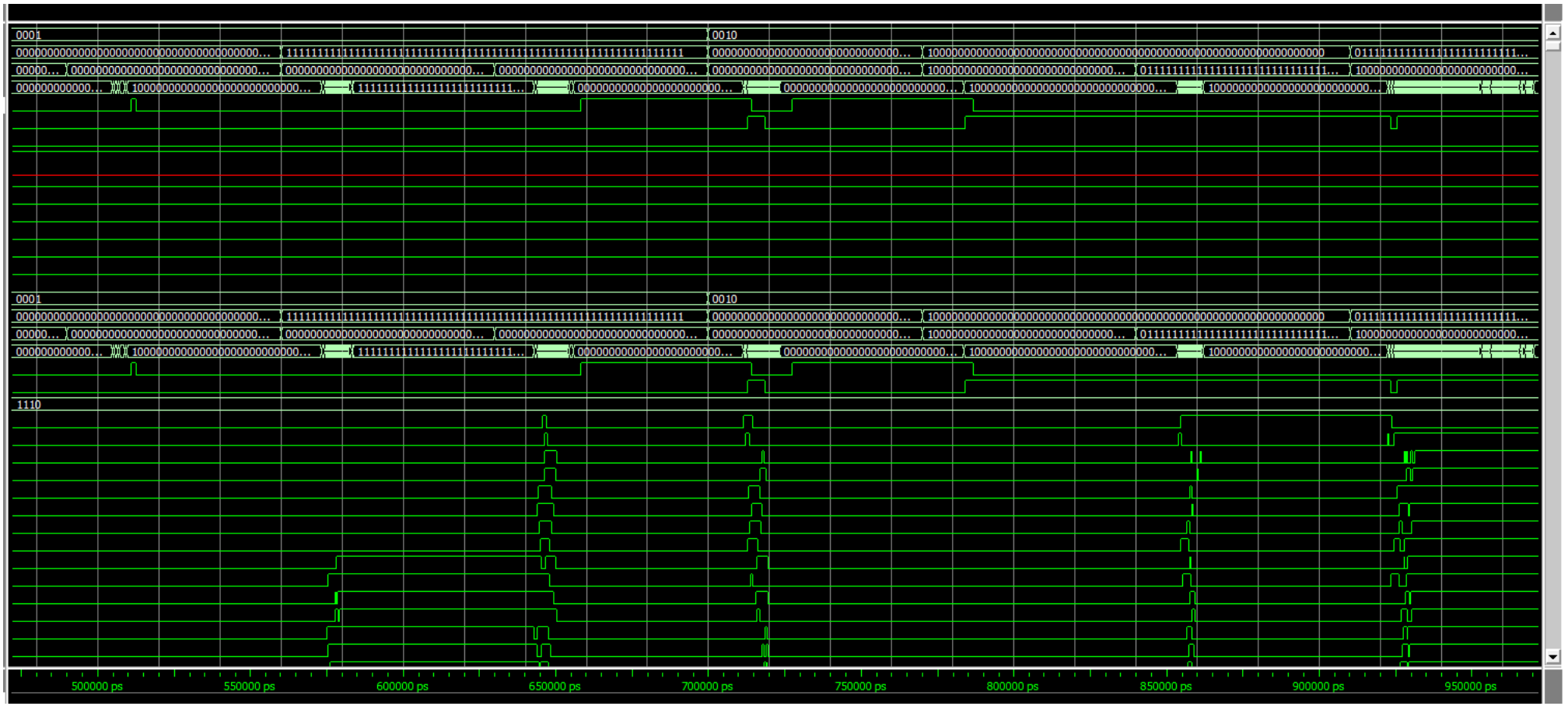

0000
0001
0010
0000
0001
0010
1110
100000 ps
200000 ps
300000 ps
400000 ps
500000 ps
600000 ps
700000 ps
800000 ps
900000
0 ps

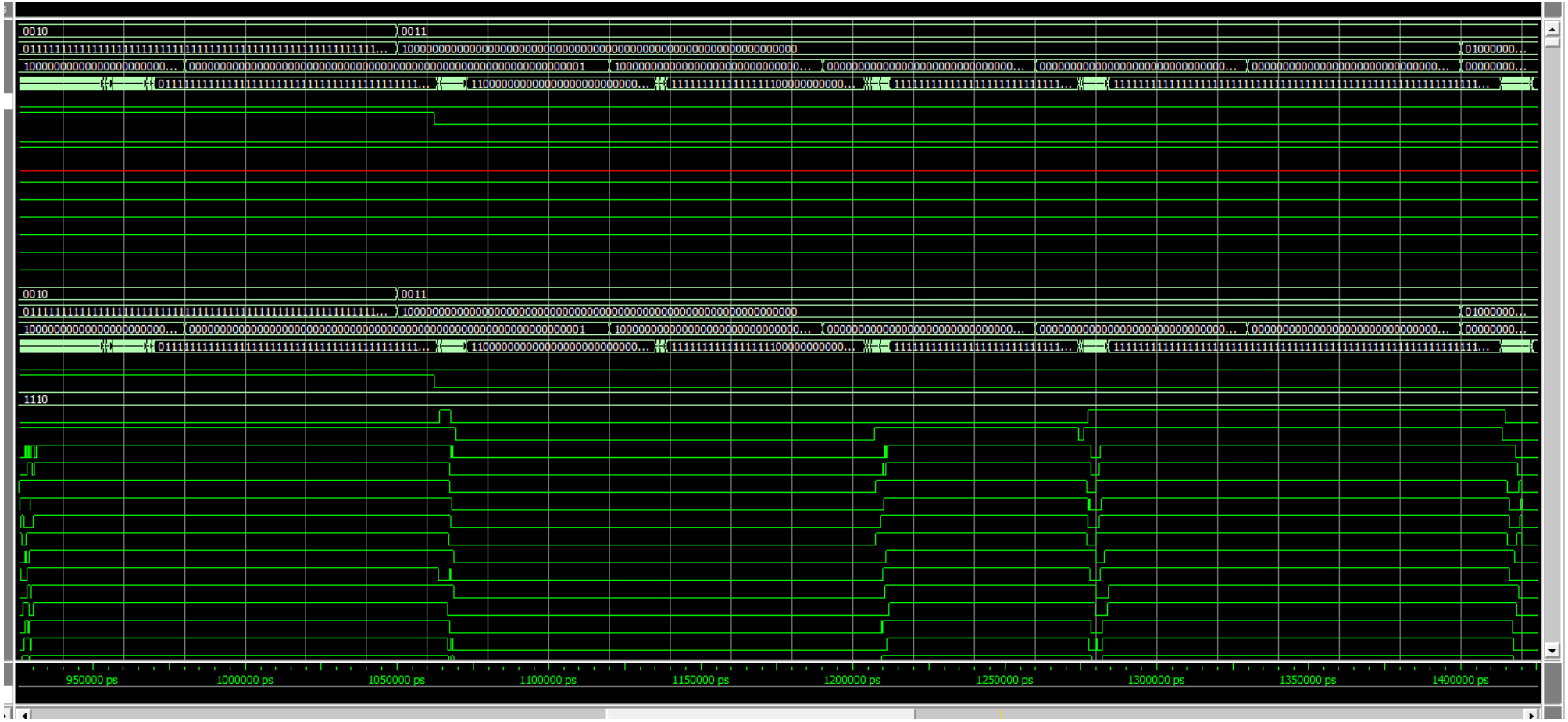

0010
0011
0100
1110
800000 ps
900000 ps
1000000 ps
1100000 ps
1200000 ps
1300000 ps
1400000 ps
1500000 ps
1600000 ps

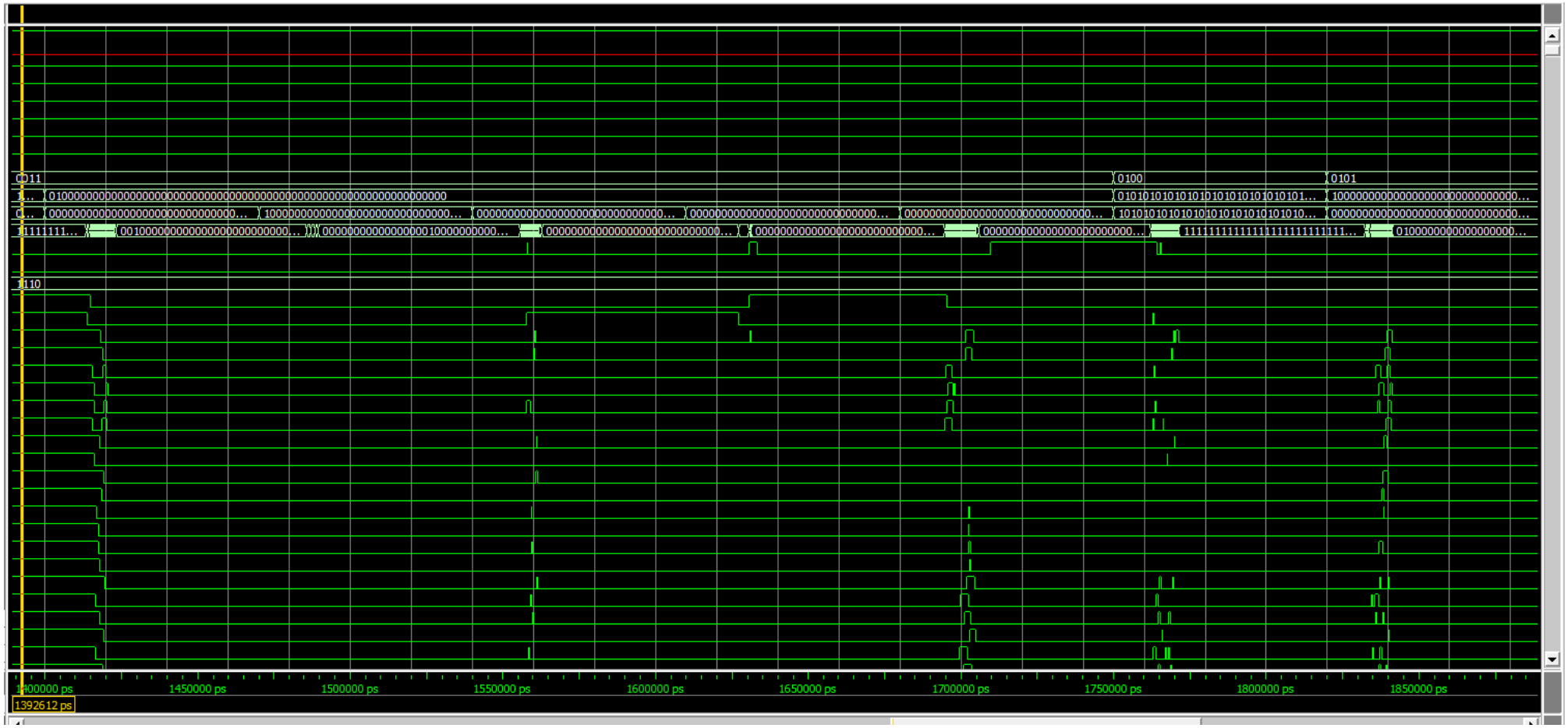

0100
0101
0110
0111
0010
1700000 ps
1800000 ps
1900000 ps
2000000 ps
2100000 ps
2200000 ps

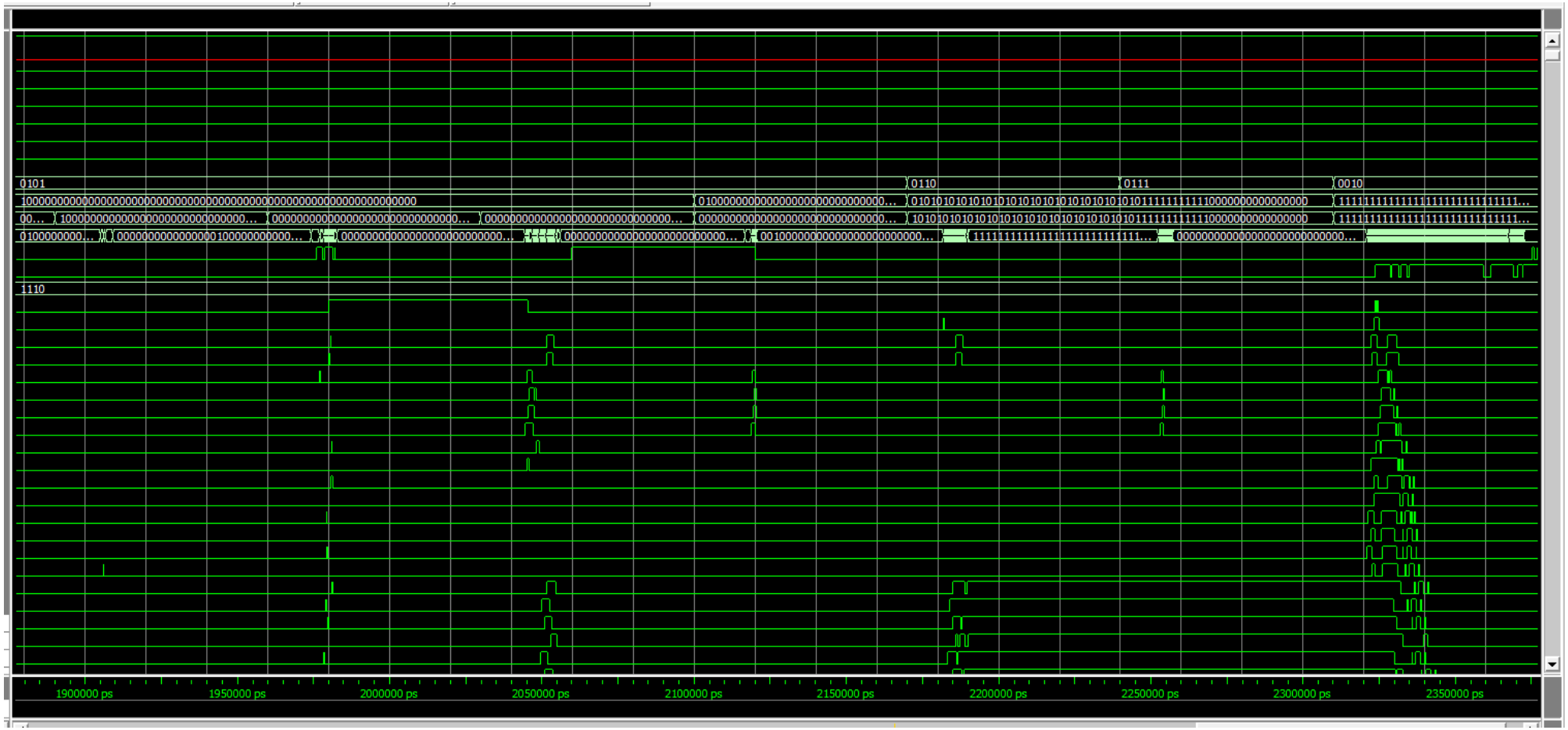
Assignment2 ALU 64 Correct

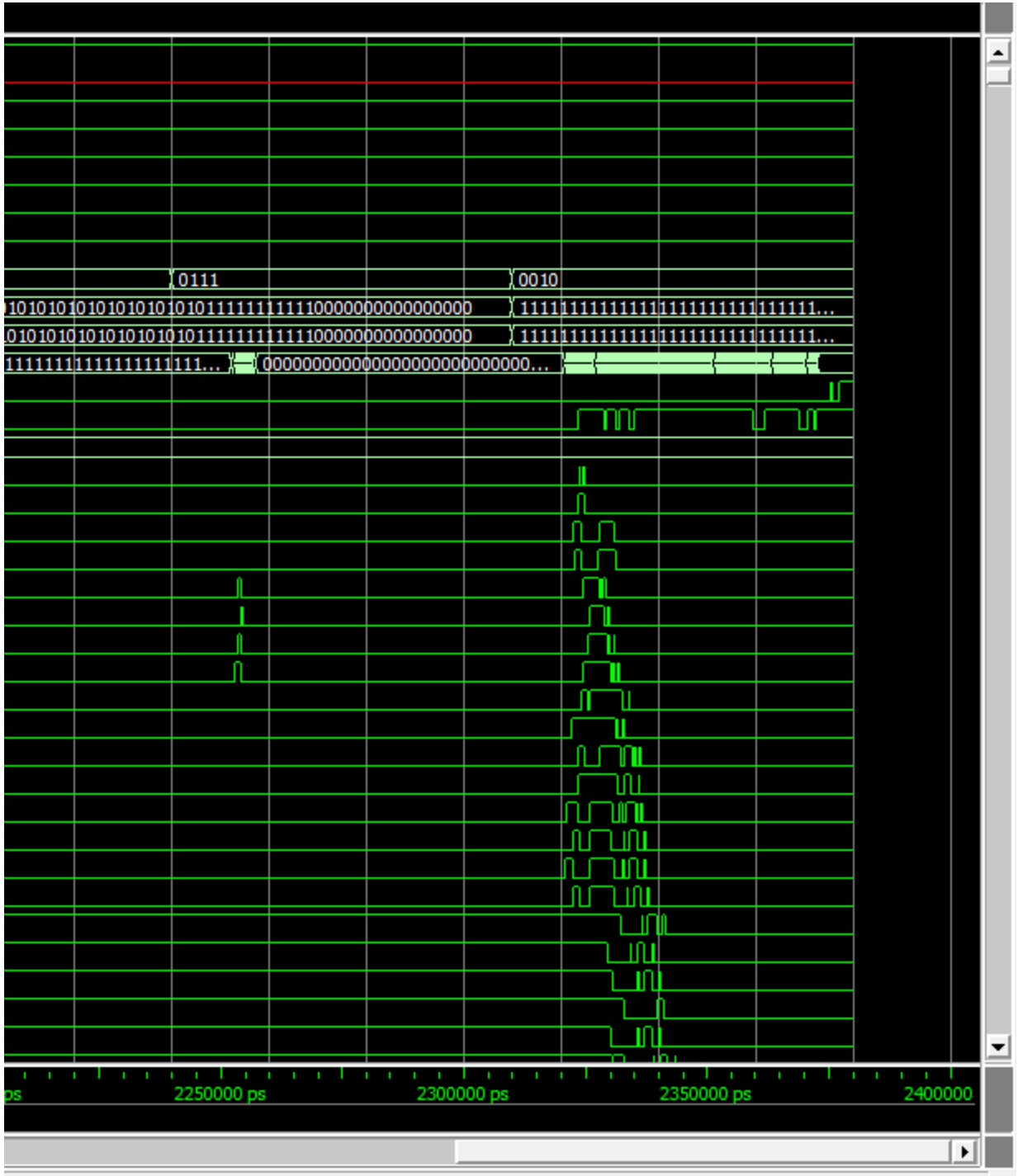



0001
0010
0001
0010
1110
500000 ps
550000 ps
600000 ps
650000 ps
700000 ps
750000 ps
800000 ps
850000 ps
900000 ps
950000 ps

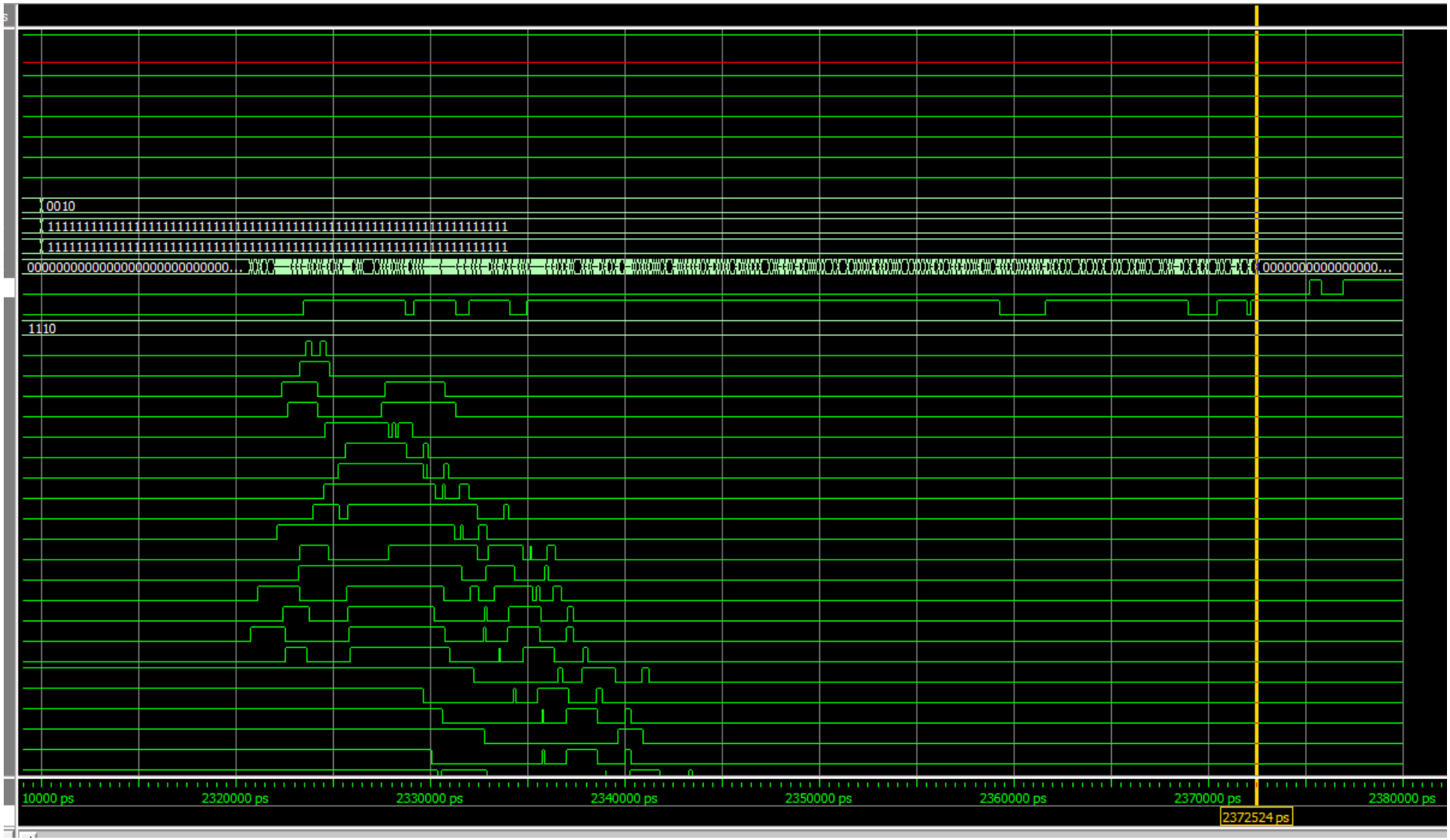

0010
0011
1110
950000 ps
1000000 ps
1050000 ps
1100000 ps
1150000 ps
1200000 ps
1250000 ps
1300000 ps
1350000 ps
1400000 ps


0 11
0 100
0 101
1110
1400000 ps
1450000 ps
1500000 ps
1550000 ps
1600000 ps
1650000 ps
1700000 ps
1750000 ps
1800000 ps
1850000 ps
1392612 ps


0101
0110
0111
0010
1110
1900000 ps
1950000 ps
2000000 ps
2050000 ps
2100000 ps
2150000 ps
2200000 ps
2250000 ps
2300000 ps
2350000 ps


0111
0010
2250000 ps
2300000 ps
2350000 ps
2400000

Worst case delay:



--worst case delay 1 and 0 with a carry, use 1 and 1 in the first bit to create carry for other bits, subtraction as bit flipping will also cause delay