Ordering & quality

Technical documentation

Design & development

Support & training

参考文献

TEXAS INSTRUMENTS

CD4066B
ZHCSKT0I – NOVEMBER 1998 – REVISED MAY 2024

CD4066B CMOS 四路双向开关

1 特性

- 15V 数字或 ±7.5V 峰峰值开关
- 工作电压为 15V 时
  典型导通电阻为 125Ω
- 在 15V 信号输入范围内匹配的
  开关导通电阻不超过 5Ω
- 在整个峰峰值信号范围内具有
  平坦的导通电阻
- 高开关输出电压比：
  f_{is} = 10kHz、R_L = 1kΩ 时典型值为 80dB
- 高度线性：f_{is} = 1kHz、V_{is} = 5V_{p-p}、
  V_{DD} – V_{SS} ≥ 10V、R_L = 10kΩ 时失真典型值小于
  0.5%
- 超低关断状态开关泄漏，从而产生较低的失调电流
  和高有效关断状态电阻：V_{DD} – V_{SS} = 10V、T_A =
  25°C 时的典型值为 10pA
- 较高控制输入阻抗
  （控制电路与信号电路相隔离）：
  典型值为 10^{12}Ω
- 低开关间串扰：f_{is} = 8MHz、R_L = 1kΩ 时典型值为
  –50dB
- 匹配的控制输入到信号输出电容：可减少输出信号
  瞬态
- 频率响应，
  开启 = 40MHz（典型值）
- 针对 20V 下的静态电流进行了 100% 测试
- 5V、10V 和 15V 参数额定值

2 应用

- 模拟信号开关和多路复用：信号门控、调制器、静
  噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用
- 模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
- 楼宇自动化

3 说明

CD4066B 器件是一款用于模拟或数字信号传输或多路
复用的四路双向开关。该器件与 CD4016B 器件引脚对
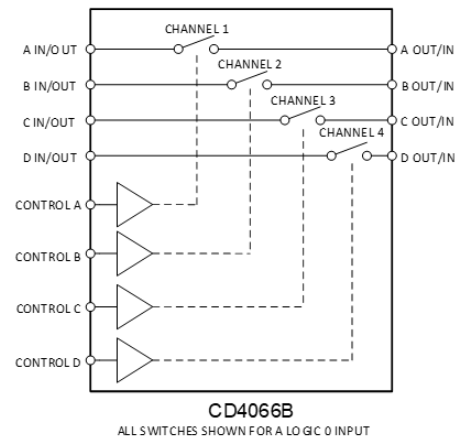引脚兼容，但导通状态电阻低得多。此外，导通状态电
阻在整个信号输入范围内相对恒定。

CD4066B 器件包含四个双向开关，每个开关都具有独
立的控件。3V 至 18V 的宽工作电源电压范围支持用于
广泛的应用。与单通道开关相比，优点包括峰值输入信
号电压摆幅等于最大电源电压以及在输入信号范围内具
有更恒定的导通状态阻抗。而对于采样保持应用，建议
使用 CD4016B 器件。

封装信息

器件型号	封装[1]	封装尺寸[2]
CD4066B	N（PDIP，14）	19.3mm × 9.4mm
	D（SOIC，14）	8.65mm × 6mm
	NS（SOP，14）	10.2mm × 7.8mm
	PW（TSSOP，14）	5mm × 6.4mm

(1) 有关更多信息，请参阅节 11
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

通过数字控制逻辑进行双向信号传输

Table of Contents

4 Pin Configuration and Functions

```
            ┌───┬─┐───┐
SIG A IN/OUT │1    14│ V_DD
SIG A OUT/IN │2    13│ CONTROL A
SIG B OUT/IN │3    12│ CONTROL D
SIG B IN/OUT │4    11│ SIG D IN/OUT
 CONTROL B   │5    10│ SIG D OUT/IN
 CONTROL C   │6     9│ SIG C OUT/IN
      V_SS   │7     8│ SIG C IN/OUT
            └───────┘
```

图 4-1. N, J, D, NS, or PW Packages 14-Pin PDIP, CDIP, SOIC, SOP, or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SIG A IN/OUT	1	I/O	Input/Output for Switch A
SIG A OUT/IN	2	I/O	Output/Input for Switch A
SIG B OUT/IN	3	I/O	Output/Input for Switch B
SIG B IN/OUT	4	I/O	Input/Output for Switch B
CONTROL B	5	I	Control pin for Switch B
CONTROL C	6	I	Control pin for Switch C
V_{SS}	7	—	Low Voltage Power Pin
SIG C IN/OUT	8	I/O	Input/Output for Switch C
SIG C OUT/IN	9	I/O	Output/Input for Switch C
SIG D OUT/IN	10	I/O	Output/Input for Switch D
SIG D IN/OUT	11	I/O	Input/Output for Switch D
CONTROL D	12	I	Control Pin for D
CONTROL A	13	I	Control Pin for A
V_{DD}	14	—	Power Pin

(1)   I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_{DD} – V_{SS}	Supply voltage		20	V
V_{DD}		– 0.5	20	V
V_{SS}		– 20	0.5	V
I_{SEL} or I_{EN}	Logic control input pin current ($\overline{EN}$, Ax, SELx)	– 30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS} – 0.5	V_{DD}+0.5	V
I_S or $I_{D\,(CONT)}$	Source or drain continuous current (Sx, D)	– 20	20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} – V_{SS} [1]	Power supply voltage differential	3		18	V
V_{DD}	Positive power supply voltage	3		18	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		V_{DD}	V
I_S or $I_{D\,(CONT)}$	Source or drain continuous current (Sx, D)	– 10		10	mA
T_A	Ambient temperature	– 55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $3V \leqslant (V_{DD} – V_{SS}) \leqslant 24V$, and the minimum V_{DD} is met.

提交文档反馈   3

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

5.4 Thermal Information

THERMAL METRIC[1]		CD406x				UNIT
		N (PDIP)	D (SOIC)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.7	109.7	112.4	101.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.5	69.4	70.4	44.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.0	67.9	76.4	68.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	50.3	25.8	28.9	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.3	67.1	75.4	67.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS		MIN TYP MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})						
V_{OS}	Switch output voltage		V_{DD} = 5V V_{is} = 0V		0.4	V
			V_{DD} = 5V V_{is} = 5V		4.6	V
			V_{DD} = 10V V_{is} = 0V		0.5	V
			V_{DD} = 10V V_{is} = 10V		9.5	V
			V_{DD} = 15V V_{is} = 0V		1.5	V
			V_{DD} = 15V V_{is} = 15V		13.5	V
ΔR_{ON}	On-state resistance difference between any two switches		R_L = 10k Ω, V_C = VDD	V_{DD} = 5V	15	Ω
	On-state resistance difference between any two switches	On-state resistance difference between any two switches		V_{DD} = 10V	10	
	On-state resistance difference between any two switches	On-state resistance difference between any two switches		V_{DD} = 15V	5	
V_{IHC}	Control input, high voltage		See Figure 7	V_{DD} = 5V	3.5	V
				V_{DD} = 10V	7	V
				V_{DD} = 15V	11	V

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

5.5 Electrical Characteristics（续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)[1]

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
	Maximum control input repetition rate	V_{IN} = V_{DD}, C_L = 50pF, R_L = 1kΩ V_C = 10V (square wave centered on 5V), t_r, t_f = 20ns, V_{os} = 1/2V_{os} at 1kHz	V_{DD} = 5V				6	MHz
			V_{DD} = 10V				9	
			V_{DD} = 15V				9.5	
C_{IN}	Input Capacitance					5	7.5	pF
I_{IS}	Switch input current	V_{DD} = 5V V_{is} = 0V	T_A = ‑55°C				0.64	mA
			T_A = ‑40°C				0.61	
			T_A = 25°C				0.51	
			T_A = 85°C				0.42	
			T_A = 125°C				0.36	
		V_{DD} = 5V V_{is} = 5V	T_A = ‑55°C				-0.64	mA
			T_A = ‑40°C				-0.61	
			T_A = 25°C				-0.51	
			T_A = 85°C				-0.42	
			T_A = 125°C				-0.36	
		V_{DD} = 10V V_{is} = 0V	T_A = ‑55°C				1.6	mA
			T_A = ‑40°C				1.5	
			T_A = 25°C				1.3	
			T_A = 85°C				1.1	
			T_A = 125°C				0.9	
		V_{DD} = 10V V_{is} = 10V	T_A = ‑55°C				-1.6	mA
			T_A = ‑40°C				-1.5	
			T_A = 25°C				-1.3	
			T_A = 85°C				-1.1	
			T_A = 125°C				-0.9	
		V_{DD} = 15V V_{is} = 0V	T_A = ‑55°C				4.2	mA
			T_A = ‑40°C				4	
			T_A = 25°C				3.4	
			T_A = 85°C				2.8	
			T_A = 125°C				2.4	
		V_{DD} = 15V V_{is} = 15V	T_A = ‑55°C				-4.2	mA
			T_A = ‑40°C				-4	
			T_A = 25°C				-3.4	
			T_A = 85°C				-2.8	
			T_A = 125°C				-2.4	

Product Folder Links: *CD4066B*

English Data Sheet: *SCHS051*

5.5 Electrical Characteristics （续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Quiescent Device Current All switches OFF	V_{is} = 0 to 5V V_{DD} = 5V	T_A = −55°C				5	µA
			T_A = −40°C				5	
			T_A = 25°C			4	6	
			T_A = 85°C				7	
			T_A = 125°C				7.5	
		V_{is} = 0 to 10V V_{DD} = 10V	T_A = −55°C				6	
			T_A = −40°C				6	
			T_A = 25°C			5	7	
			T_A = 85°C				8	
			T_A = 125°C				9	
		V_{is} = 0 to 15V V_{DD} = 15V	T_A = −55°C				7	
			T_A = −40°C				7.5	
			T_A = 25°C			5.5	8	
			T_A = 85°C				9	
			T_A = 125°C				10	
		V_{is} = 0 to 20V V_{DD} = 20V	T_A = −55°C				8.5	
			T_A = −40°C				8.5	
			T_A = 25°C			6.5	9	
			T_A = 85°C				10	
			T_A = 125°C				11	
r_{ON}	ON Resistance r_{ON} Max	to $(V_{DD}+V_{SS})/2$,V_C = V_{DD},R_L = 10kΩ returned V_{is} = V_{SS} to V_{DD}	V_{DD} = 5V	T_A = −55°C			800	Ω
				T_A = −40°C			850	
				T_A = 25°C		470	1050	
				T_A = 85°C			1200	
				T_A = 125°C			1300	
			V_{DD} = 10V	T_A = −55°C			310	
				T_A = −40°C			330	
				T_A = 25°C		180	400	
				T_A = 85°C			500	
				T_A = 125°C			500	
			V_{DD} = 15V	T_A = −55°C			200	
				T_A = −40°C			210	
				T_A = 25°C		125	240	
				T_A = 85°C			300	
				T_A = 125°C			320	

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

5.5 Electrical Characteristics （续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
V_{ILC}	Control input, low voltage (max)	$\|I_{is}\|$ < 10 µA, V_{is} = V_{SS}, V_{OS} = V_{DD}, and V_{is} = V_{DD}, V_{OS} = V_{SS}	V_{DD} = 5V	T_A = – 55°C				1	V
				T_A = – 40°C				1	
				T_A = 25°C				1	
				T_A = 85°C				1	
				T_A = 125°C				1	
			V_{DD} = 10V	T_A = – 55°C				1	
				T_A = – 40°C				1	
				T_A = 25°C				1	
				T_A = 85°C				1	
				T_A = 125°C				1	
			V_{DD} = 15V	T_A = – 55°C				1	
				T_A = – 40°C				1	
				T_A = 25°C				1	
				T_A = 85°C				1	
				T_A = 125°C				1	
I_{IN}	Input current (max)		V_{is} ⩽ V_{DD}, V_{DD} – V_{SS} = 18V, V_{CC} ⩽ V_{DD} – V_{SS} V_{DD} = 18V	T_A = – 55°C		-0.8		0.8	µA
				T_A = – 40°C		-0.8		0.8	
	Input current (max)	Input current (max)		T_A = 25°C		-0.7	±0.2	0.7	
				T_A = 85°C		-0.6		0.6	
	Input current (max)	Input current (max)		T_A = 125°C		-0.55		0.55	

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.

5.6 Switching Characteristics

T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Signal input	Signal output	V_{IN} = V_{DD}, t_r, t_f = 20ns, C_L = 50pF, R_L = 1k Ω	5V		20	40	ns
				10V		10	20	
				15V		7	15	
t_{plh}	Signal input	Signal output	V_{IN} = V_{DD}, t_r, t_f = 20ns, C_L = 50pF, R_L = 1k Ω	5V		35	70	ns
				10V		20	40	
				15V		15	30	
t_{phl}	Signal input	Signal output	V_{IN} = V_{DD}, t_r, t_f = 20ns, C_L = 50pF, R_L = 1k Ω	5V		35	70	ns
				10V		20	40	
				15V		15	30	

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

5.7 Typical Characteristics
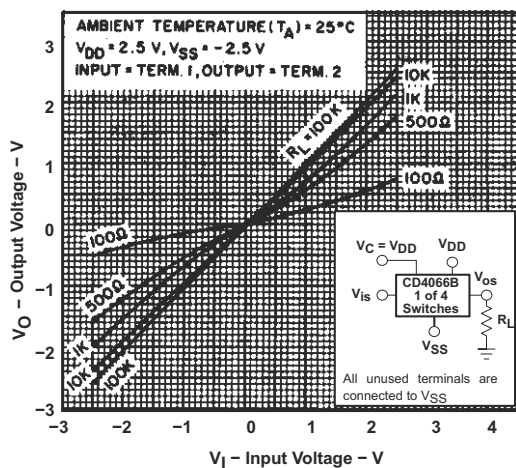

图 5-1. Typical ON Characteristics for 1 of 4 Channels
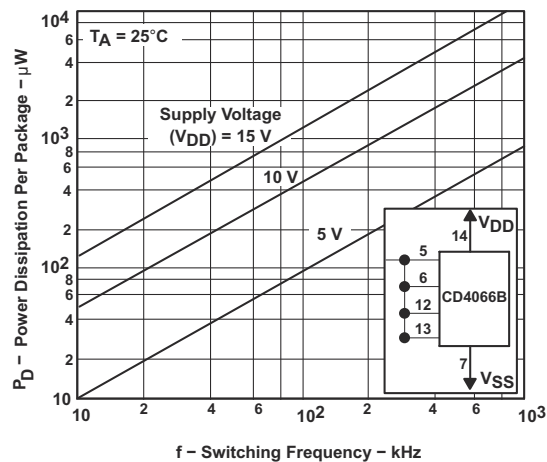
图 5-2. Power Dissipation per Package vs Switching Frequency

Product Folder Links: *CD4066B*

English Data Sheet: *SCHS051*

6 Parameter Measurement Information

$$r_{on} = \frac{|V_{is} - V_{os}|}{|I_{is}|}$$

Copyright © 2016, Texas Instruments Incorporated

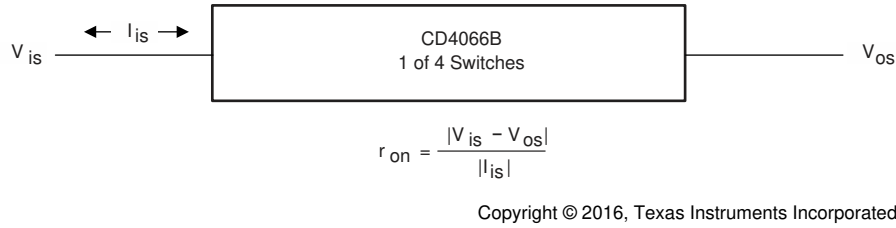图 **6-1. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification**
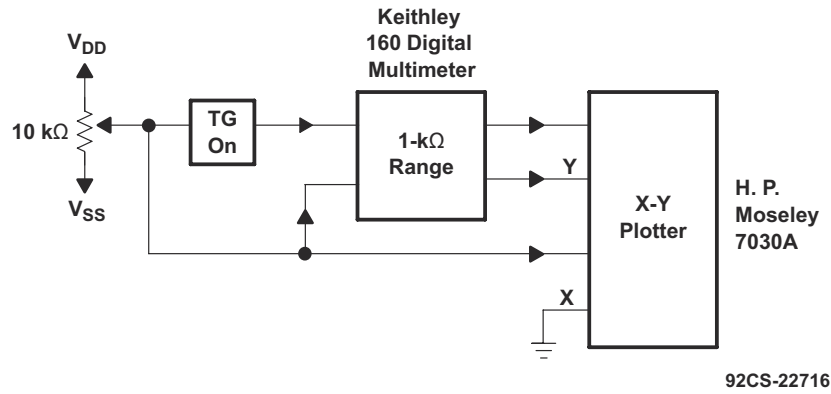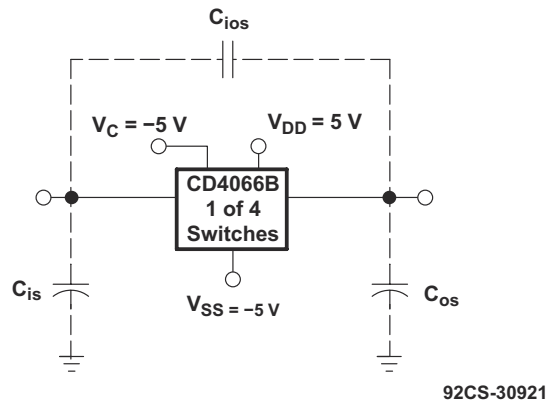
92CS-22716

图 **6-2. Channel On-State Resistance Measurement Circuit**

92CS-30921

Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

图 **6-3. Typical On Characteristics for One of Four Channels**

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

$V_C = V_{SS}$

V_{DD}

$V_{is} = V_{DD}$

CD4066B
1 of 4
Switches

V_{os}

V_{SS}
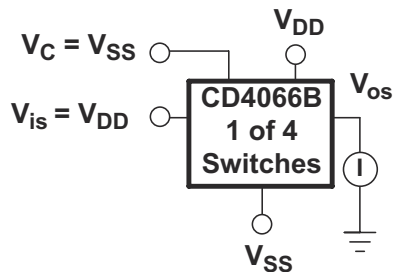
92CS-30922

All unused terminals are connected to V_{SS}.

图 **6-4. Off-Switch Input or Output Leakage**

$V_C = V_{DD}$

V_{DD}

V_{is}

CD4066B
1 of 4
Switches

V_{os}

V_{SS} 50 pF   200 kΩ

V_{DD} $t_r = t_f = 20$ ns
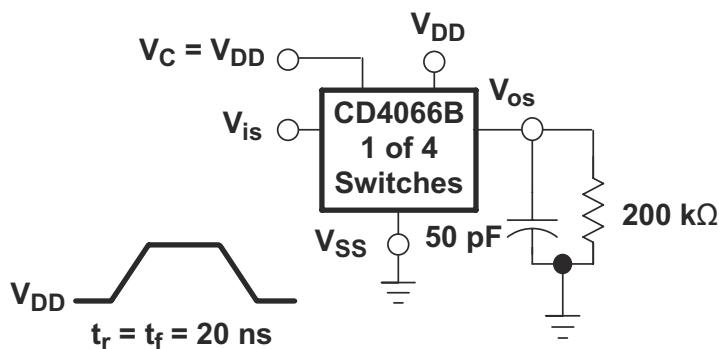
92CS-30923

All unused terminals are connected to V_{SS}.

图 **6-5. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})**

+10 V $t_r = t_f = 20$ ns

V_C V_{DD}

V_{is} CD4066B
1 of 4
Switches V_{os}

1 kΩ V_{SS} 10 kΩ
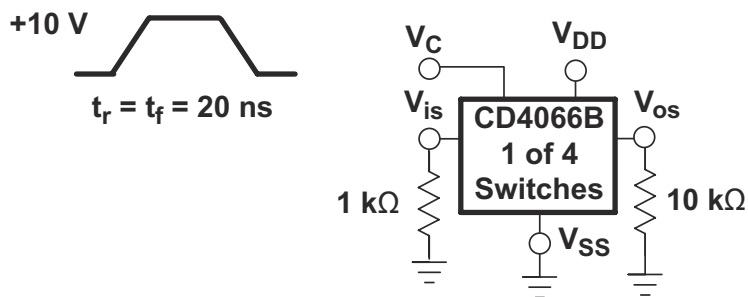
92CS-30924

All unused terminals are connected to V_{SS}.

图 **6-6. Crosstalk-Control Input to Signal Output**

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051
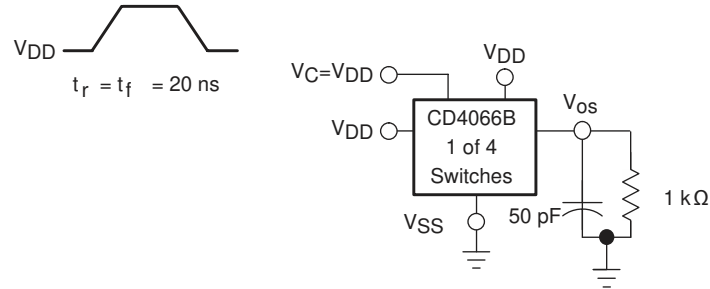
Copyright © 2016, Texas Instruments Incorporated

All unused pins are connected to V_{SS}.

Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

图 6-7. Propagation Delay, t_{PLH}, t_{PHL} Control-Signal Output
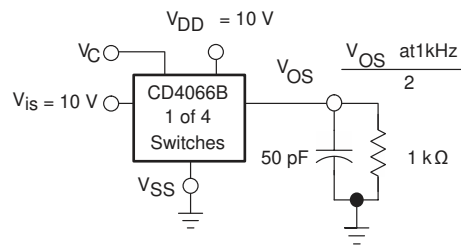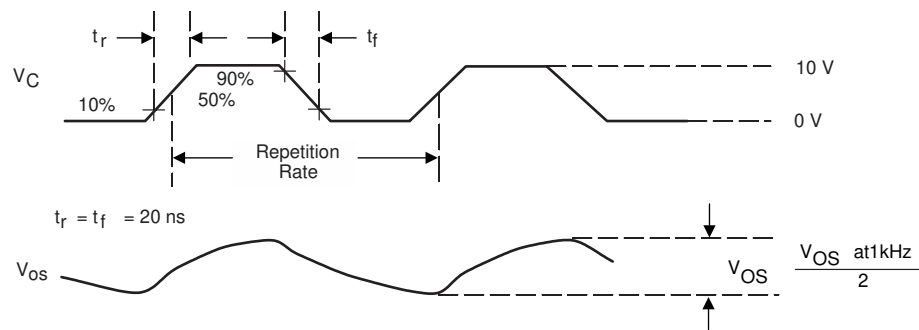
Copyright © 2016, Texas Instruments Incorporated

All unused pins are connected to V_{SS}.

图 6-8. Maximum Allowable Control-Input Repetition Rate

Product Folder Links: *CD4066B*

English Data Sheet: *SCHS051*

92CS-27555
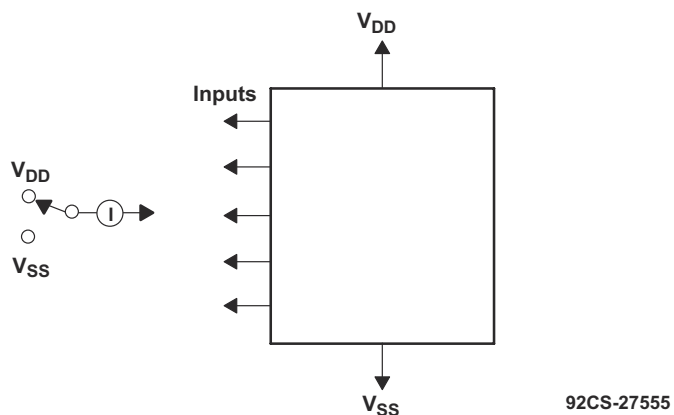
Measure inputs sequentially to both V_{DD} and V_{SS}. Connect all unused inputs to either V_{DD} or V_{SS}. Measure control inputs only.

图 **6-9. Input Leakage-Current Test Circuit**
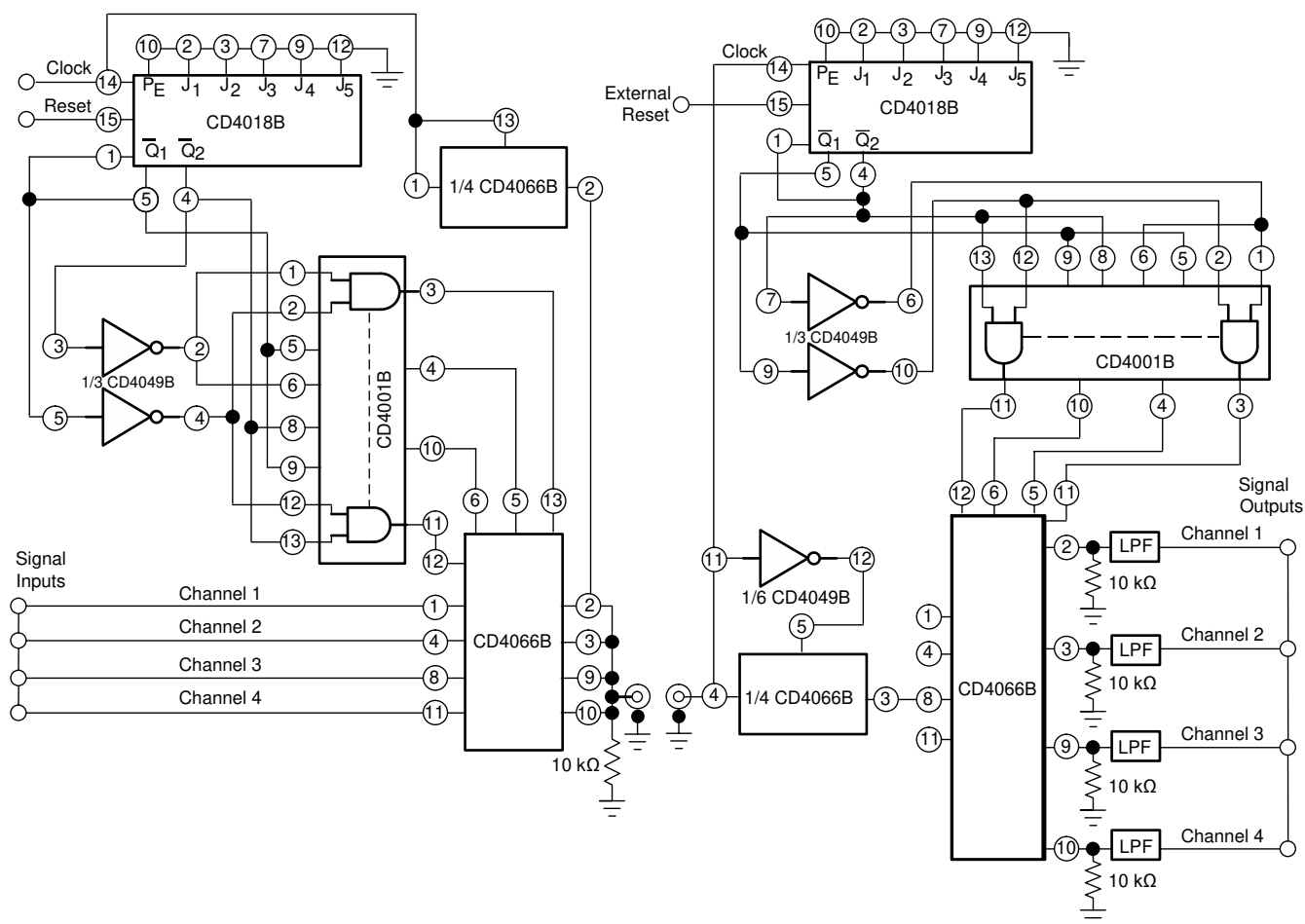
Copyright © 2016, Texas Instruments Incorporated

图 **6-10. Four-Channel PAM Multiplex System Diagram**

Product Folder Links: *CD4066B*

English Data Sheet: *SCHS051*

7 Detailed Description

7.1 Overview

CD4066B has four independent digitally controlled analog switches with a bias voltage of V_{SS} to allow for different voltage levels to be used for low output. Both the p and n devices in a given switch are biased on or off simultaneously by the control signal. As shown in 图 7-1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). Thus, when the control of the device is low, the output of the switch goes to V_{SS} and when the control is high the output of the device goes to V_{DD}.

7.2 Functional Block Diagram
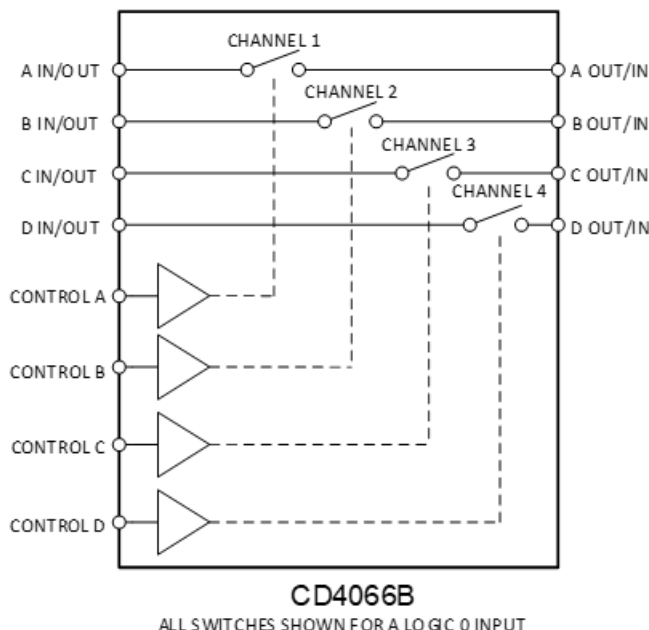
A. All control inputs are protected by the CMOS protection network.
B. All p substrates are connected to V_{DD}.
C. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$.
D. Signal-level range: $V_{SS} \leqslant V_{is} \leqslant V_{DD}$.

图 7-1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

7.3 Feature Description

Each switch has different control pins, which allows for more options for the outputs. Bias Voltage allows the device to output a voltage other than 0V when the device control is low. The CD4066B has a large absolute maximum voltage for V_{DD} of 20V.

7.4 Device Functional Modes

表 7-1 lists the functions of this device.

表 7-1. Function Table

INPUTS		OUTPUT
SIG IN/OUT	CONTROL	SIG OUT/IN
H	H	H
L	H	L
X	L	Hi-Z

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B device bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B device.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into pins 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8V (calculated from r_{on} values shown).

No V_{DD} current flows through R_L if the switch current flows into pins 2, 3, 9, or 10.

8.2 Typical Application
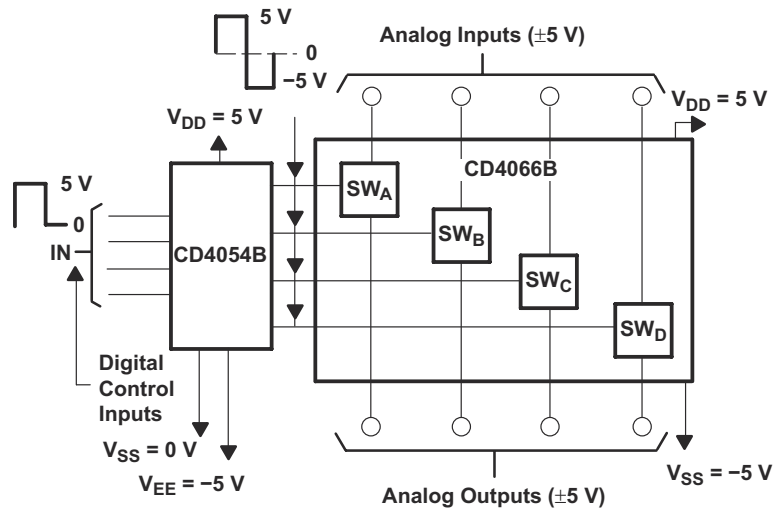
图 8-1. Bidirectional Signal Transmission Through Digital Control Logic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommended output conditions:
   - Load currents should not exceed ±10mA.

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

8.2.3 Application Curve
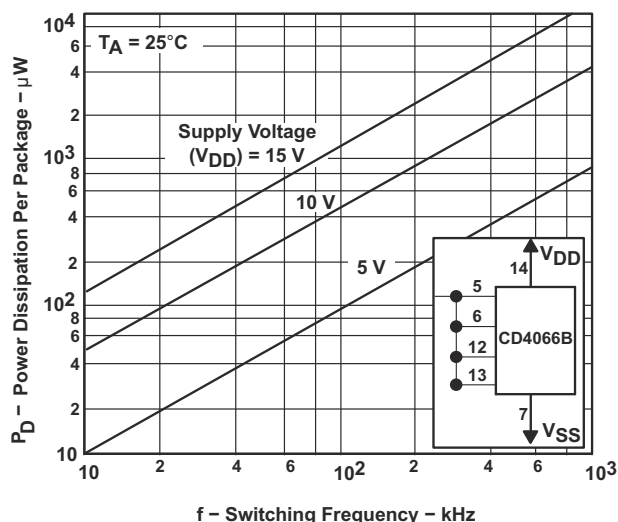
图 8-2. Power Dissipation vs. Switching Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in *Recommended Operating Conditions*.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF is recommended; if there are multiple VCC pins, then 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1µF and a 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input *and* gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

8.4.2 Layout Example
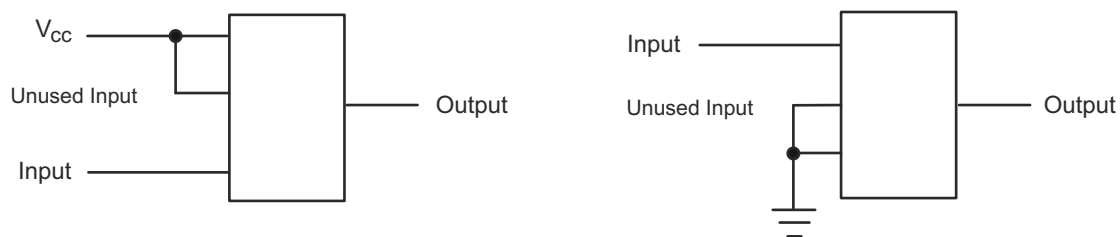
图 8-3. Diagram for Unused Inputs

Product Folder Links: *CD4066B*

English Data Sheet: SCHS051

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　　　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4066BE	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BEE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4066BE	Samples
CD4066BF	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4066BF	Samples
CD4066BF3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4066BF3A	Samples
CD4066BM96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CD4066BM	Samples
CD4066BNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4066B	Samples
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	CM066B	Samples
JM38510/05852BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples
M38510/05852BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 05852BCA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4066B, CD4066B-MIL :

- Catalog : CD4066B

- Automotive : CD4066B-Q1, CD4066B-Q1

- Military : CD4066B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4066BPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4066BM96	SOIC	D	14	2500	340.5	336.1	32.0
CD4066BM96G4	SOIC	D	14	2500	340.5	336.1	32.0
CD4066BM96G4	SOIC	D	14	2500	356.0	356.0	35.0
CD4066BMT	SOIC	D	14	250	210.0	185.0	35.0
CD4066BNSR	SO	NS	14	2000	356.0	356.0	35.0
CD4066BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
CD4066BPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4066BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BE	N	PDIP	14	25	506.1	9	600	5.4
CD4066BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BEE4	N	PDIP	14	25	506.1	9	600	5.4
CD4066BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4066BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4066BNS	NS	SOP	14	50	530	10.5	4000	4.1
CD4066BPW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD4066BPWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS
INSTRUMENTS

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060 TYP
[0.38-1.52]

1

14

12X .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

J0014A

(.300) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

SYMM
₵

14X (∅ .039)
[1]

7

8

SYMM
₵
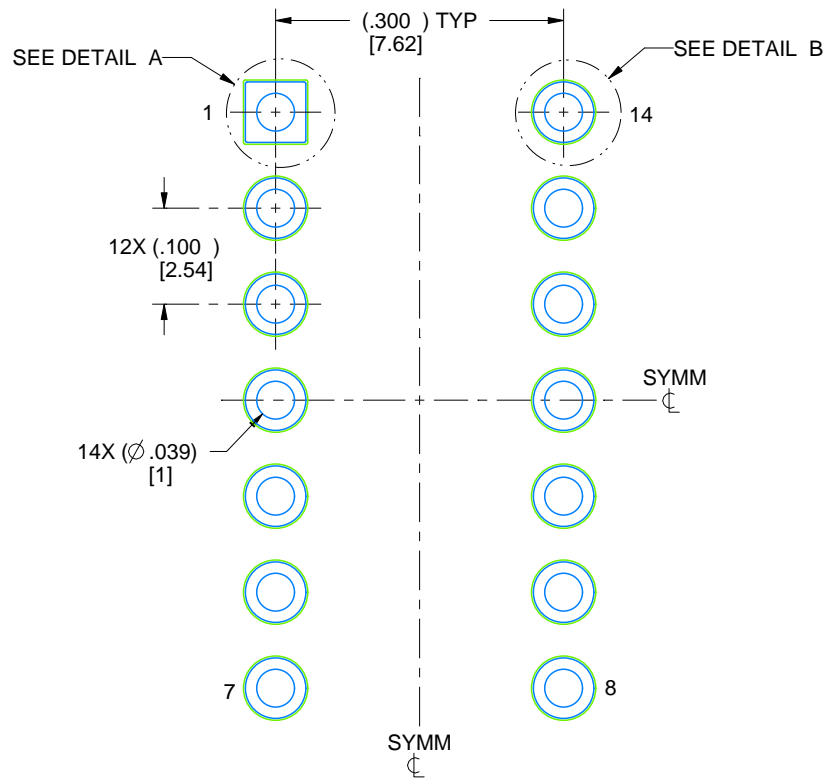
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(∅ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X

4214771/A   05/2017

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

$$\frac{0.344\ (8,75)}{0.337\ (8,55)}$$

$$\frac{0.244\ (6,20)}{0.228\ (5,80)}$$

$$\frac{0.157\ (4,00)}{0.150\ (3,80)}$$

14   8

1   7

Pin 1
Index Area

0.050 (1,27)

$$\frac{0.020\ (0,51)}{0.012\ (0,31)}$$

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

$$\frac{0.010\ (0,25)}{0.004\ (0,10)}$$

$$\frac{0.010\ (0,25)}{0.005\ (0,13)}$$

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

$$\frac{0.050\ (1,27)}{0.016\ (0,40)}$$

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
          D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E. Reference JEDEC MS−012 variation AB.
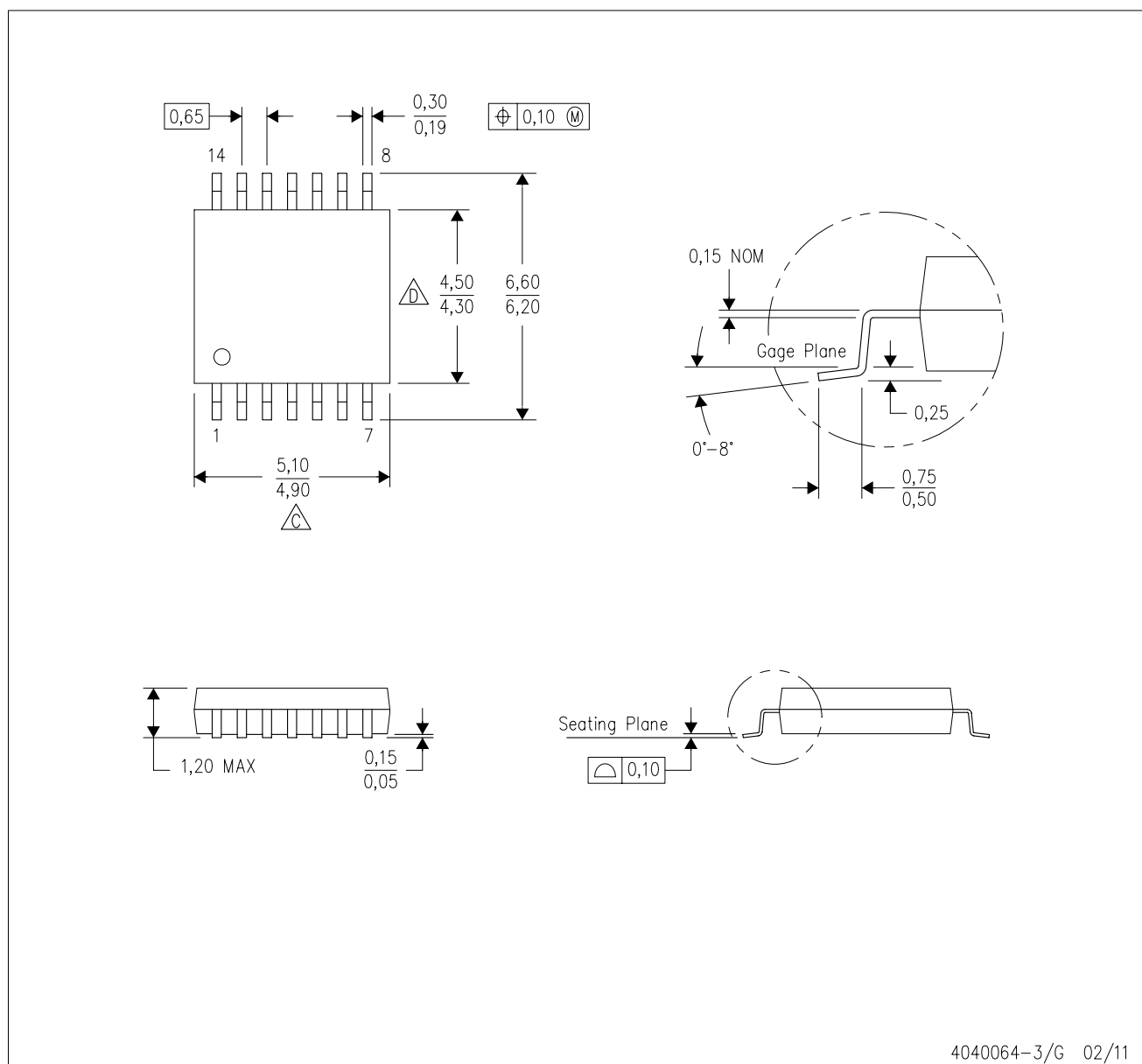
Texas
Instruments
www.ti.com

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

14x1,50

12x1,27

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0.07
All Around

Example
Solder Mask Opening
(See Note E)

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

$\oplus$ | 0,10 Ⓜ

14   8

Ⓓ 4,50
   4,30

6,60
6,20

1   7

5,10
4,90

Ⓒ

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,10

4040064−3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B. This drawing is subject to change without notice.
          Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
          Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E. Falls within JEDEC MO−153

PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

|←12x0,65

14x0,30 →|

12x0,65

14x1,55

5,60

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284−2/G 08/15

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

重要声明和免责声明