Heart Pulse Signal Detector CT1798C

The CT1798C is a chip dedicates to detect the heart-pulse signal from human body.

Features

1. Build-in switched capacitor filter for minimum external compoents
2. Build-in 50Hz/60Hz notch filter for highly reject AC noise
3. On chip 1V band-gap reference to stabilize oscillation frequency
4. Low operating current @ 1mA
5. Low standby current < 3uA
6. On chip hand-holding detect function
7. Build-in differential amplifier for slope detector with Auto Leveling

Block diagram

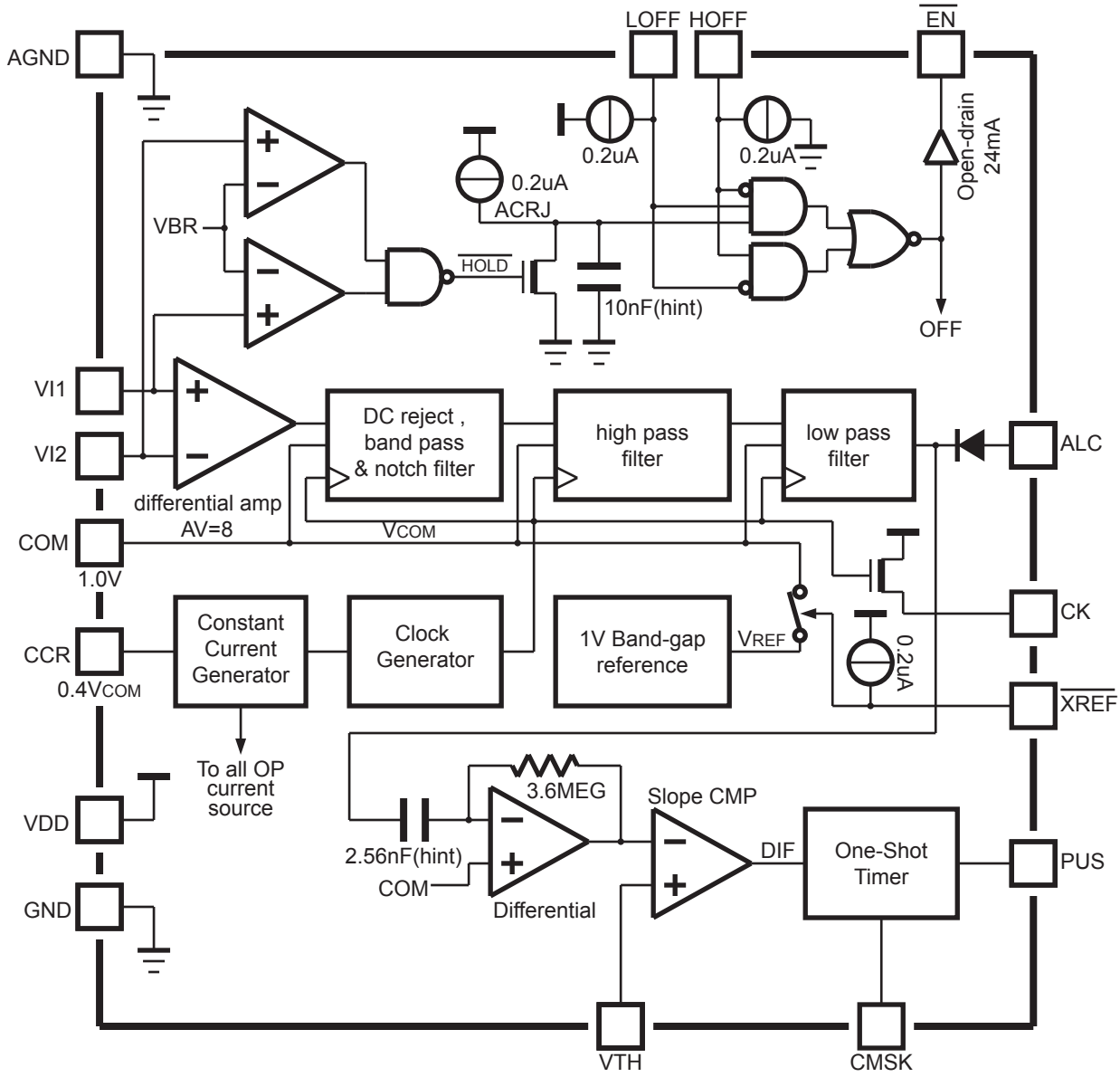


Fig. 1

Heart Pulse Signal Detector CT1798C

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied Voltage	Vmax	9	V
Power dissipation	Pd	350	mW
Operating temperature	Topr	-25~+75	°C
Storage temperature	Tstg	-55~125	°C

Electrical characteristics (unless otherwise noted, Ta=25°C, V_{DD}=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note.
Quiescent Current	I_{DD}	-	3	15	uA	
Operation Current	I_{DD}	-	1	3	mA	
Operation Voltage range	V_{DD}	2.4	-	6.5	V	
Voltage Reference(ON)	V_{REF}	0.80	1.00	1.20	V	1
Voltage Reference(Standby)	V_{REF}	0.4	0.6	0.8	V	
Constant Current resistor range	R_{CC}	50	200	2000	KΩ	2
Constant Current Voltage	V_{RCC}	0.38	0.40	0.42	V	
Constant Current	I_{CC}	-	2	-	uA	3
Hand-hold detect voltage	V_{BG}	0.14	0.15	0.16	V_{COM}	
Clock Frequency	F_{CK}	-	1068	-	Hz/uA	4
Pull-up Current(XREF,LOFF)	I_{PU}	0.1	0.2	0.5	uA	
Pull-down Current(HOFF)	I_{PD}	0.1	0.2	0.5	uA	
Input DC resistance(VI1,VI2)	R_{VI}	1E9	-	-	Ω	
Input capacitance(VI1,VI2)	C_{VI}	-	16	40	pF	
Charge Current(CMSK)	I_{MSK}	1/5.5	1/5	1/4.5	I_{CC}	
Minimum High Level Output Voltage(PUS)	V_{OH}	V_{DD}-0.2	-	-	V	5
Maximum Low Level Output Voltage(PUS)	V_{OL}	-	-	0.2	V	5
Maximum Low Level Output Voltage(ENb)	V_{OL1}	-	-	0.2	V	6
Output Sink Current(ALC)	I_{OL}	12	-	-	mA	

Note1. No loadding

Note2. Whole chip constant current depend on this resistor

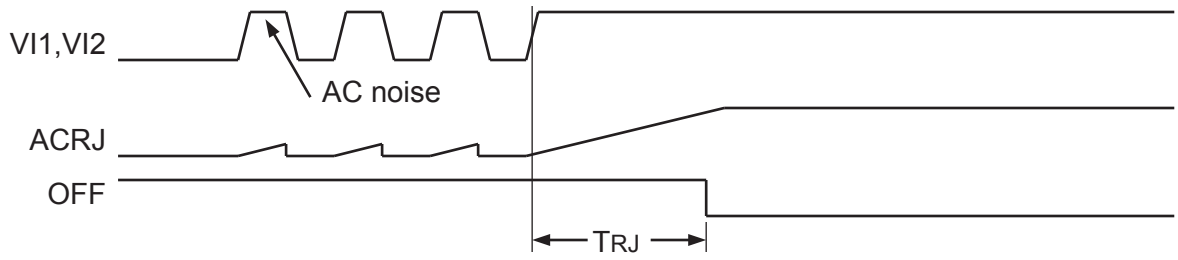
Note3. Depend on RCC setting

Note4. For notch frequency at 50Hz, this frequency must be 2136Hz(40π*17Hz)

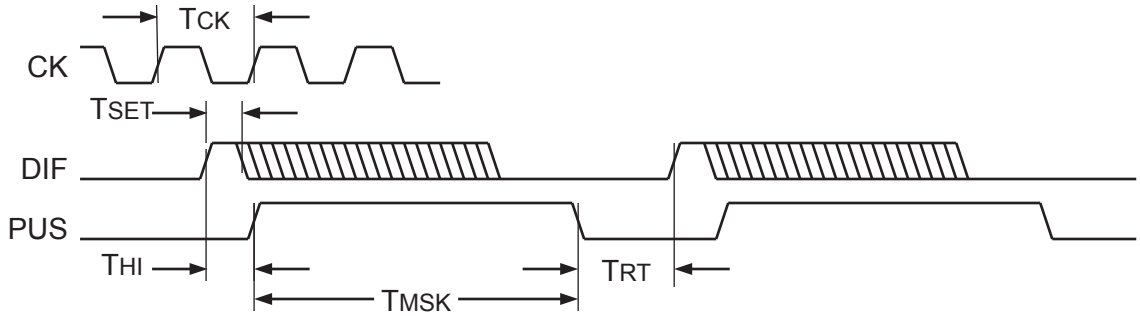
Note5. Sink current<8mA; Source current<4mA

Note6. Sink current<24mA

Hand-holding detect timming (AC Reject function,HOFF=0,LOFF=VDD)



Pulse Output timming(No CMSK or CMSK<20pF)

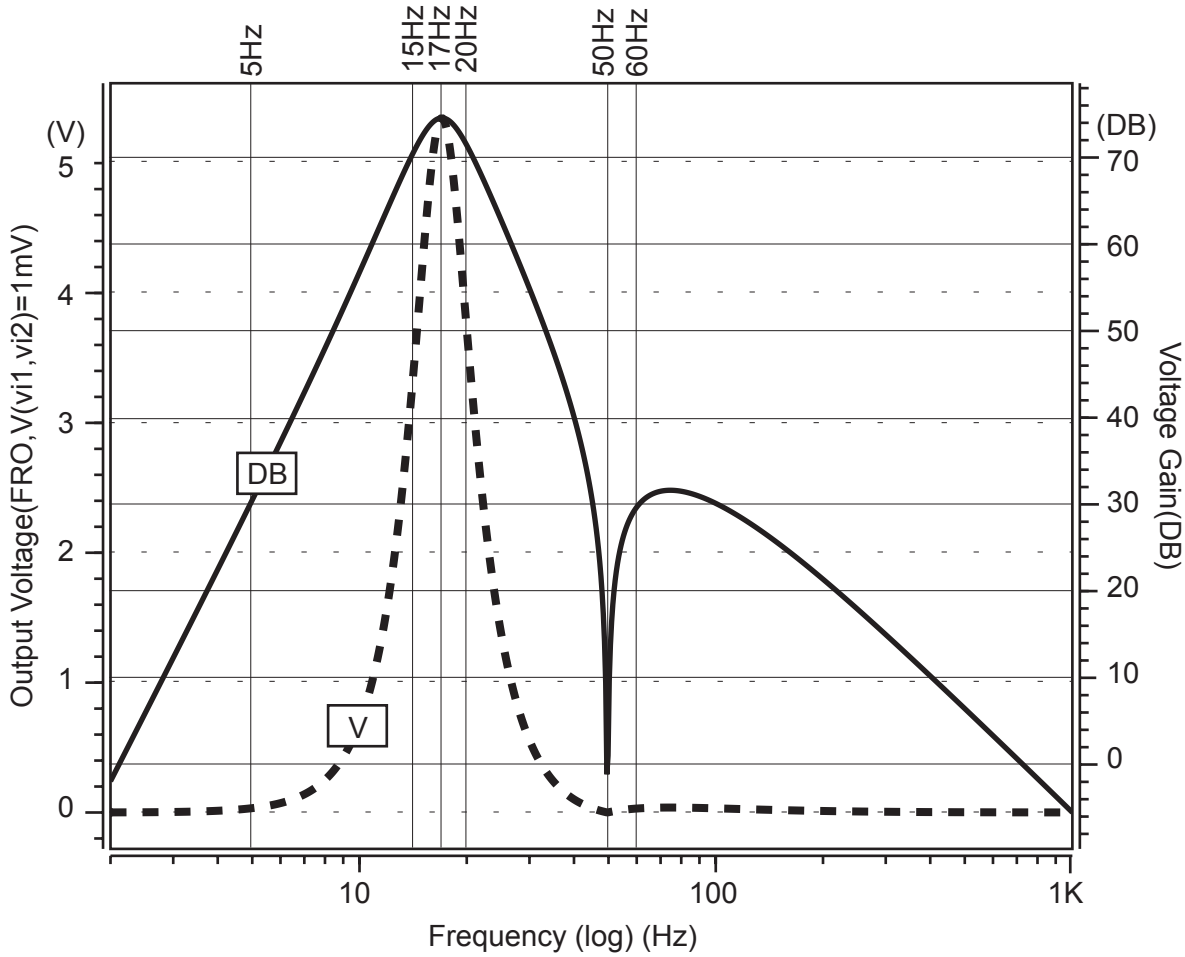


Timming characteristics (unless otherwise noted, Ta=25°C, VDD=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
AC Reject time	TRJ	20	20	120	mS	
System clock period	TCK	50	468.2	2000	uS	1
Pulse output setting time	TSET	0	-	1	TCK	
Pulse output delay time	THI	1	-	2	TCK	
Pulse width	TMSK	-	512	-	TCK	
Re-trigger period	TRT	1	-	2	TCK	

Note1. TCK(uS)=2.314 x RCC(KΩ)

Filter Response Diagram

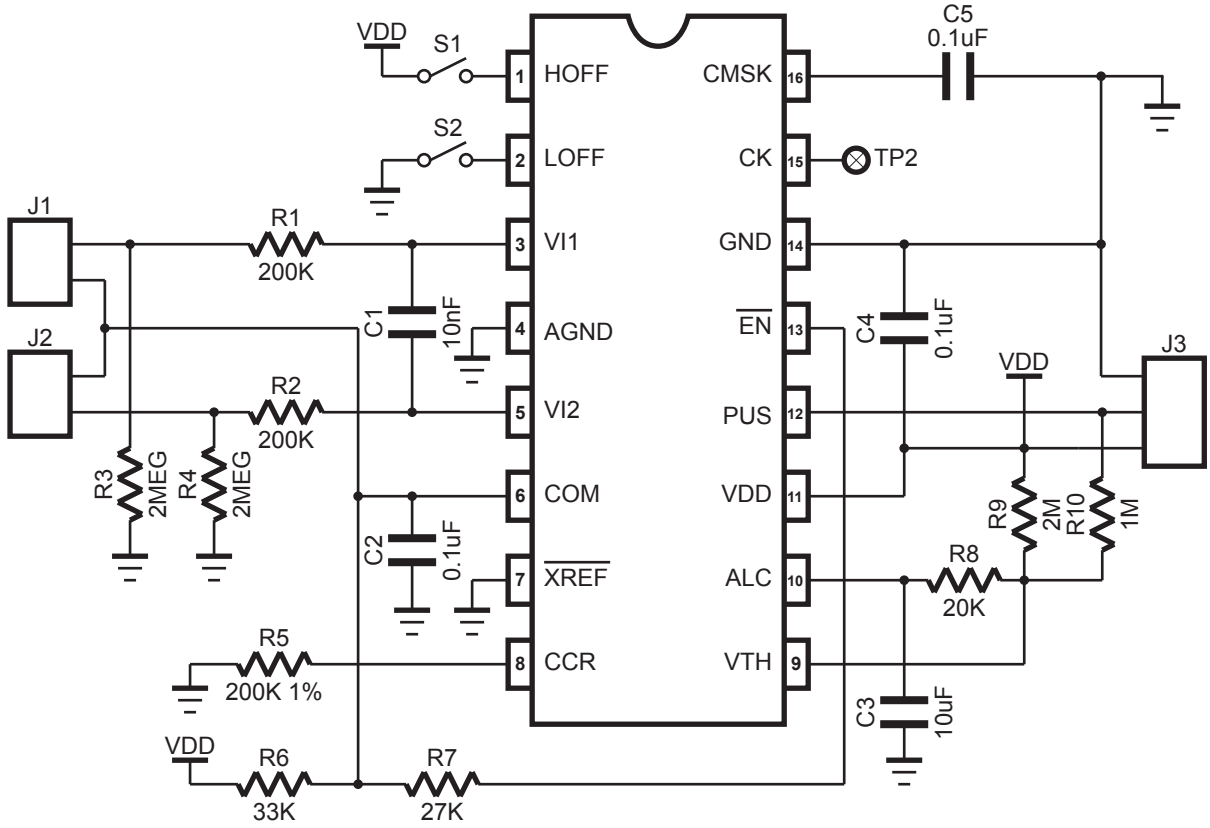


** Clock frequency=2136Hz
** Input voltage(VI2,VI1)=1mV

PIN Description

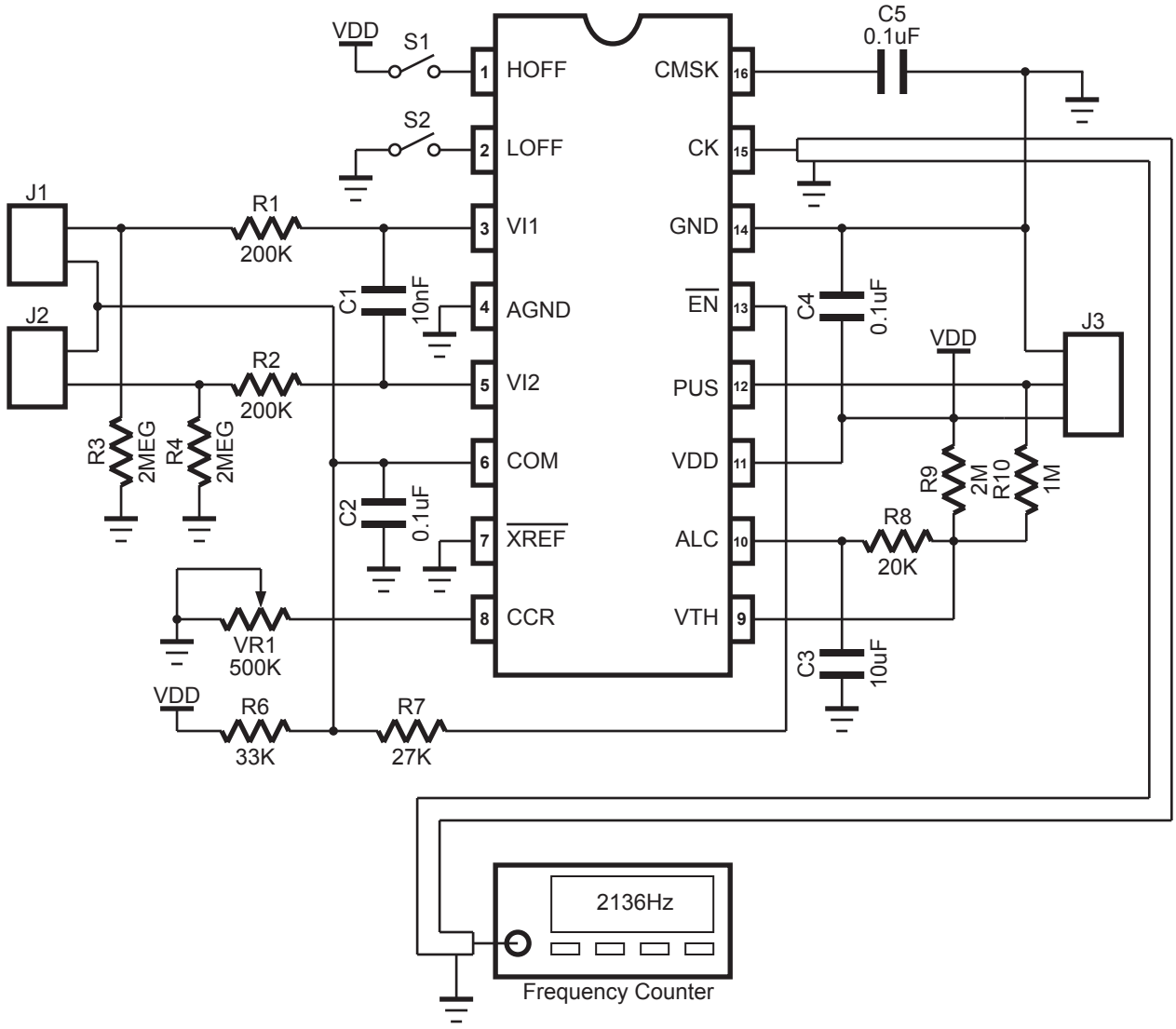
PIN	Description
VDD	Supply voltage.
GND	Ground.
AGND	Analog Ground.
COM	Whole chip analog circuit BIAS voltage. This pin must connect a bypass capacitor to AGND for reduce high frequency noise.
VI1	ECG signal input and hand holding detect input.
VI2	ECG signal input and hand holding detect input.
CCR	Resistor of constant current generator. Swicthed capacitor filter must have a regular clock frequency, CT1798C using integration oscillator to generate this clock. CT1798C build-in high precision capacitor inside, the clock frequency accuracy depend on COM pin voltage and constant current accuracy.
CMSK	Capacitor for output pulse width one-shot monostable multivibrator. If no capacitor connect on this pin, CT1798C will generate fixed width output pulse automatically, the pulse width is 512/clock_frequency.
VTH	Threshold voltage of filter output slope detector. Haert-rate signal on filter output 0.6V minimally. CT1798C must bias this pin below COM pin voltage externally. If need more sensitive could be bias this pin near to COM pin voltage.
PUS	Active high digital output of heart rate.
$\overline{\text{XREF}}$	External reference voltage selector. If connect this pin to GND will disable internal band-gap voltage reference, at this time must supply a regular voltage on COM pin externally.
$\overline{\text{EN}}$	Open drain output of power ON signal.
HOFF	This pin pull down internally, connect this pin to VDD cause entry power down state even hand holding or not. (When HOFF=1 and LOFF=0 will entry power ON state even hand not holding.)
LOFF	This pin pull high internally, connect this pin to GND cause entry power down state even hand holding or not.
CK	Source follower clock output signal, this just for test clock frequency only.
ALC	Auto level capacitor. It can be connected with VTH pin by 10~20K Resistor to Auto leveling Threshold voltage for slope detector.

Application example circuit (SOP-16)



Application example circuit (SOP-16)

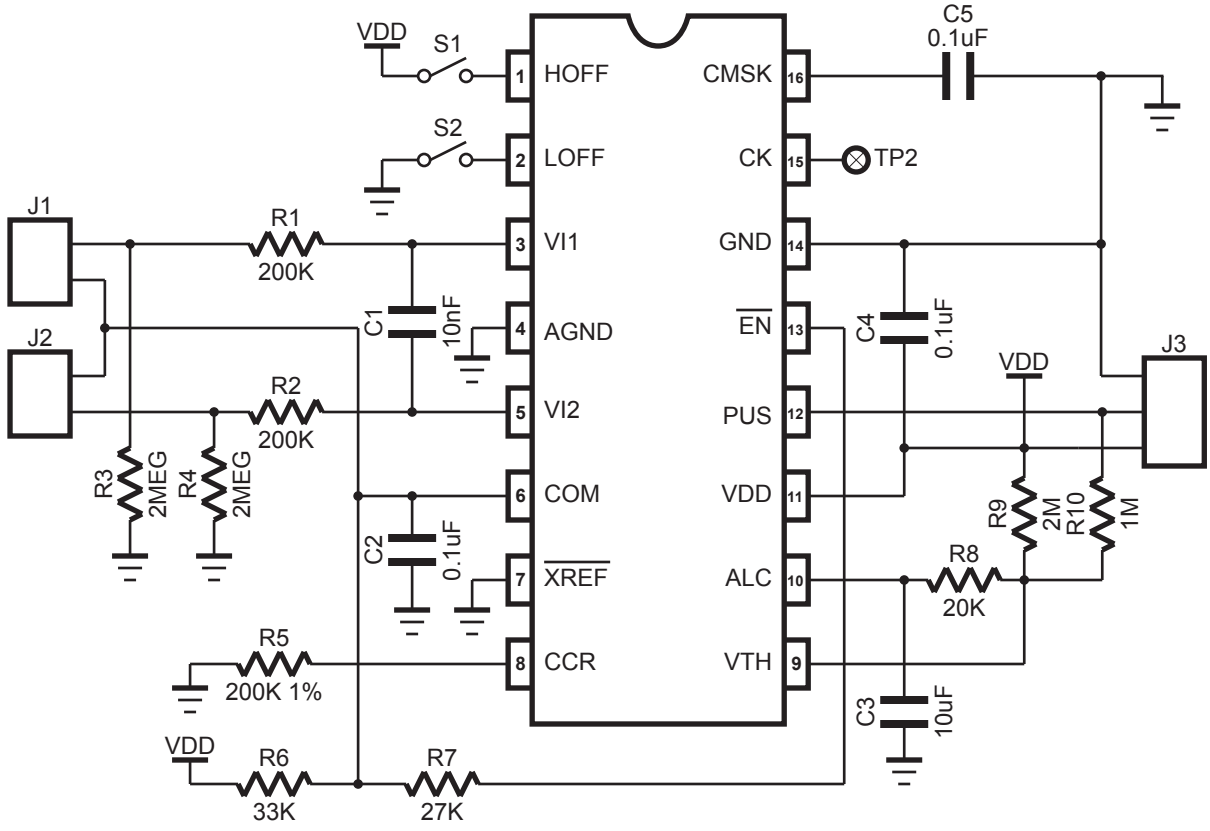
** High precision clock frequency adject for highly 50/60Hz rejection **



*** CK output could be driving 50Ω loadding
*** Adject VR1 for CK output frequency at 2136.283Hz(reject 50Hz) or 2563.54Hz(reject 60Hz)
*** Attenuation ratio could be more then 80dB when correct the clock frequency

Application example circuit (SOP-16)

** Power saving control **



*** Build-in Internal pull-low (0.2uA) on HOFF pin
*** Build-in Internal pull-high(0.2uA) on LOFF pin
*** HOFF logical high level must be greater then 1/5VDD
*** LOFF logical low level must be smaller the 1/5VDD
*** Both VI1 & VI2 must be greater then 0.15*V_{COM} for indicate hand holded

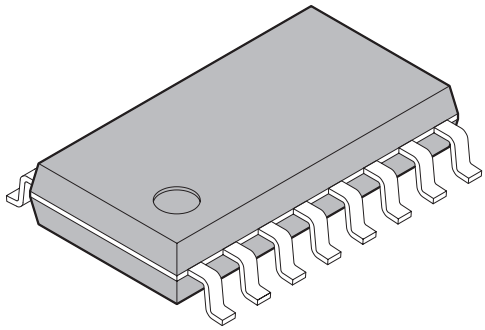
Power Mode Truth Table

HOFF	LOFF	Power
0	0	OFF
1	1	OFF
1	0	Always ON
0	1	Depend on Holding or not

Packaging Information

16-Lead Plastic Small Outline Gull Wing Package Types (SOP16)

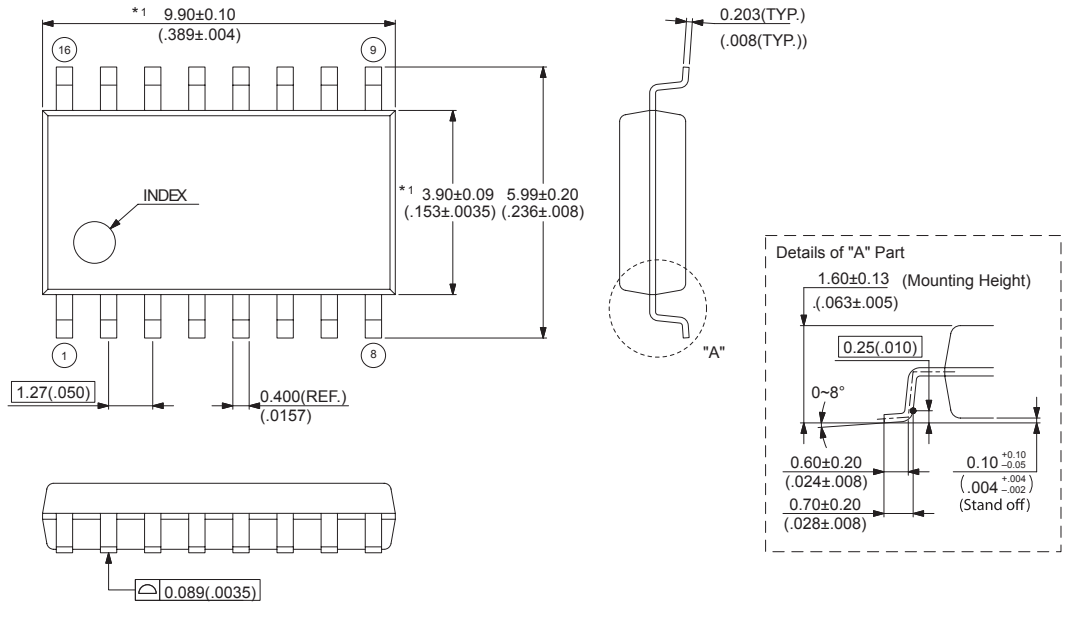
16-pin plastic SOP



Lead Pitch	1.27 mm
Package Dimensions Width x Length	3.90 x 9.90 mm
Lead Shape	Gull Wing
Sealing Method	Plastic Mold
Mounting Height	1.73 mm MAX
Weight	0.155 g
Code (Reference)	

16-Pin Plastic SOP

Note 1) *1 These dimensions do not include mold protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note:The values in parentheses are reference values.

Ordering Information