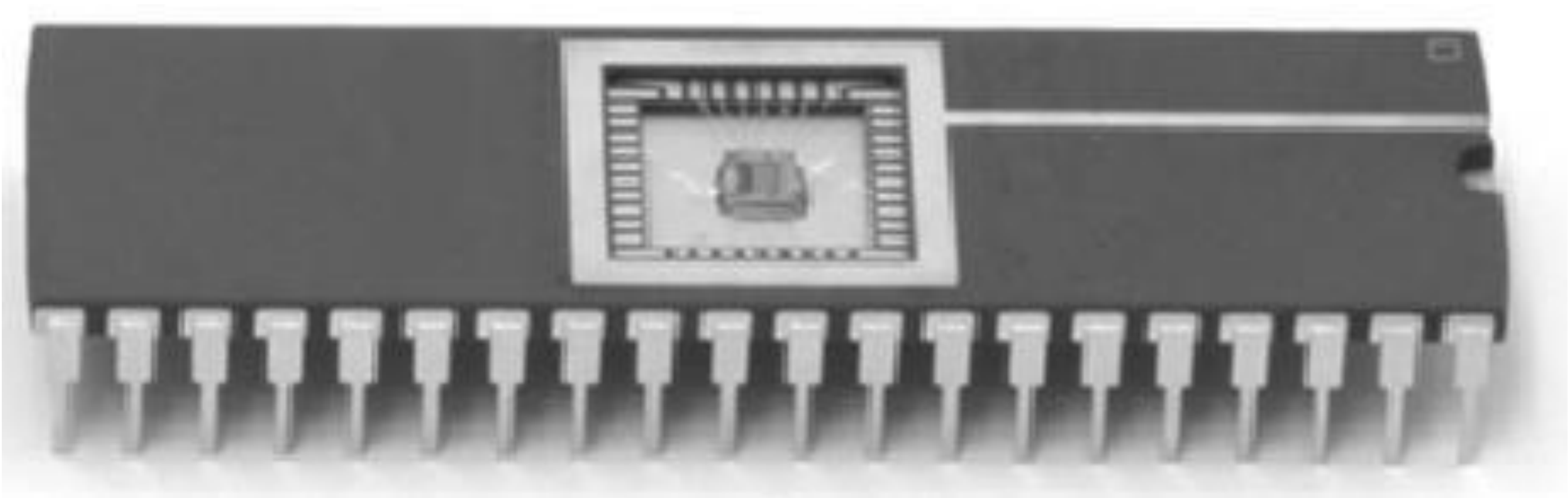
TECNOLOGÍA

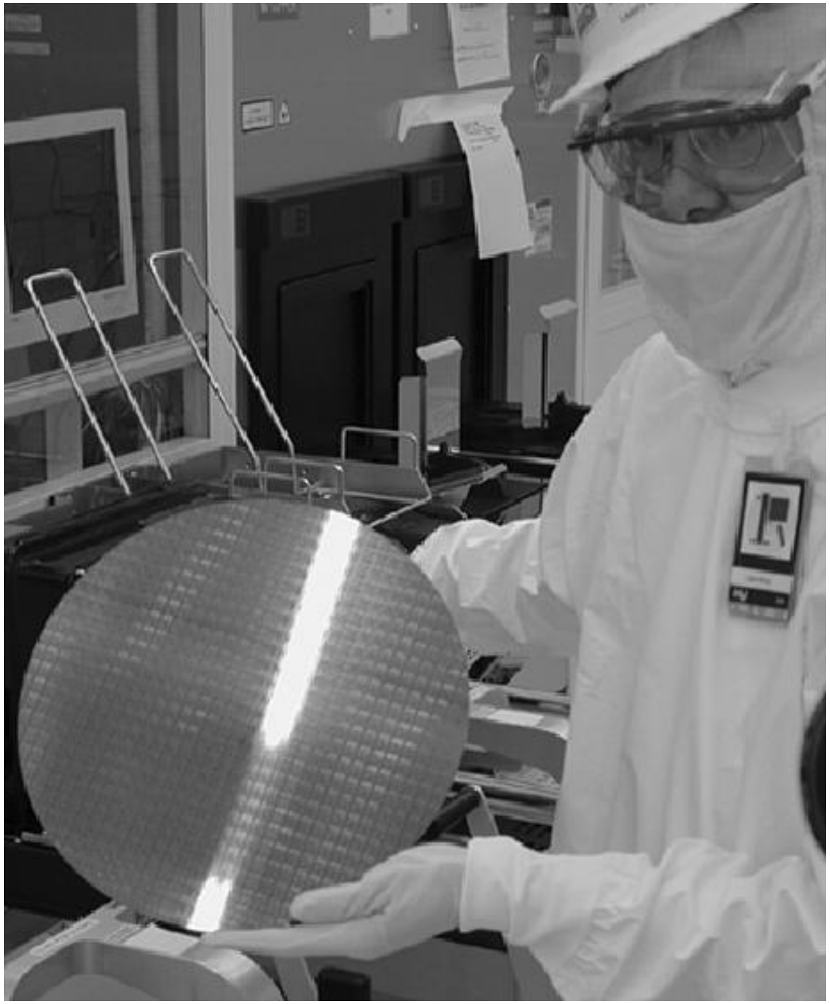
Técnicas Digitales I

Luis Eduardo Toledo

CIRCUITO INTEGRADO



OBLEA DE SILICIO



Logic Levels

- Discrete voltages represent 1 and 0
- For example:
  - 0 = *ground* (GND) or 0 volts
  - 1 = V_{DD} or 5 volts
- What about 4.99 volts? Is that a 0 or a 1?
- What about 3.2 volts?

FROM ZERO TO ONE

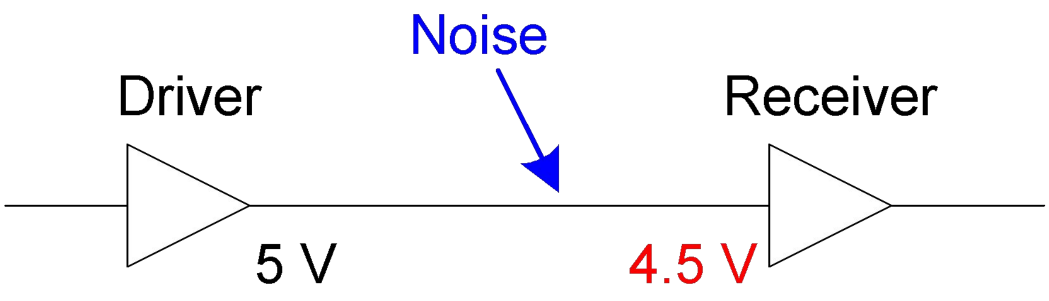
Logic Levels

- *Range* of voltages for 1 and 0
- Different ranges for inputs and outputs to allow for *noise*

What is Noise?

What is Noise?

- **Anything that degrades the signal**
  - E.g., resistance, power supply noise, coupling to neighboring wires, etc.
- **Example:** a gate (driver) outputs 5 V but, because of resistance in a long wire, receiver gets 4.5 V

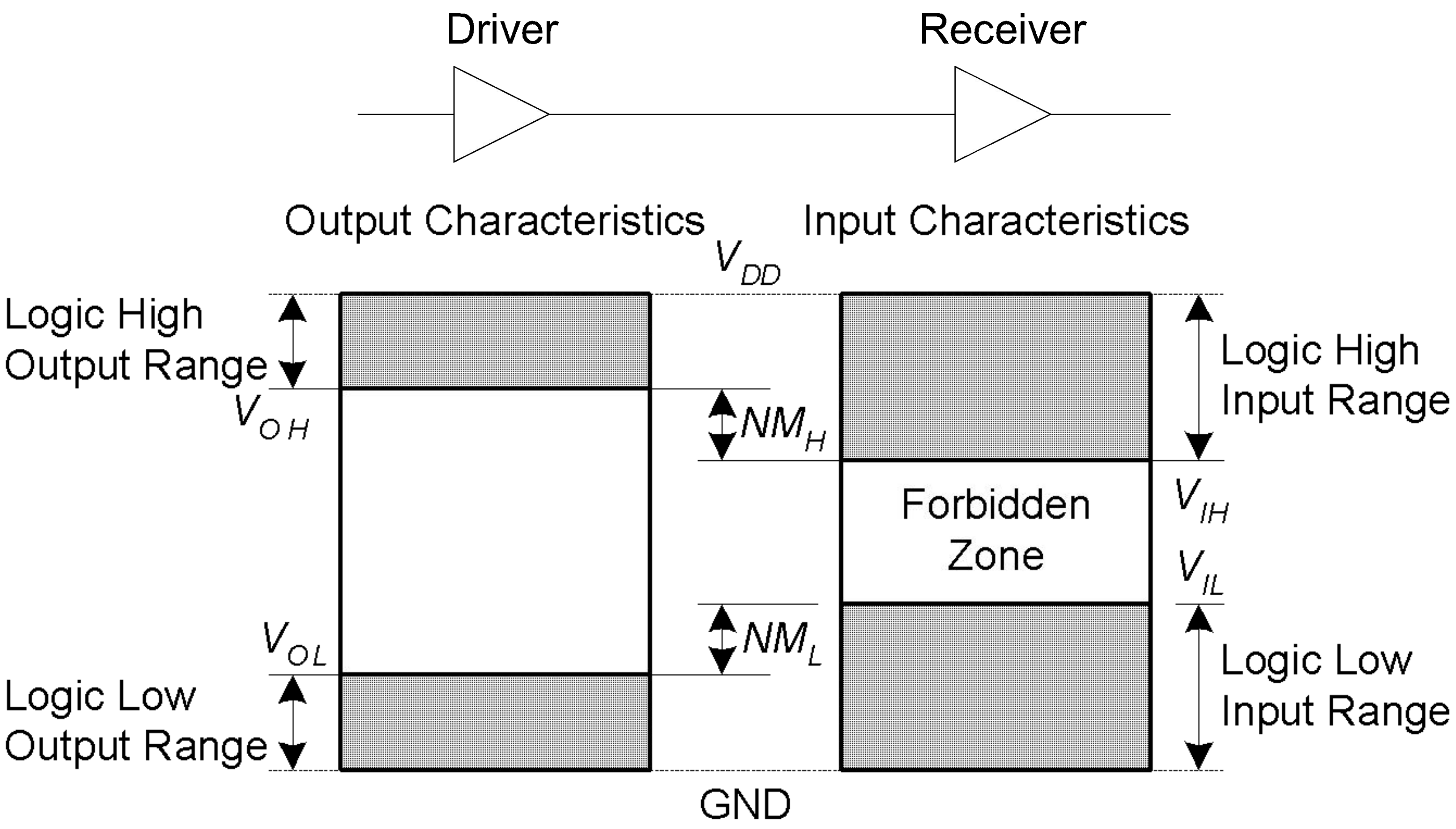


The Static Discipline

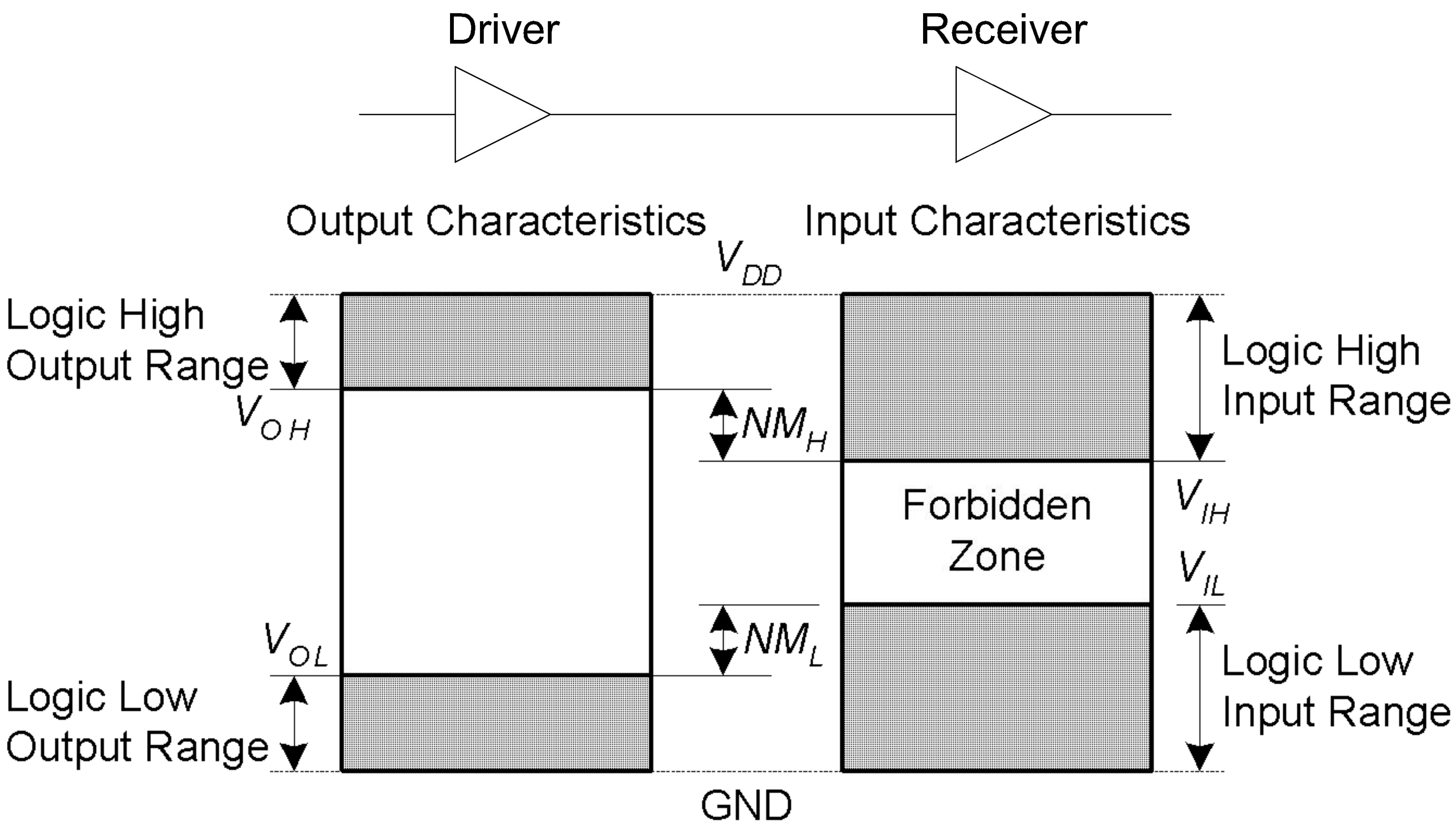
- With logically valid inputs, every circuit element must produce logically valid outputs

- Use limited ranges of voltages to represent discrete values

Logic Levels



Noise Margins

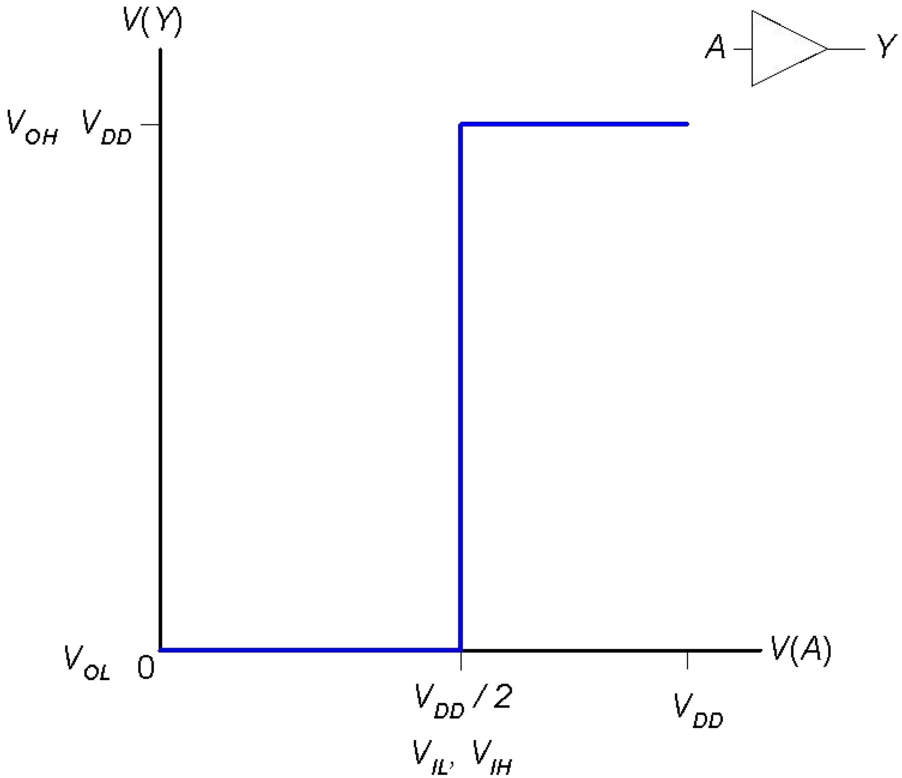


$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

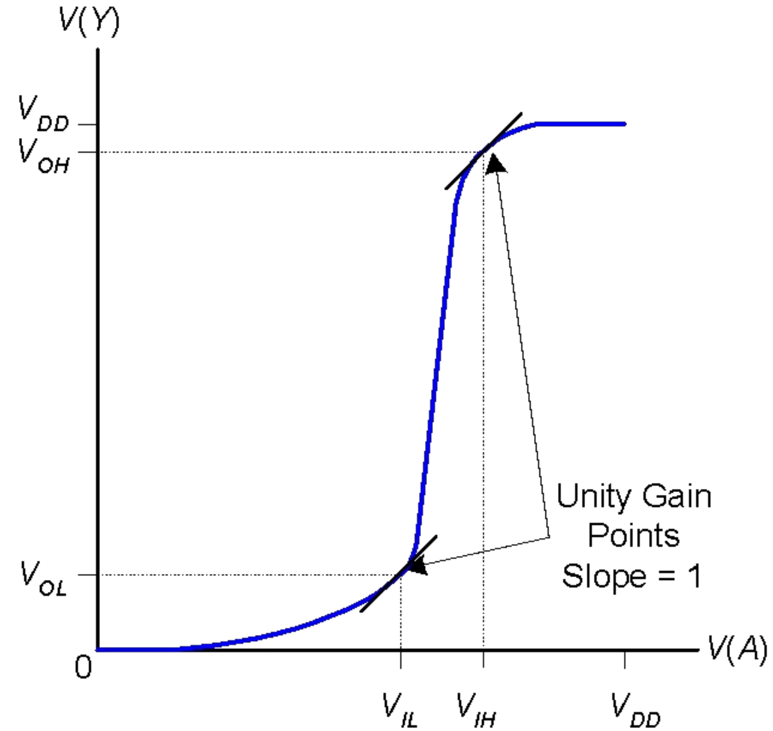
DC Transfer Characteristics

Ideal Buffer:



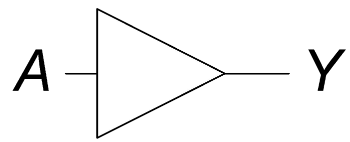
$NM_H = NM_L = V_{DD}/2$

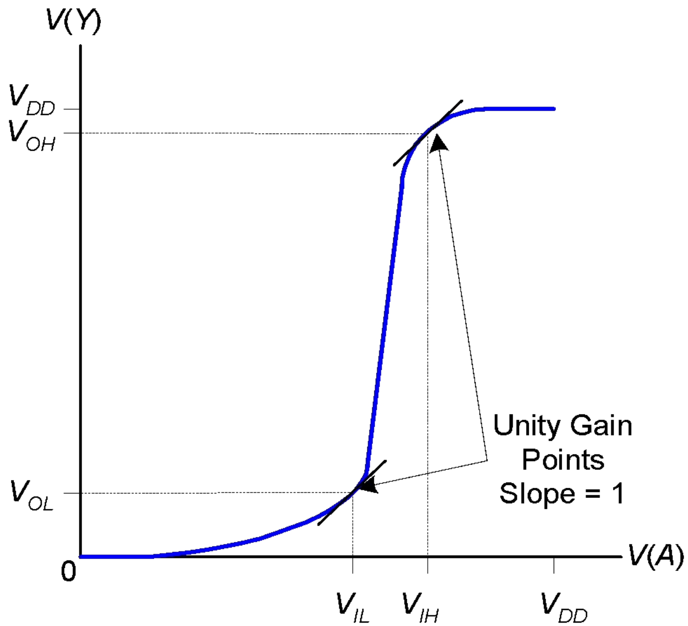
Real Buffer:

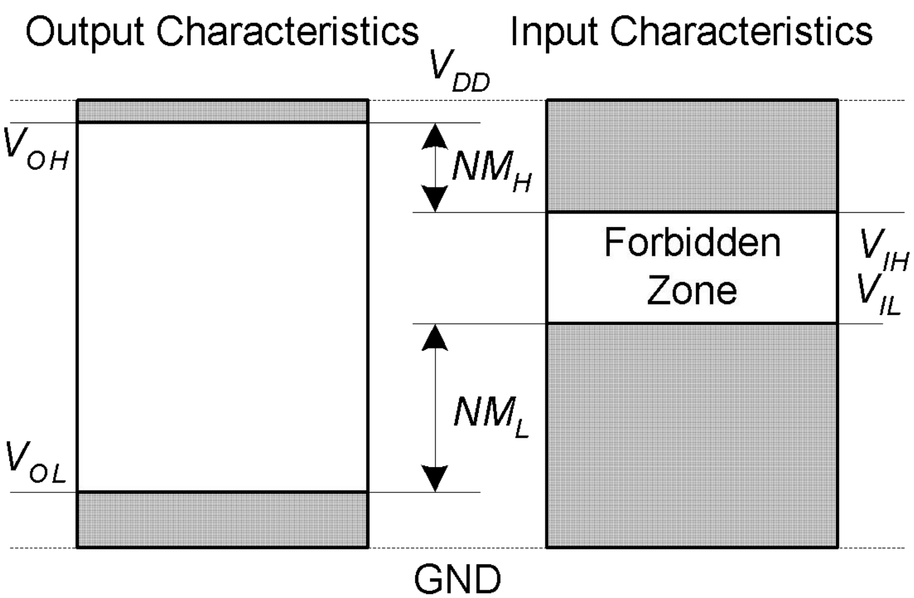


$NM_H, NM_L < V_{DD}/2$

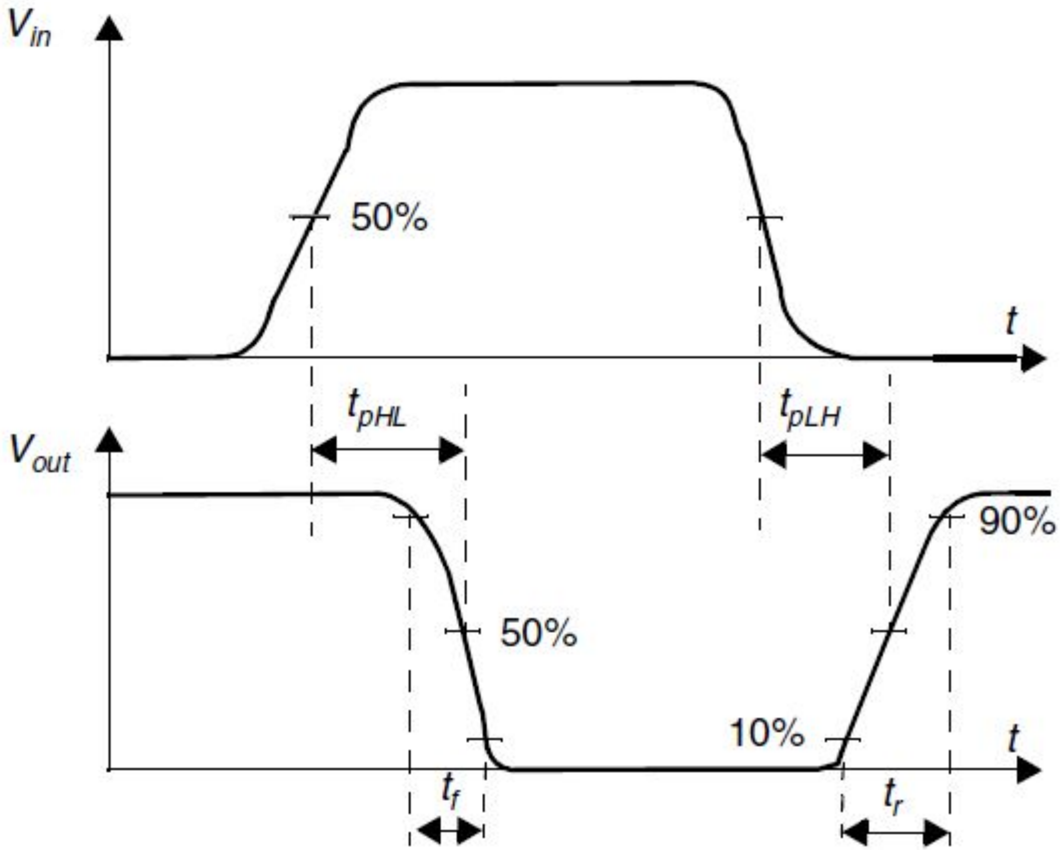
DC Transfer Characteristics







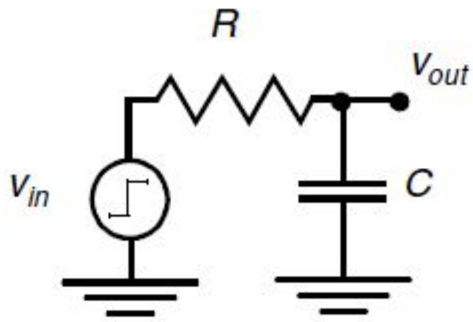
DEFINICIÓN DE RETARDO DE PROPAGACIÓN



$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

RETARDO DE PROPAGACIÓN DE UN CIRCUITO RC DE PRIMER ORDEN

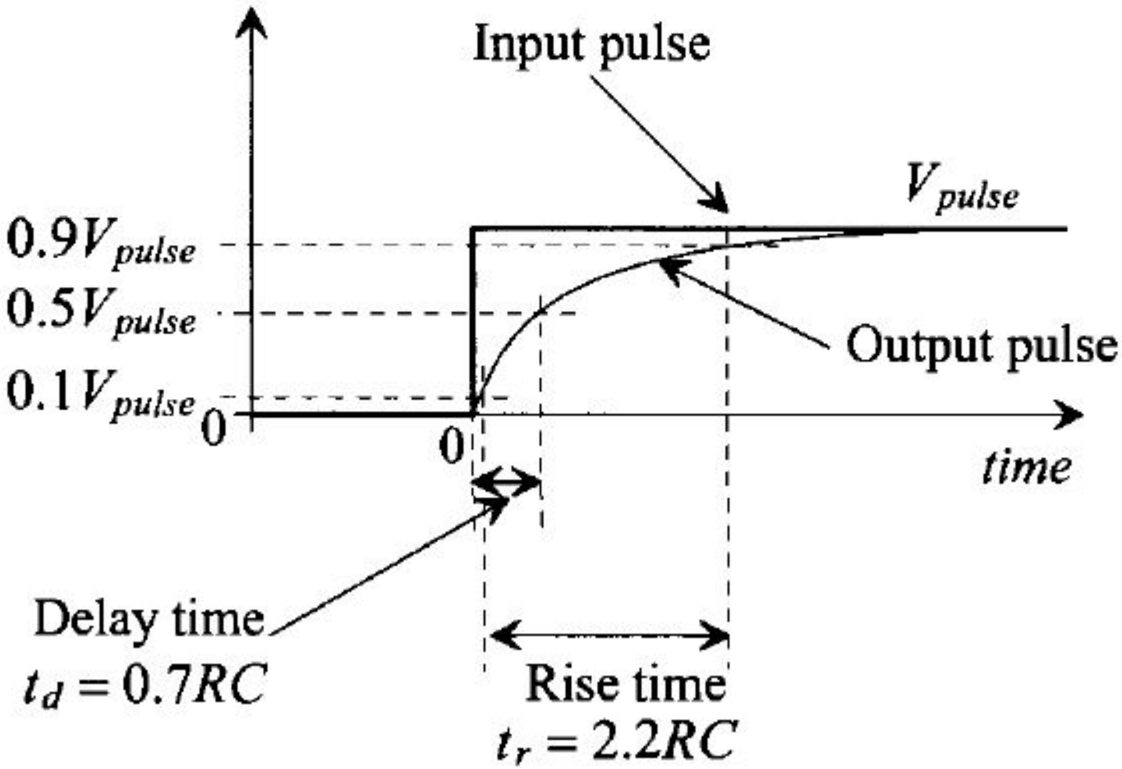
LOS CIRCUITOS DIGITALES SE PUEDEN MODELAR COMO SIMPLES CIRCUITOS RC



CUANDO SE APLICA UN ESCALON A ***Vin*** (DE ***0*** A ***V***), LA RESPUESTA TRANSITORIA ES:

$$v_{out}(t) = (1 - e^{-t/\tau})\, V \qquad \tau = RC$$

RETARDO DE PROPAGACIÓN DE UN CIRCUITO RC DE PRIMER ORDEN



$$\frac{V_{pulse}}{2} = V_{pulse}(1 - e^{-t_d/RC}) \rightarrow t_d \approx 0.7RC$$

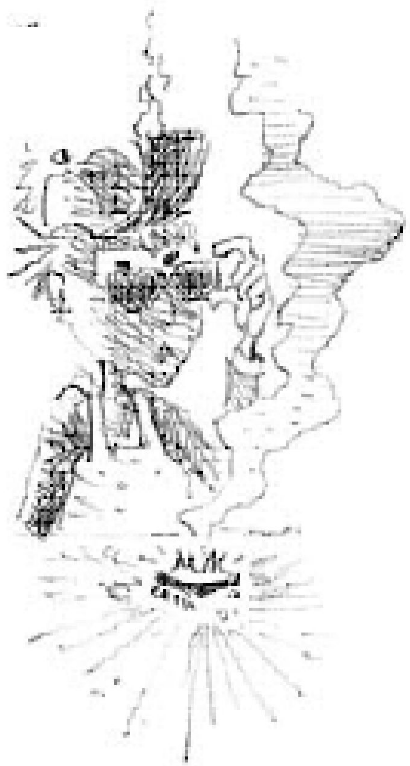
$$0.1V_{pulse} = V_{pulse}(1 - e^{-t_{10\%}/RC})$$

$$0.9V_{pulse} = V_{pulse}(1 - e^{-t_{90\%}/RC})$$

$$t_r = t_{90\%} - t_{10\%} \approx 2.2RC$$

V_{DD} Scaling

- In 1970's and 1980's, V_{DD} = 5 V
- V_{DD} has dropped
  - Avoid frying tiny transistors
  - Save power
- 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, …
- Be careful connecting chips with different supply voltages



Chips operate because they contain magic smoke

Proof:

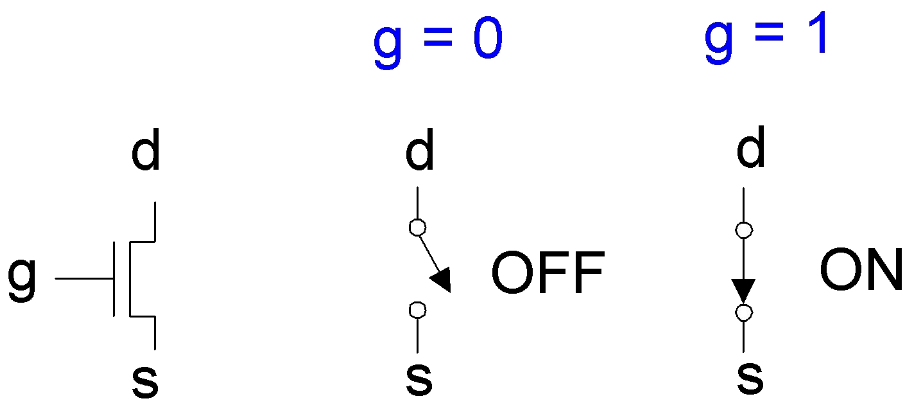
- if the magic smoke is let out, the chip stops working

Logic Family Examples

Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7

Transistors

- Logic gates built from transistors
- 3-ported voltage-controlled switch
  - 2 ports connected depending on voltage of 3rd
  - d and s are connected (ON) when g is 1



Robert Noyce, 1927-1990

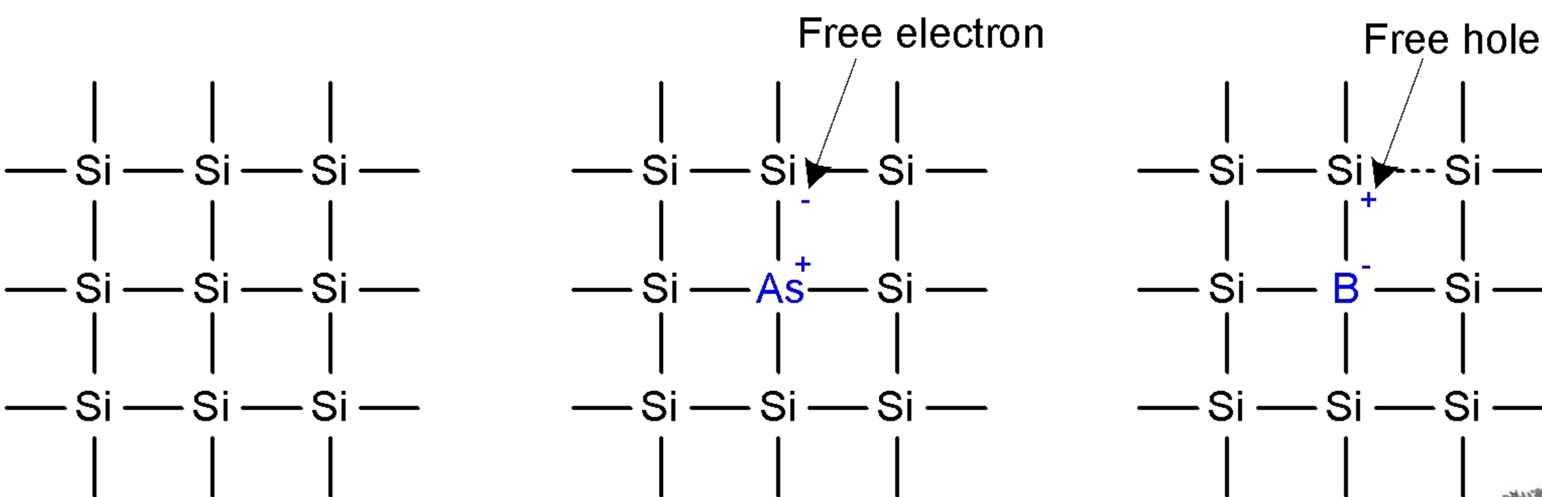
FROM ZERO TO ONE

- Nicknamed "Mayor of Silicon Valley"
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit

ELSEVIER

Silicon

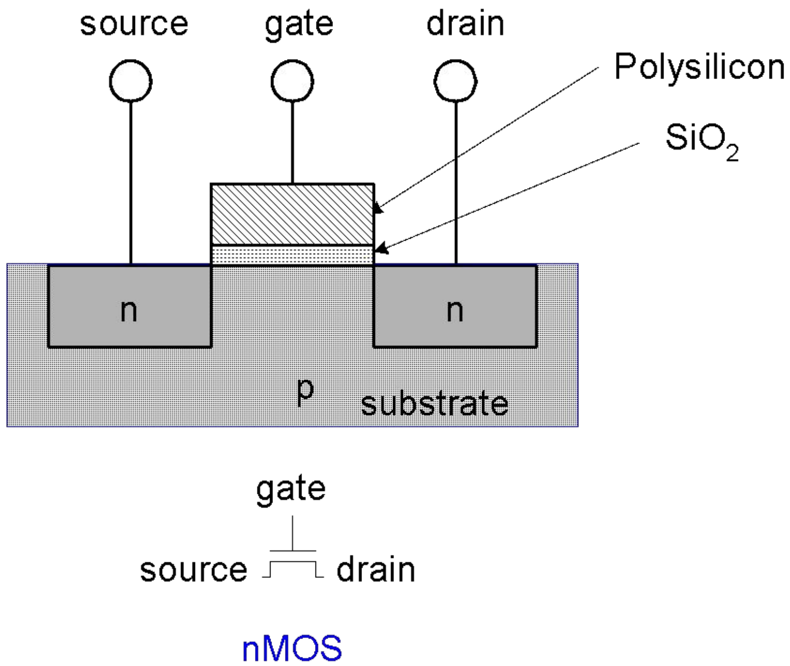
- Transistors built from silicon, a semiconductor
- Pure silicon is a poor conductor (no free charges)
- Doped silicon is a good conductor (free charges)
  - n-type (free *n*egative charges, electrons)
  - p-type (free *p*ositive charges, holes)



Silicon Lattice　　n-Type　　p-Type

MOS Transistors

- **Metal oxide silicon (MOS) transistors:**
  - Polysilicon (used to be **metal**) gate
  - **Oxide** (silicon dioxide) insulator
  - Doped **silicon**



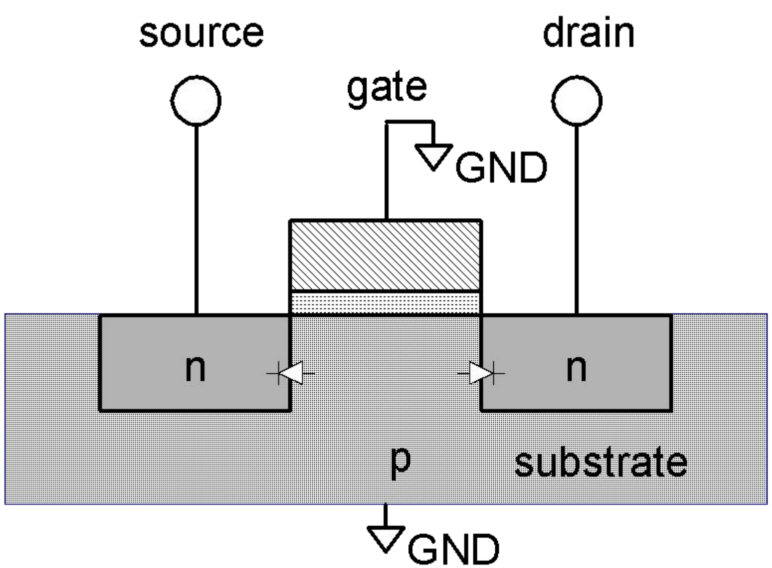
Transistors: nMOS

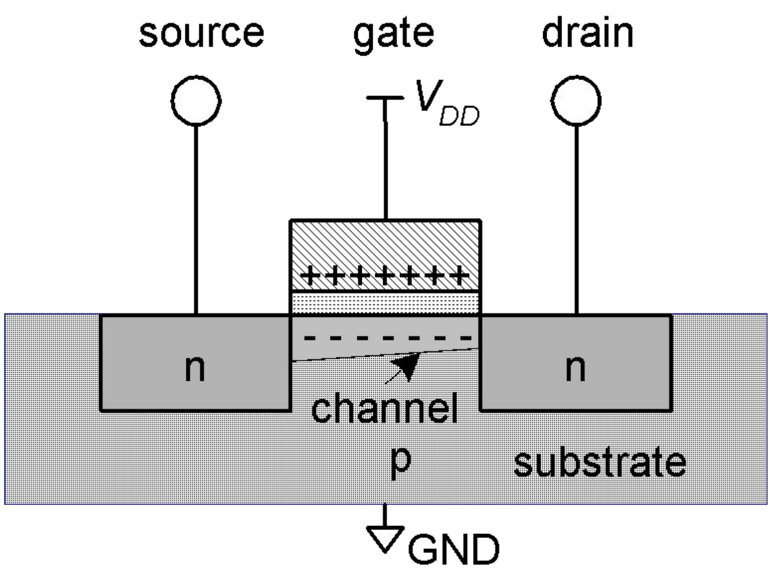
Gate = 0

OFF (no connection between source and drain)

Gate = 1

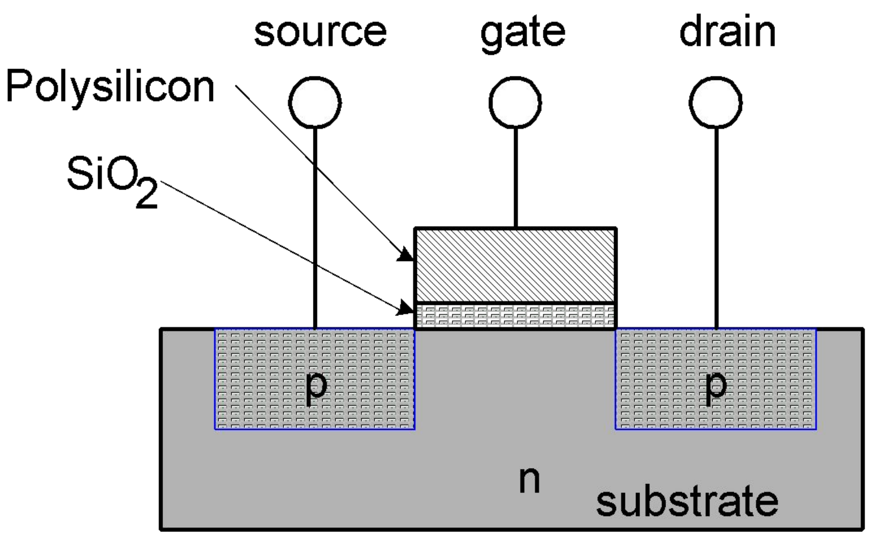
ON (channel between source and drain)

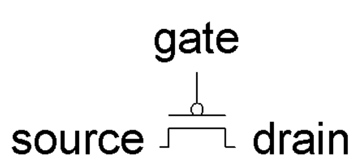




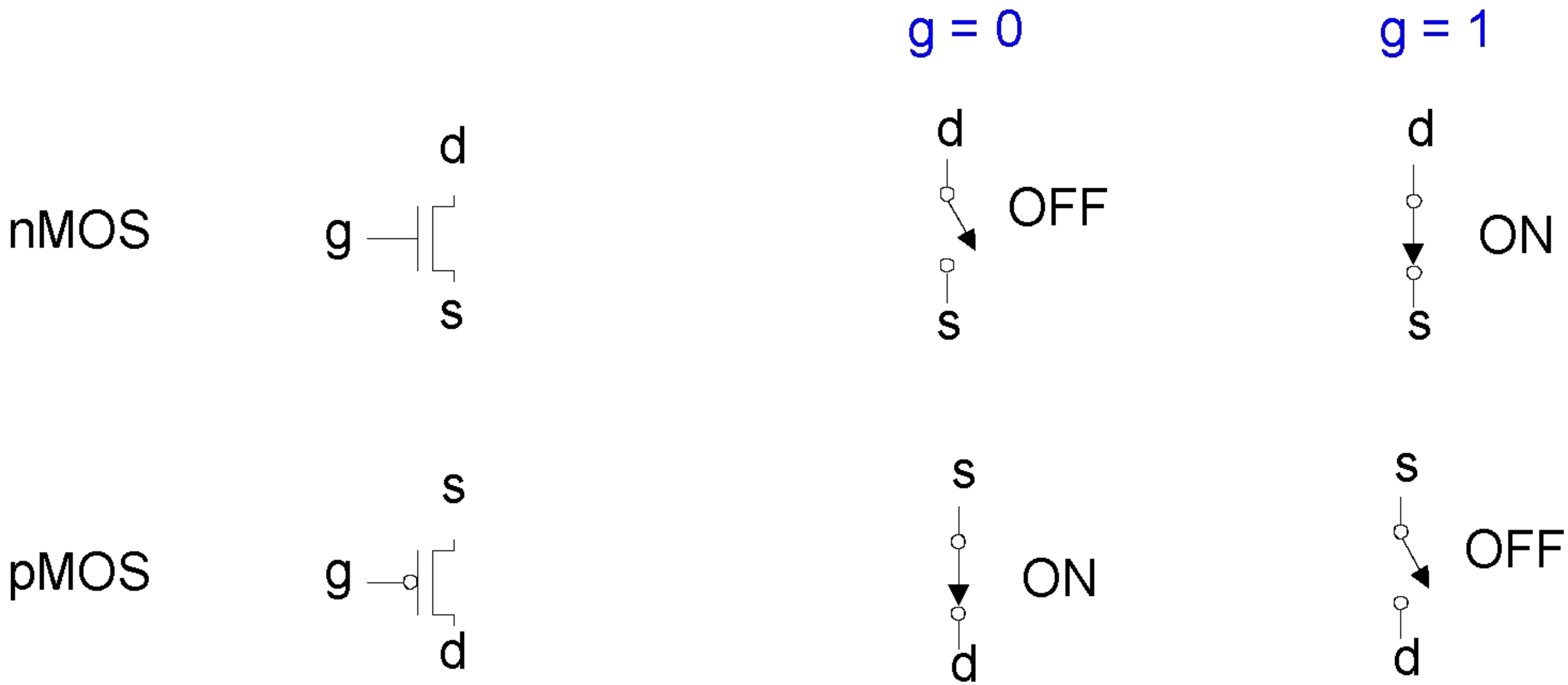
Transistors: pMOS

- pMOS transistor is opposite
  - ON when Gate = 0
  - OFF when Gate = 1



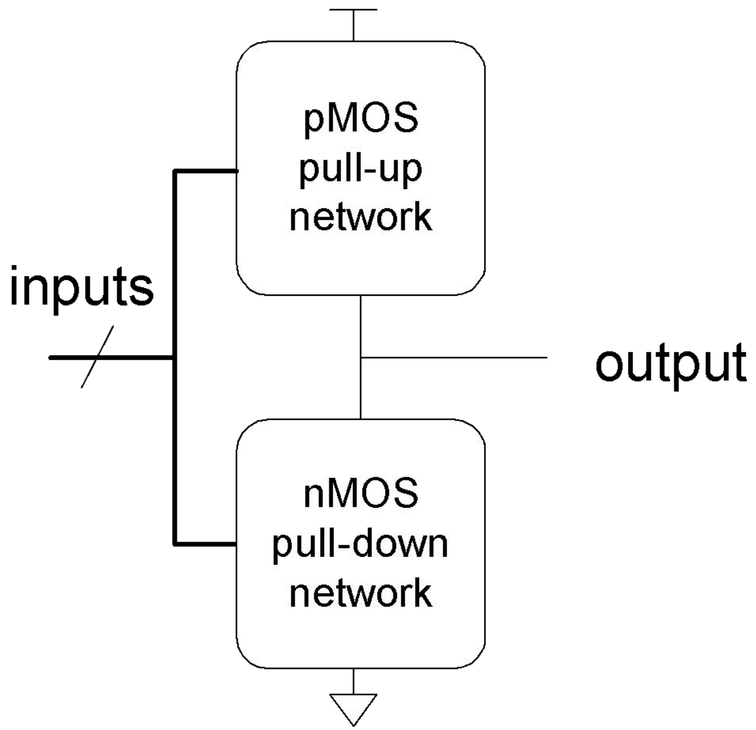


Transistor Function



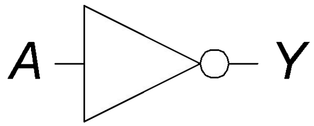
Transistor Function

- **nMOS:** pass good 0's, so connect source to GND
- **pMOS:** pass good 1's, so connect source to V_{DD}



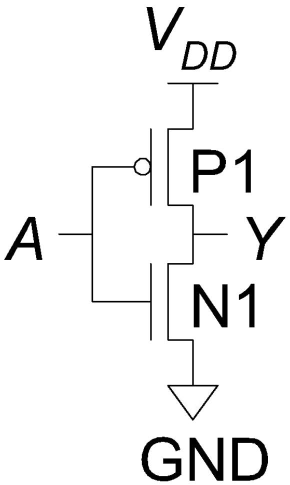
CMOS Gates: NOT Gate

NOT



$Y = \overline{A}$

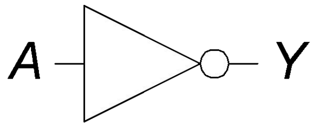
A	Y
0	1
1	0



A	P1	N1	Y
0			
1			

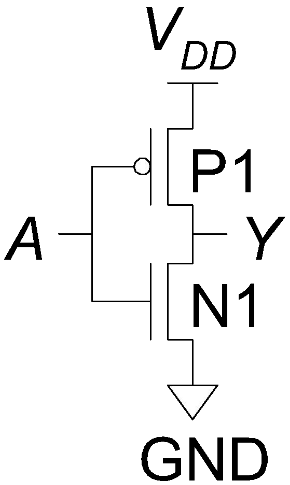
CMOS Gates: NOT Gate

NOT



$$Y = \overline{A}$$

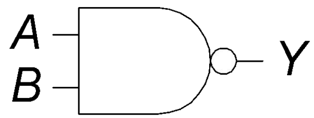
A	Y
0	1
1	0



A	P1	N1	Y
0	ON	OFF	1
1	OFF	ON	0

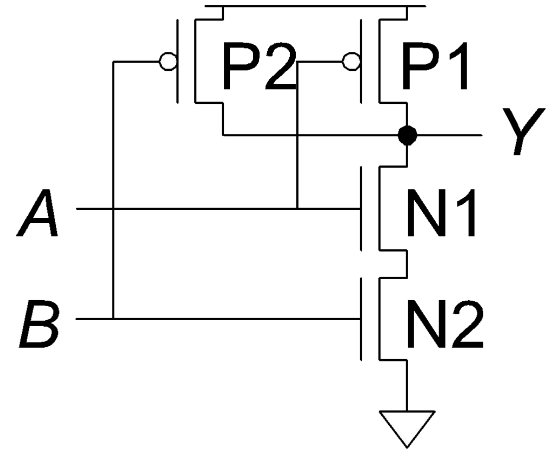
CMOS Gates: NAND Gate

NAND



$Y = \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

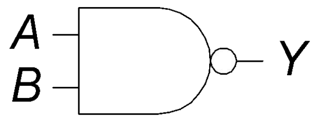


A	*B*	P1	P2	N1	N2	*Y*
0	0					
0	1					
1	0					
1	1					

FROM ZERO TO ONE

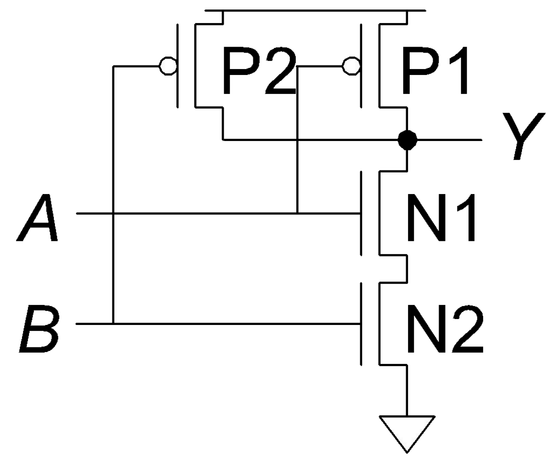
CMOS Gates: NAND Gate

NAND



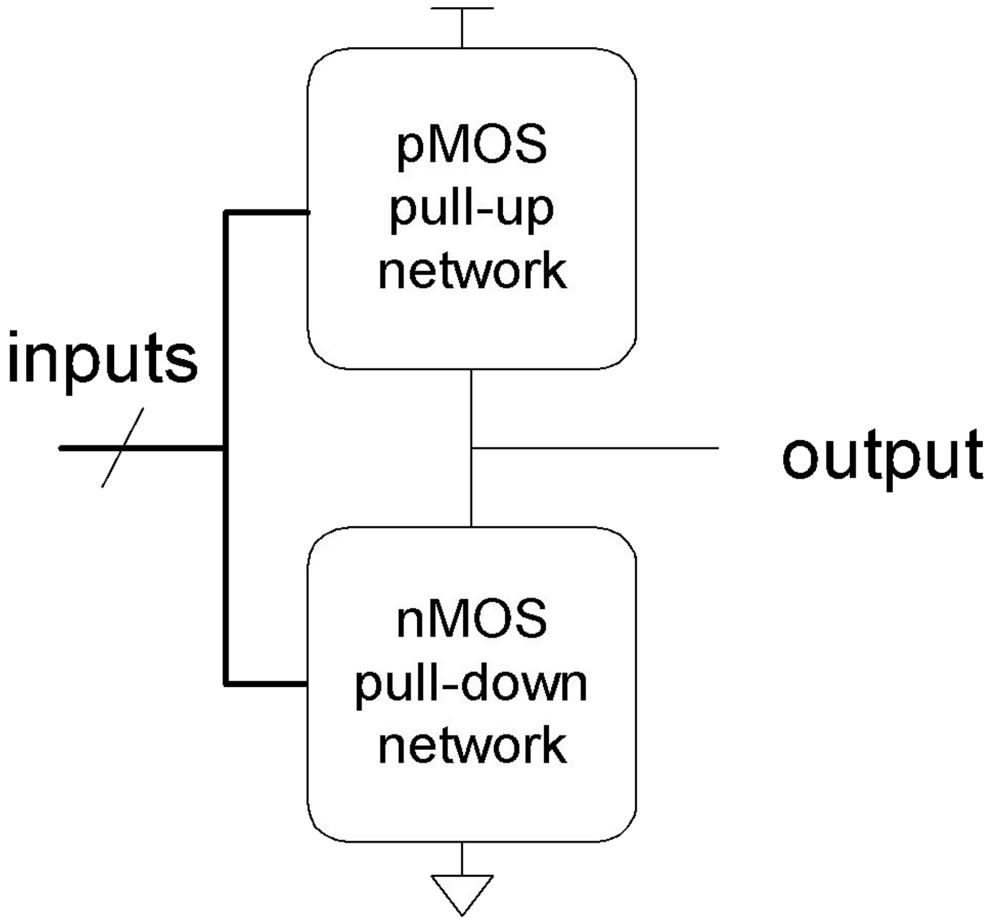
$Y = \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



A	*B*	P1	P2	N1	N2	*Y*
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

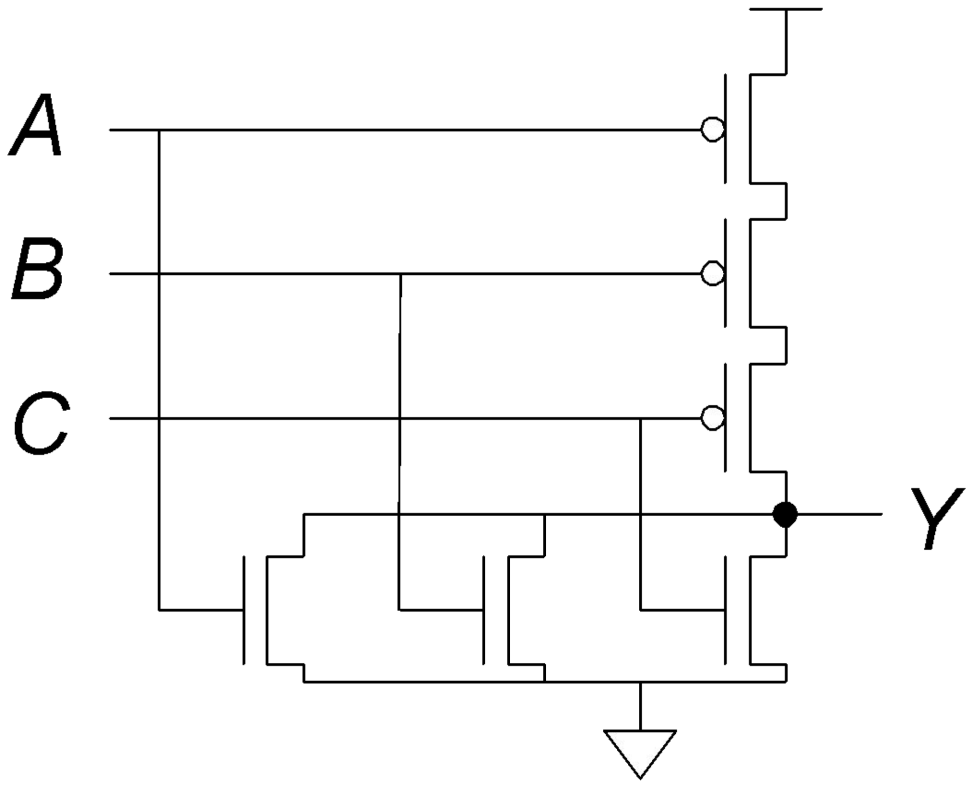
CMOS Gate Structure



NOR Gate

How do you build a three-input NOR gate?

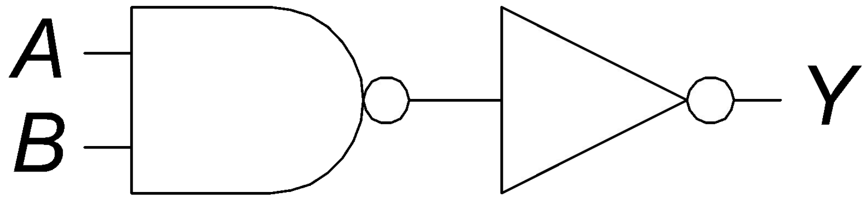
NOR3 Gate



Other CMOS Gates

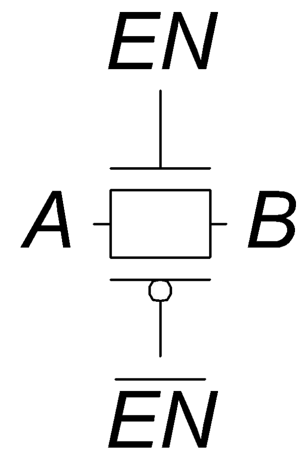
How do you build a two-input AND gate?

AND2 Gate



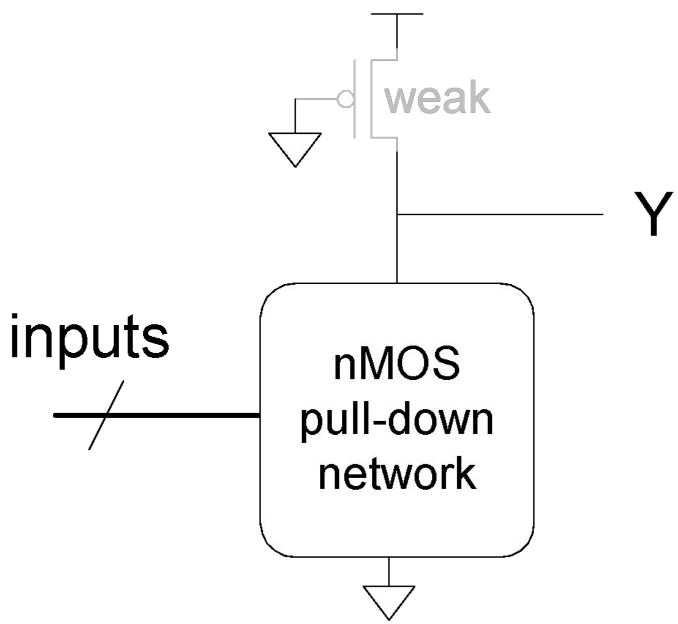
Transmission Gates

- nMOS pass 1’s poorly
- pMOS pass 0’s poorly
- Transmission gate is a better switch
  - passes both 0 and 1 well
- When *EN* = 1, the switch is ON:
  - *EN* = 0 and *A* is connected to *B*
- When *EN* = 0, the switch is OFF:
  - *A* is not connected to *B*



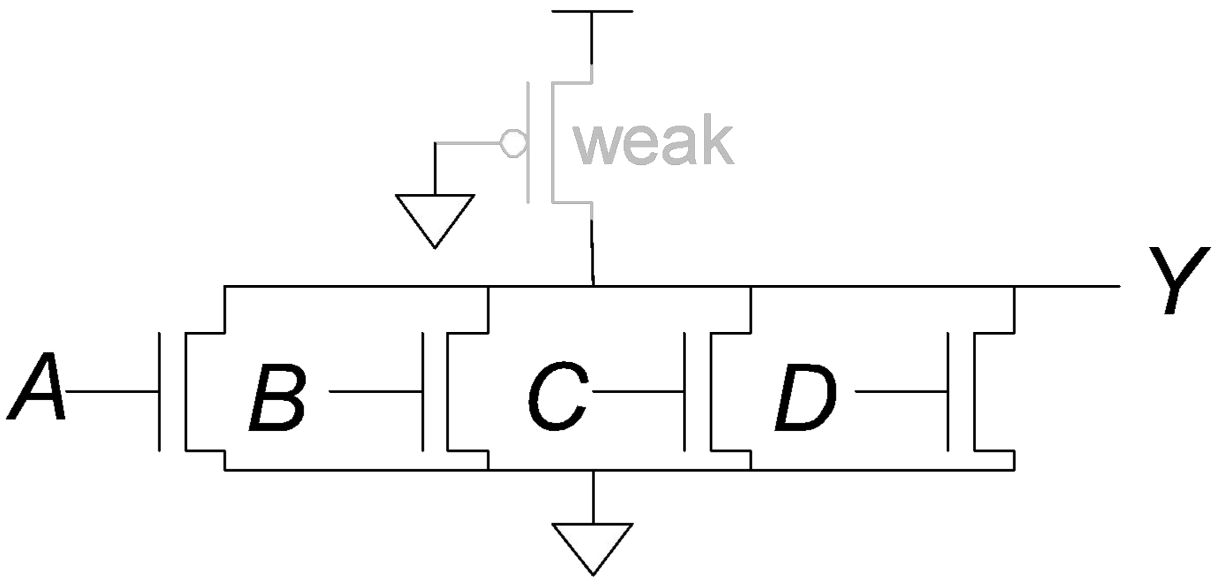
Pseudo-nMOS Gates

- Replace pull-up network with *weak* pMOS transistor that is always on
- pMOS transistor: pulls output HIGH *only* when nMOS network not pulling it LOW



Pseudo-nMOS Example

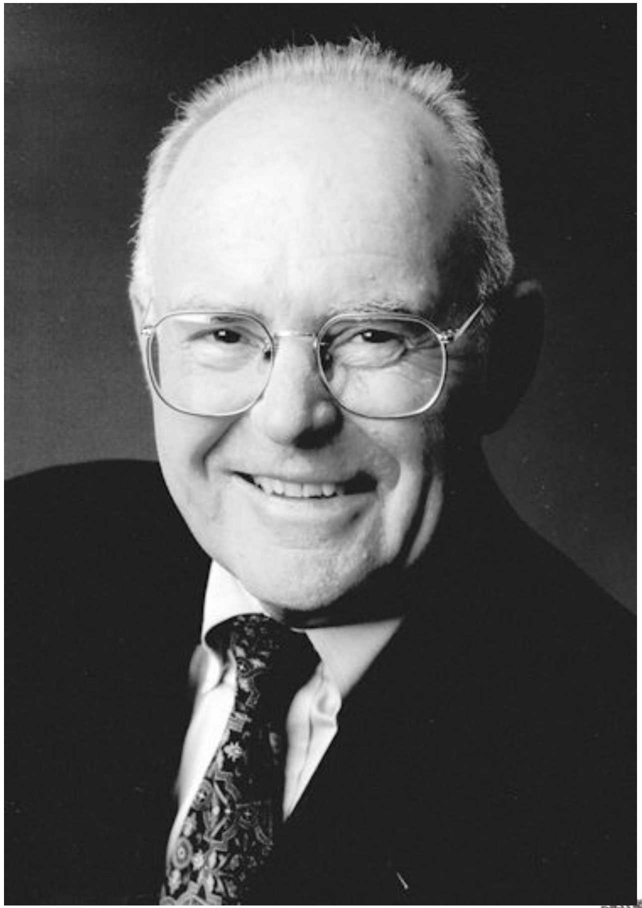
Pseudo-nMOS **NOR4**



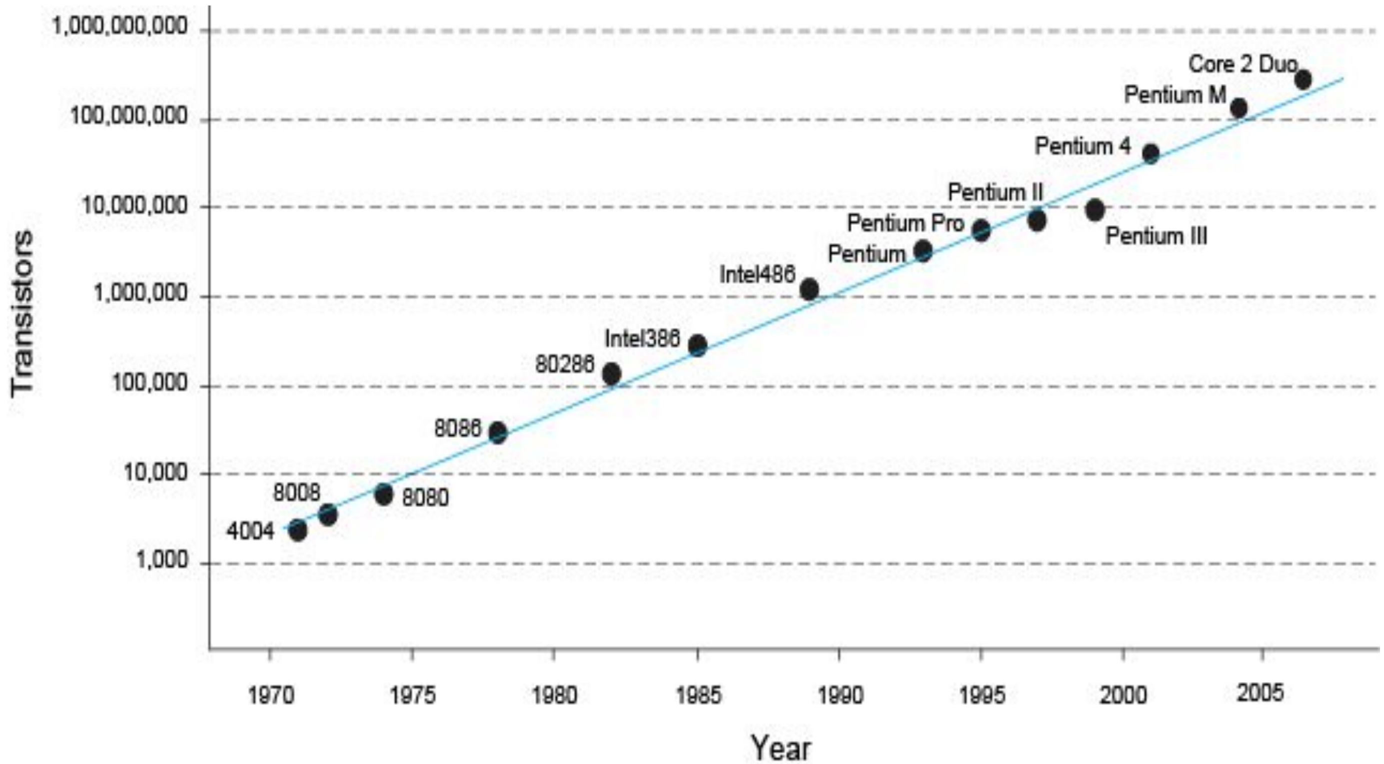
Gordon Moore, 1929-

FROM ZERO TO ONE

- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** number of transistors on a computer chip doubles every year (observed in 1965)
- Since 1975, transistor counts have doubled every two years.



Moore's Law



- *"If the automobile had followed the same development cycle as the computer, a Rolls-Royce would today cost $100, get one million miles to the gallon, and explode once a year . . ."*

  – Robert Cringley

Power Consumption

- Power = Energy consumed per unit time
  - Dynamic power consumption
  - Static power consumption

Dynamic Power Consumption

- **Power to charge transistor gate capacitances**
  - Energy required to charge a capacitance, C, to V_{DD} is CV_{DD}^2
  - Circuit running at frequency f: transistors switch (from 1 to 0 or vice versa) at that frequency
  - Capacitor is charged $f/2$ times per second (discharging from 1 to 0 is free)
- Dynamic power consumption:

$$\boxed{P_{dynamic} = \tfrac{1}{2} C V_{DD}^2 f}$$

FROM ZERO TO ONE

ELSEVIER

Static Power Consumption

- Power consumed when no gates are switching
- Caused by the *quiescent supply current*, I_{DD} (also called the *leakage current*)
- Static power consumption:

$$\boxed{P_{static} = I_{DD}V_{DD}}$$

Power Consumption Example

- Estimate the power consumption of a wireless handheld computer
  - $V_{DD} = 1.2$ V
  - $C = 20$ nF
  - $f = 1$ GHz
  - $I_{DD} = 20$ mA

FROM ZERO TO ONE

Power Consumption Example

- Estimate the power consumption of a wireless handheld computer
  - $V_{DD} = 1.2$ V
  - $C = 20$ nF
  - $f = 1$ GHz
  - $I_{DD} = 20$ mA

$$P = \tfrac{1}{2} C V_{DD}^2 f + I_{DD} V_{DD}$$

$$= \tfrac{1}{2}(20\text{ nF})(1.2\text{ V})^2(1\text{ GHz}) + (20\text{ mA})(1.2\text{ V})$$

$$\mathbf{= (14.4 + 0.024)\ W \approx 14.4\ W}$$