DISPOSITIVOS PROGRAMABLES

Técnicas Digitales I

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UTN

CONFIGURACIONES BASICAS COMBINACIONALES

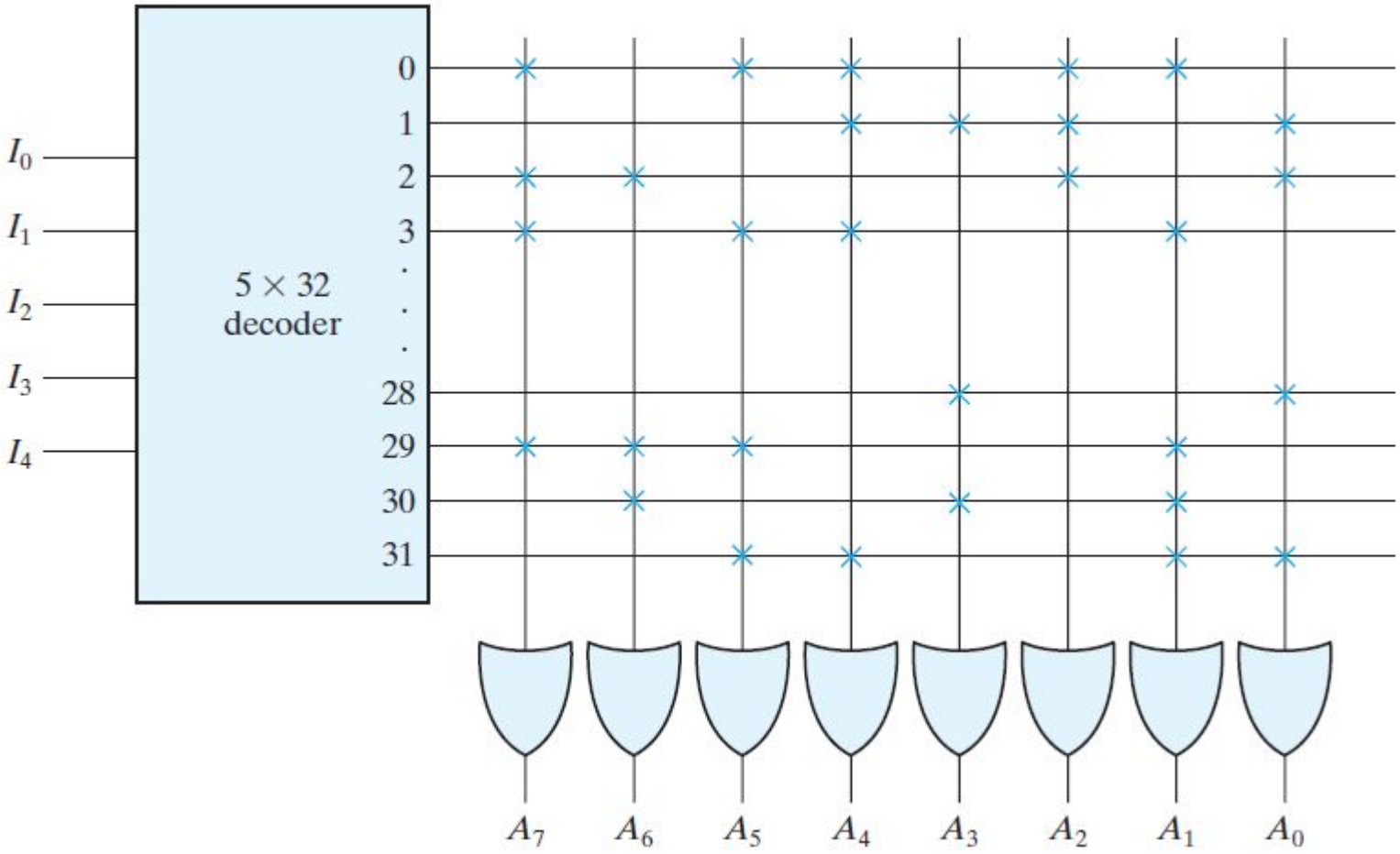
(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL)

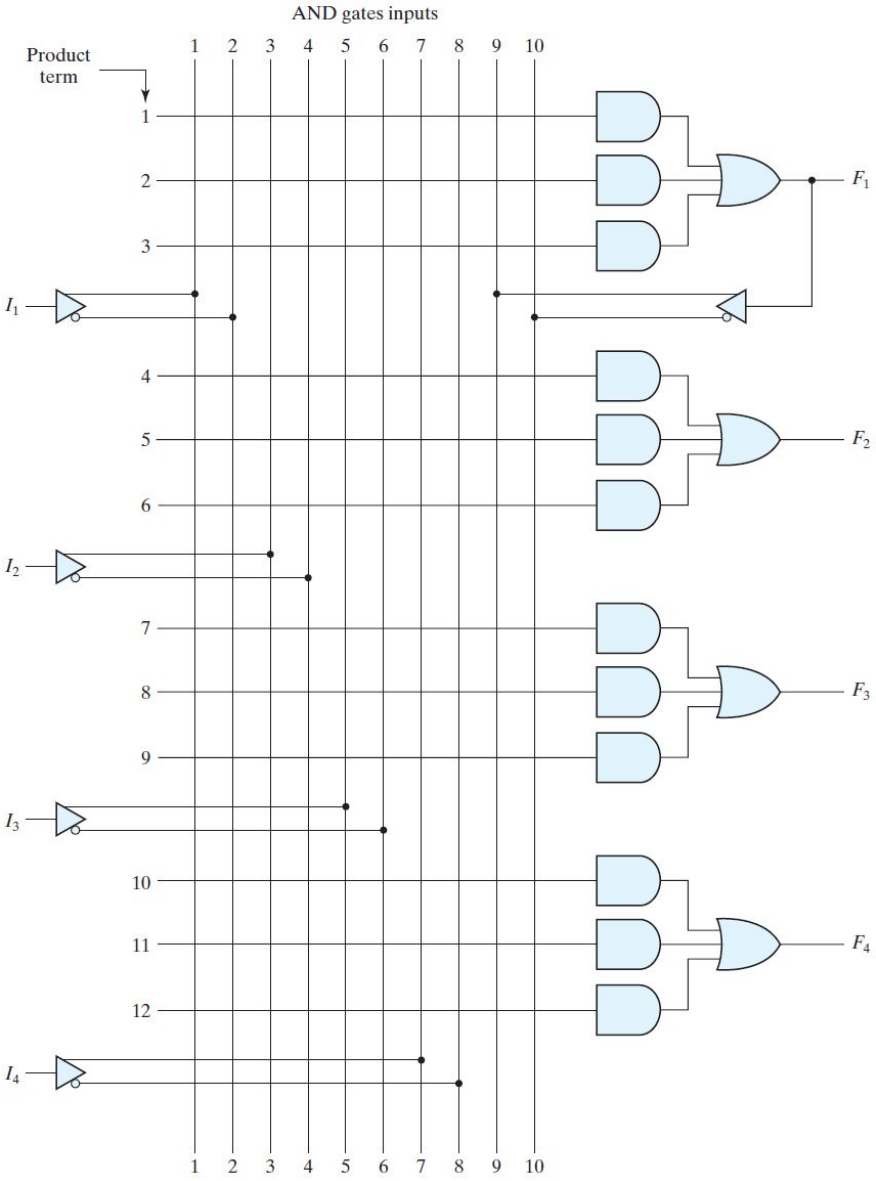
(c) Programmable logic array (PLA)

UTN

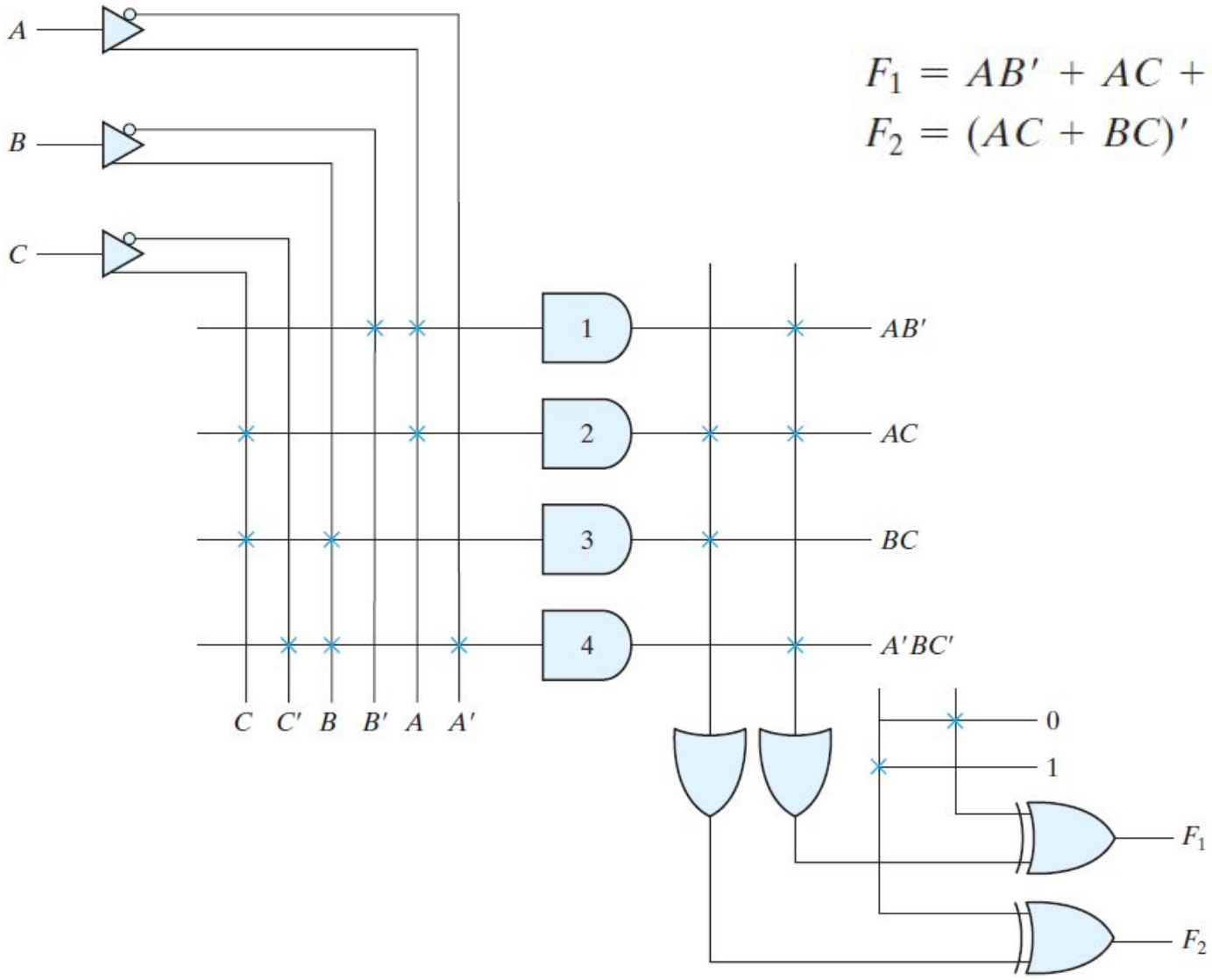
ROM



PAL

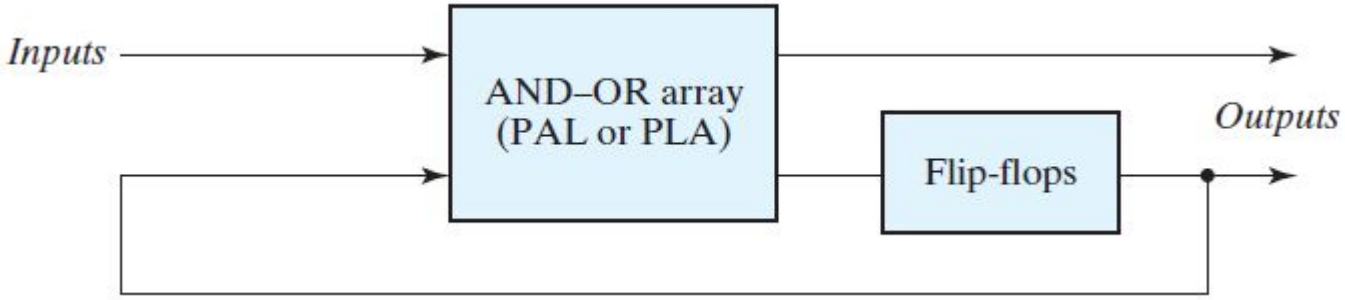

AND gates inputs
1 2 3 4 5 6 7 8 9 10
Product term
1
2
3
4
5
6
7
8
9
10
11
12
I_1
I_2
I_3
I_4
F_1
F_2
F_3
F_4
1 2 3 4 5 6 7 8 9 10

PLA



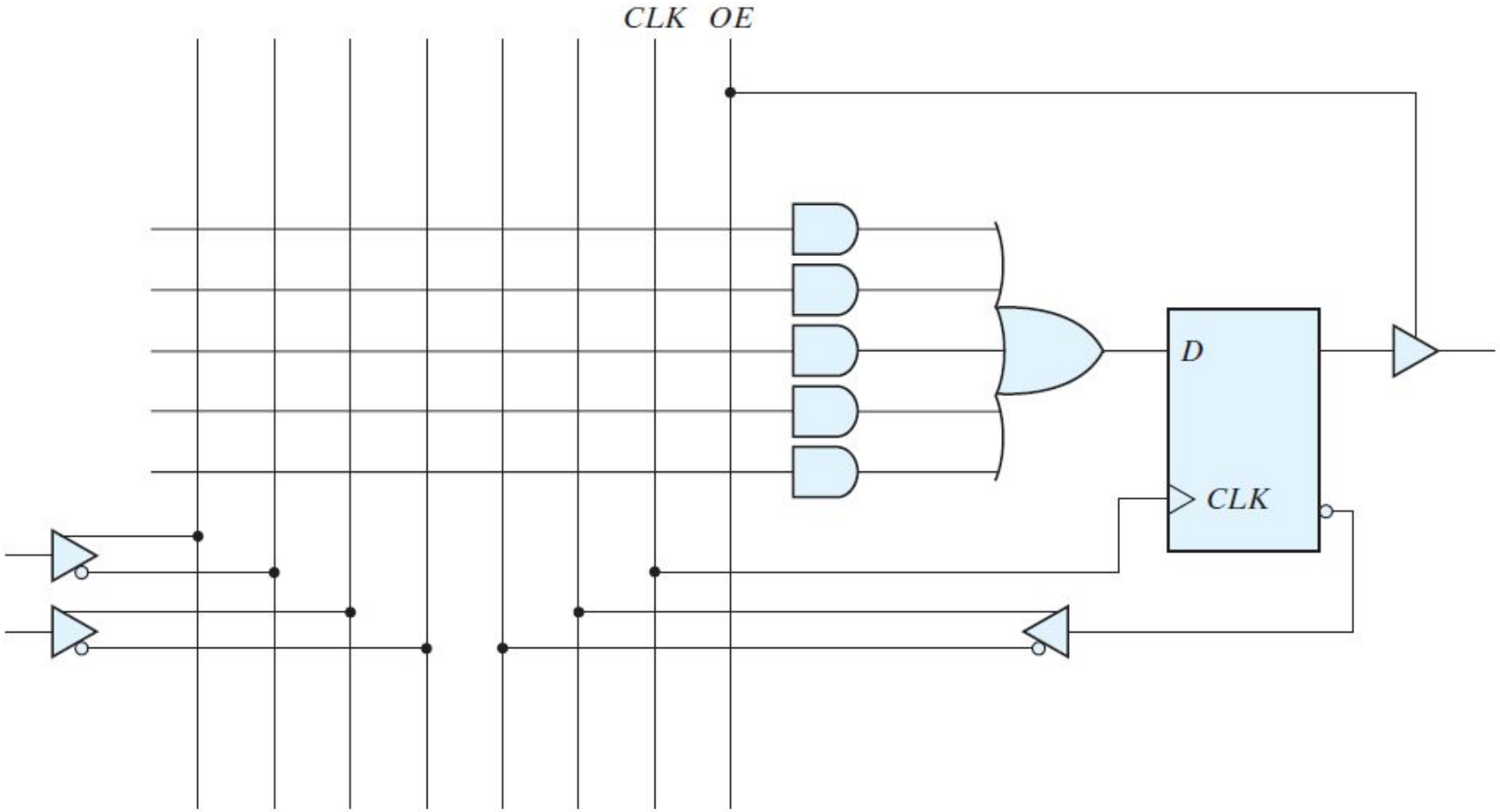
$$F_1 = AB' + AC + A'BC'$$
$$F_2 = (AC + BC)'$$

CONFIGURACIONES SECUENCIALES



1. Sequential (or simple) programmable logic device (SPLD)
2. Complex programmable logic device (CPLD)
3. Field-programmable gate array (FPGA)

SPLD
SIMPLE PROGRAMMABLE LOGIC DEVICE



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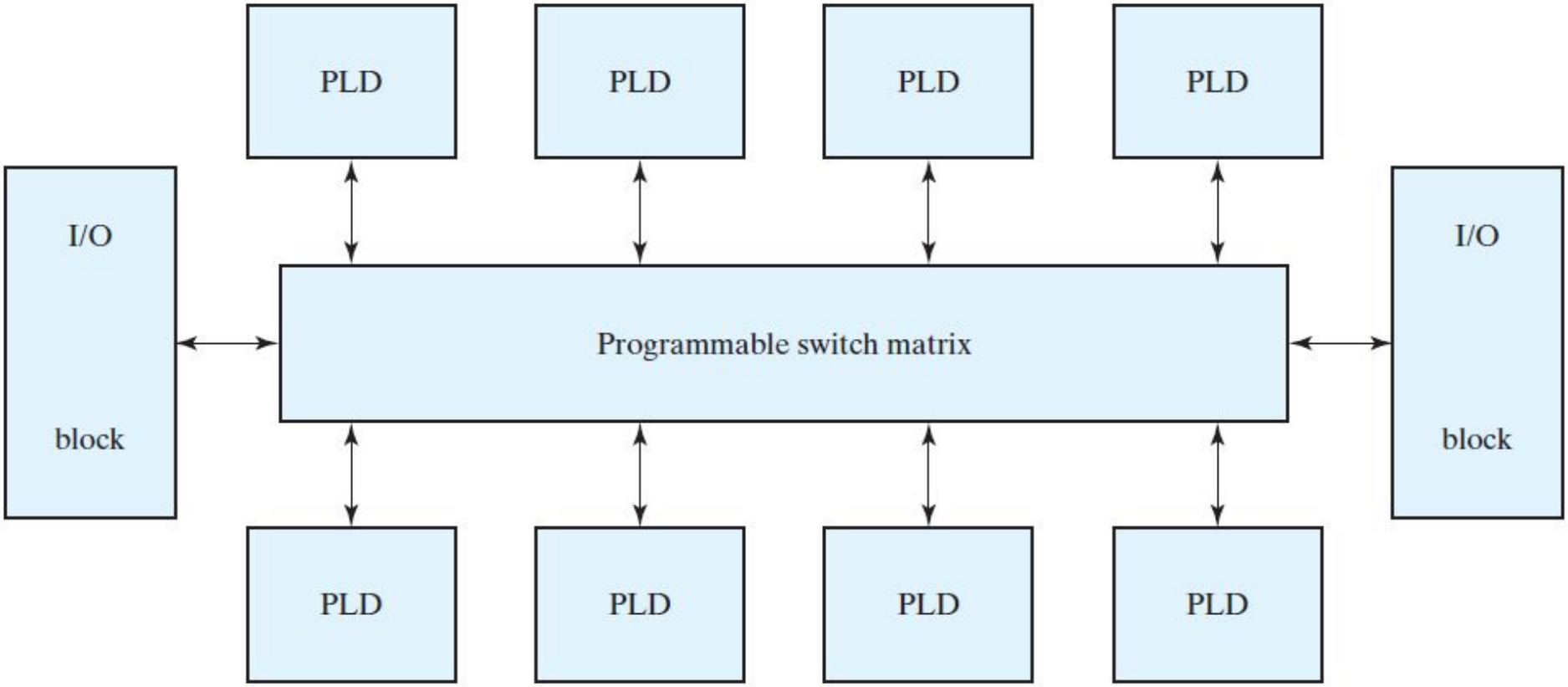
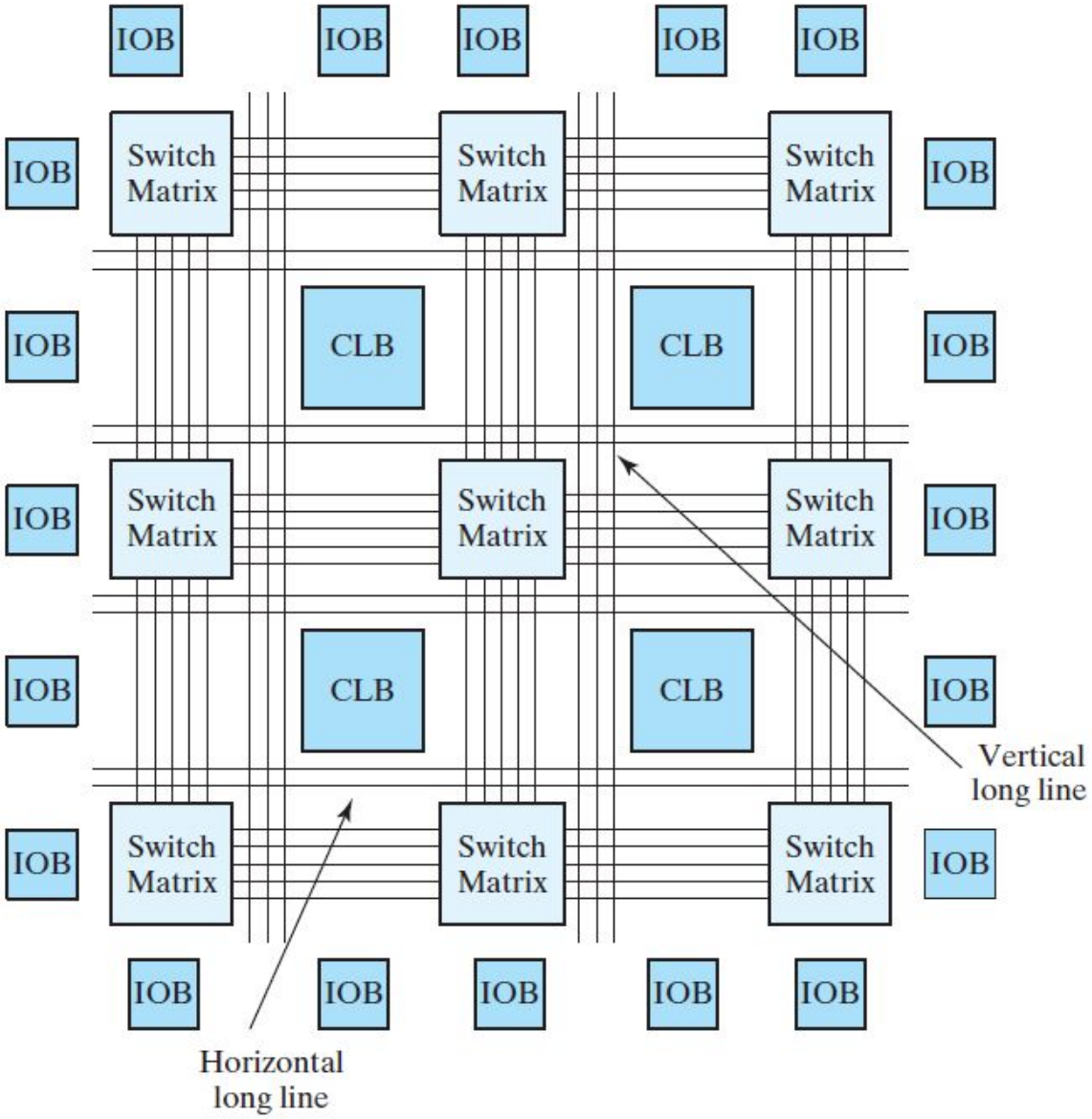
CPLD
COMPLEX PROGRAMMABLE LOGIC DEVICE



FPGA
FIELD-PROGRAMMABLE GATE ARRAY



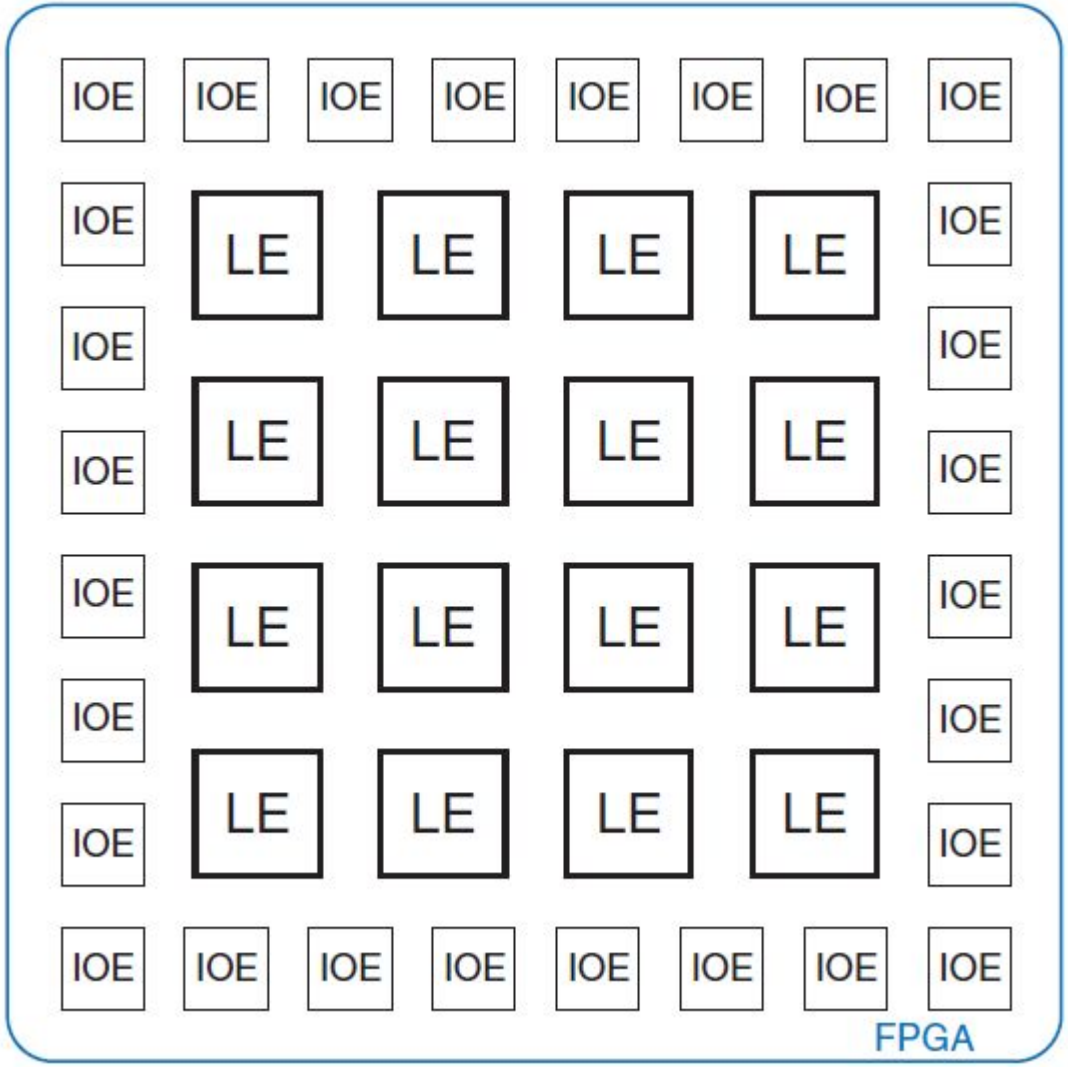
CONFIGURABLE LOGIC BLOCK (CLBs)

INPUT/OUTPUT BLOCK (IOBs)

ARQUITECTURA BÁSICA DE XILINX SPARTAN

UTN

FPGA
FIELD-PROGRAMMABLE GATE ARRAY



LOGIC ELEMENT (LEs)

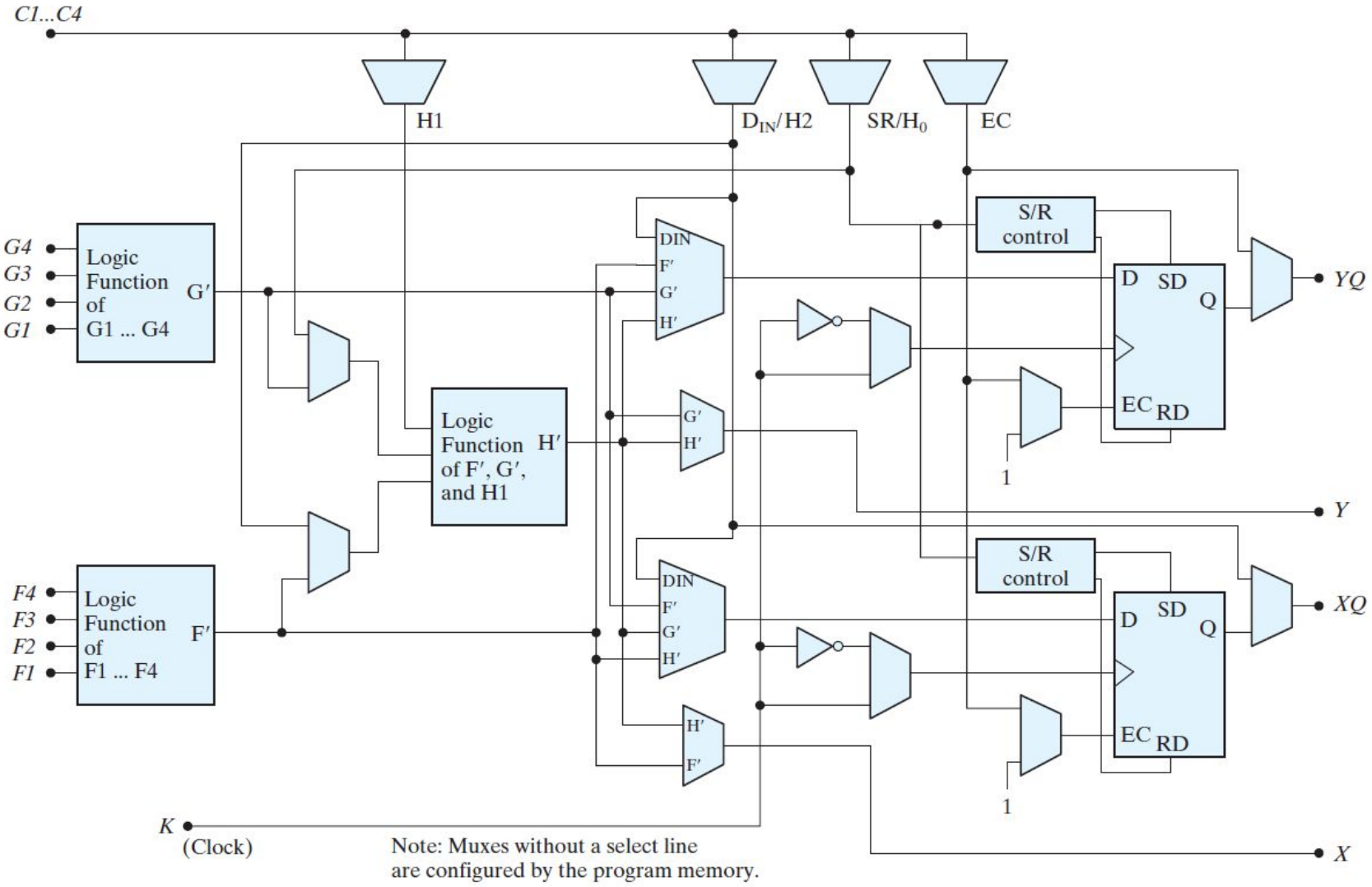
INPUT/OUTPUT ELEMENT (IOEs)

ALGUNAS FPGAS INCLUYEN OTROS BLOQUES CONSTRUCTIVOS COMO MULTIPLICADORES, RAMS, ETC.

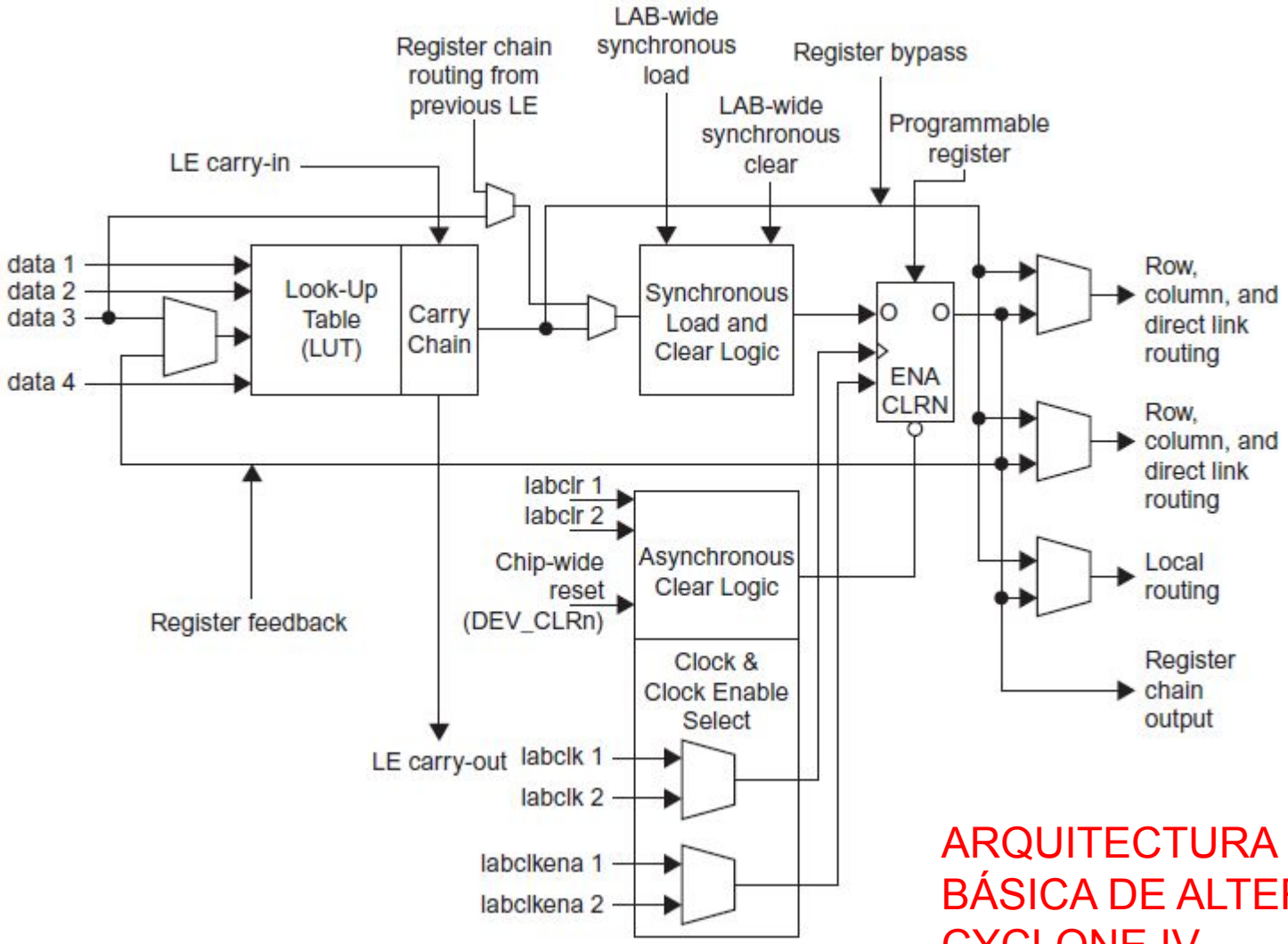
ARQUITECTURA BÁSICA DE ALTERA

UTN

ARQUITECTURA DE UN CLB
CONFIGURABLE LOGIC BLOCK



ARQUITECTURA DE UN LE
LOGIC ELEMENT



LOGIC ARRAY BLOCK (LAB) (16 LEs)

ARQUITECTURA BÁSICA DE ALTERA CYCLONE IV

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ARQUITECTURA DE UN CLB
CONFIGURABLE LOGIC BLOCK

Un bloque lógico típico consiste de lookup tables (LUTs), multiplexores, compuertas y flip-flops.

Una lookup table es una tabla de verdad almacenada en una SRAM y suministra las funciones combinacionales del circuito para el bloque lógico.

Por ejemplo, una SRAM de 16 x 2 puede almacenar la tabla de verdad de un circuito combinacional que tiene 4 entradas y dos salidas.

UTN

LOOKUP TABLE
LUTs

Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

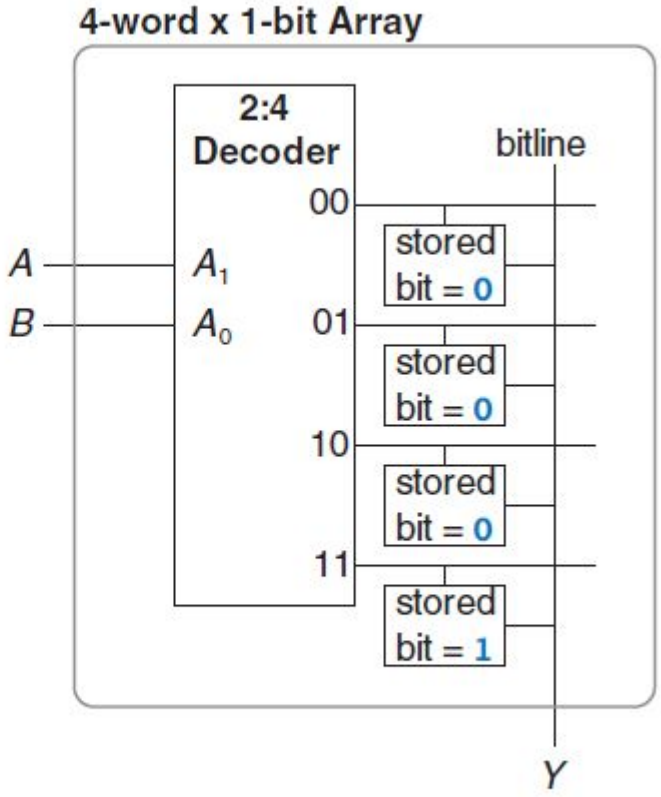

Figure 5.53 4-word × 1-bit memory array used as a lookup table