EA772 Circuitos Lógicos
Prof. José Mario De Martino – Prova 01 – 2°. Semestre 2009

1.

a) $01011011_2 = 2^6 + 2^4 + 2^3 + 2^1 + 2^0 = 91_{10}$

b) $53_{10} = 110101_2$

53 / 2 = 26 resto = 1

26 / 2 = 13 resto = 0

13 / 2 = 6 resto = 1

6 / 2 = 3 resto = 0

3 / 2 = 1 resto = 1

1 / 2 = 0 resto = 1

c) $458_{10} = 1CA_{16}$

458 / 16 = 28 resto = 10 → A

28 / 16 = 1 resto = 12 → C

1 / 16 = 0 resto = 1 → 1

d) $3E8_{16} = 3 \cdot 16^2 + 14 \cdot 16^1 + 8 \cdot 16^0 = 1000_{10}$

2.

	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
$x'_3 x'_2$	0	1	1	1
$x'_3 x_2$	1	1	0	0
$x_3 x_2$	0	1	1	1
$x_3 x'_2$	0	0	1	1

$fsp_1 = x'_2 x_1 + x_3 x_1 + x'_3 x_2 x'_1 + x'_3 x'_2 x_0 + x_2 x'_1 x_0$ (6 portas)

$fsp_2 = x'_2 x_1 + x_3 x_1 + x'_3 x_2 x'_1 + x'_3 x'_2 x_0 + x_3 x_2 x_0$ (6 portas)

$fsp_3 = x'_2 x_1 + x_3 x_1 + x'_3 x_2 x'_1 + x'_3 x'_1 x_0 + x_3 x_2 x_0$ (6 portas)

$fsp_4 = x'_2 x_1 + x_3 x_1 + x'_3 x_2 x'_1 + x'_3 x'_1 x_0 + x_2 x'_1 x_0$ (6 portas)

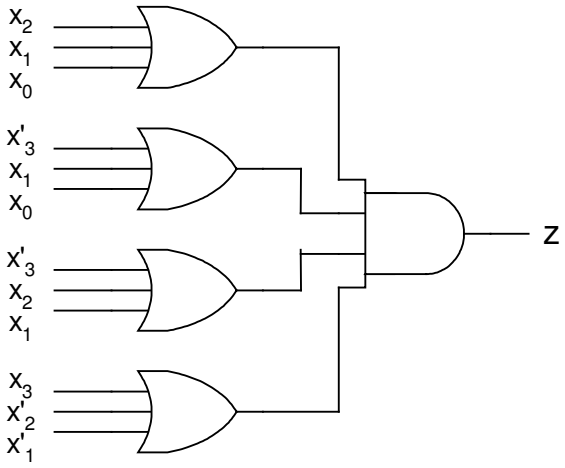
fsp_1, fsp_2, fsp_3 e fsp_4 têm custos equivalentes (mesmo número de portas).

	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
$x'_3 x'_2$	0	1	1	1
$x'_3 x_2$	1	1	0	0
$x_3 x_2$	0	1	1	1
$x_3 x'_2$	0	0	1	1

$fps_1 = (x_2 + x_1 + x_0)\ (x'_3 + x_1 + x_0)\ (x'_3 + x_2 + x_1)\ (x_3 + x'_2 + x'_1)$ (5 portas)

fps_1 tem o menor custo (menor número de portas), portanto é a melhor solução.

Diagrama esquemático do circuito:



3.

x_2	x_1	x_0	z_1	z_0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Z_1	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
x'_2	1	1	0	1
x_2	1	0	0	0

$z_{1sp} = x'_2 x'_1 + x'_2 x'_0 + x'_1 x'_0$ (4 portas)

Z_1	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
x'_2	1	1	0	1
x_2	1	0	0	0

$z_{1ps} = (x'_1 + x'_0)\ (x'_2 + x'_0)\ (x'_2 + x'_1)$ (4 portas)

z_{1sp} e z_{1ps} têm mesmo custo (mesmo número de portas). Arbitrariamente é escolhido z_{1sp}

Z_0	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
x'_2	1	0	1	0
x_2	0	1	0	1

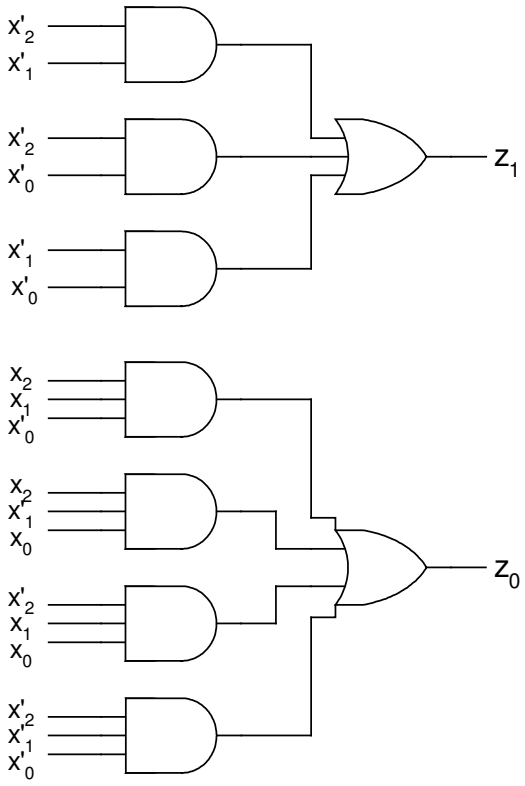
$z_{0sp} = x'_2 x'_1 x'_0 + x'_2 x_1 x_0 + x_2 x'_1 x_0 + x_2 x_1 x'_0$ (5 portas)

Z_0	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
x'_2	1	0	1	0
x_2	0	1	0	1

$z_{0ps} = (x_2 + x_1 + x'_0)\ \ (x_2 + x'_1 + x_0)\ \ (x'_2 + x_1 + x_0)\ \ (x'_2 + x'_1 + x'_0)$ (5 portas)

z_{0sp} e z_{0ps} têm mesmo custo (mesmo número de portas). Arbitrariamente é escolhido z_{0sp}

O desenho esquemático do circuito é:



4.

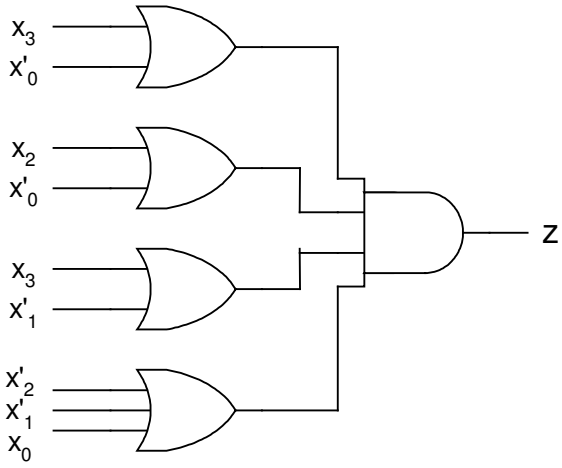
1	0001 n	00x1 n	0xx1 n
	0010 n	0x01 n	x0x1 n
		x001 n	0x1x n
2	0011 n	001x n	
	0101 n	0x10 n	
	0110 n		
	1001 n	0x11 n	
		x011 n	
3	0111 n	01x1 n	
	1011 n	011x n	
	1110 n	x110	
		10x1 n	

	1	2	3	5	6	7	9	11	14	
0xx1	x		x	x		x				←
x0x1	x		x				x	x		←
0x1x		x	x		x	x				←
		↑		↑			↑	↑	↑	←

x110 | x x

fps = $(x_3 + x'_0)\ (x_2 + x'_0)\ (x_3 + x'_1)\ (x'_2 + x'_1 + x_0)$

Diagrama esquemático do circuito:



5.

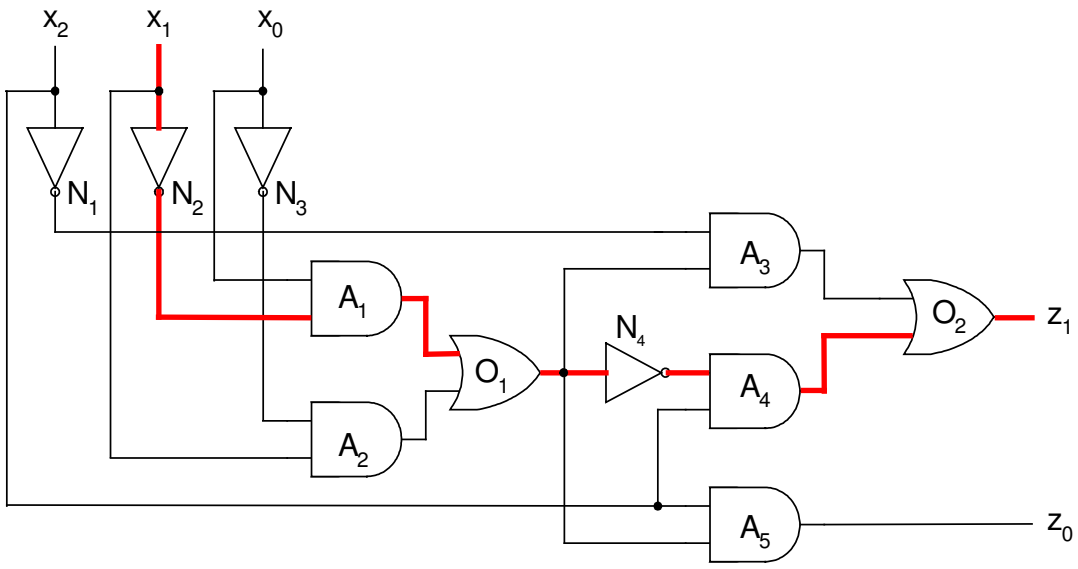
a) Fator de carga de entrada:

$I(x_2) = 3$ $I(x_1) = I(x_0) = 2$

b) Fanout de cada saída:

$Fanout(z_1) = Fanout(z_0) = 12$ (Fanout CMOS = 12)

c)



$t_{pHL}(x_1, z_1) = t_{pLH}(O_2) + t_{pLH}(A_4) + t_{pLH}(N_4) + t_{pHL}(O_1) + t_{pHL}(A_1) + t_{pHL}(N_2)$

$t_{pLH}(O_2) = 0,12 + 0,037\ L$

$t_{pLH}(A_4) = 0,15 + 0,037 \cdot 1 = 0,187$

$t_{pLH}(N_4) = 0,02 + 0,038 \cdot 1 = 0,058$

$t_{pHL}(O_1) = 0,20 + 0,019 \cdot 3 = 0,257$

$t_{pHL}(A_1) = 0,16 + 0,017 \cdot 1 = 0,177$

$t_{pHL}(N_2) = 0,05 + 0,017 \cdot 1 = 0,067$

$t_{pLH}(x_2, z_0) = 0,866 + 0,037\ L\ ns$