

Nome: _____ RA: _____

- | EA | Entrada | |
|----|---------|-------|
| | x = 0 | x = 1 |
| A | F, 0 | C, 0 |
| B | H, 1 | G, 1 |
| C | H, 0 | D, 1 |
| D | B, 0 | H, 0 |
| E | B, 0 | C, 0 |
| F | C, 1 | G, 1 |
| G | H, 1 | B, 1 |
| H | C, 0 | A, 1 |
| | PE, z | |

- [illegible]

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Characteristics of a family of CMOS gates

Gate type	Fan-in	Propagation delays		Load factor	Size
		t_{pLH} [ns]	t_{pHL} [ns]	[standard loads]	[equiv. gates]
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0	2
AND	3	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0	2
AND	4	$0.28 + 0.039L$	$0.21 + 0.019L$	1.0	3
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0	2
OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$	1.0	2
OR	4	$0.13 + 0.038L$	$0.45 + 0.025L$	1.0	3
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0	1
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0	1
NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0	2
NAND	4	$0.10 + 0.037L$	$0.12 + 0.051L$	1.0	2
NAND	5	$0.21 + 0.038L$	$0.34 + 0.019L$	1.0	4
NAND	6	$0.24 + 0.037L$	$0.36 + 0.019L$	1.0	5
NAND	8	$0.24 + 0.038L$	$0.42 + 0.019L$	1.0	6
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0	1
NOR	3	$0.16 + 0.111L$	$0.08 + 0.017L$	1.0	2
NOR	4	$0.23 + 0.149L$	$0.08 + 0.017L$	1.0	4
NOR	5	$0.38 + 0.038L$	$0.23 + 0.018L$	1.0	4
NOR	6	$0.46 + 0.037L$	$0.24 + 0.018L$	1.0	5
NOR	8	$0.54 + 0.038L$	$0.23 + 0.018L$	1.0	6
XOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	

Tabela 1: Características de portas lógicas CMOS.

Delays					Input factor	Size
t_{pLH} [ns]	t_{pHL} [ns]	t_{su} [ns]	t_h [ns]	t_w [ns]	[std. loads]	[equiv. gates]
$0.49 + 0.038L$	$0.54 + 0.019L$	0.30	0.14	0.2	1	6

L : output load of the flip-flop

Tabela 2: Características do flip-flop JK CMOS.