EA772 Circuitos Lógicos
Prof. José Mario De Martino – Prova 03 – 1°. Semestre 2009

1.

a) 86 + 84 = 0A C = 1 V = 1 N = 0 Z = 0
b) 39 + D5 = 0E C = 1 V = 0 N = 0 Z = 0
c) 94 + F2 = 86 C = 1 V = 0 N = 1 Z = 0
d) 5A + 16 = 70 C = 0 V = 0 N = 0 Z = 0
e) D3 + 1F = F2 C = 0 V = 0 N = 1 Z = 0
f) E5 + 1B = 00 C = 1 V = 0 N = 0 Z = 1
g) 8C + 92 = 1E C = 1 V = 1 N = 0 Z = 0
h) 32 + 4E = 80 C = 0 V = 1 N = 1 Z = 0
i) AC + 37 = E3 C = 0 V = 0 N = 1 Z = 0
j) 73 + 65 = D8 C = 0 V = 1 N = 1 Z = 0

2.

x_3	x_2	x_1	x_0	f
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

f

	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
$x'_3 x'_2$	0	1	1	0
$x'_3 x_2$	1	1	0	0
$x_3 x_2$	0	1	0	1
$x_3 x'_2$	0	1	0	0

f

	$x'_1 x'_0$	$x'_1 x_0$	$x_1 x_0$	$x_1 x'_0$
x'_2	0	1	x'_3	0
x_2	x'_3	1	0	x_3

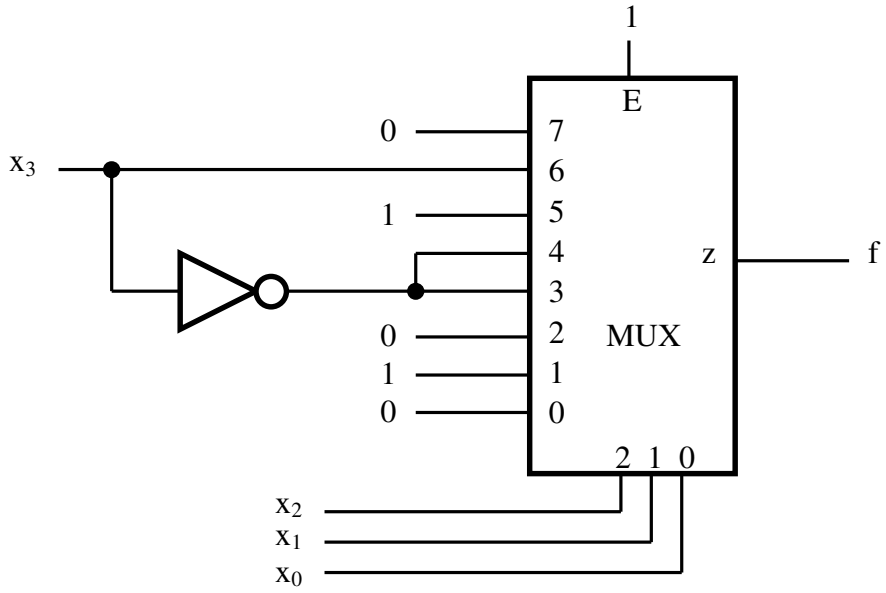


Figura 1: Circuito do exercício 2.

3.

LD

	$Q'_1 Q'_0$	$Q'_1 Q_0$	$Q_1 Q_0$	$Q_1 Q'_0$
$Q'_3 Q'_2$	0	0	0	0
$Q'_3 Q_2$	0	0	0	0
$Q_3 Q_2$	1	X	X	X
$Q_3 Q'_2$	0	0	0	0

$LD = Q_3 Q_2$

A Figura 2 apresenta o circuito resultante.

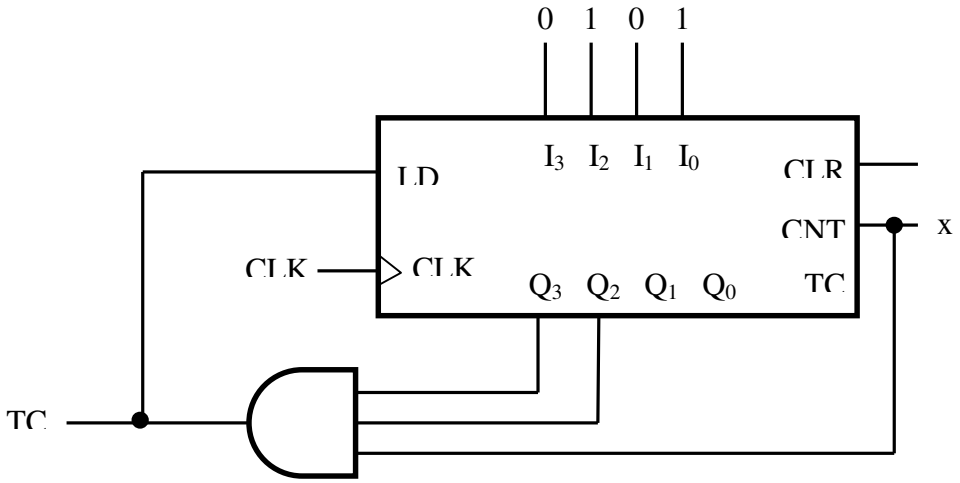
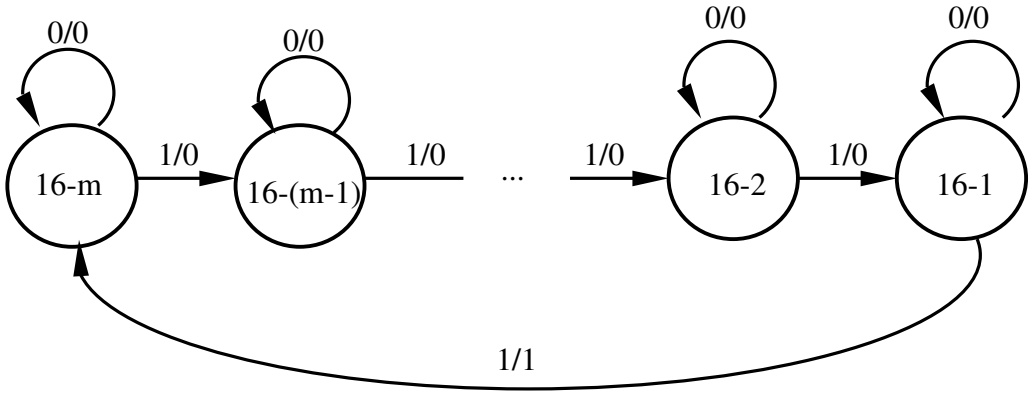
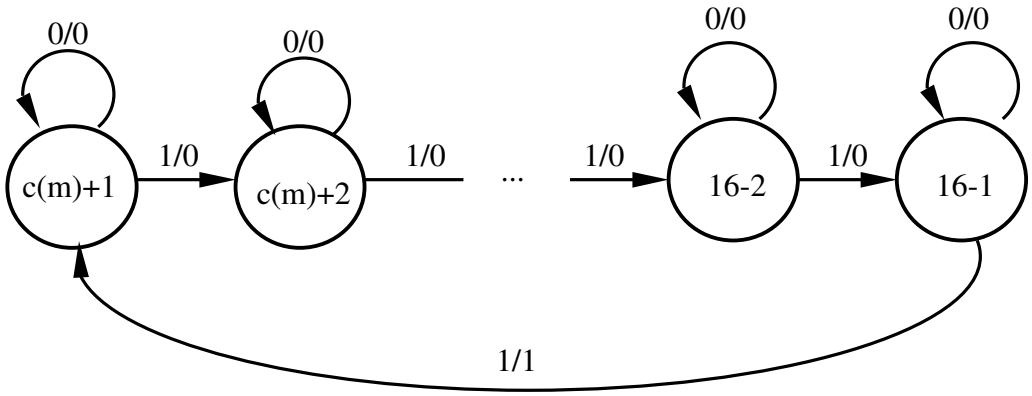


Figura 2: Circuito do exercício 3.

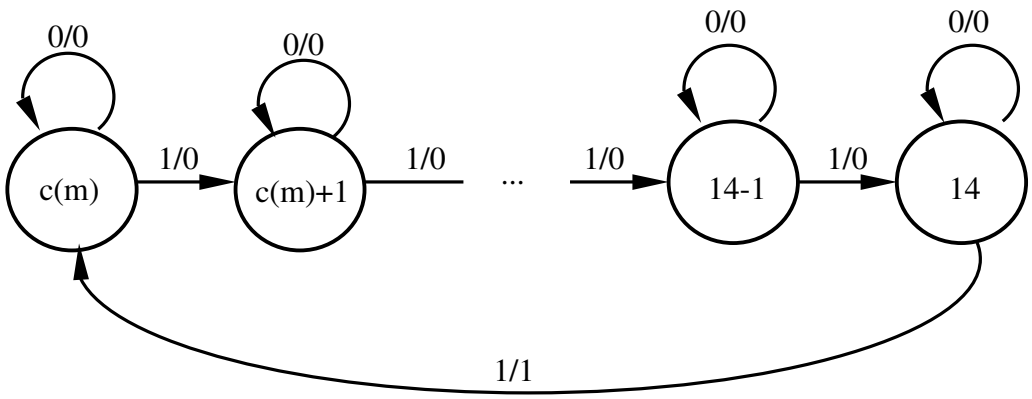
4.



Considerando c(m) o complemento bit a bit de m, sendo que c(m) = 15 – m, podemos escrever 16 – m = 15 – m + 1 = c(m) + 1



Assim, se inicarmos a contagem em c(m) precisamos terminar a contagem um estado antes, ou seja, em 16-2 = 14.
Portanto, temos um contador módulo 15 que inicia a contagem em c(m)



z

	$Q'_1 Q'_0$	$Q'_1 Q_0$	$Q_1 Q_0$	$Q_1 Q'_0$
$Q'_3 Q'_2$	0	0	0	0
$Q'_3 Q_2$	0	0	0	0
$Q_3 Q_2$	0	0	X	1
$Q_3 Q'_2$	0	0	0	0

$z = Q_3 Q_2 Q_1$

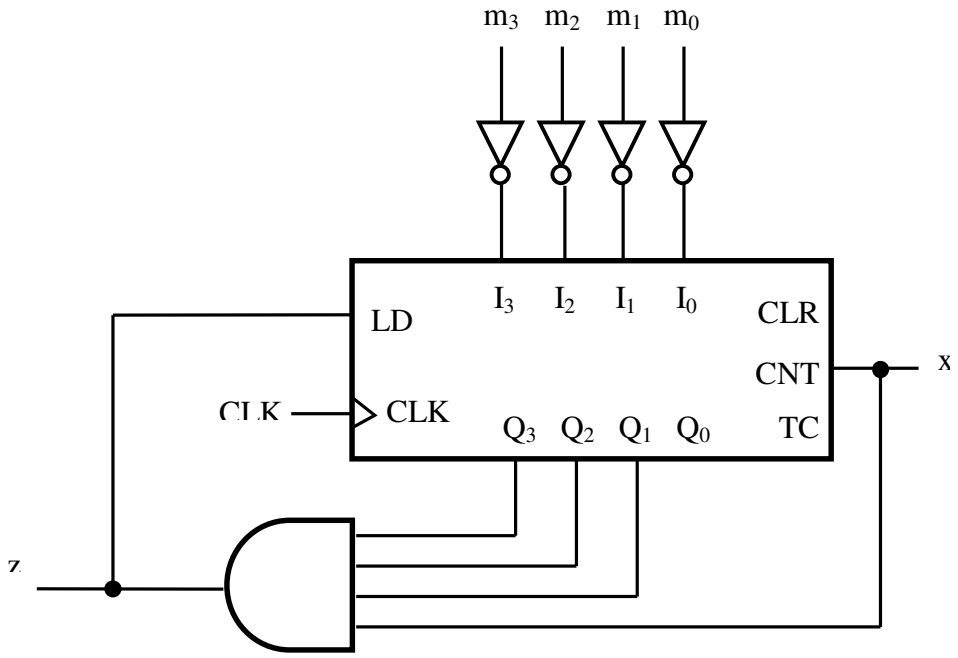


Figura 4: Circuito do exercício 4.

5.

Resultado Soma Binária					Reusltado Soma BCD				
C_{out}	z_3	z_2	z_1	z_0	C_{out}	b_3	b_2	b_1	b_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Para corrigir, somar 6

C sinal de correção

	$z'_1 z'_0$	$z'_1 z_0$	$z_1 z_0$	$z_1 z'_0$
$z'_3 z'_2$	0	0	0	0
$z'_3 z_2$	0	0	0	0
$z_3 z_2$	1	1	1	1
$z_3 z'_2$	0	0	1	1

$C = z_3 z_2 + z_3 z_1 + C_{out}$

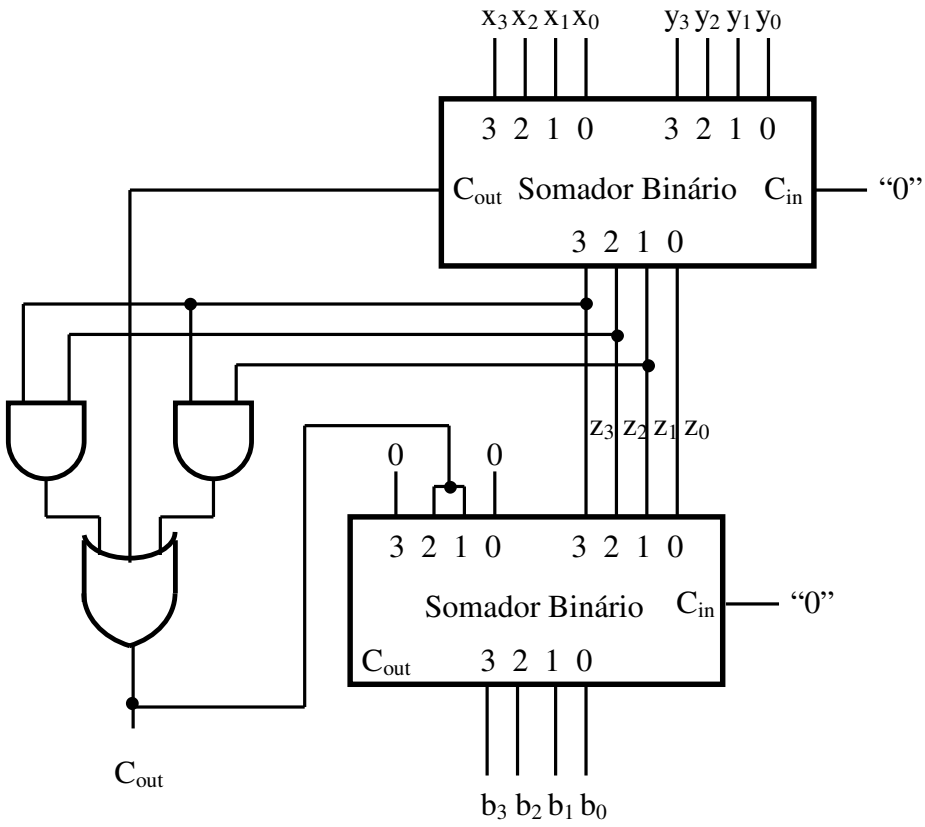


Figura 3: Circuito exercício 5.