



KIIT, Deemed to be University
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Digital System Design Laboratory [EC 29005]

Verilog Testbench code

Test-bench Verilog code for the Experiment 1 for SOP simulation is given below with comments (//).

```
module    test_SOP( ) ;

    reg    A,B,C ;    // Inputs required to simulate the circuit and should be signed reg type

    wire   F ;        // Outputs required to simulate the circuit and should be signed wire type

    SOP     CKT1 (F,A,B,C) ; // Circuit to be simulated called

    initial                                // Initialization begins
        begin
            A = 0 ; B = 0 ; C = 0 ;    // Assigned values to the inputs for simulation
            #10                        // Delay for 10 nano seconds
            A = 0 ; B = 0 ; C = 1 ;
            #10
            A = 0 ; B = 1 ; C = 0 ;
            #10
            A = 0 ; B = 1 ; C = 1 ;
            #10
            A = 1 ; B = 0 ; C = 0 ;
            #10
            A = 1 ; B = 0 ; C = 1 ;
            #10
            A = 1 ; B = 1 ; C = 0 ;
            #10
            A = 1 ; B = 1 ; C = 1 ;
            #10

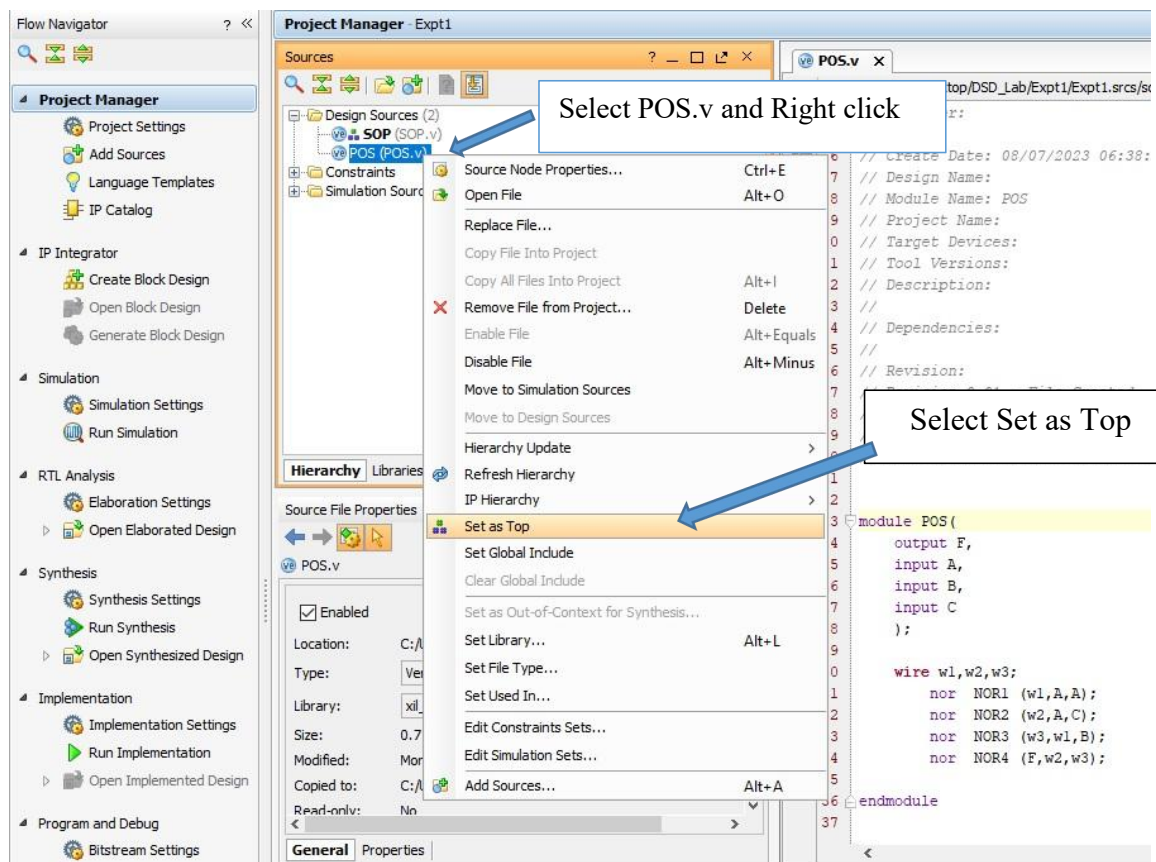
        $finish ;

    end                                // Initialization ends here

endmodule
```

When there are multiple design sources in the project ?

Considering in experiment 1 there are two Design Verilog files SOP.v and POS.v . To view the RTL schematic of POS change the Top Module to POS by **right click** on POS.v then select **Set as Top** in the **Design Sources**.



To simulate the POS change the Top Module to POS by **right click** on POS.v then select **Set as Top** in the **Simulation Sources**.

The screenshot displays the Xilinx IDE interface with the following components:

- Flow Navigator:** Shows project settings, IP integrator, simulation, RTL analysis, synthesis, implementation, and program and debug options.
- Project Manager - Expt1:** The central pane showing the project hierarchy. The **Sources** tab is active, displaying a tree structure with Design Sources (2), Constraints, and Simulation Sources (4). The file **test_POS (test_POS.v) (1)** is selected.
- Simulation Sources:** A callout box points to the **Simulation Sources** folder in the project tree.
- Right-click context menu:** A menu is open for the selected file **test_POS (test_POS.v) (1)**. The **Set as Top** option is highlighted. Other options include Source Node Properties..., Open File, Replace File..., Copy File Into Project, Copy All Files Into Project, Remove File from Project..., Enable File, Disable File, Move to Simulation Sources, Move to Design Sources, Hierarchy Update, Refresh Hierarchy, IP Hierarchy, Set Global Include, Clear Global Include, Set as Out-of-Context for Synthesis..., Set Library..., Set File Type..., Set Used In..., Edit Constraints Sets..., Edit Simulation Sets..., and Add Sources....
- test_POS.v:** The code editor shows the Verilog code for the **test_POS** module, starting with `module test_POS(`.
- Source File Properties:** A panel at the bottom shows the properties for the selected file, including Location, Type (Verilog), Library (xilinx_defaultlib), Size (0.9 KB), Modified (Today at 10:31:58 AM), Copied to, and Read-only status.