Design code for sequence generator

```
module sequence_gen(op,clk);

input clk;
output [3:0]op;
reg [3:0]op;
  initial
    begin
  op[3:0] = 4'b1100 ;
     end
always @( posedge clk)
  op <= {op[3]^op[1], op[3:1]};

endmodule
```

Testbench

```
module test_sequence_gen();
  reg clk;
  wire [3:0] op;

  sequence_gen SG1 (op,clk);

  initial
    begin
     clk=0;
    forever #10 clk = ~clk;
end

  initial
    begin
    #200
    $finish;
  end
endmodule
```