KIIT, Deemed to be University
School of Electronics Engineering
Digital System Design Laboratory [EC 29005]

EXPERIMENT - 5

Aim:

Design and simulate JK flip-flop and D flip-flop using Verilog behavioral modeling. Designing of JK flip-flop using D flip-flop and 2X1 Multiplexer.

Component/Software Used:

Component/Software	Specification
ICs	7476, 7474,74157,7404
Bread Board, Power supply, LEDs, Resistors,Switches, Connecting wires	As per requirement
Software(s) Used	Vivado 2016.1

Theory:

Flip-flop:

Flip - flop is the basic one bit digital memory circuit . It can store either 0 or 1.Flip-flops are the basic building blocks of most sequential circuits. Flip-flops are the fundamental components of shift registers and counters. A Flip-flop has two outputs, **Q** and $\overline{\mathbf{Q}}$, which are always in opposite states. If Q is 1, then $\overline{Q}$ is 0, and the flip-flop is said to be **set** or **on**. If Q is 0, then $\overline{Q}$ is 1 and the flip-flop is said to be **reset**, **off**, or **cleared**. It can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states. There are several types of flip flop, and the inputs vary with each type.

Flip-flop triggers only during a signal transition (from 0 to 1 or from 1 to 0), and is disabled during the rest of the clock cycle pulse duration. Positive edge means positive transition i.e. signal transition from 0 to 1. Negative edge means negative transition, i.e. signal transition from 1 to 0.

Flip-flops have **asynchronous** inputs that are used to force the flip-flop into a particular state independent of the clock. The input that sets the flip-flop to **1** is called a **Preset**. The input that clears the flip-flop to **0** is called **Clear**. When power is turned on in a digital system, the state of the flip-flop is unknown. The direct inputs are useful for bringing all the flip-flops in the system to a know starting state prior to the clocked operation.

JK flip-flop:

The J-K flip-flop is very versatile and also the most widely used. The outputs are complement to each other. A clock input is included in edge-triggered flip-flops.

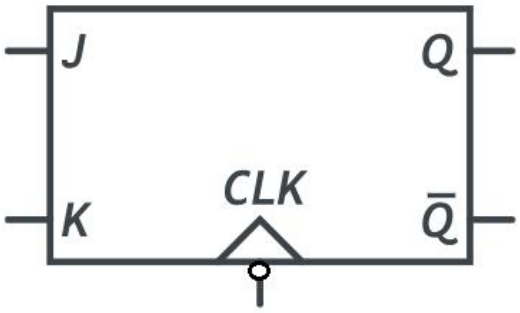


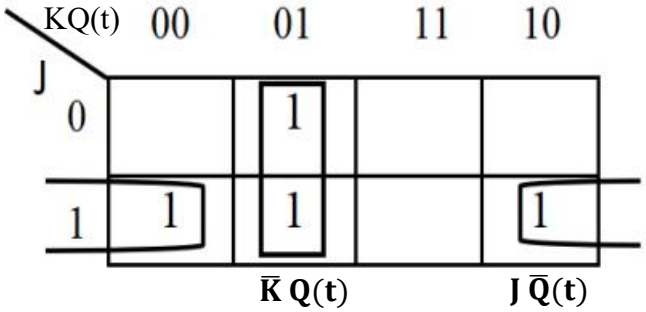
Figure 5.1 JK FF symbol(Negative edge)

Inputs			Output	Comments
CLK	J	K	Q	
1	X	X	Q(t)	**No change**
0	0	0	Q(t)	**No change**
0	0	1	0	**Reset**
0	1	0	1	**Set**
0	1	1	$\bar{Q}$(t)	**Toggle**

Table 5.1: JK Flip-Flop function table

Inputs		P.S	N.S
J	K	Q(t)	Q(t + 1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 5.2: Characteristic table of J-K FF



$$Q(t+1) = J\,\bar{Q}(t) + \bar{K}\,Q(t)$$

Characteristic Equation of JK FF

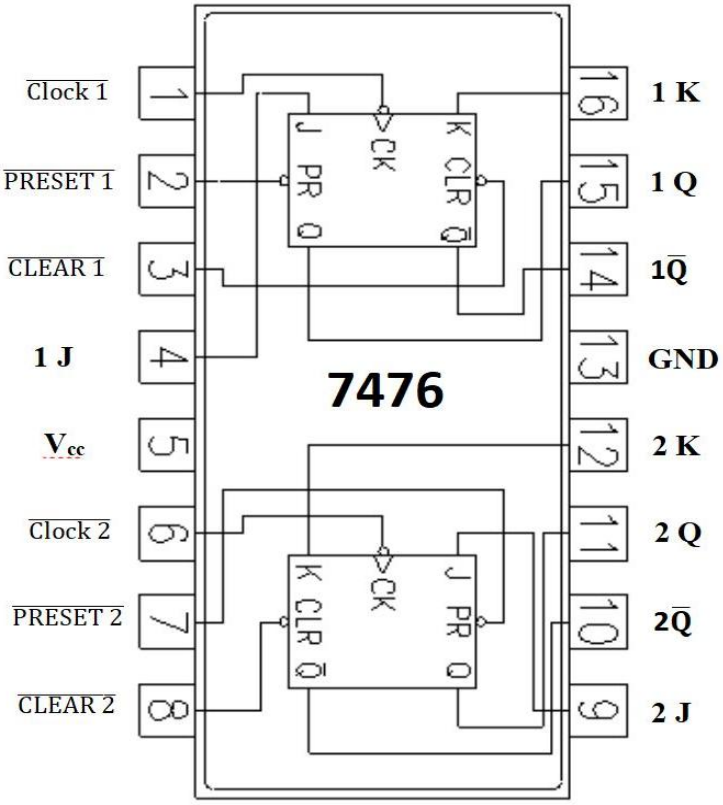


Figure 5.2: Pin diagram of IC 7476

Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc - Positive Power Supply
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

Table 5.3: Pin Description of 7476 IC

D flip-flop:

In D flip-flop, the output is same as input, i.e. when D= 0, the flip-flop is reset and when D = 1, the flip-flop is set.

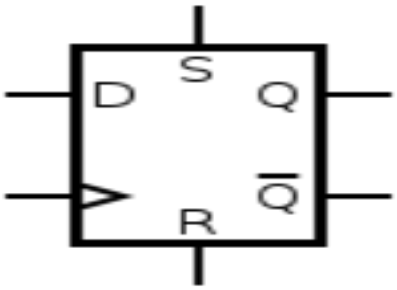


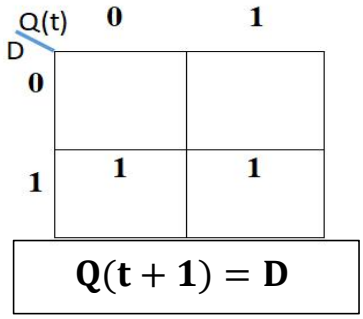
Figure 5.3 : D FF Symbol (Postive edge)

Inputs		Output	Comments
CLK	**D**	**Q**	
0	X	Q(t)	**No change**
1	0	0	**Reset**
1	1	1	**Set**

Table 5.4: D FF function table

P.S	Input	N.S
Q(t)	**D**	**Q(t + 1)**
0	0	0
0	1	1
1	0	0
1	1	1

Table 5.5: Characteristic table of D FF



Characteristic Equation of D FF

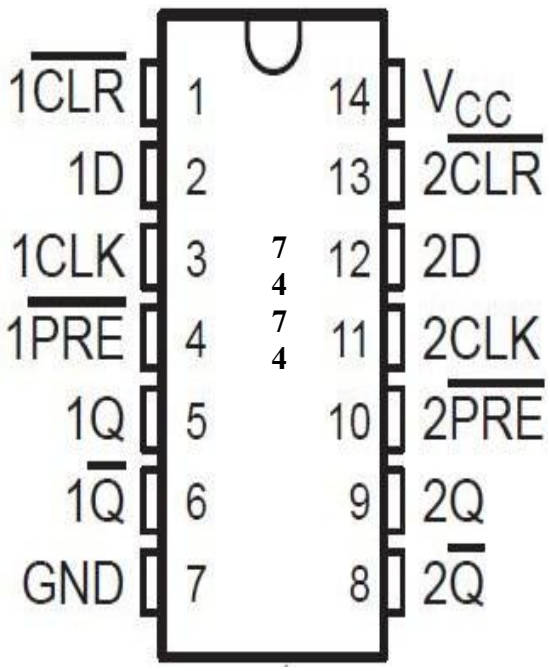


Figure 5.4 :Pin diagram of IC 7474

Pin Number	Description
1	Clear 1 Input
2	D1 Input
3	Clock 1 Input
4	Preset 1 Input
5	Q1 Output
6	Complement Q1 Output
7	Ground
8	Complement Q2 Output
9	Q2 Output
10	Preset 2 Input
11	Clock 2 Input
12	D2 Input
13	Clear 2 Input
14	Vcc - Positive Power Supply

Table 5.6: Pin Description of 7474 IC

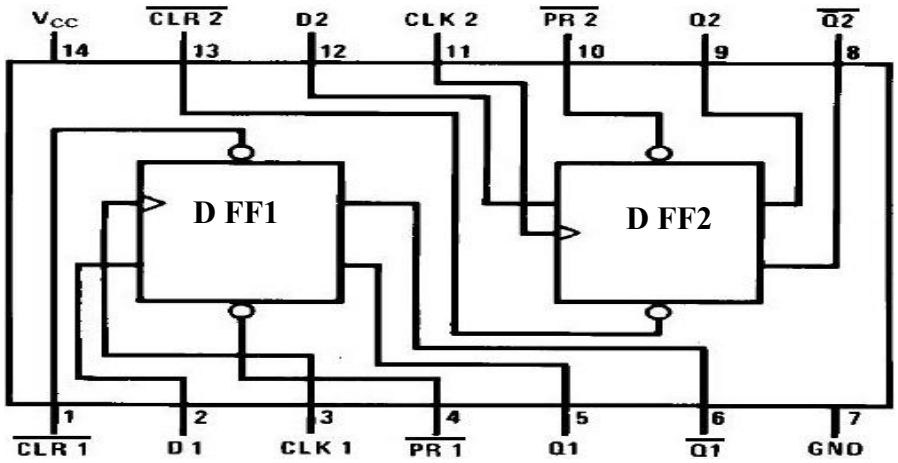


Figure 5.5: IC 7474 internal connection

Conversion of D flip-flop to JK flip-flop:

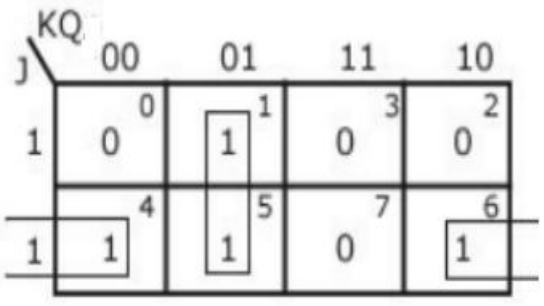
To convert one type of flip-flop into another type, a combination circuit is designed using function table, next state equation and the excitation table such that if the inputsof the required flip-flop are fed as inputs of the combinational circuit and the outputof the combinational circuit is connected to the inputs of the actual flip-flop, then the output of the actual flip-flop is the output of the required flip-flop.

P.S	N.S	Flip-flop inputs		
Q(t)	Q(t+1)	J	K	D
0	0	0	X	0
0	1	1	X	1
1	0	X	1	0
1	1	X	0	1

Table 5.7: Excitation table

Flip flop I/Ps		P.S	N.S	Required I/P's
J	K	Q(t)	Q(t+1)	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Table 5.8:Conversion table D flip-flop to JK FF



$$D(J,K,Q) = \sum m(1,4,5,6)$$

$$= J\overline{Q} + \overline{K}Q$$

Boolean expressions for D

From the above conversion table and the k-map simplification of the Boolean expressions for D input is: $\mathbf{D = J\bar{Q} + \bar{K}Q}$. The D flip-flop can be converted into a JK flip-flop by giving the value of D in the D flip-flop. Figure 5.6 shows the logic diagram for D flip-flop converted to form the JK flip-flop using required logic gates to implement the combinational logic. Boolean function can be implemented using multiplexer thus the combinational logic is replaced by 2X1 Mux where select input is assigned the output of D flip-flop $S_0 = Q$, and the inputs are assigned $I_0 = J$, $I_1 = \bar{K}$.

Figure 5.7 shows the logic diagram for D flip-flop converted to form the JK flip-flop using multiplexer and required logic gate.

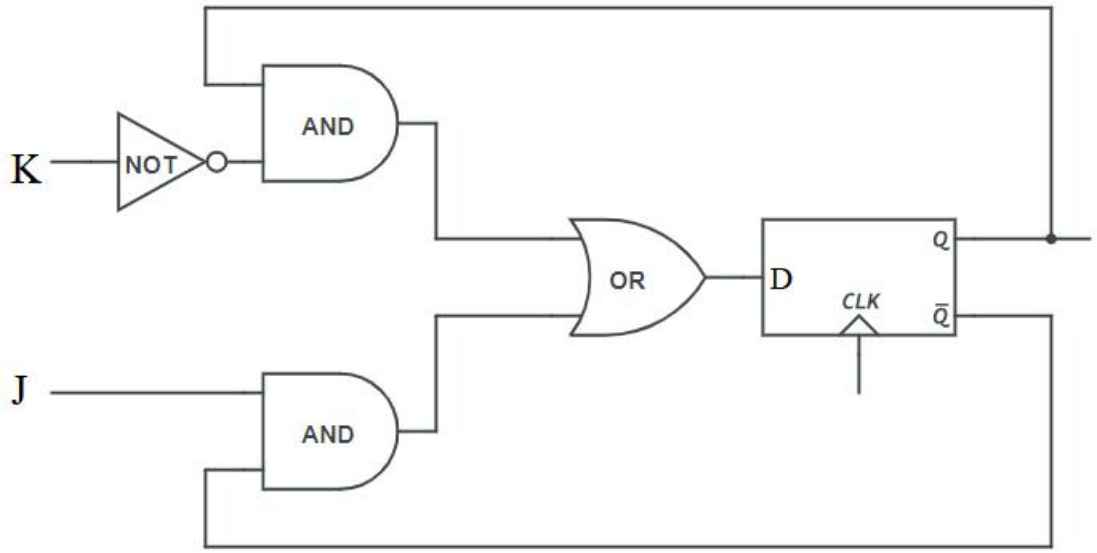


Figure 5.6: Logic diagram for JK FF using D FF and logic gates

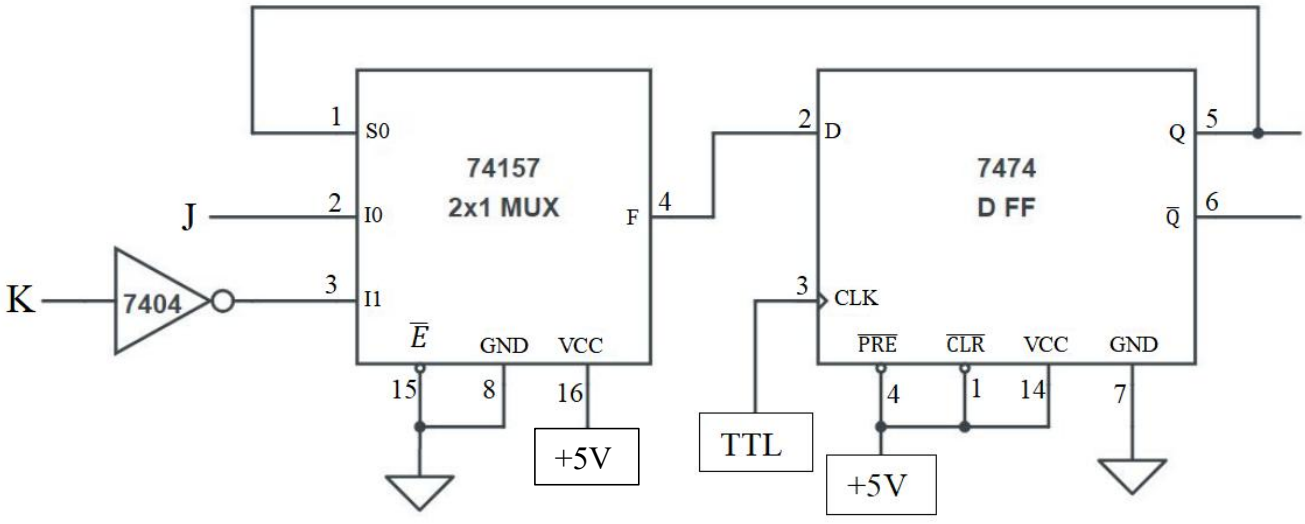


Figure 5.7: Logic diagram for JK FF using D FF (7474 IC) and 2X1 Mux (74157 IC)

Procedure

For Software Simulation:

a) Create a module with required number of variables and mention it's input/output.

b) Write the description of given Boolean function using operators or by using the

built in primitive gates.

c) Synthesize to create RTL Schematic.
d) Create another module referred as test bench to verify the functionality and to obtain the waveforms of input and output.
e) Follow the steps required to simulate the design and compare the obtained output with the corresponding truth table.
f) Take the screenshots of the RTL schematic and simulated waveforms.

Note: Students need to write the Verilog HDL code by their own for which they can refer Appendix - A if required.

For Hardware implementation:

a) Turn off the power of the Trainer Kit before constructing any circuit.
b) Connect **power supply (+ 5 V DC)** pin and **ground** pin to the respective pins of the trainer kit.
c) Place the ICs properly on the bread board in the Trainer Kit.
d) Connect VCC and GND pins of each chip to the power supply and ground bus strips on the bread board.
e) Connect the input and output pins of chips to the input switches and output LEDs respectively in the Trainer Kit.
f) Check the connections before you turn on the power.
g) Apply various combinations of inputs according to truth tables and observe outputs of LEDs.

Observation:

To be written by students

Design Problem:

Design and Simulation of D Flip-Flop using JK Flip-Flop in Verilog HDL.
Hardware implementation of D Flip-Flop using JK Flip-Flop.

Solution:

Flip flop I/P	P.S	N.S	Required I/P's	
D	**Q(t)**	**Q(t+1)**	**J**	**K**
0	0	0	0	X
1	0	1	1	X
0	1	0	X	1
1	1	1	X	0

Table 5.9: Conversion table of JK flip-flop to D flip-flop

From the above conversion table, k-map simplification of the Boolean expressions for J and K inputs are: $\mathbf{J = D}$, $\mathbf{K = \overline{D}}$ .The JK flip-flop can be converted into a D flip-flop by giving the value of J and K in the JK flip-flop. Figure 5.8: shows the logic diagram for D flip-flop converted from JK flip-flop.

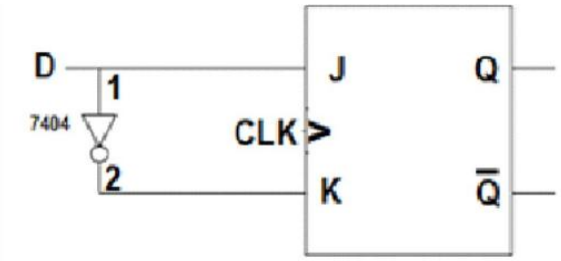


Figure 5.8: The logic diagram for D flip-flop converted from JK flip-flop.

Conclusion:

To be written by students.

Sample viva-voice questions

1. What is flip-flop?
2. What is latch circuit?
3. Drawthe truthtables of S-R, J-K, D and T FF.
4. What are the disadvantages of S-R flip-flop?
5. How can you remove the problem of S-R flip-flop?
6. Make the circuit diagram of S-R, J-K, D and T flip-flop.
7. What do you understand by Race Around condition? How is it overcome in J-K flip-flop?
8. Differentiate between latches and flip-flop.
9. What happens to the JK flip-flop if the J input is treated as an inverter is wired between J andK inputs?
10. Differentiate between combinational and sequential logic circuits.