KIIT, Deemed to be University

School of Electronics Engineering
Digital System Design Laboratory [EC 29005]

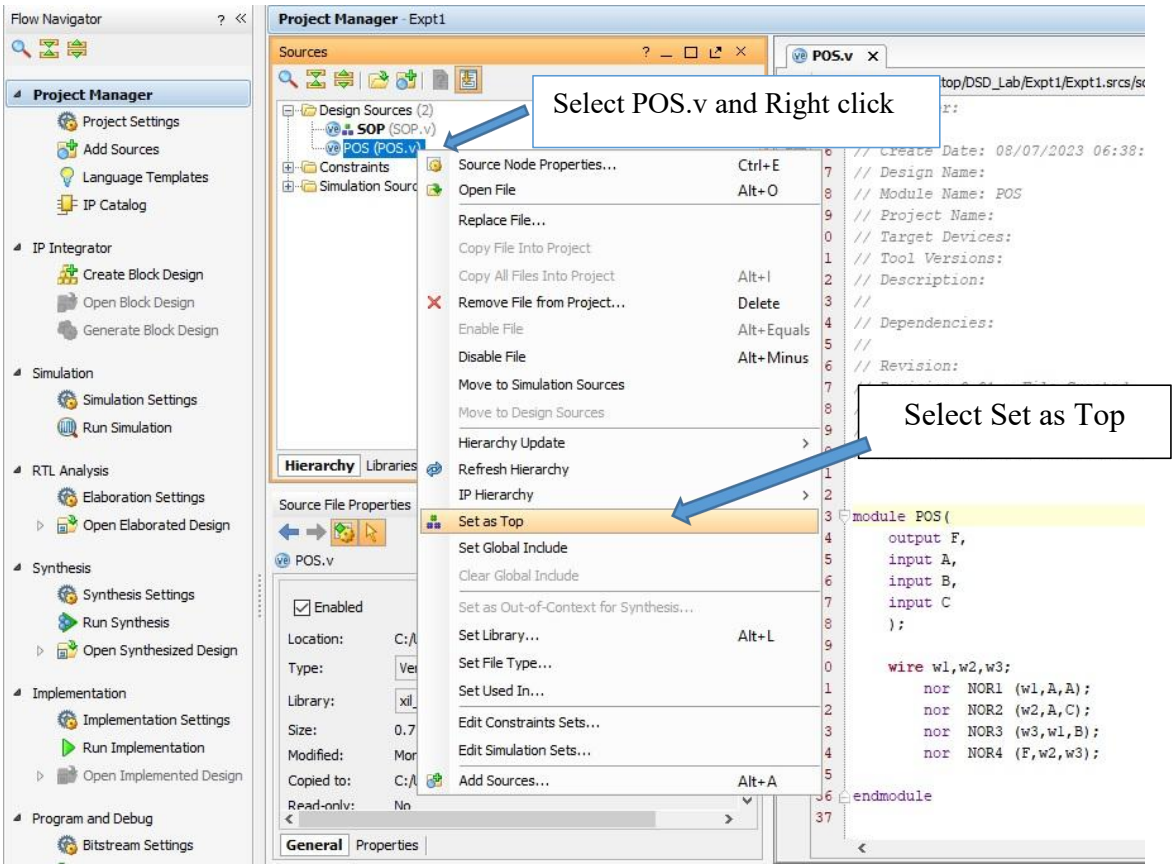
Verilog Testbench code

Test-bench Verilog code for the Experiment 1 for SOP simulation is given below with comments (//).

```
module    test_SOP( ) ;
    reg    A,B,C ;    // Inputs required to simulate the circuit and should be signed reg type
    wire   F ;        // Outputs required to simulate the circuit and should be signed wire type
    SOP       CKT1 (F,A,B,C) ;  //  Circuit to be simulated called

    initial                    // Initialization begins
      begin
        A = 0 ; B = 0 ;  C = 0 ;    //  Assigned values to the inputs for simulation
        #10                         //  Delay for 10 nano seconds
        A = 0 ; B = 0 ; C = 1 ;
        #10
        A = 0 ; B = 1 ; C = 0 ;
        #10
        A = 0 ; B = 1 ; C = 1 ;
        #10
        A = 1 ; B = 0 ; C = 0 ;
        #10
        A = 1 ; B = 0 ; C = 1 ;
        #10
        A = 1 ; B = 1 ; C = 0 ;
        #10
        A = 1 ; B = 1 ; C = 1 ;
        #10

      $finish ;

    end                        // Initialization ends here

endmodule
```

When there are multiple design sources in the project ?

Considering in experiment 1 there are two Design Verilog files SOP.v and POS.v . To view the RTL schematic of POS change the Top Module to POS by **right click** on POS.v then select **Set as Top** in the **Design Sources**.



To simulate the POS change the Top Module to POS by **right click** on POS.v then select **Set as Top** in the **Simulation Sources**.