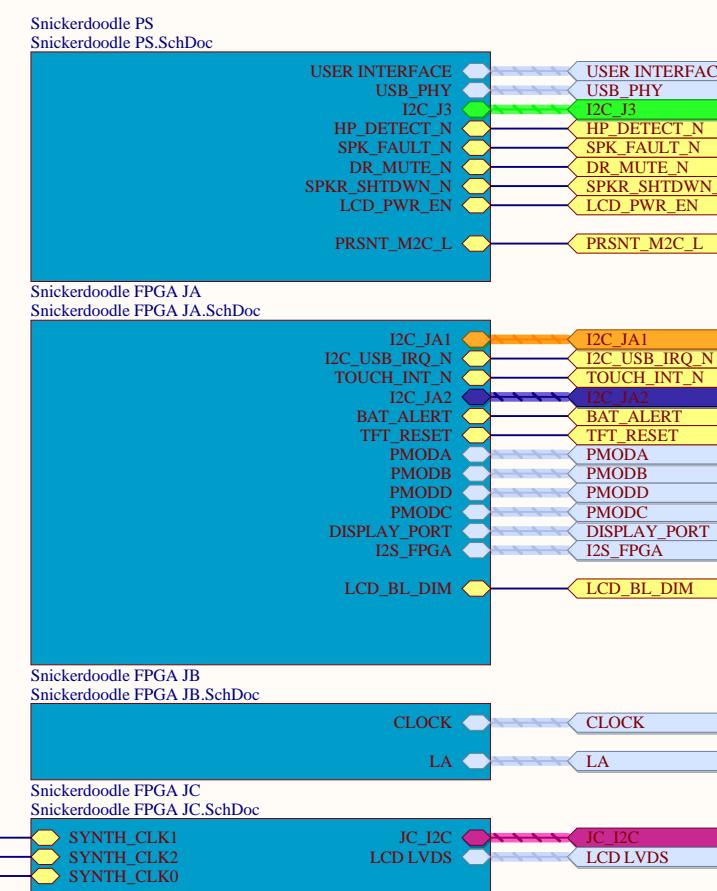


All banks are HR

A



B

A

B

C

D

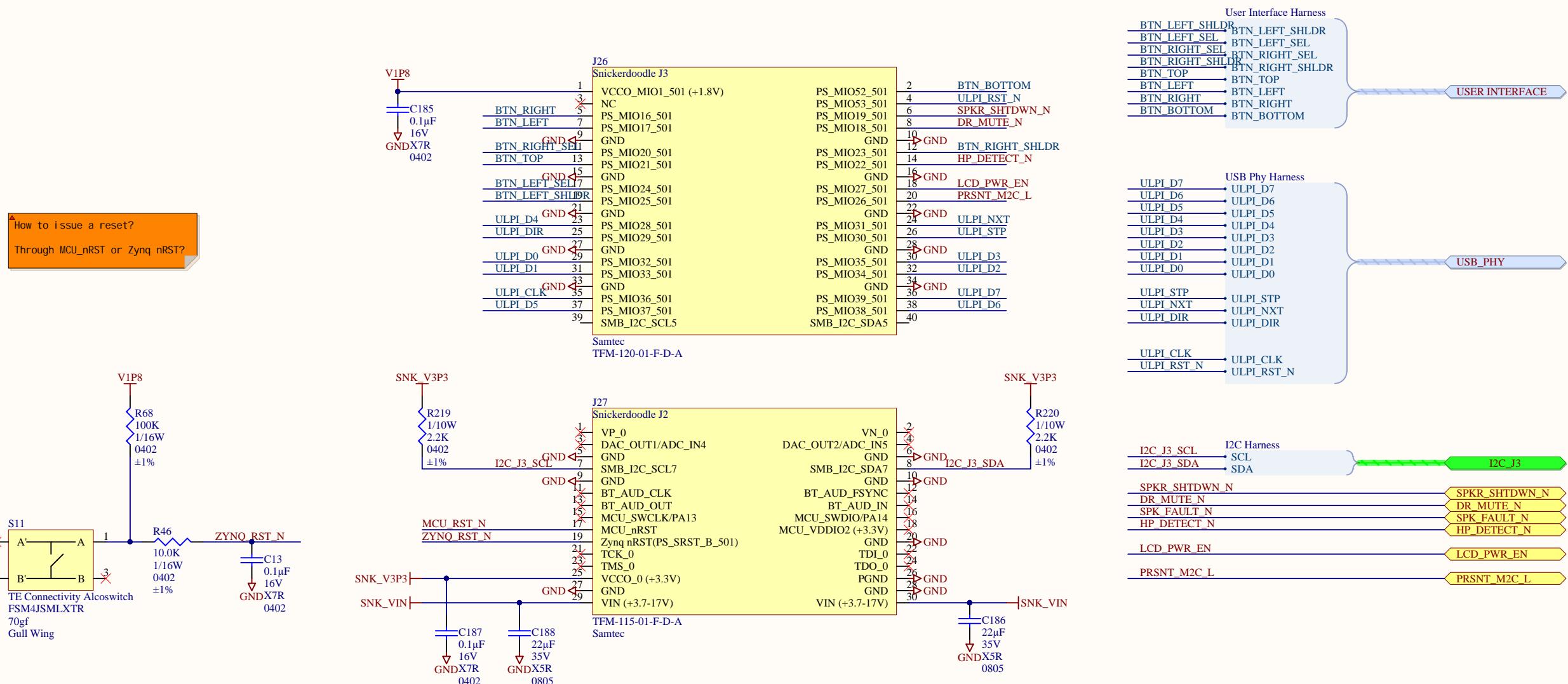
D

Not SnickerDoodle's Internal regulators for powering this board, but it would be good to make sure I2C is at the correct pullups

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle Top	
Document:	Snickerdoodle.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/17/2017	Number: 2 of 20



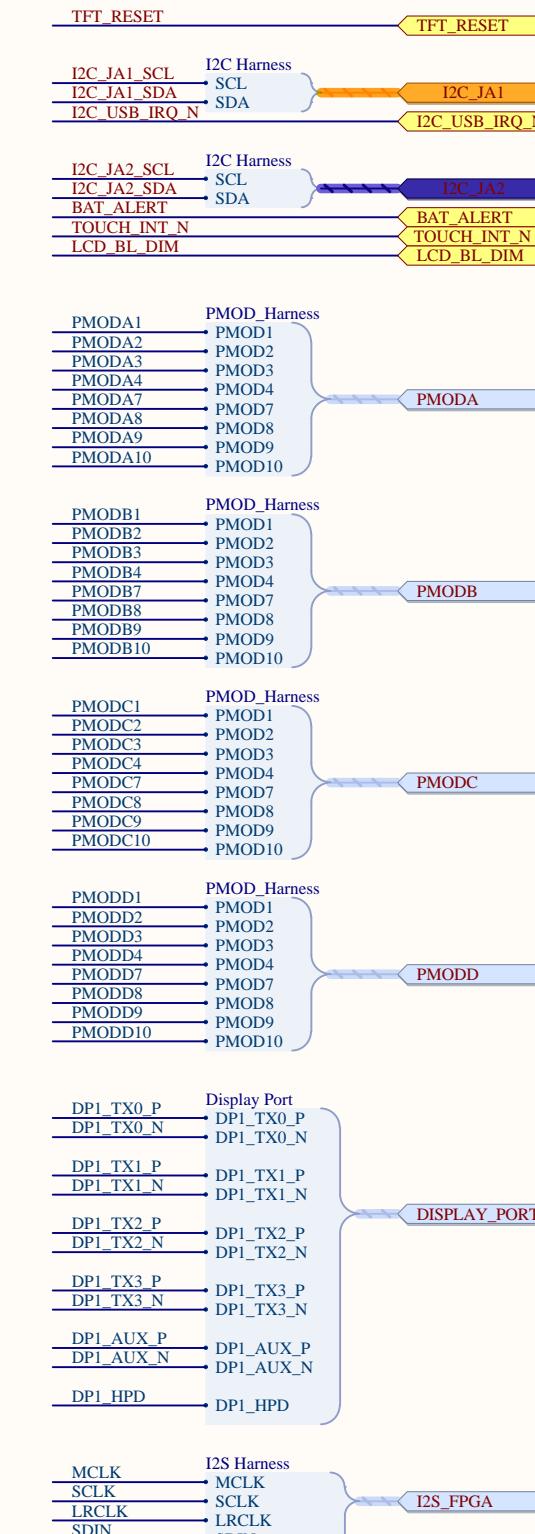
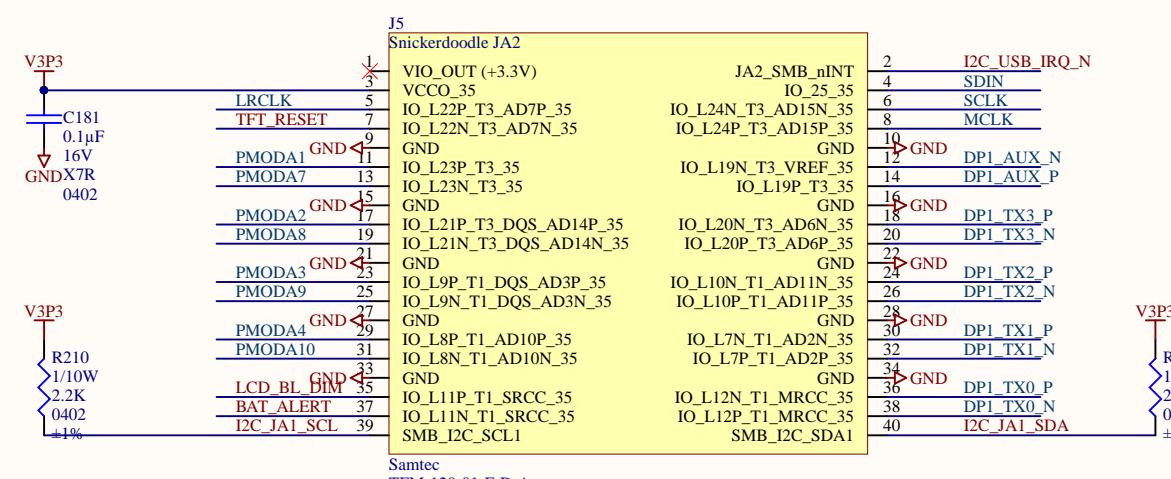
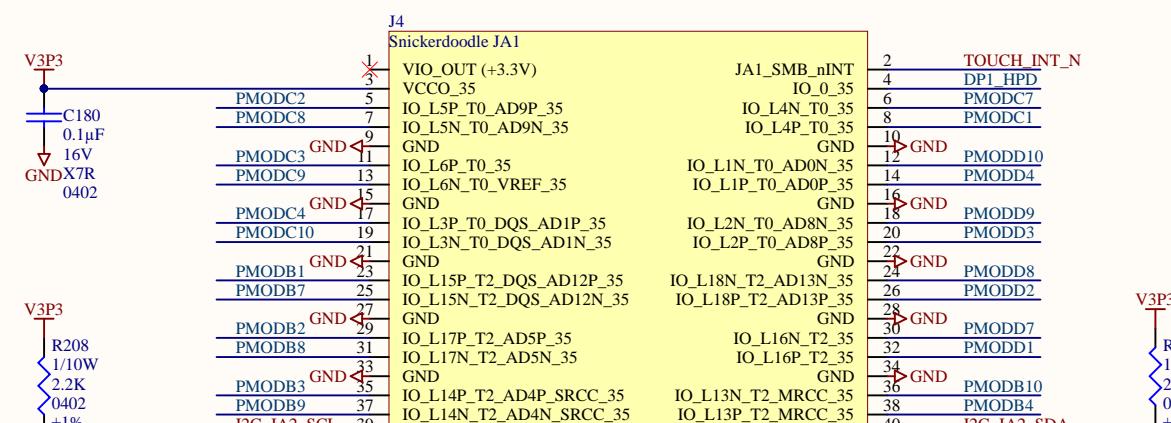
A



Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle PS	
Document:	Snickerdoodle PS.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	
Date:	9/21/2017	Revision: A
Number:	3	of 20



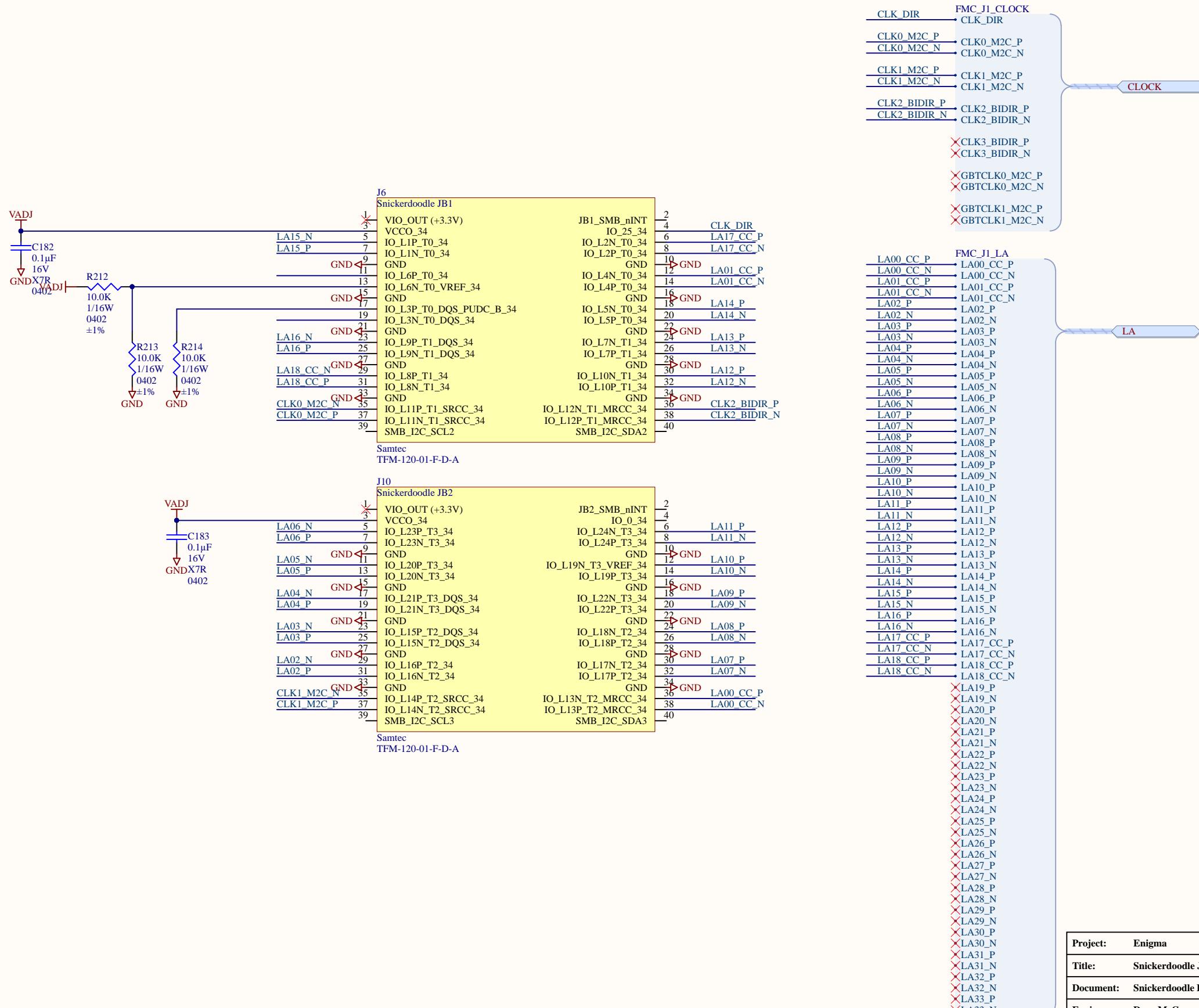
Do I need external differential termination like on the Spartan 6 FPGAs?



Do I need parallel termination of the Display Port Signals??

Project:	Enigma	Cospan Design
Title:	Snickerdoodle JA	http://www.cospandesign.com
Document:	Snickerdoodle FPGA JA.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 4 of 20



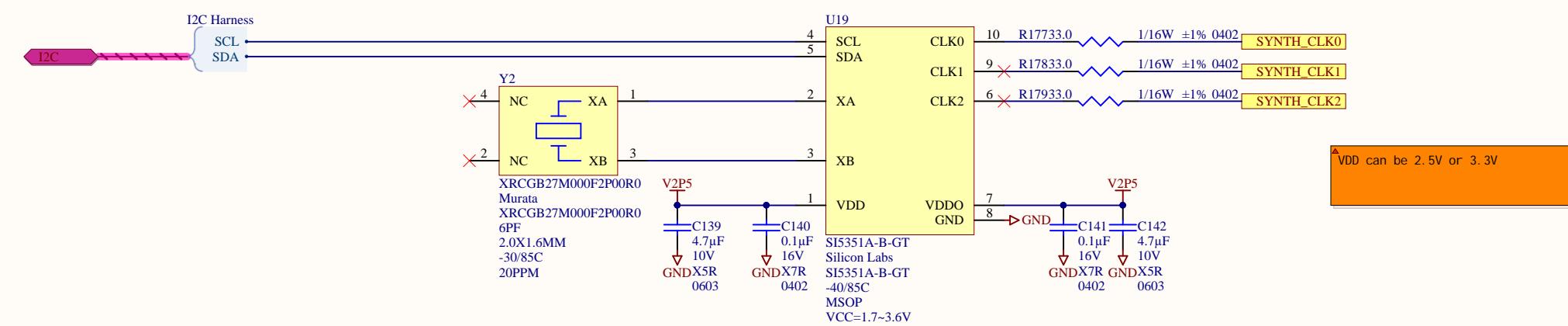


Project:	Enigma			Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle JB			
Document:	Snickerdoodle FPGA JB.SchDoc			
Engineer:	Dave McCoy			
Client:	Public			
Approved By:	NA	Revision:	A	
Date:	9/21/2017	Number:	5	of 20



A

A



B

B

C

C

D

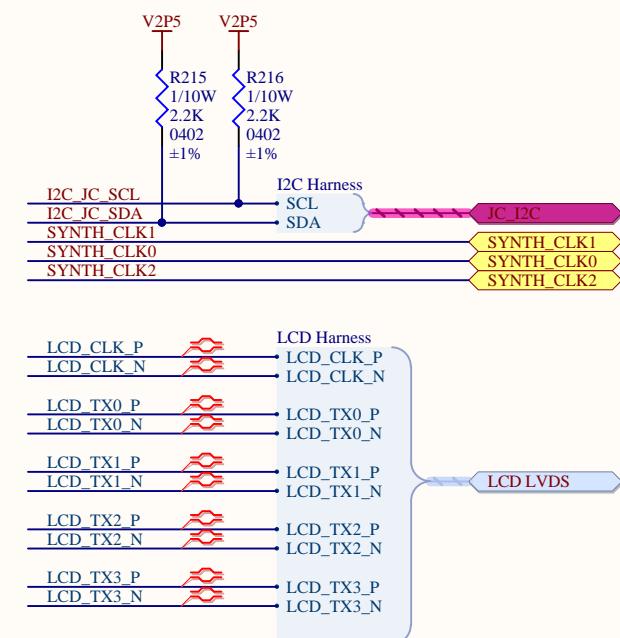
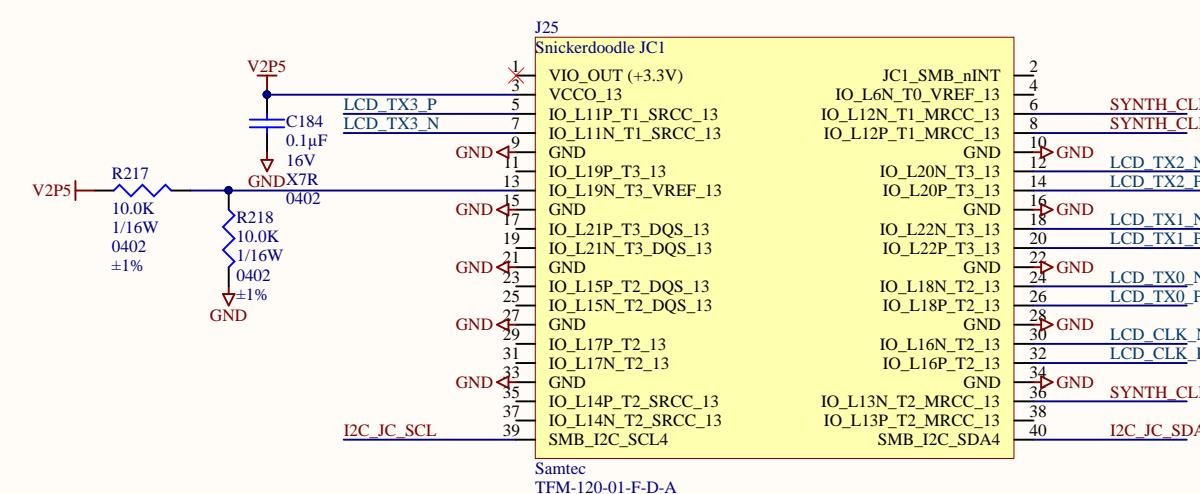
D

Project:	Project_Name	Cospan Design http://www.cospandesign.com
Title:	Clock Synthesizer	
Document:	Clock Synth.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: Rev
Date:	9/21/2017	Number: 6 of 20



A

Should I use VREF??



B

C

D

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle JC	
Document:	Snickerdoodle FPGA JC.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 7 of 20



A

A

B

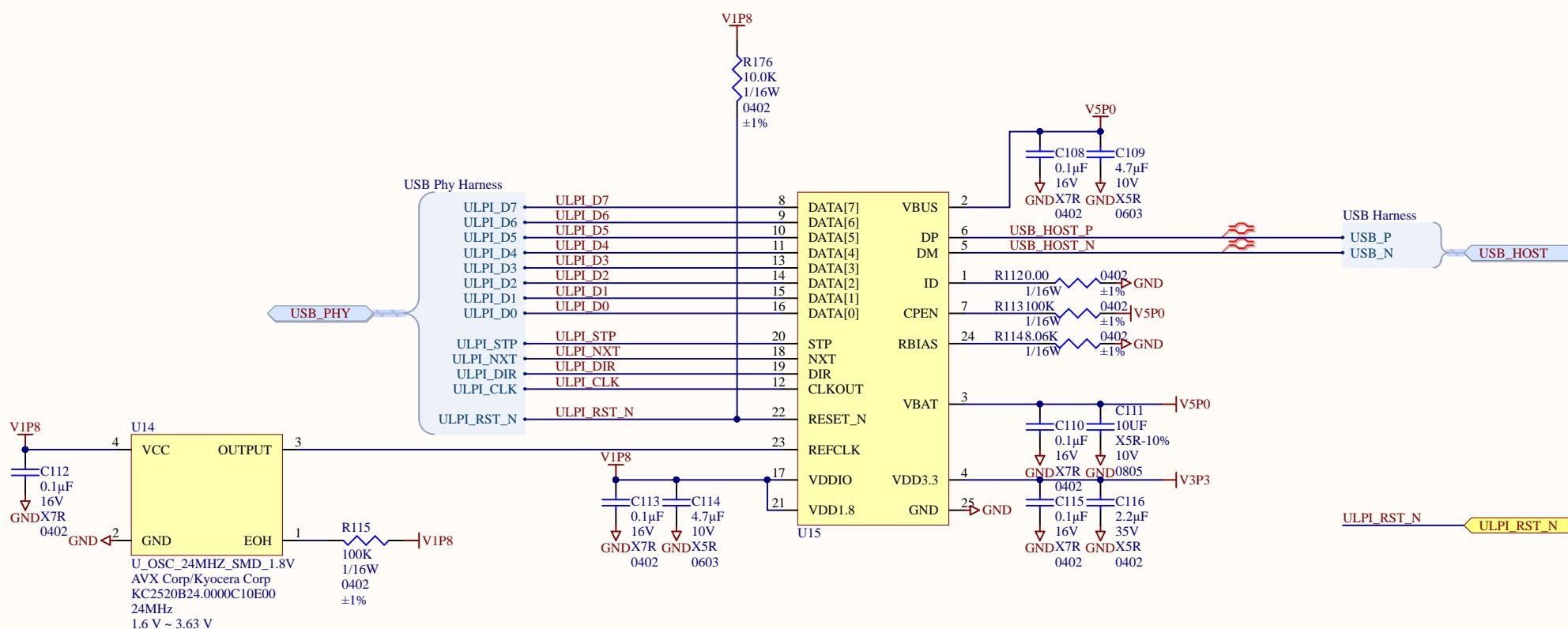
B

C

C

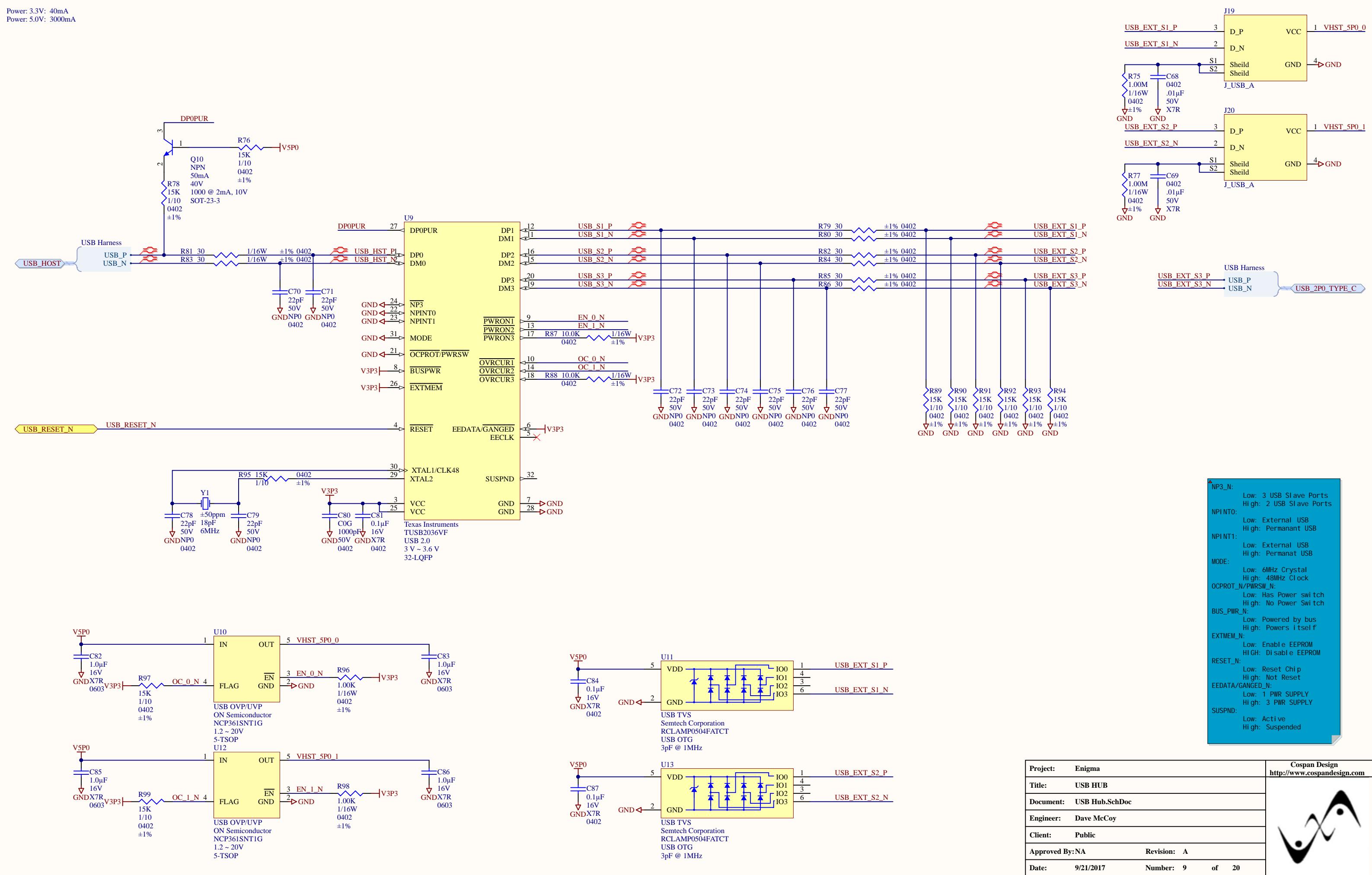
D

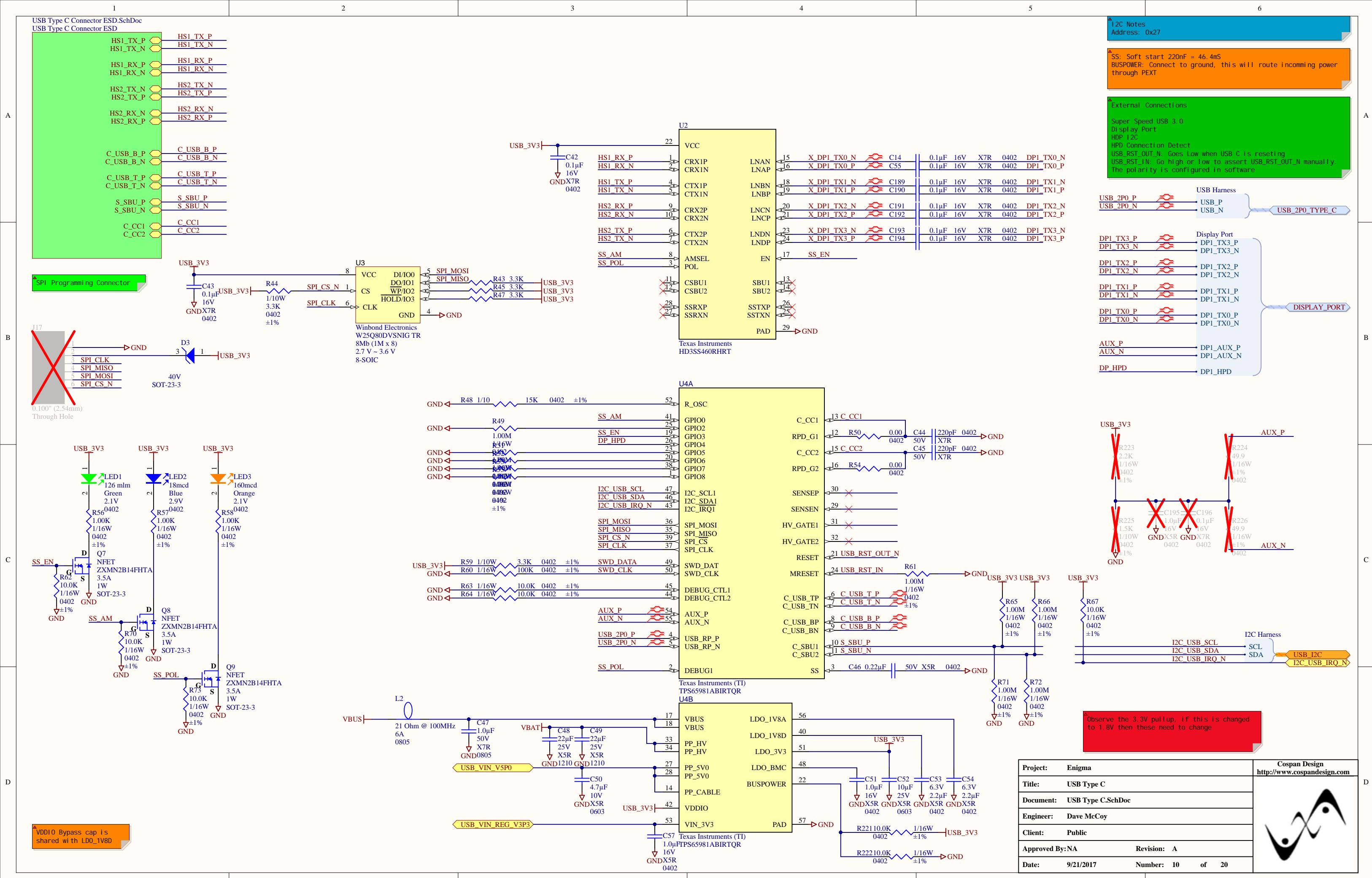
D

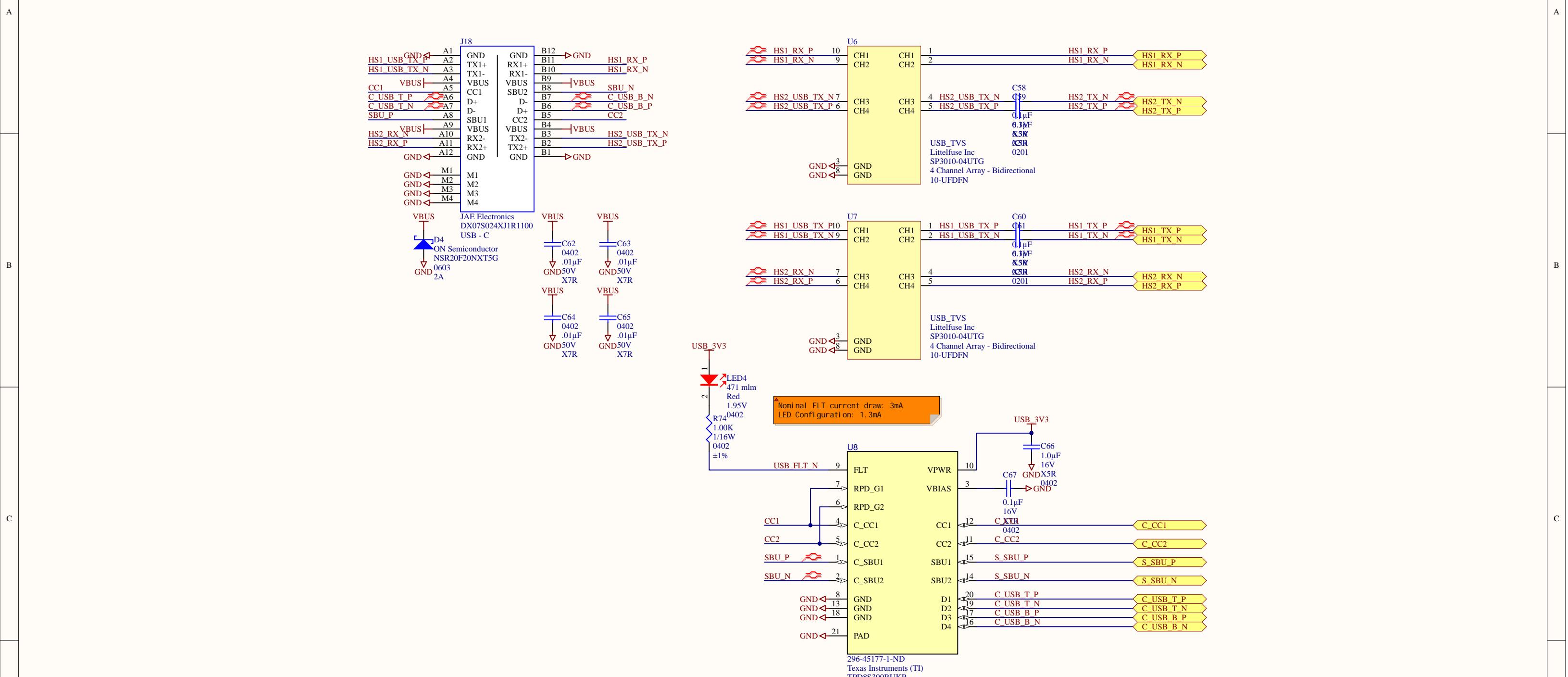


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	USB Phy	
Document:	USB Phy.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 8 of 20



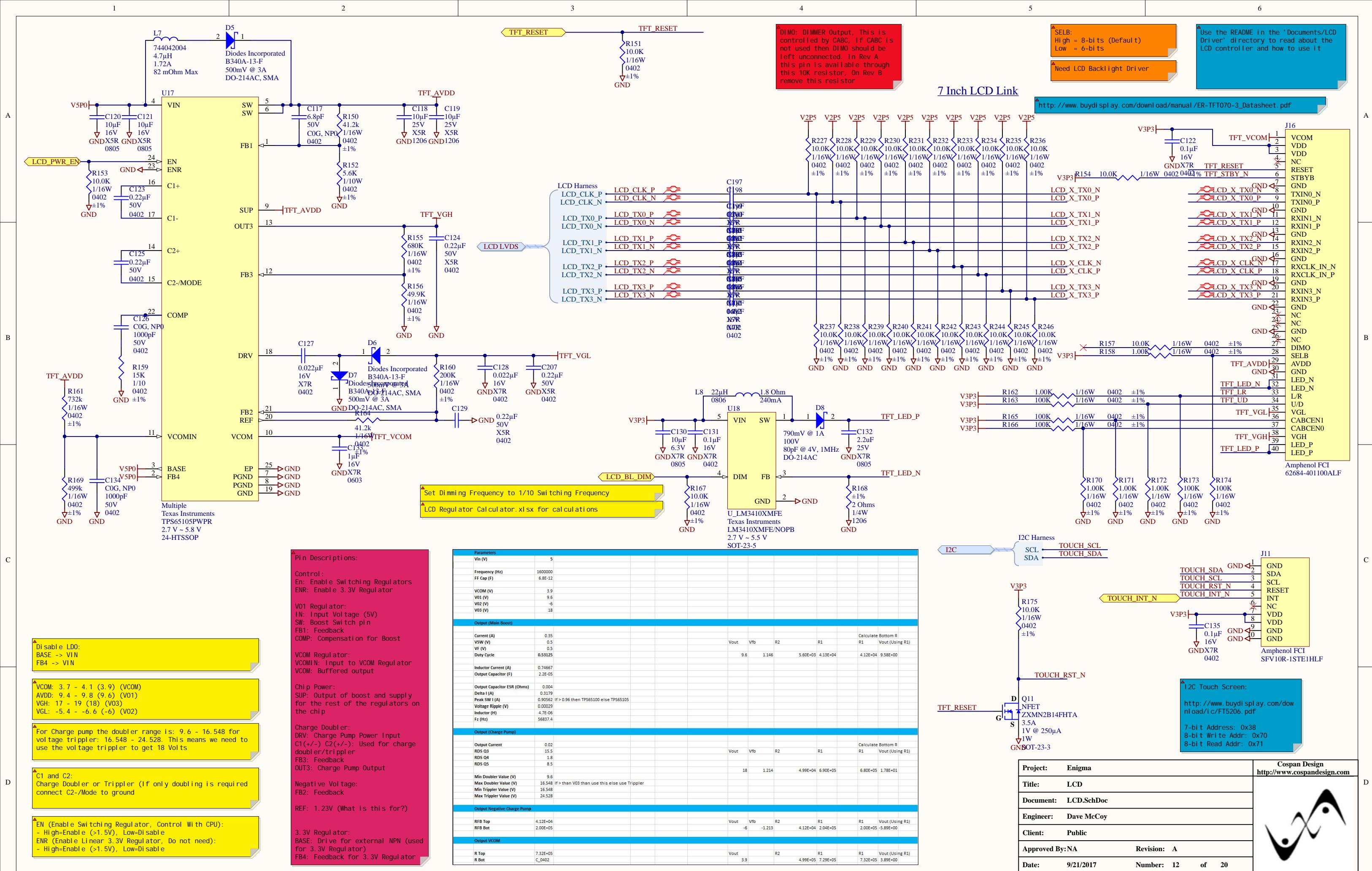




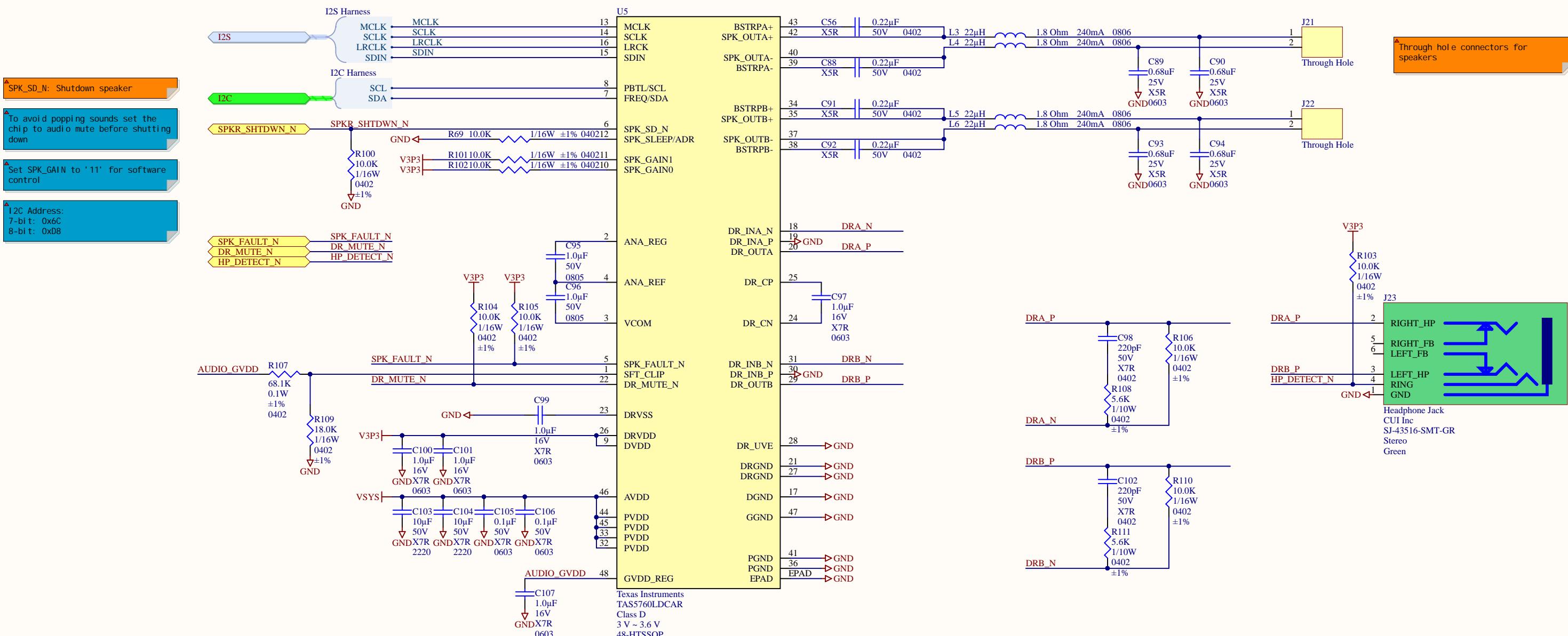


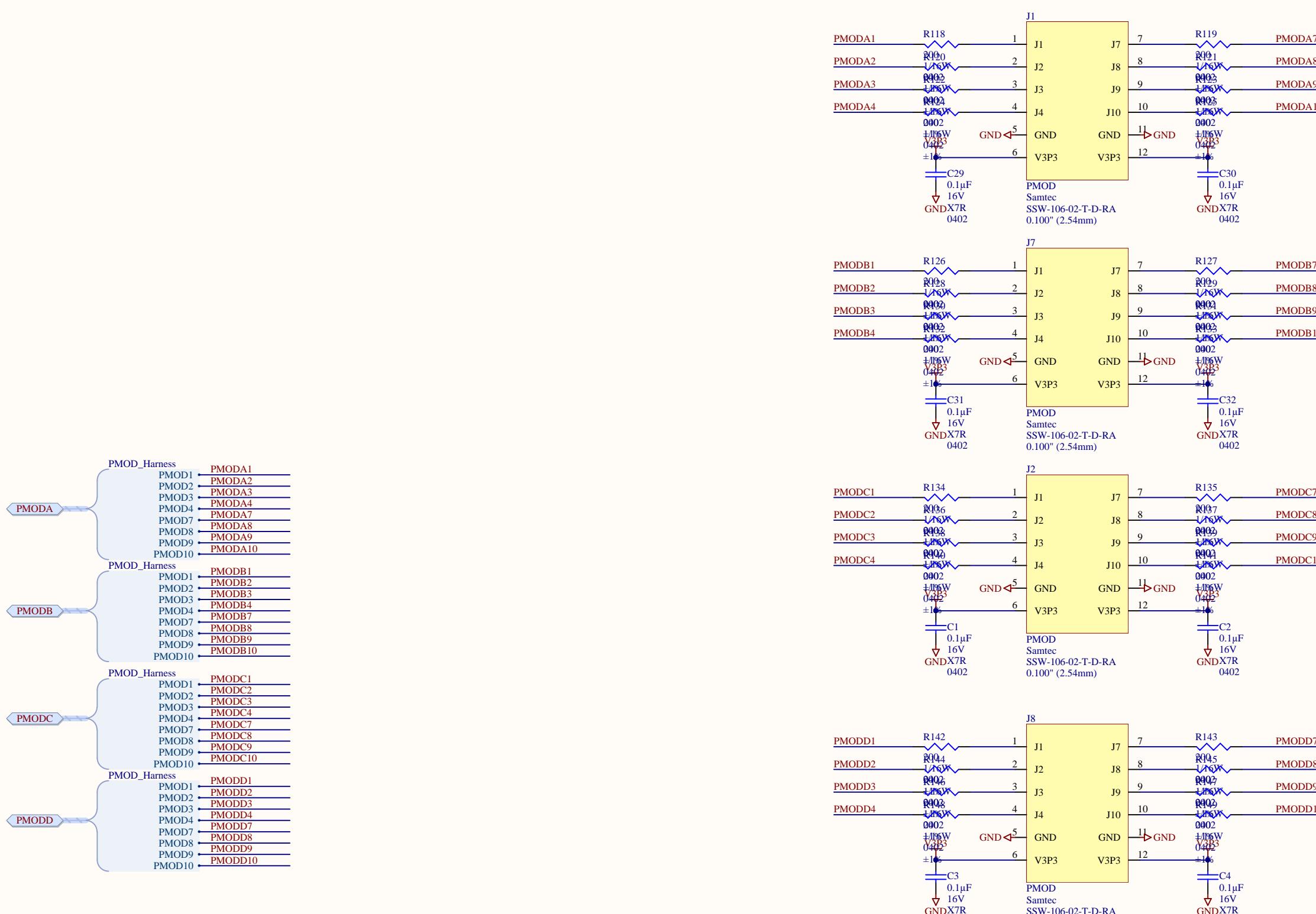
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	USB Type C Connector	
Document:	USB Type C Connector ESD.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 11 of 20





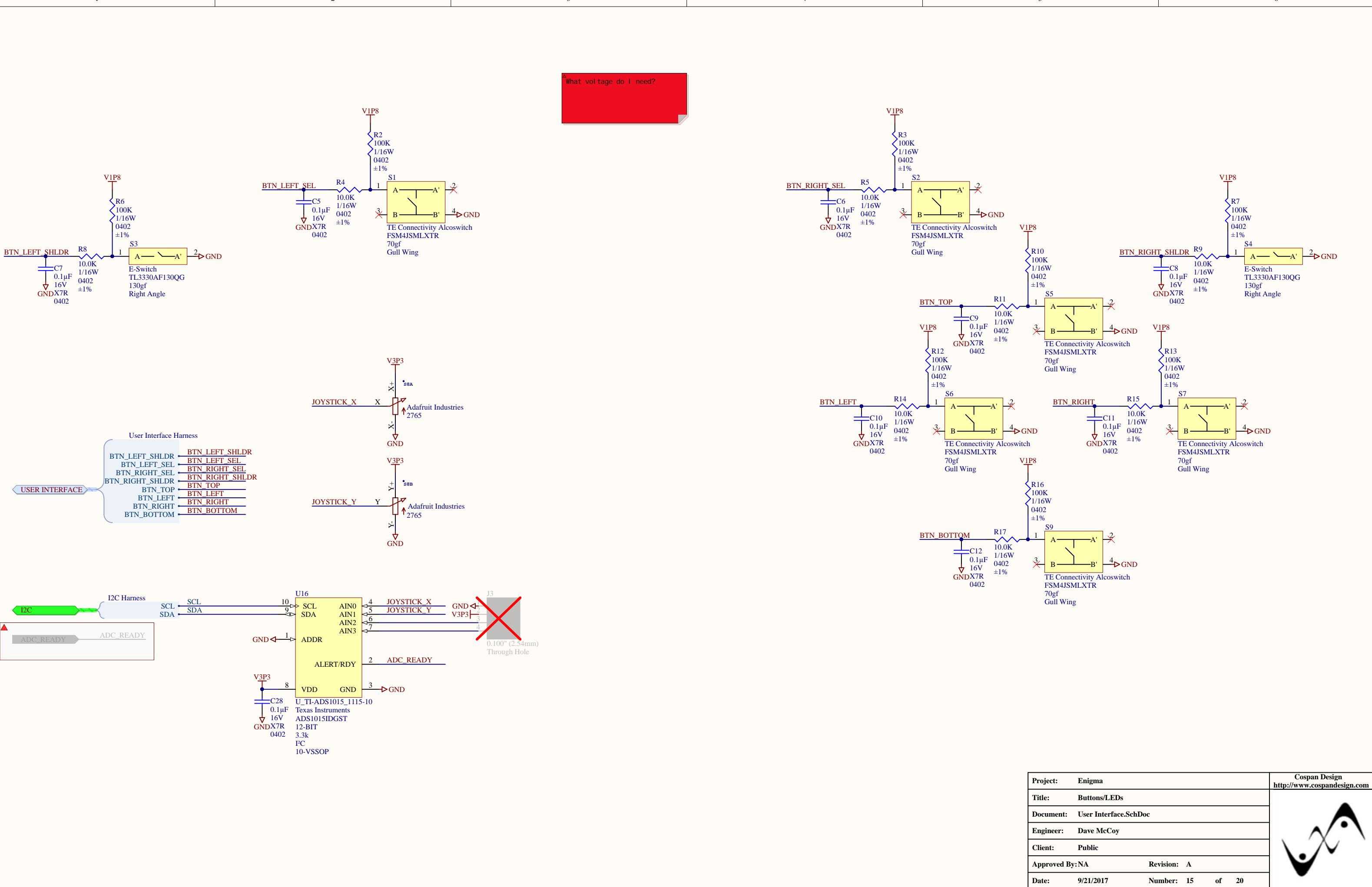
A

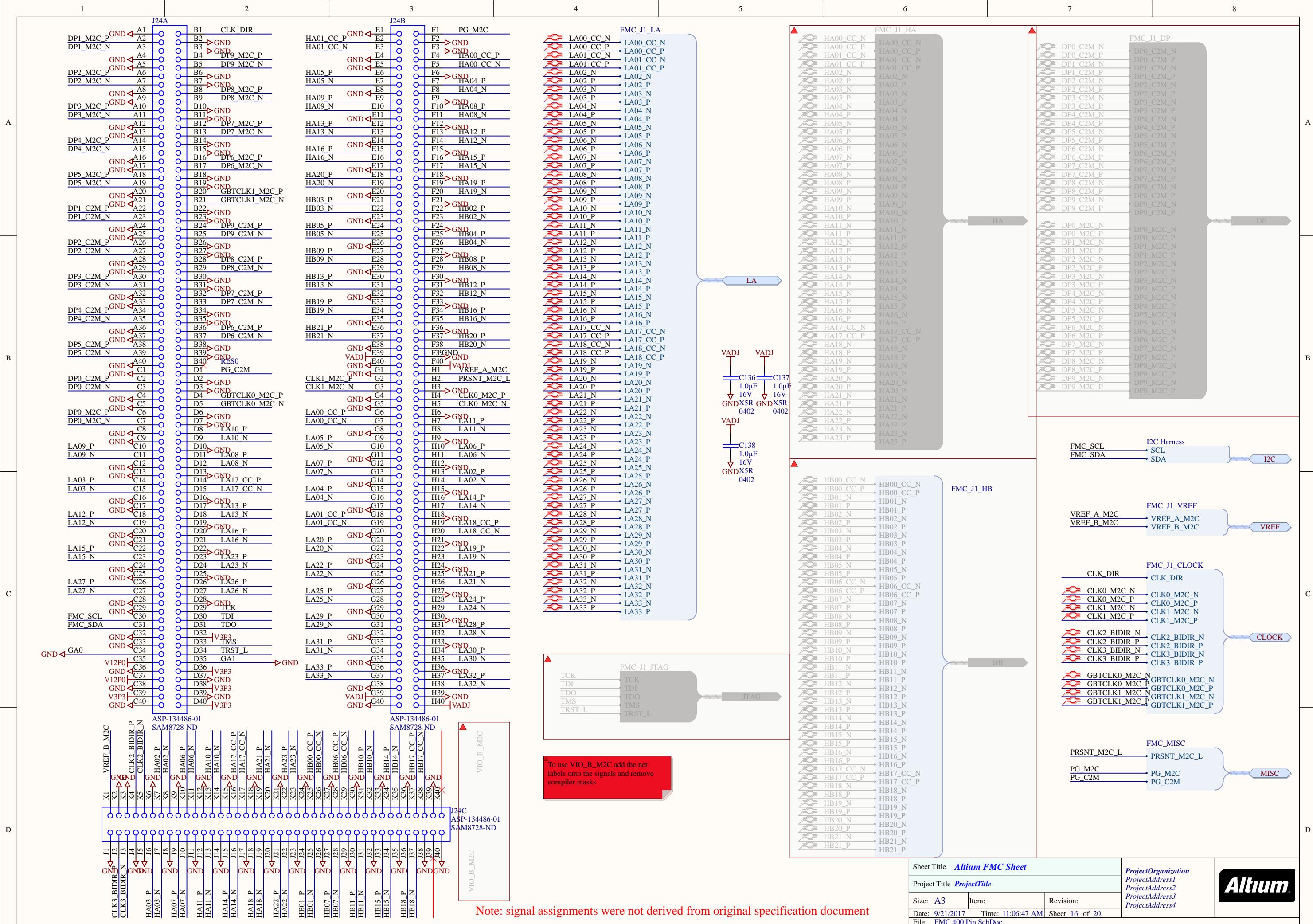


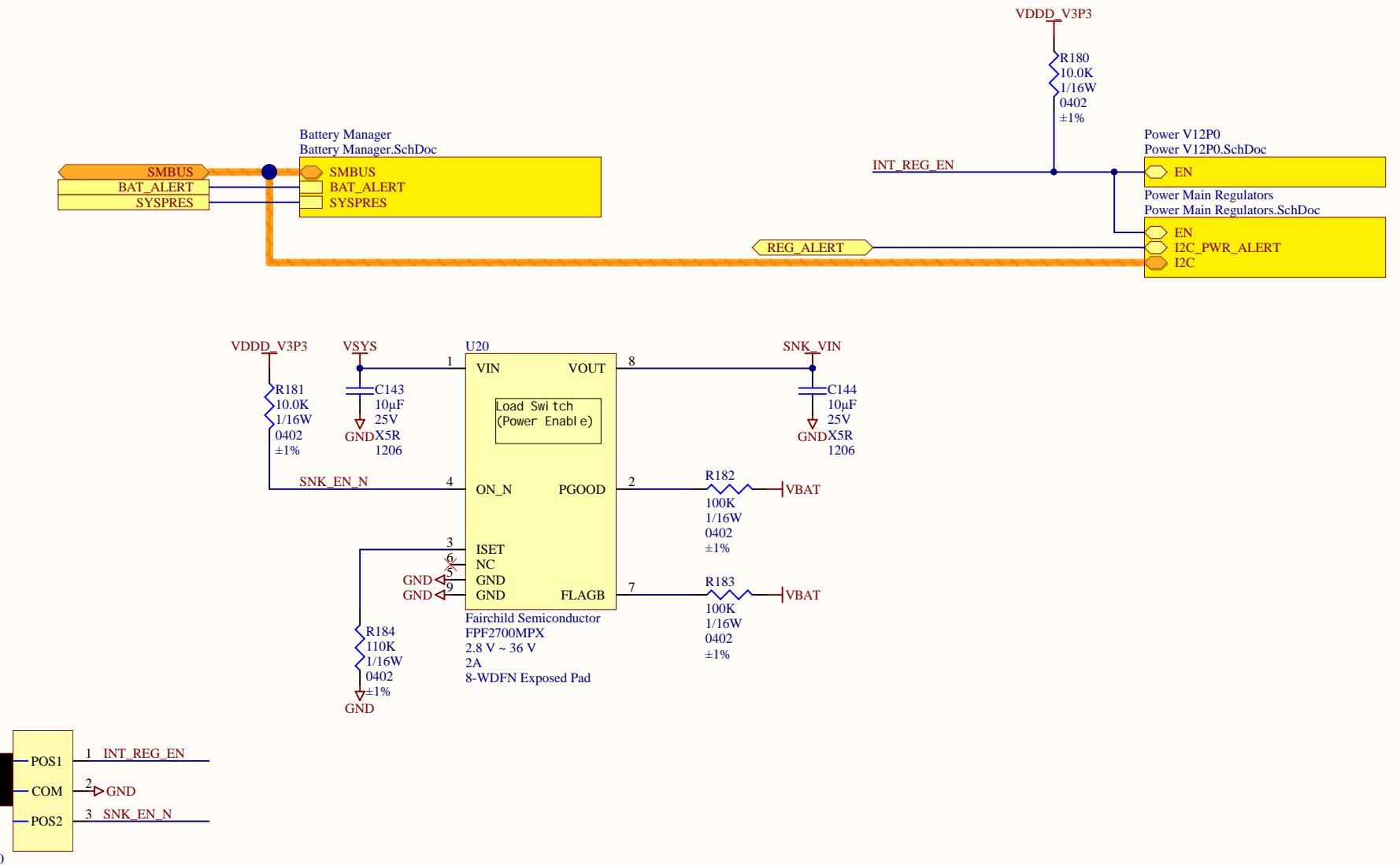


Title:	Low Speed Expansion	Cospan Design http://www.cospandesign.com
Project:	Enigma	
Document:	Arduino and PMOD Connectors.SchDoc	
Engineer:	Eng	
Drawn By:	Draw	
Revision:	Rev	
Date:	7/17/2014	Number: 14 of 20

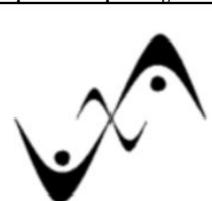








Project:	Enigma	Cospan Design
Title:	Power	http://www.cospandesign.com
Document:	Power.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/20/2017	Number: 17 of 20



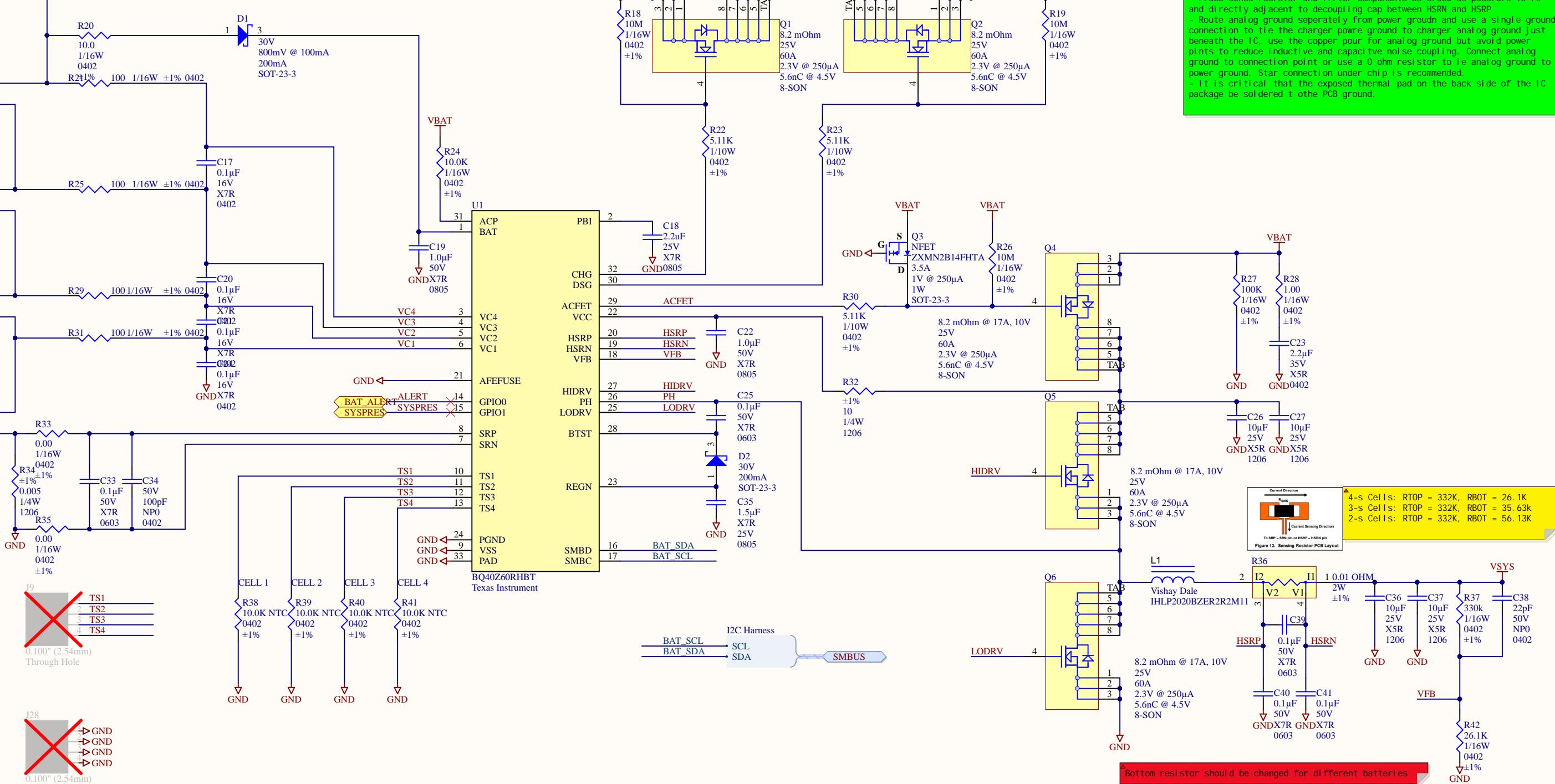
▲ GPI00 (ALERT): Alert output to host (Open Drain)
 ▲ GPI01 (SYS PRES): System presence indicator (weak pull up)
 ▲ Max Charge Current: 3A (We can't do more because the inductor would be oversaturated if we charge with more)
 ▲ VFB: 1.22V
 ▲ AFEFUSE should be hooked up to ground when not used
 Datasheet: (9.3.2.4)

A

B

C

D



Layout Notes:
 - Input Caps should be close to the switching FETs supply and ground connections, use the shortest possible copper trace connection. Caps should be on the same layer as the FETs. Vias connecting adapter and FET should be placed between caps and FET.
 - IC should be placed close to the switching FET gate pins to keep the gate-drive signal traces short. IC can be on the other side of board.
 - Inductor should be close to FET. Minimize copper area (reduce EMI) but wide enough for current. Do not use multiple layer for this connection.
 - Charge current sense resistor should be next to inductor, use Kelvin routing.
 - Place output cap next to sense resistor.
 - Output cap ground connection must be tied to the same copper that connects input cap to ground before connecting to system ground.
 - Place sense resistor and filter components as close as possible to IC and directly adjacent to decoupling cap between HSRN and HSRP.
 - Route analog ground separately from power ground and use a single ground connection to tie the charger power ground to charger analog ground just beneath the IC, use the copper pour for analog ground but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to connection point or use a 0 ohm resistor to tie analog ground to power ground. Star connection under chip is recommended.
 - It is critical that the exposed thermal pad on the back side of the IC package be soldered to the PCB ground.

Project:	Enigma	Cospan Design
Title:	Battery Manager	http://www.cospandesign.com
Document:	Battery Manager.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 18 of 20



A

A

B

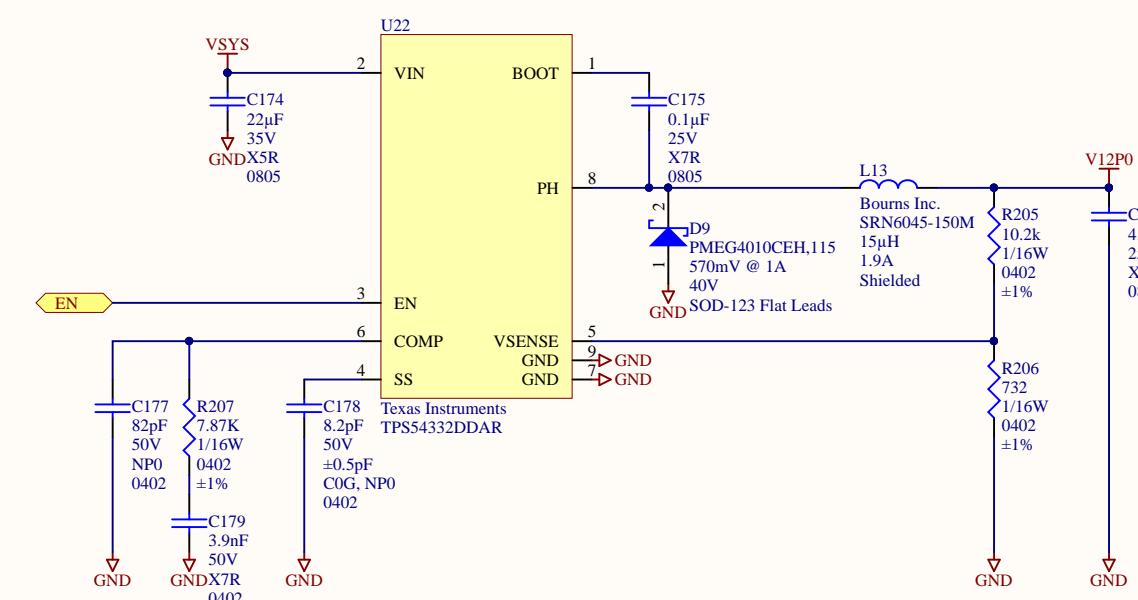
B

C

C

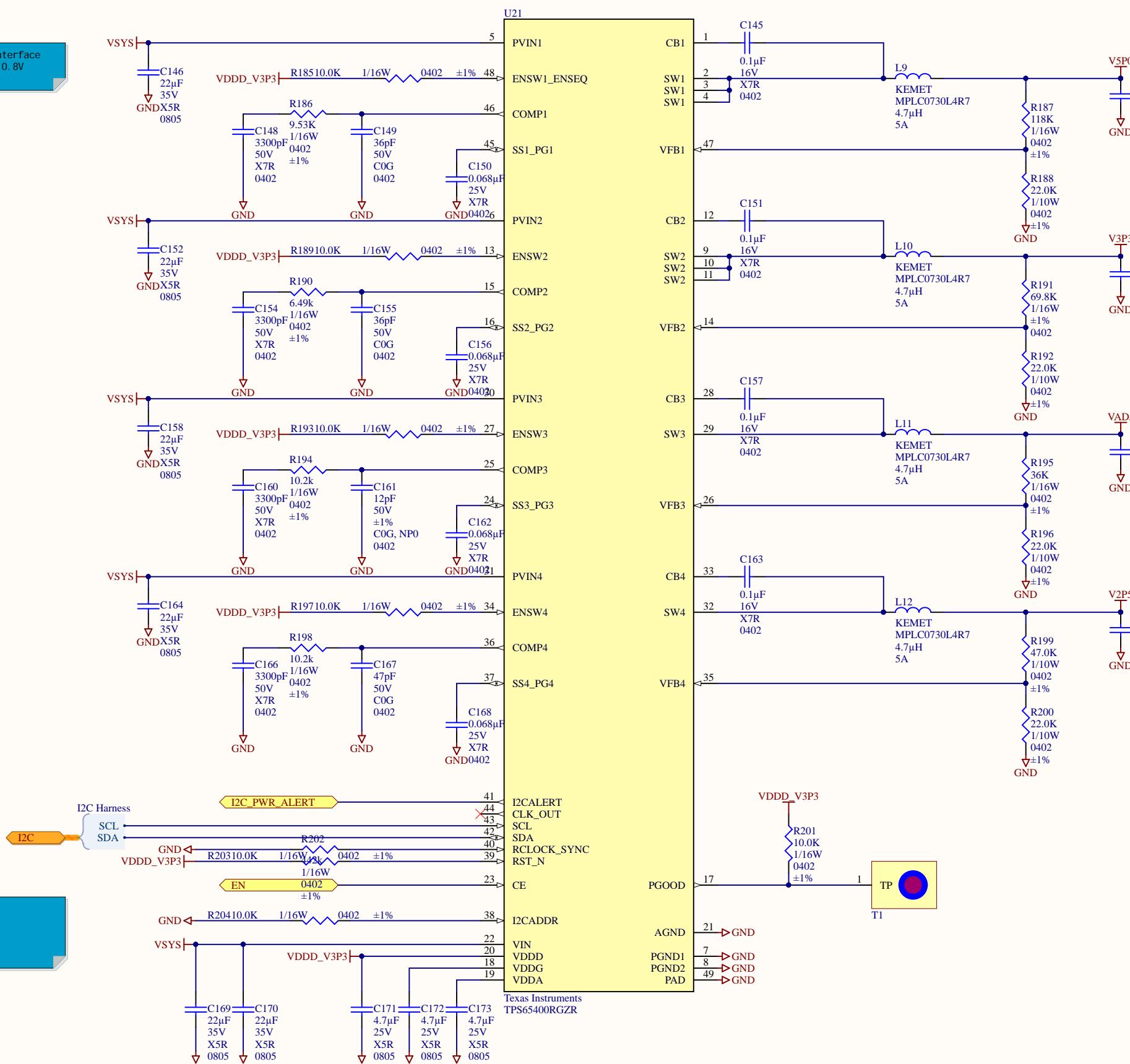
D

D



Title		
Size Tabloid	Number	Revision
Date: 9/21/2017	Sheet of	
File: C:\Users...\Power V12P0.SchDoc	Drawn By:	

All VFB can be changed through the I2C interface from 0.6 to 1.87 with a default value of 0.8V



I2C Slave Address:
Write: 0xD2
Read: 0x03
7-bit address: 0x69

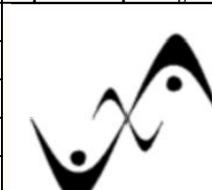
VADJ can be adjusted from 1.8 - 3.3V using I2C.
In order to change the values the VFB must be changed using the I2C bus. The following is a list of VFB values that need to be set in order to get the desired output voltage.

Output	: VFB Value
1.2V	: NA (Resistor Values will need to change)
1.8V	: 0.82V
2.5V	: 1.14V
3.3V	: 1.51V

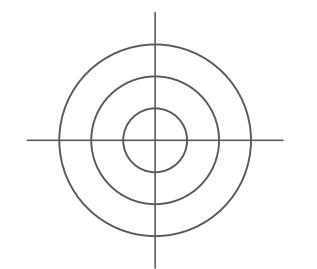
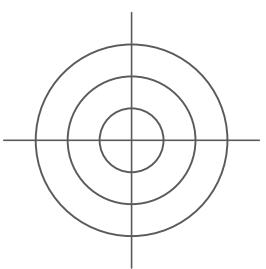
This voltage rail might need to be changed to 3.3V in order to satisfy the differential voltage requirements of the LVDS LCD interface. If so the voltage can be changed using the I2C bus for this chip.

VFB Values:	
Output	: VFB Value
2.5V	: 0.8V
3.3V	: 1.05V

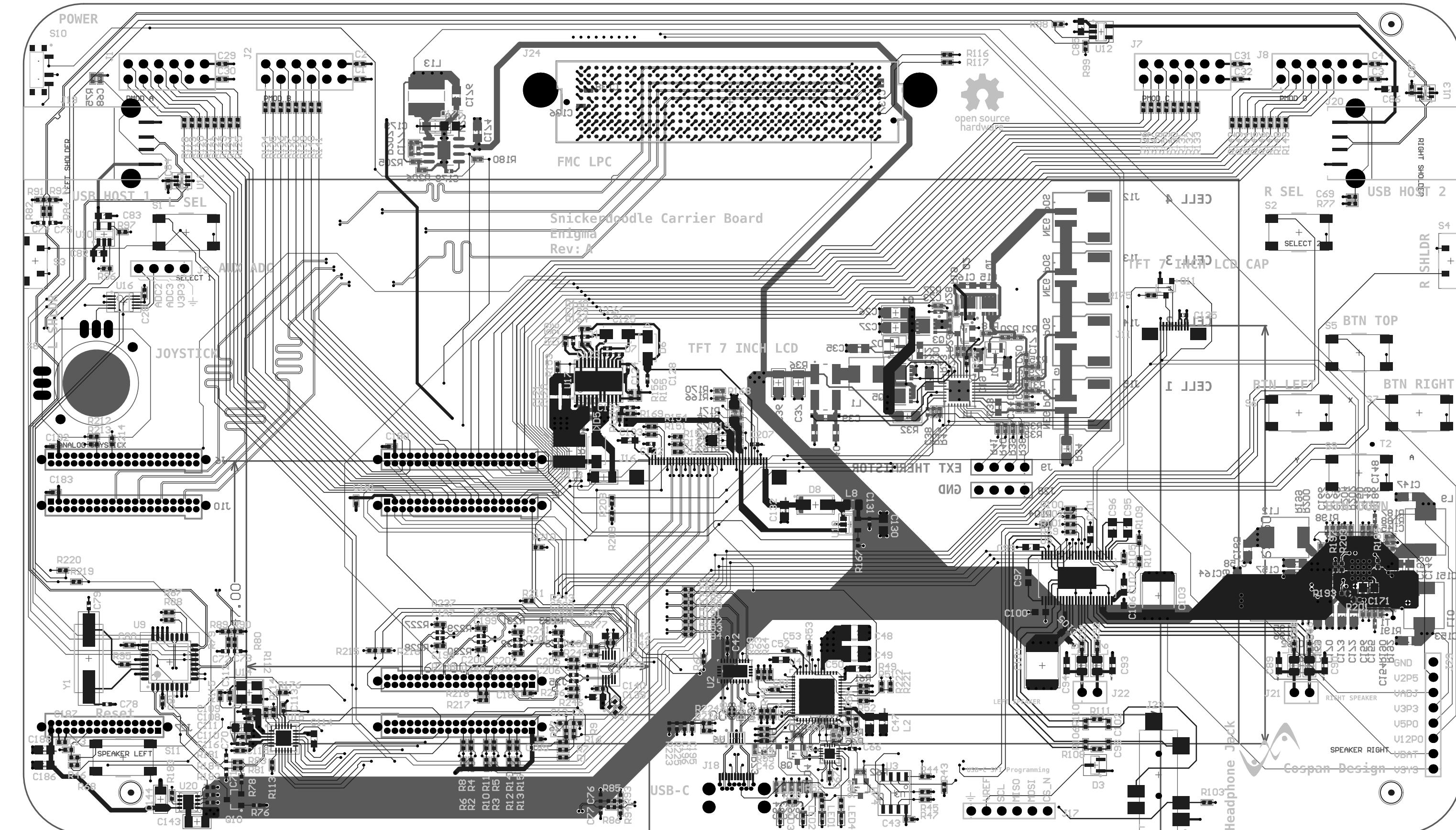
Project:	Enigma	Cospan Design
Title:	Main Regulator	http://www.cospandesign.com
Document:	Power Main Regulators.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	9/21/2017	Number: 20 of 20



D



C



Dave McCoy Cospan Design LLC

Dave McCoy

9/21/2017

Enigma

9/21/2017

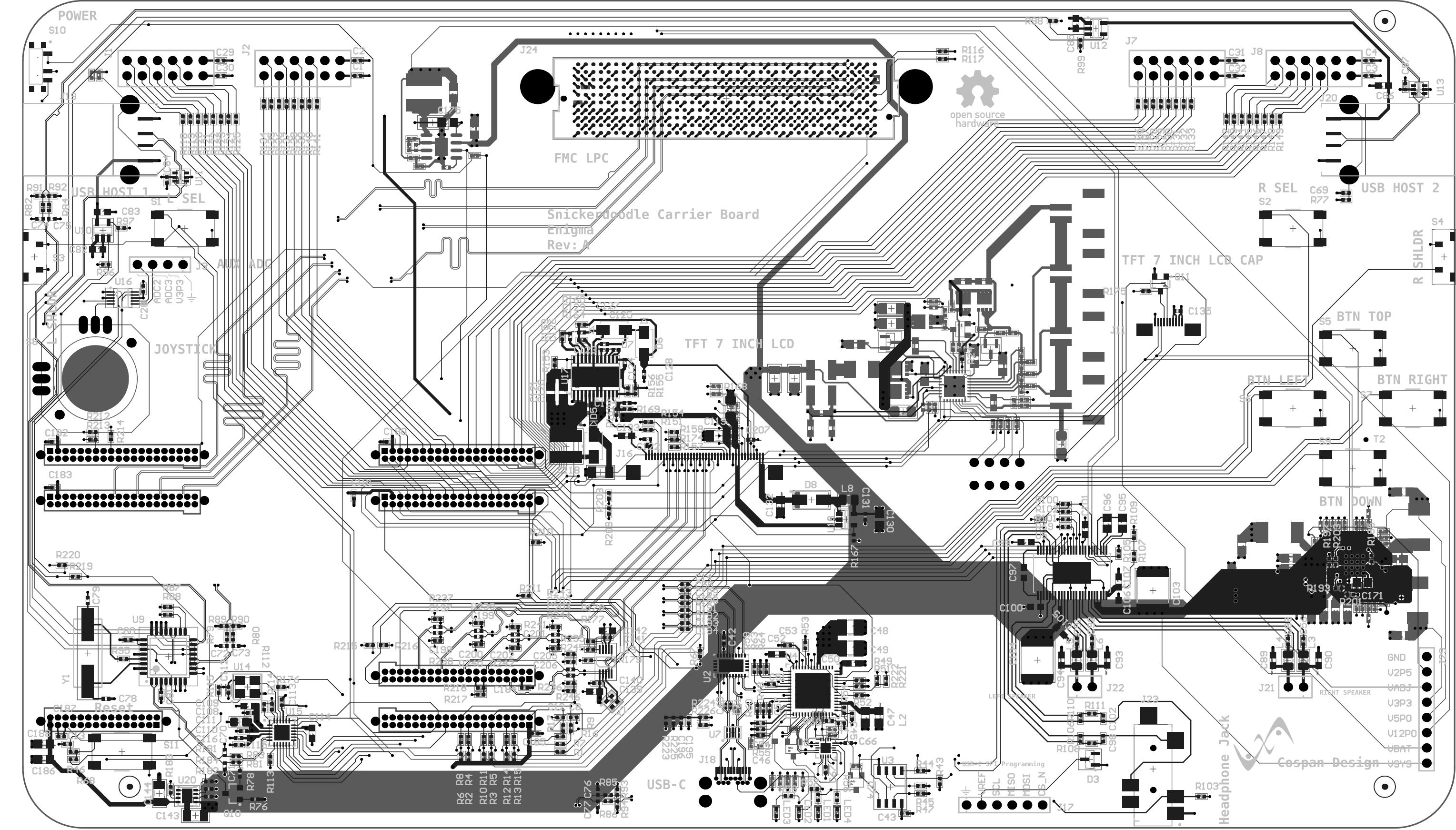
1:1 Enigma Rev A.PcbDoc

Sheet 1 of 1

GTL – TOP LAYER

GBL – BOTTOM LAYER

02 PCB BOUNDARY



MULTI-LAYER HOLES

