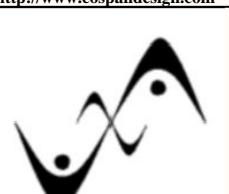
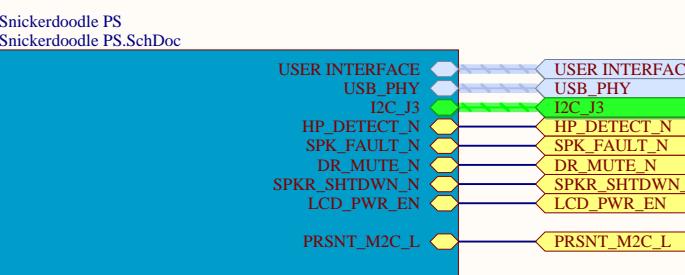


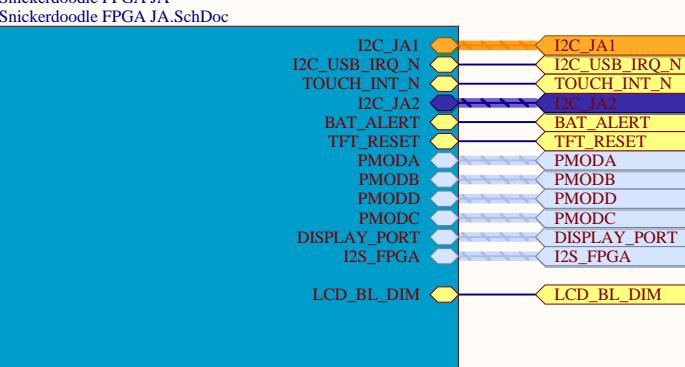
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Block Diagram.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 1 of 20



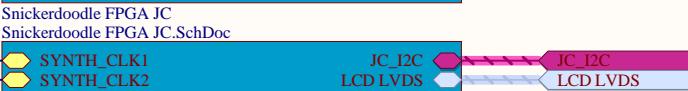
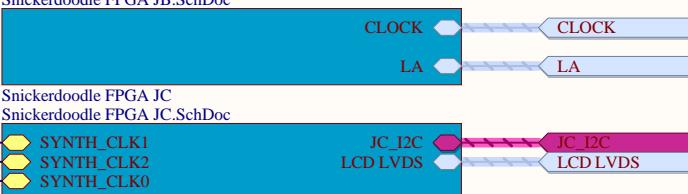
A



B



C

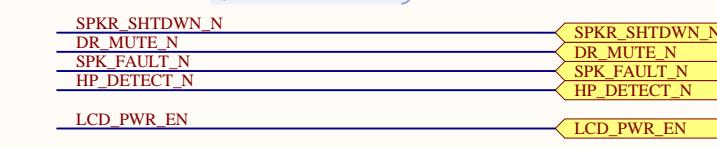
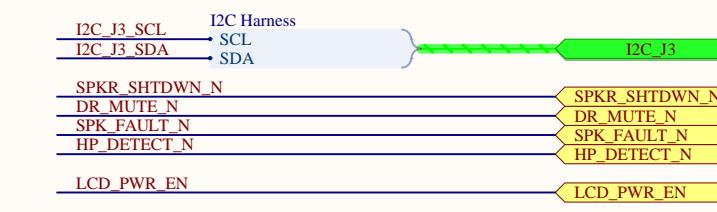
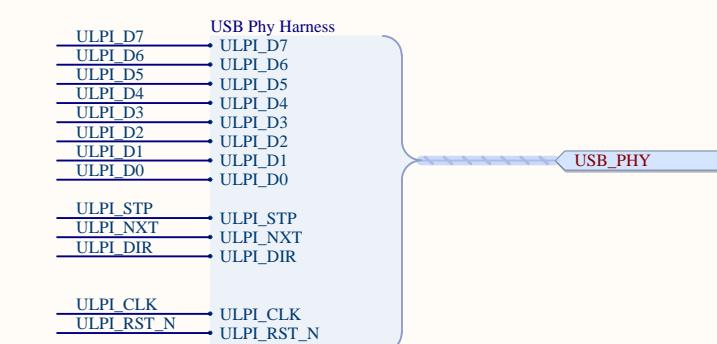
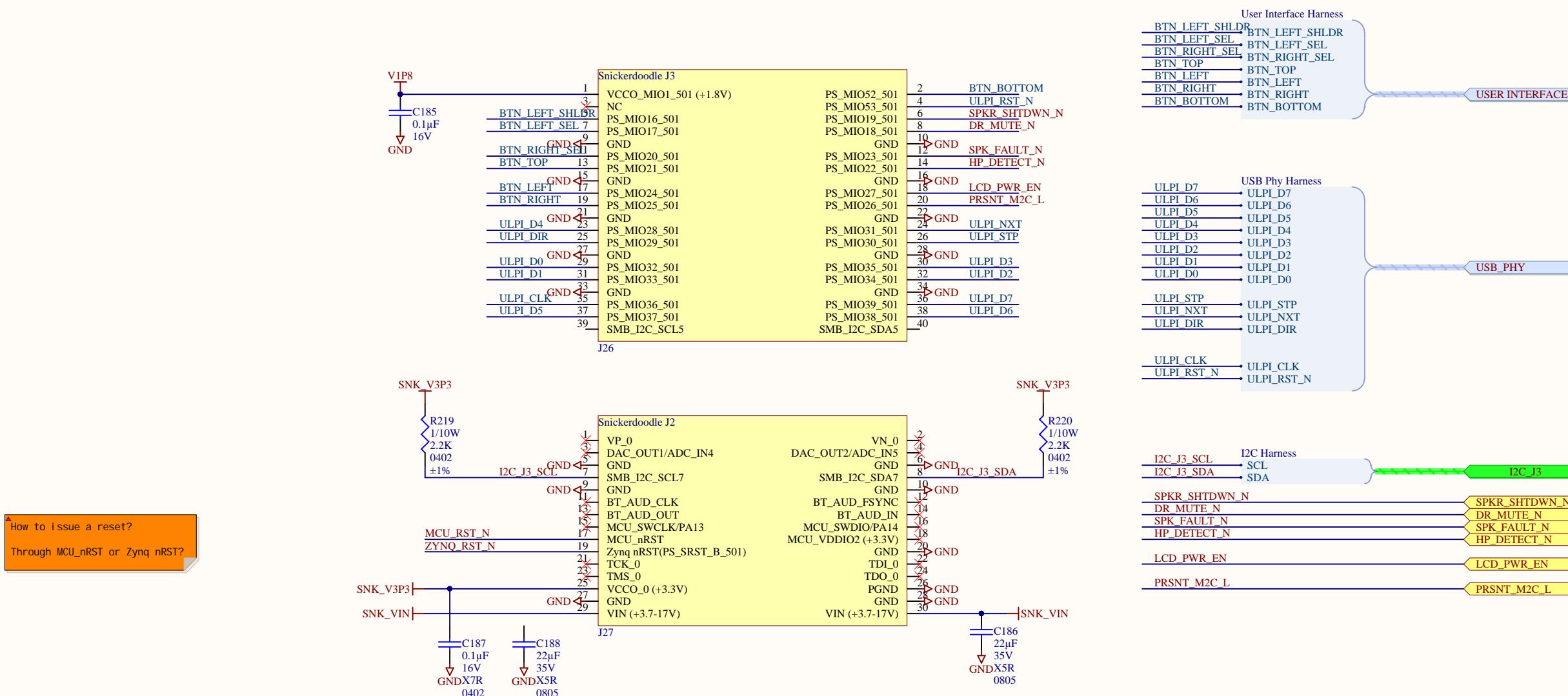


Not SnickerDoodle's Internal regulators for powering this board, but it would be good to make sure I2C is at the correct pullups

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Snickerdoodle.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 2 of 20



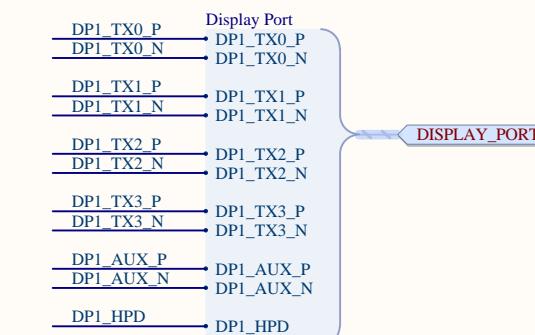
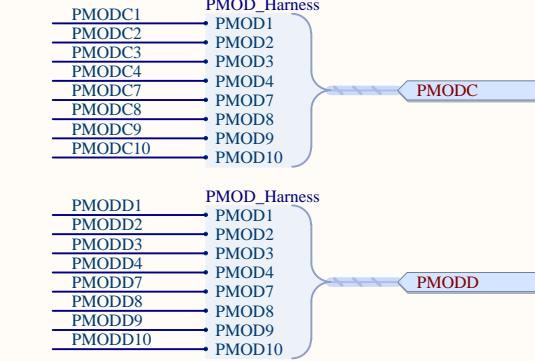
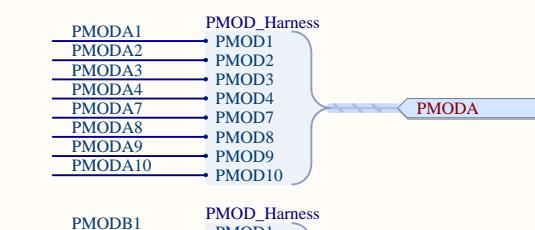
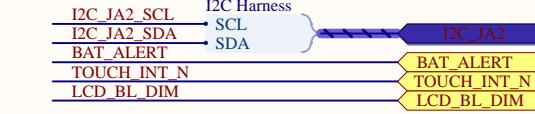
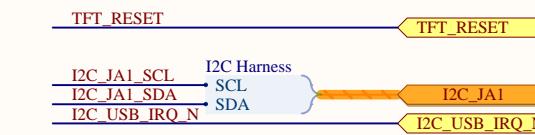
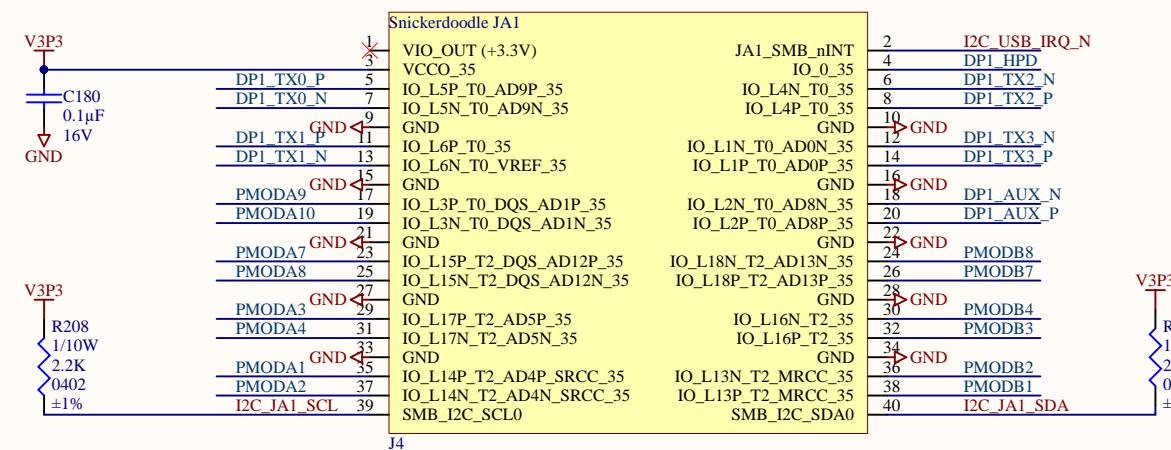
A



Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Snickerdoodle PS.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	
Revision:	*	
Date:	8/14/2017	Number: 3 of 20



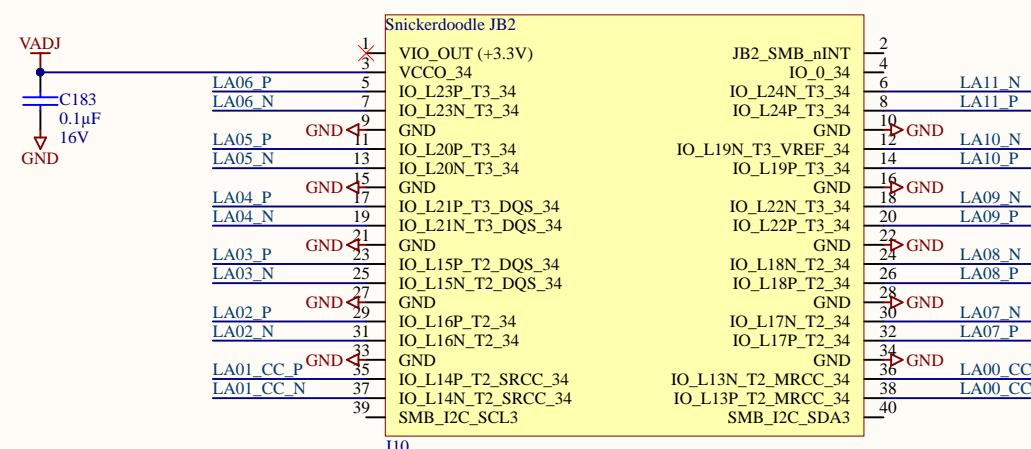
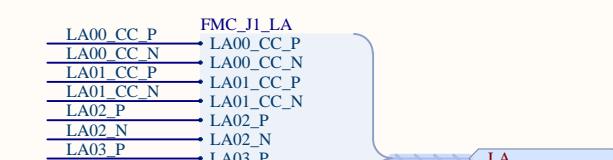
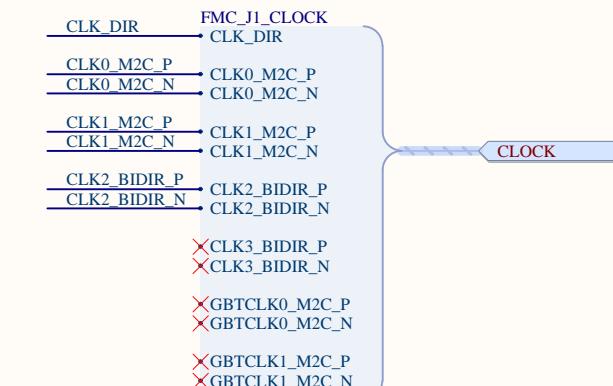
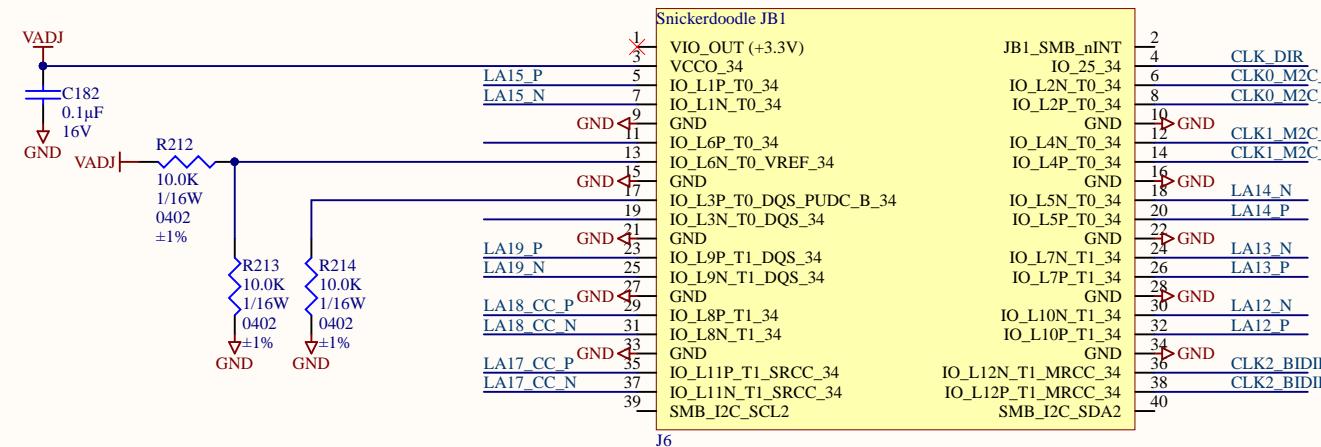
A



Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Snickerdoodle FPGA JA.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 4 of 20



A

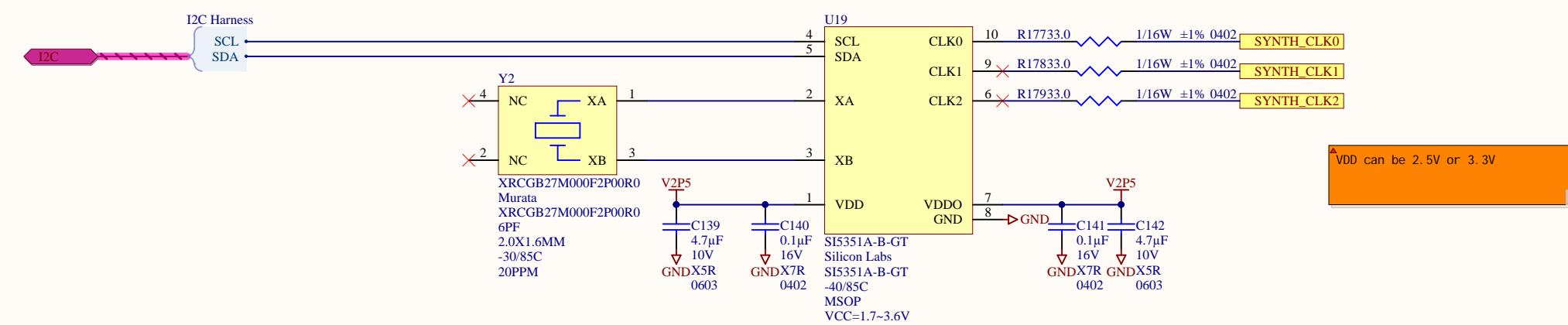


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Snickerdoodle FPGA JB.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 5 of 20



A

A



B

B

C

C

D

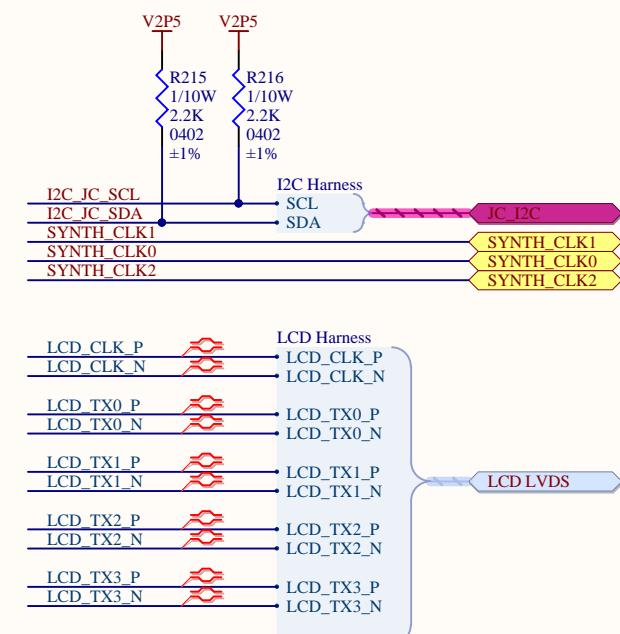
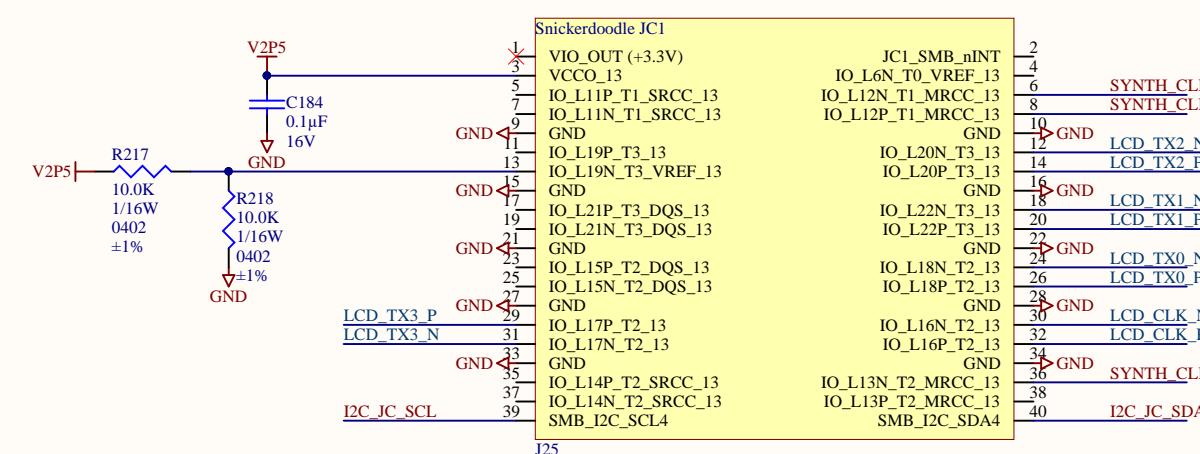
D

Project:	Project_Name	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Clock Synth.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: Rev
Date:	8/14/2017	Number: 6 of 20



A

Should I use VREF??



B

C

D

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Snickerdoodle FPGA JC.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 7 of 20



A

A

B

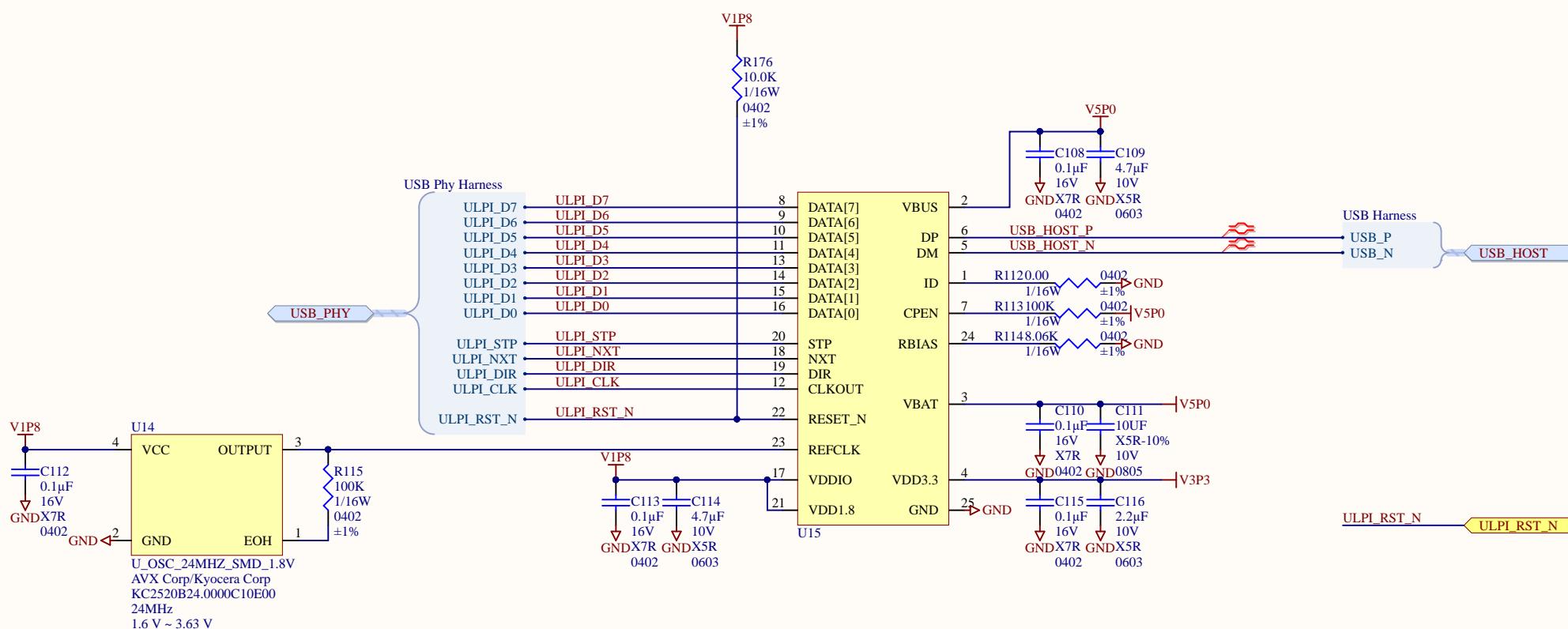
B

C

C

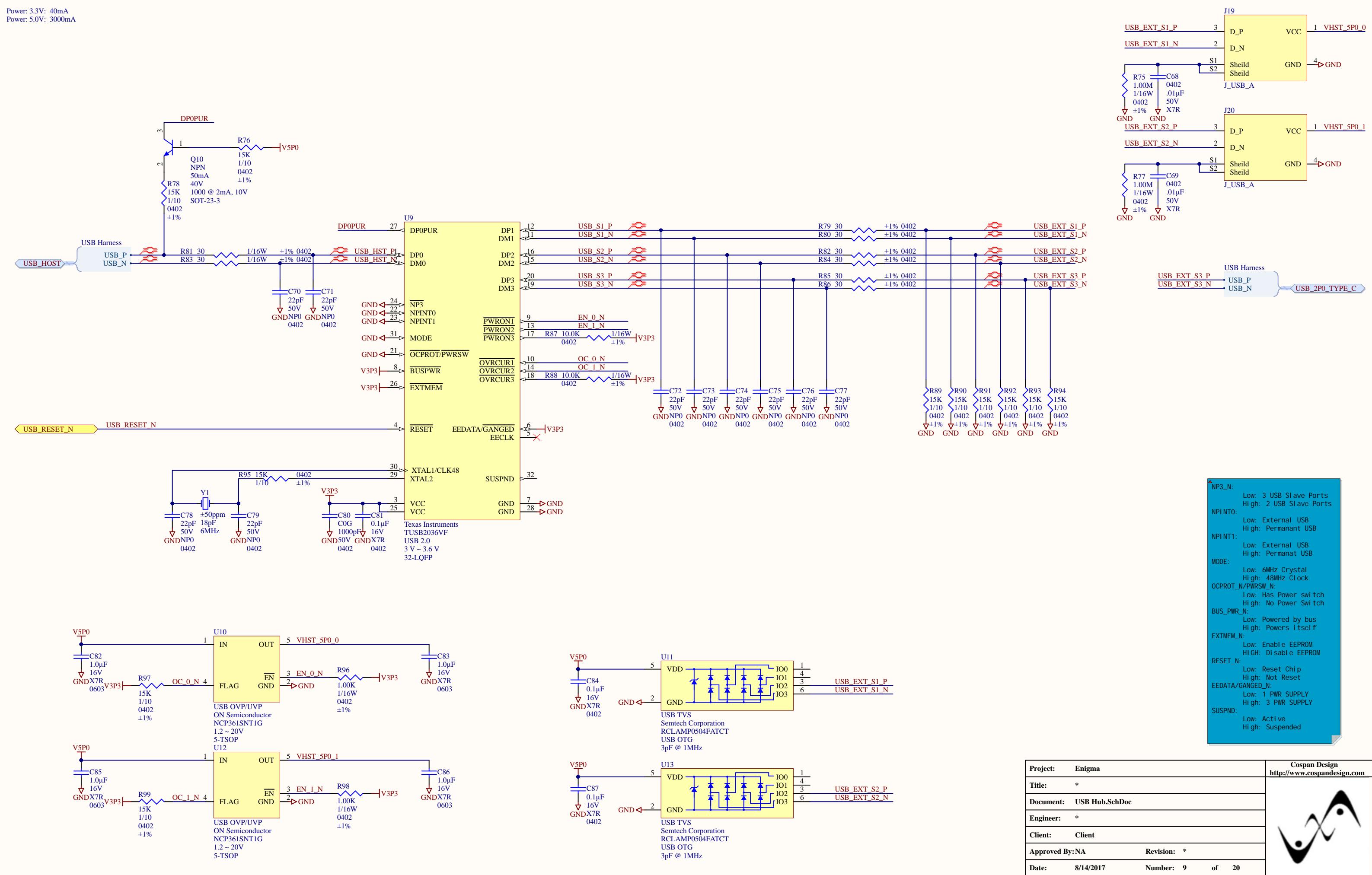
D

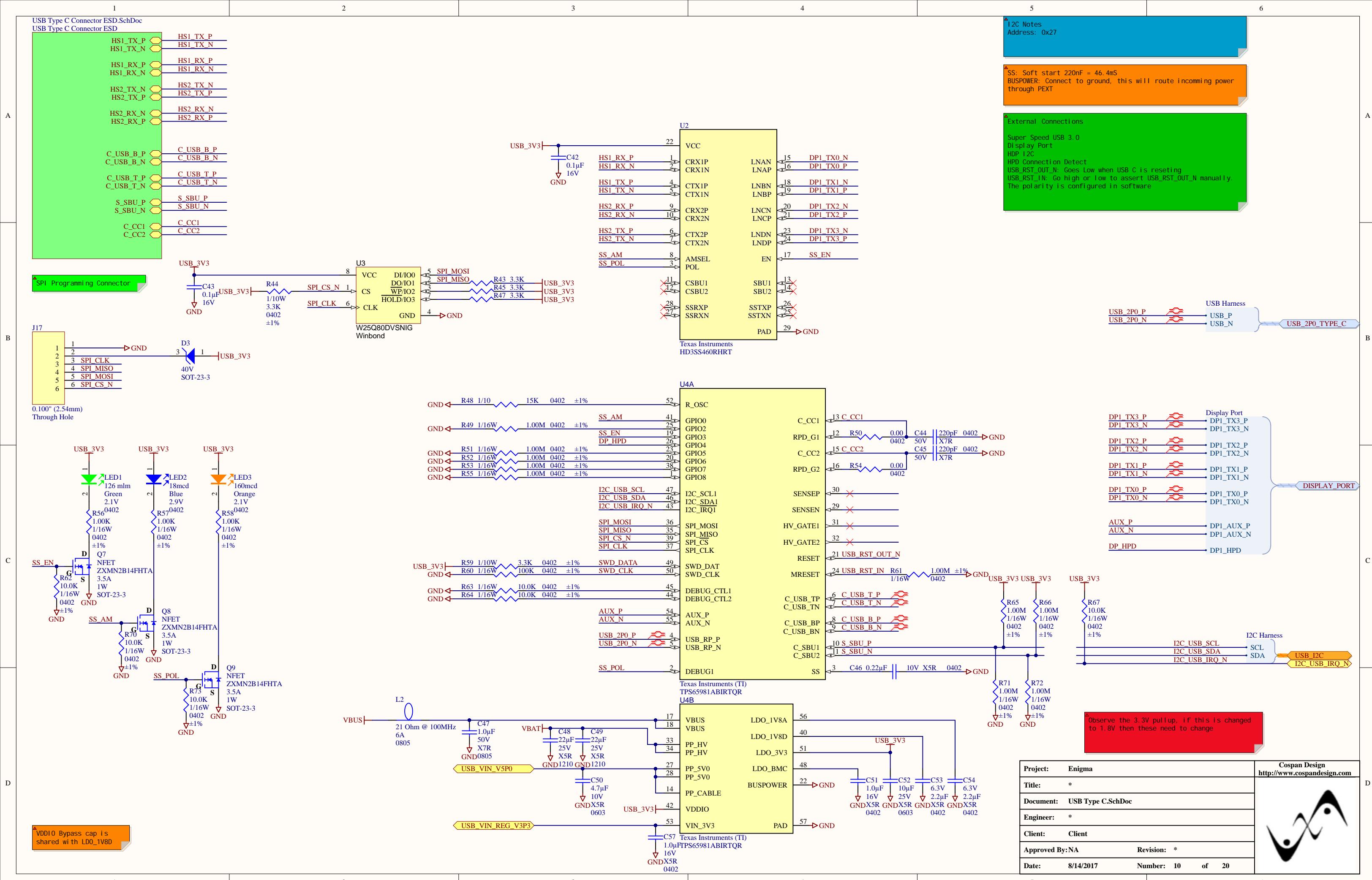
D

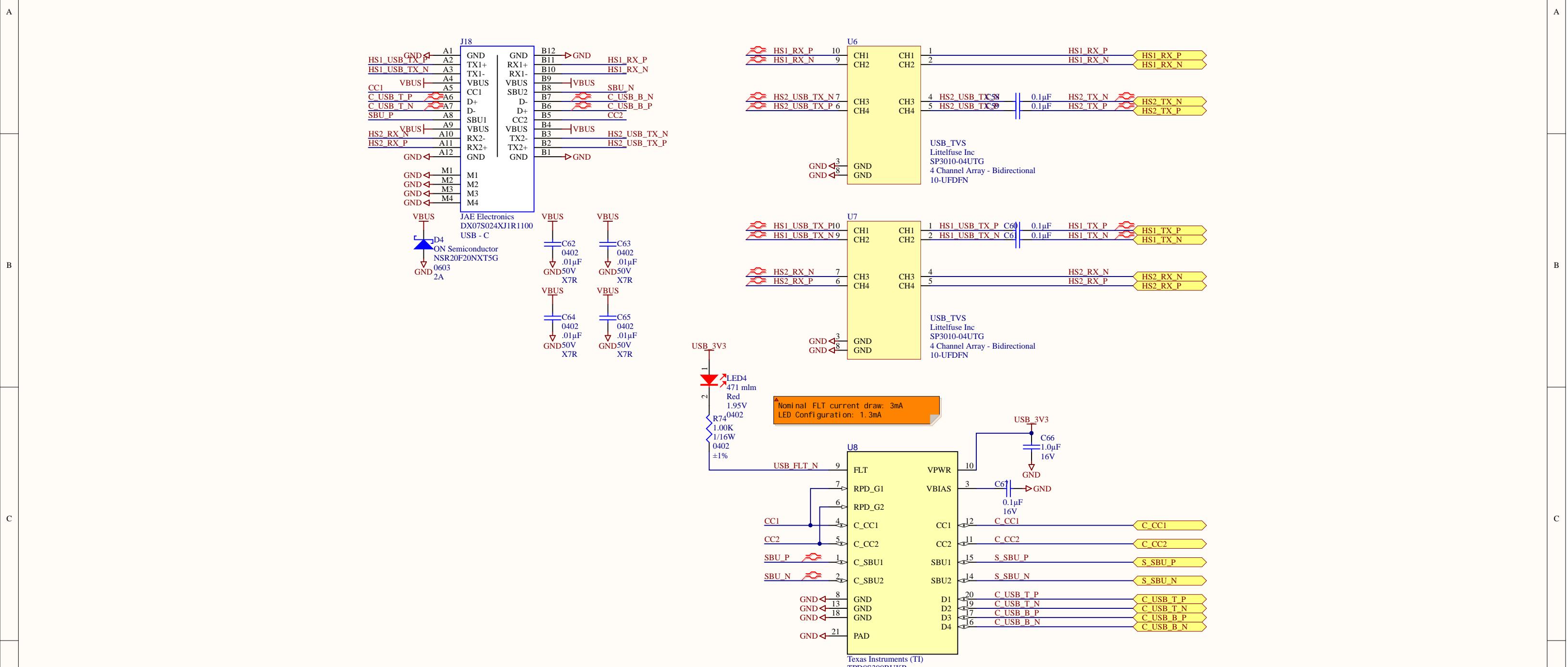


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	USB Phy.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 8 of 20



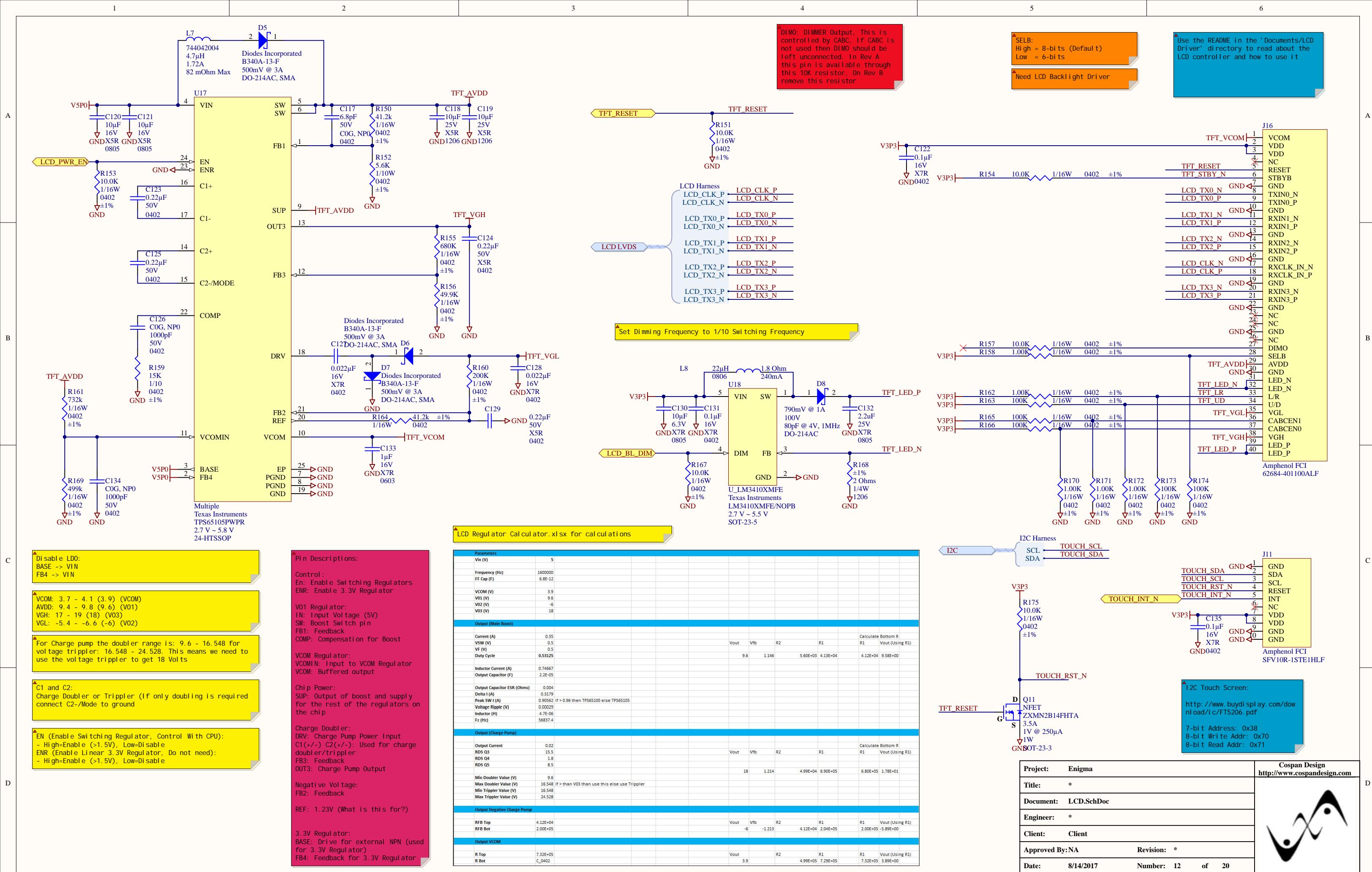


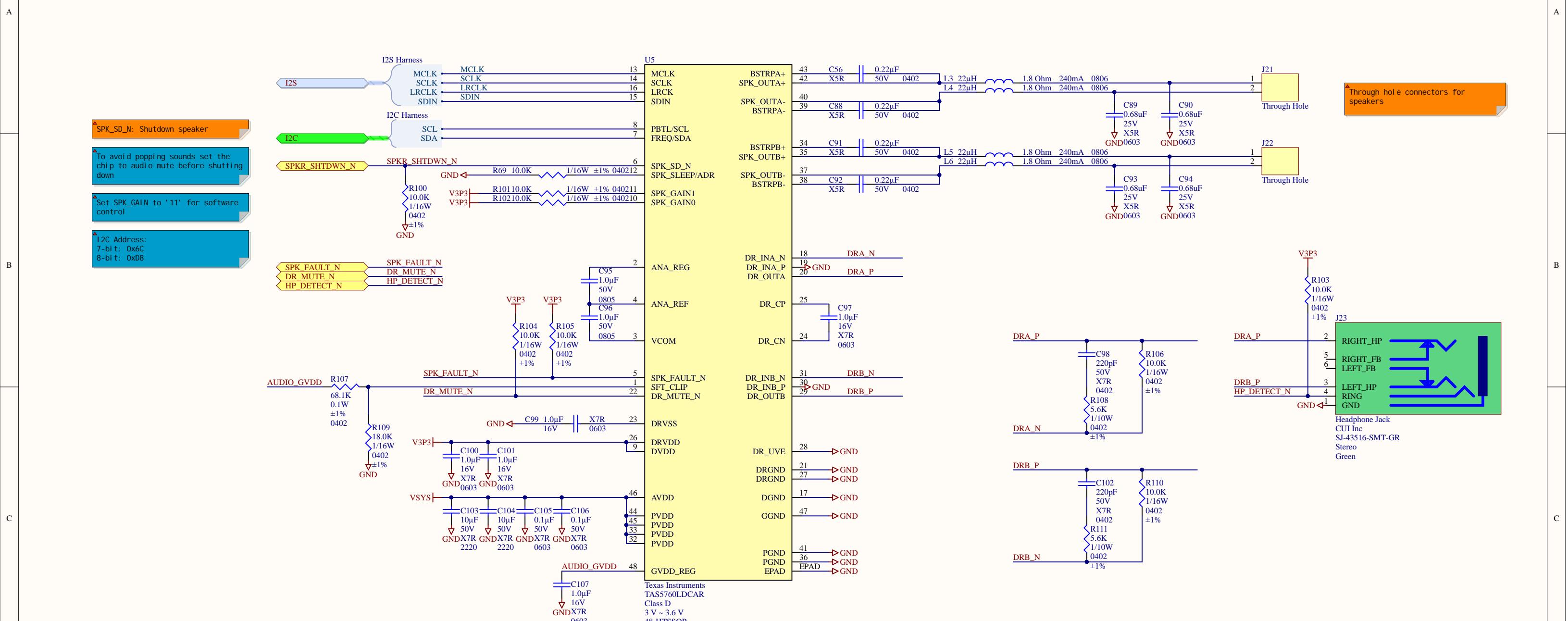




Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	USB Type C Connector ESD.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 11 of 20



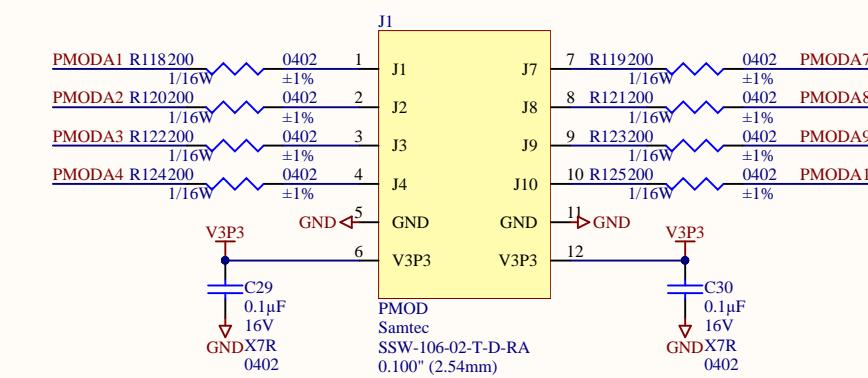




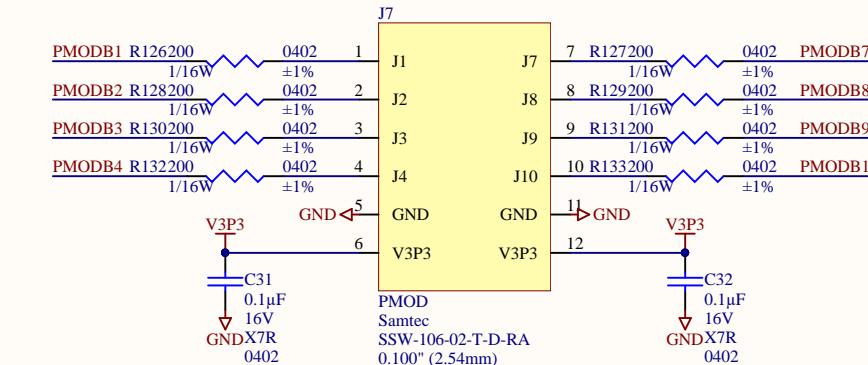
Project:	Enigma	Cospan Design
Title:	*	http://www.cospandesign.com
Document:	I2S Audio.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/14/2017	Number: 13 of 20



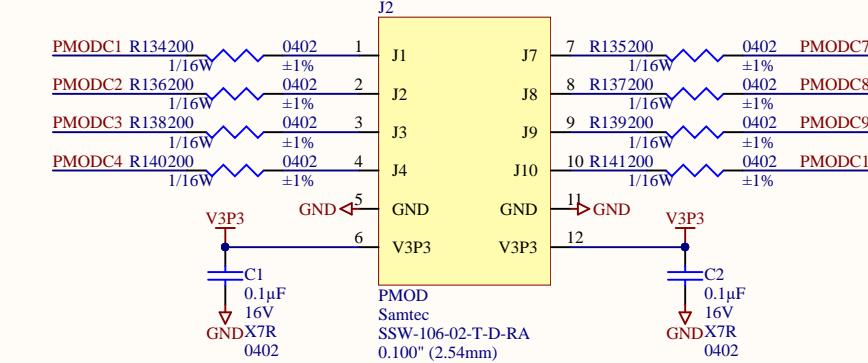
A



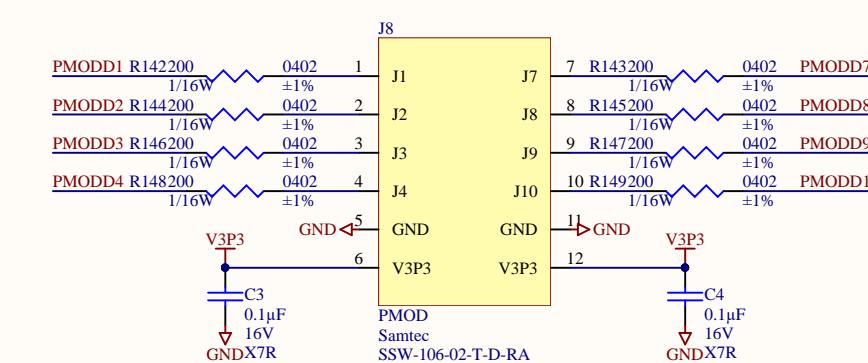
B



C

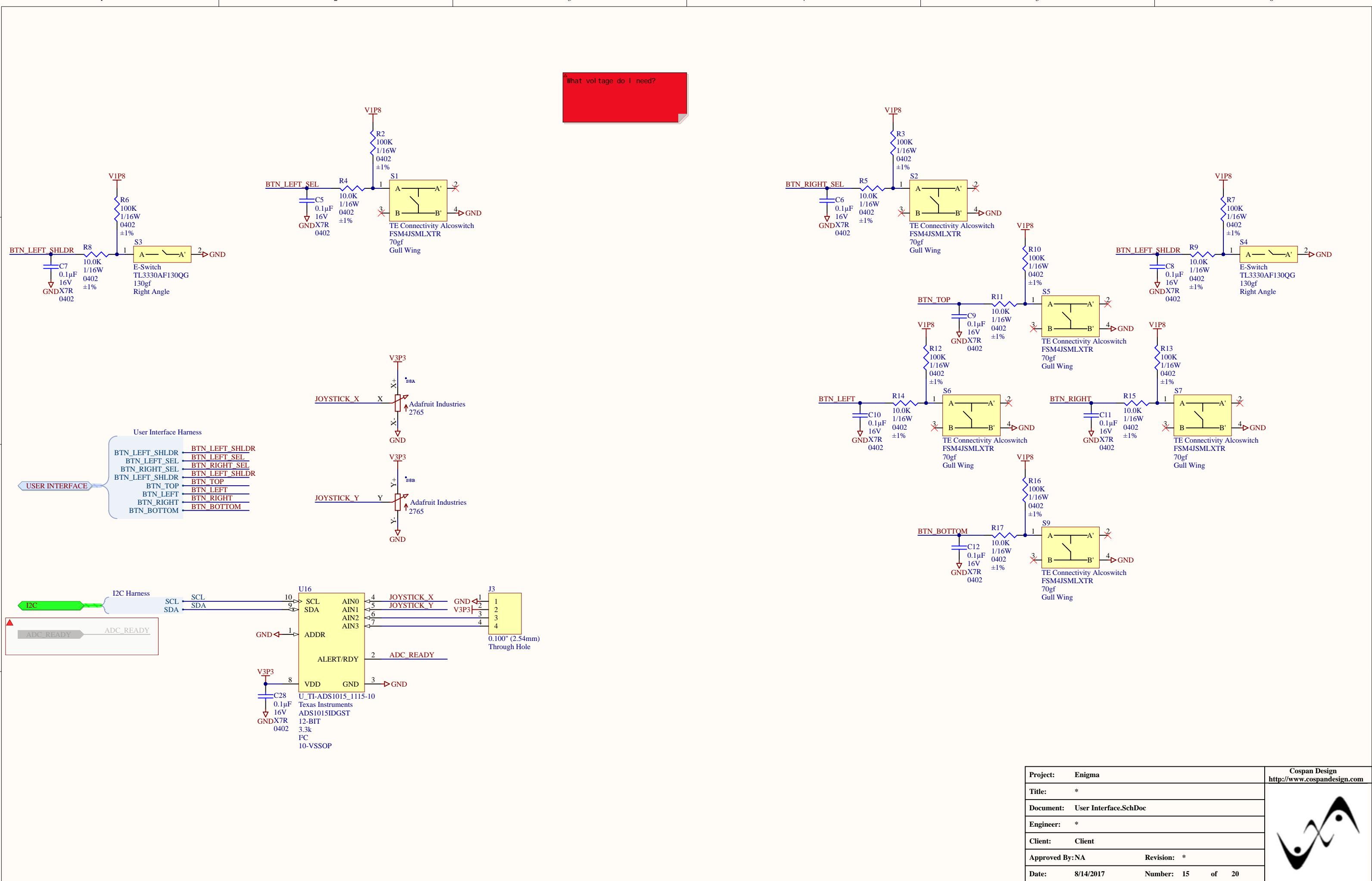


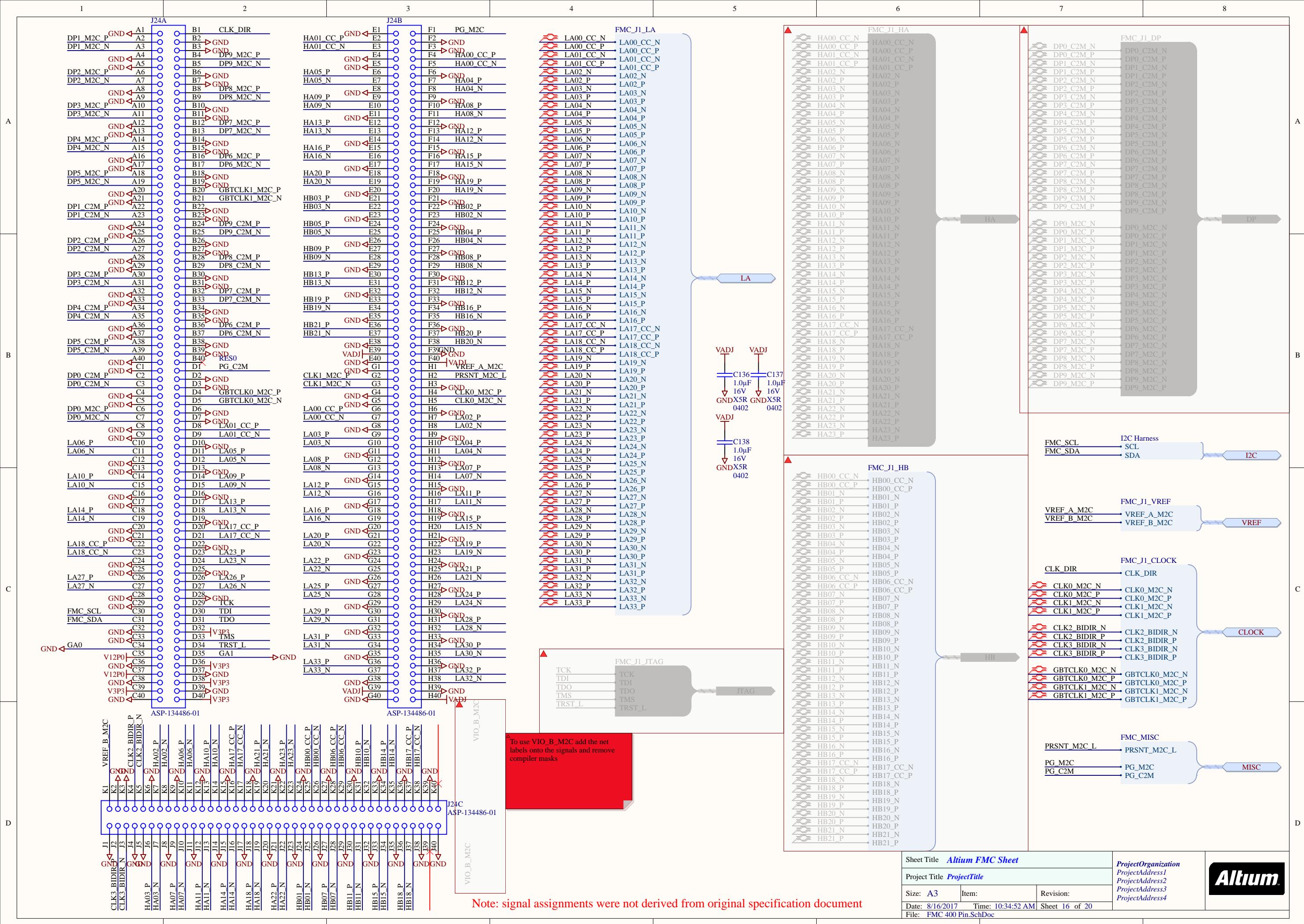
D

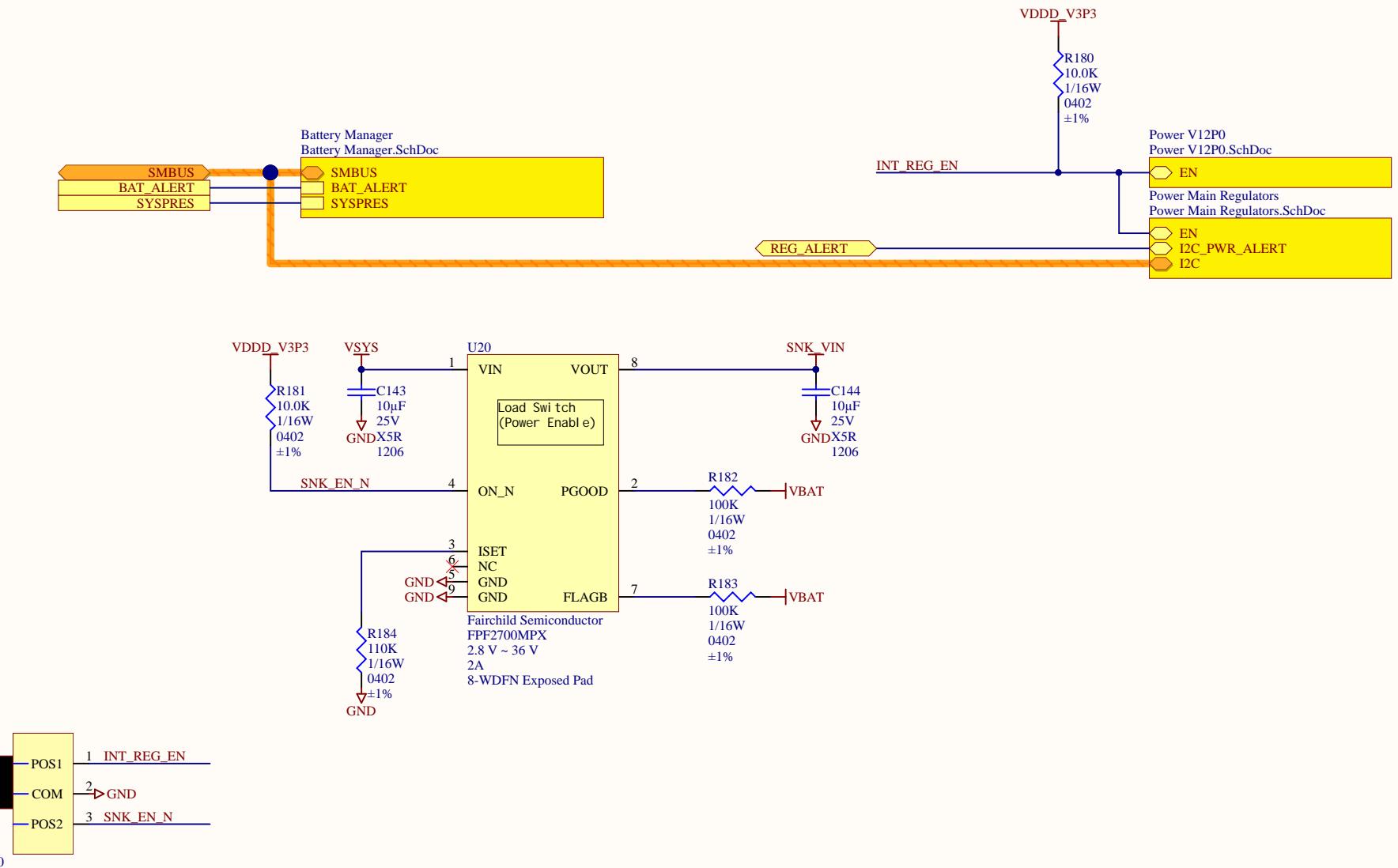


Title:	Dionysus Connectors	Cospan Design http://www.cospandesign.com
Project:	Enigma	
Document:	Arduino and PMOD Connectors.SchDoc	
Engineer:	Eng	
Drawn By:	Draw	
Revision:	Rev	
Date:	7/17/2014	
Number:	14 of 20	





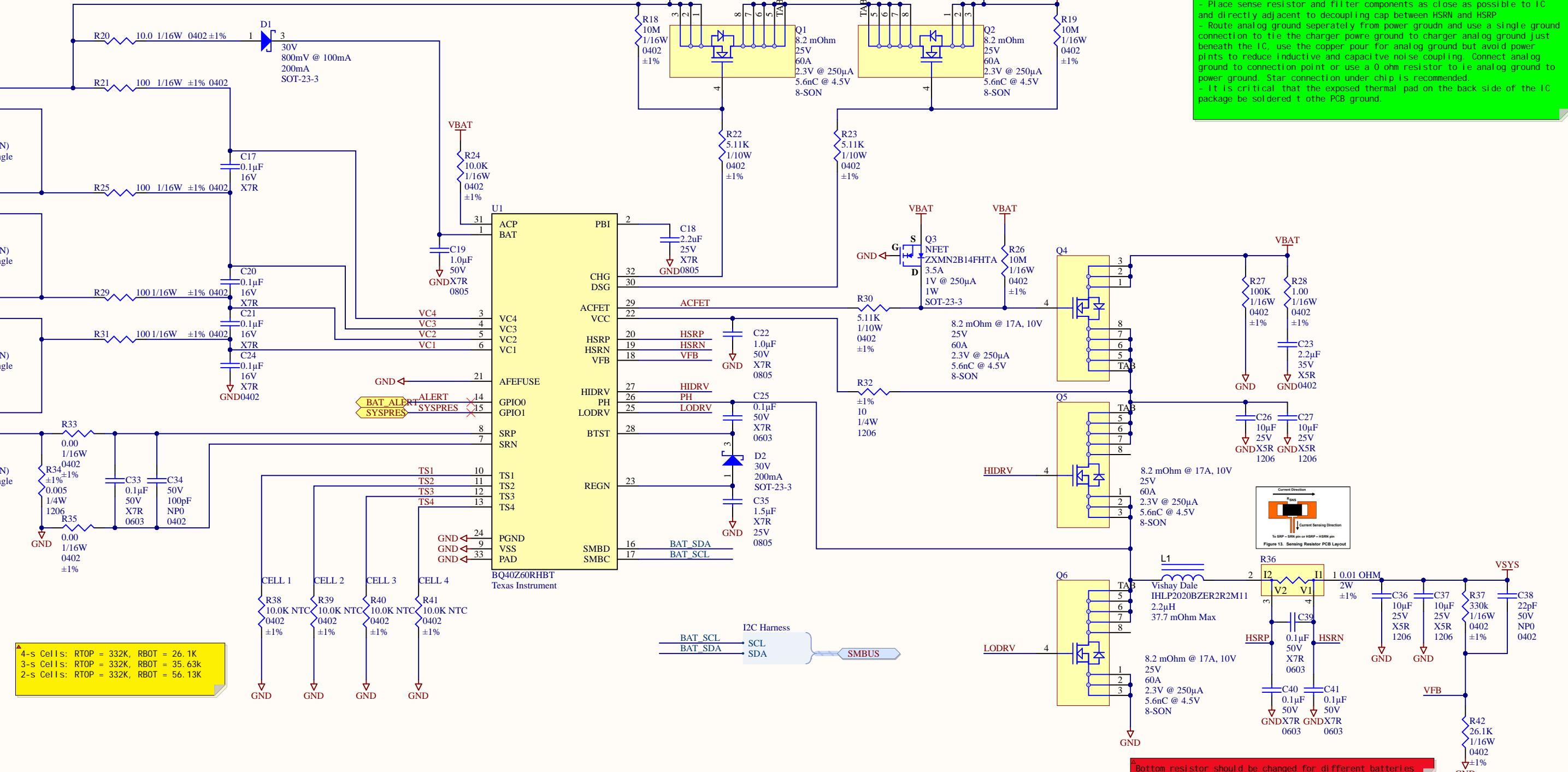




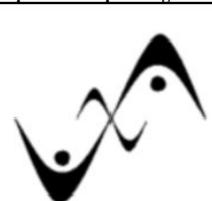
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Power.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	
Revision:	*	
Date:	8/14/2017	Number: 17 of 20



▲ GPI00 (ALERT): Alert output to host (Open Drain)
 ▲ GPI01 (SYS PRES): System presence indicator (weak pull up)
 ▲ Max Charge Current: 3A (We can't do more because the inductor would be oversaturated if we charge with more)
 ▲ VFB: 1.22V
 ▲ AFEFUSE should be hooked up to ground when not used
 Datasheet: (9.3.2.4)



Project:	Enigma	Cospan Design
Title:	Battery Manager	http://www.cospandesign.com
Document:	Battery Manager.SchDoc	
Engineer:	David McCoy	
Client:	MIT AeroAstro	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 18 of 20



A

A

B

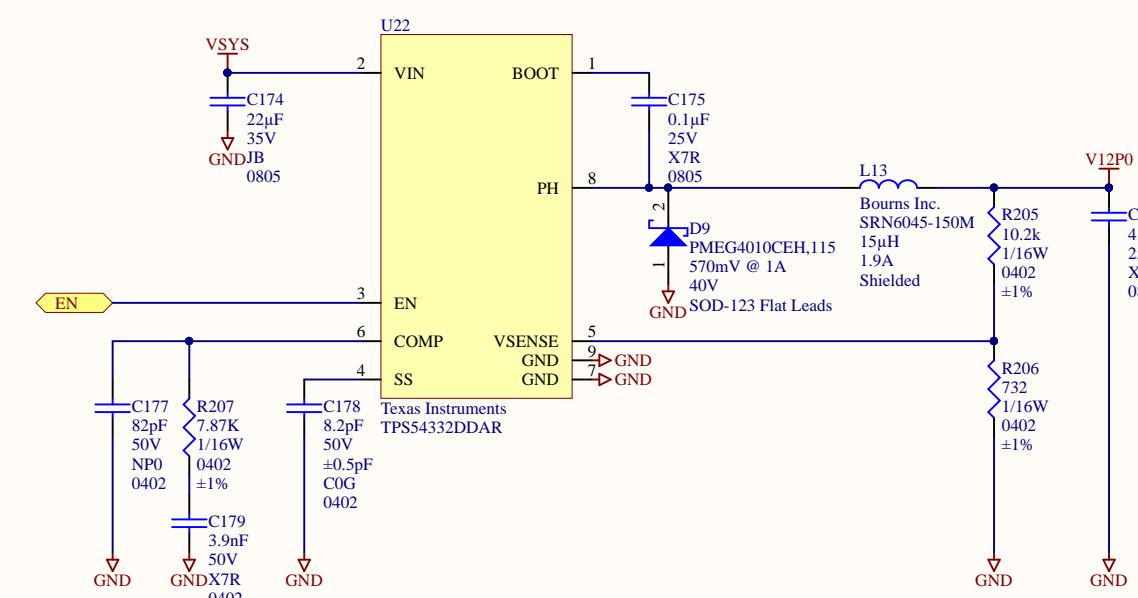
B

C

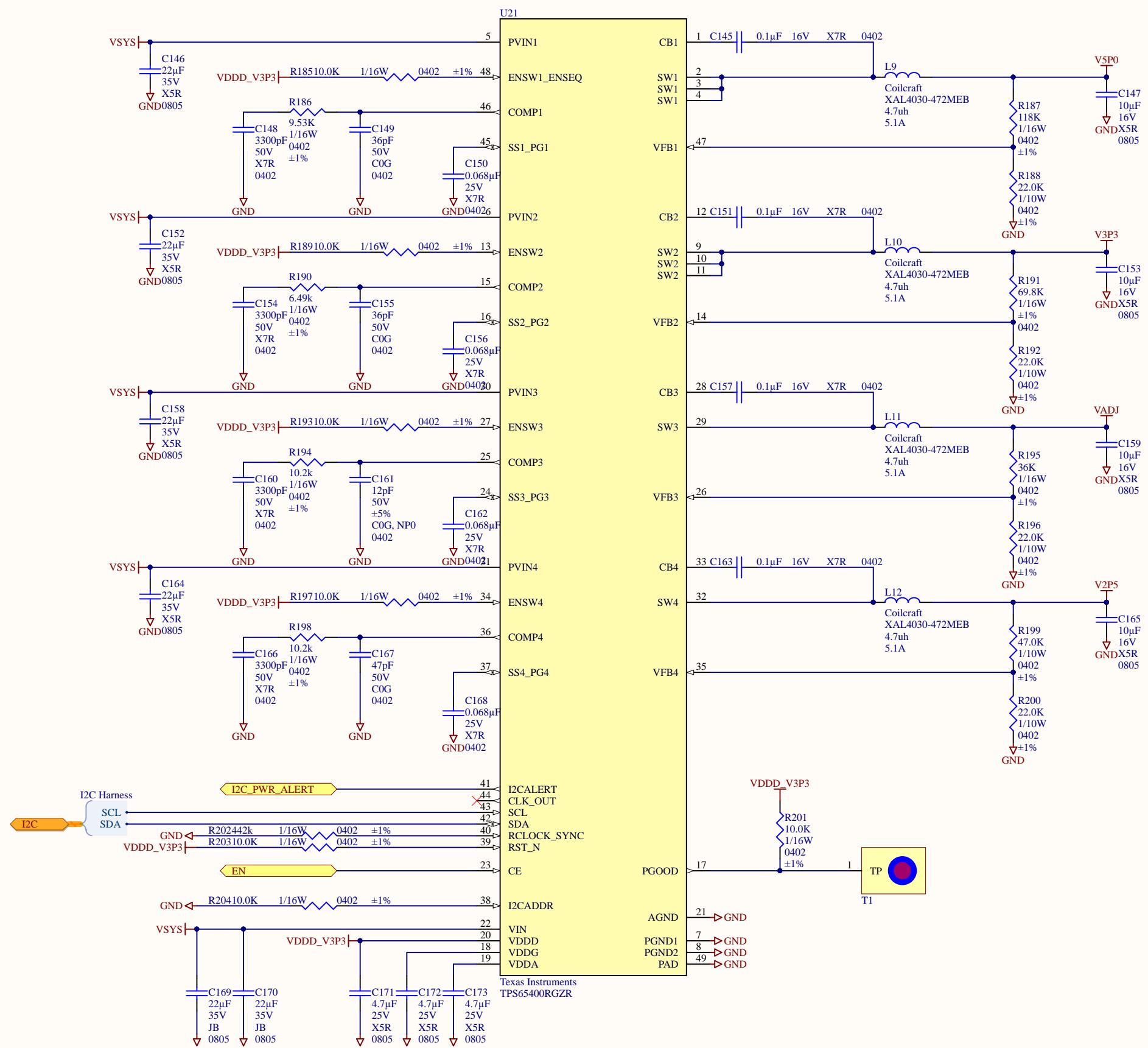
C

D

D

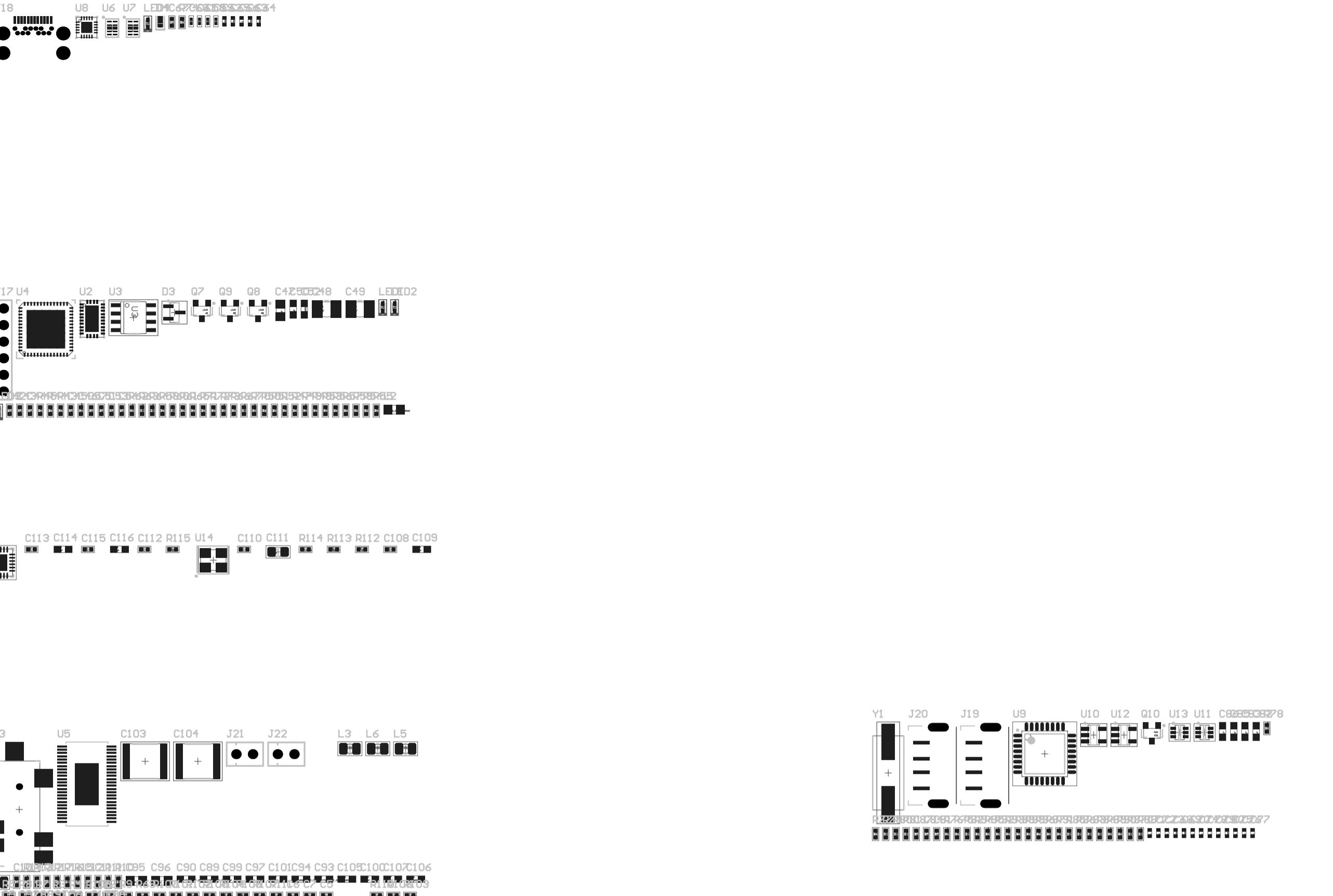
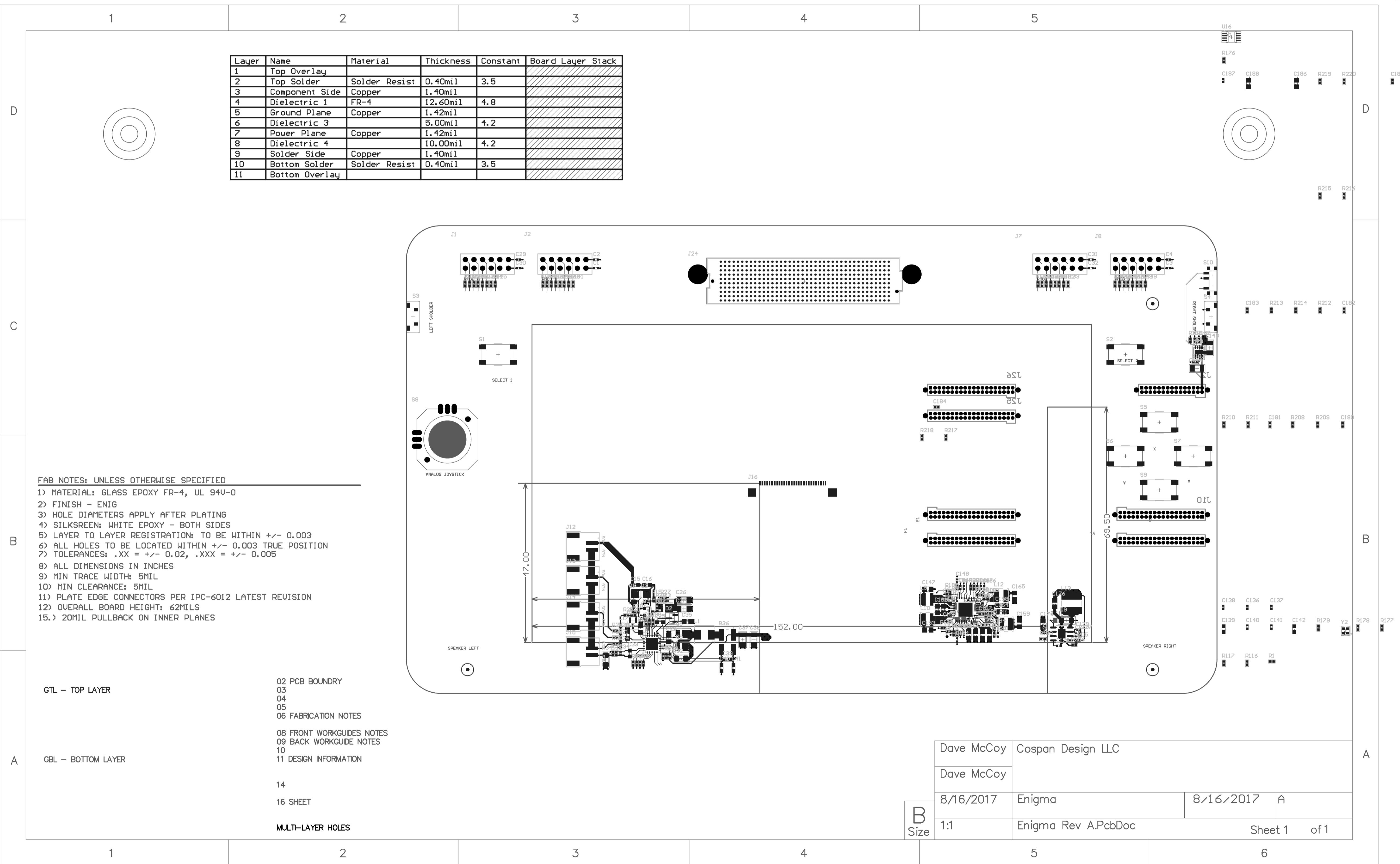


Title		
Size Tabloid	Number	Revision
Date: 8/16/2017	Sheet of	
File: C:\Users...\Power V12P0.SchDoc	Drawn By:	

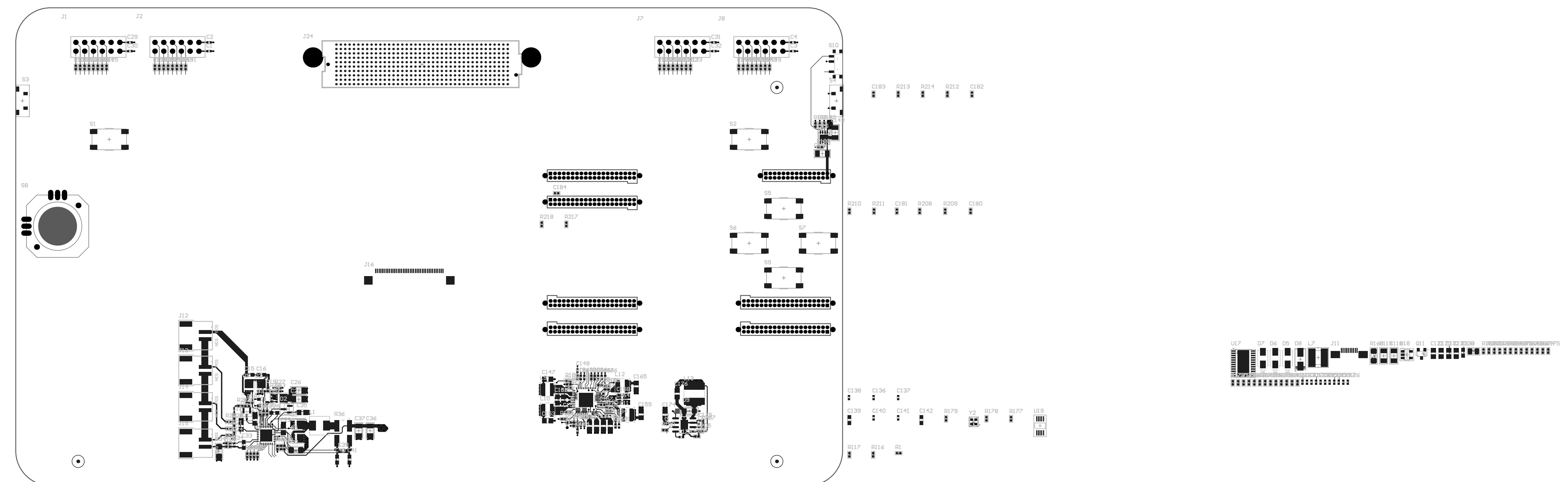


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	*	
Document:	Power Main Regulators.SchDoc	
Engineer:	*	
Client:	Client	
Approved By:	NA	Revision: *
Date:	8/16/2017	Number: 20 of 20

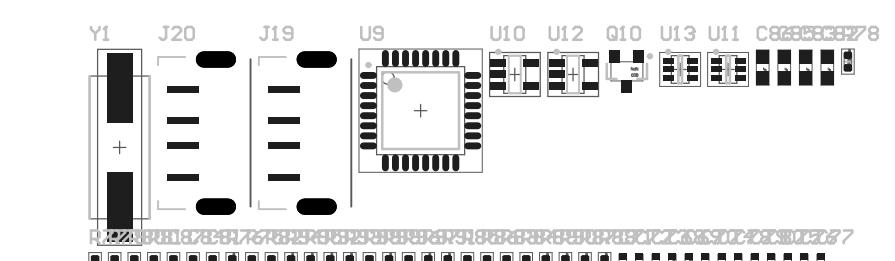
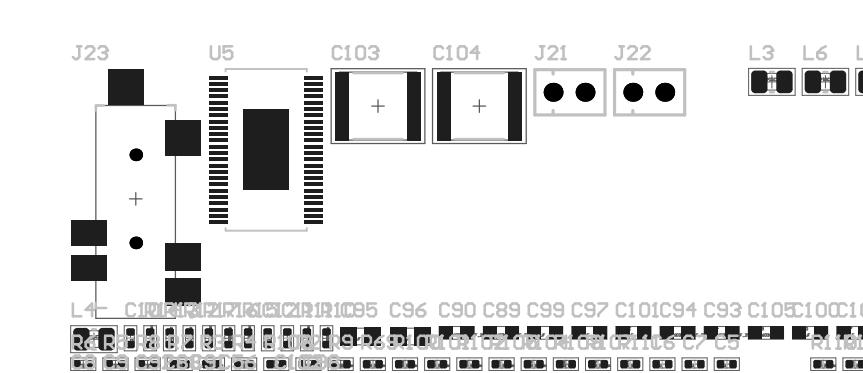
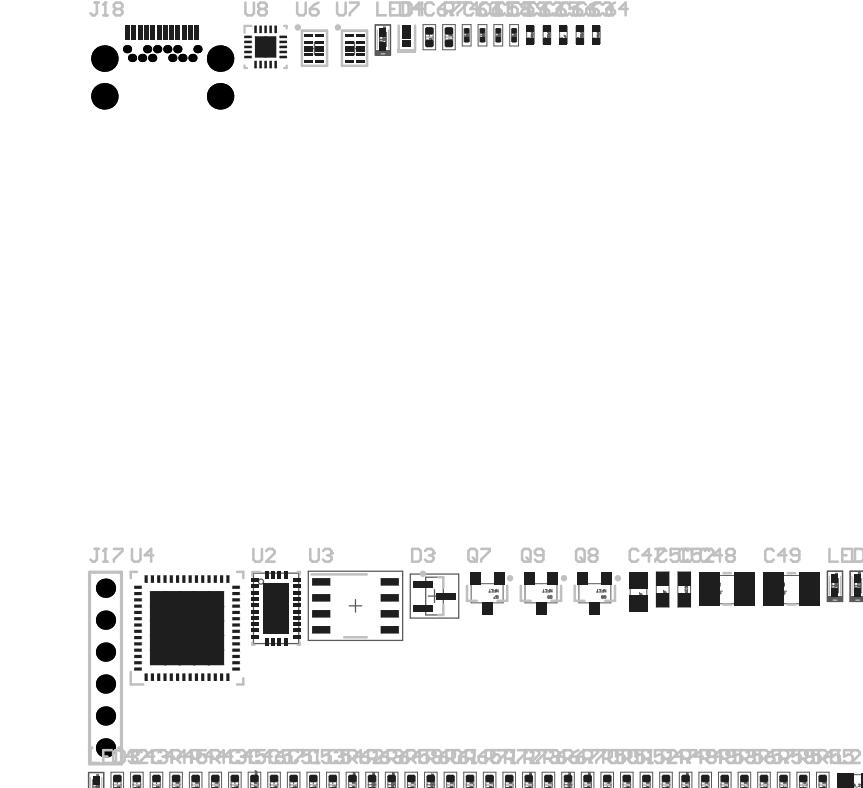




Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3		5.00mil	4.2	
7	Power Plane	Copper	1.42mil		
8	Dielectric 4		10.00mil	4.2	
9	Solder Side	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



02 PCB BOUNDARY



GTL – TOP LAYER

GBI - BOTTOM LAYER

