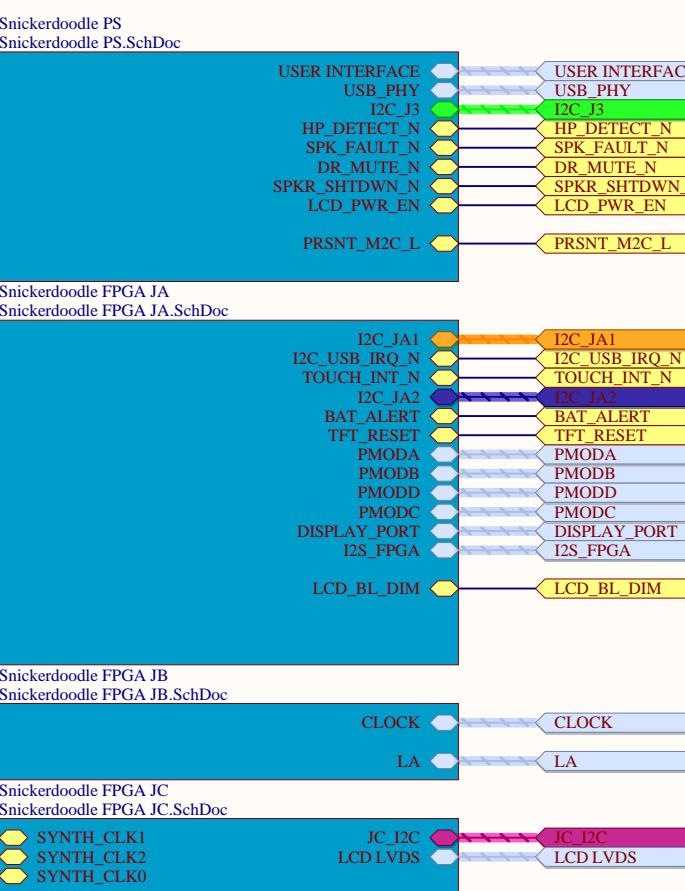


A



B

A

C

B

D

C

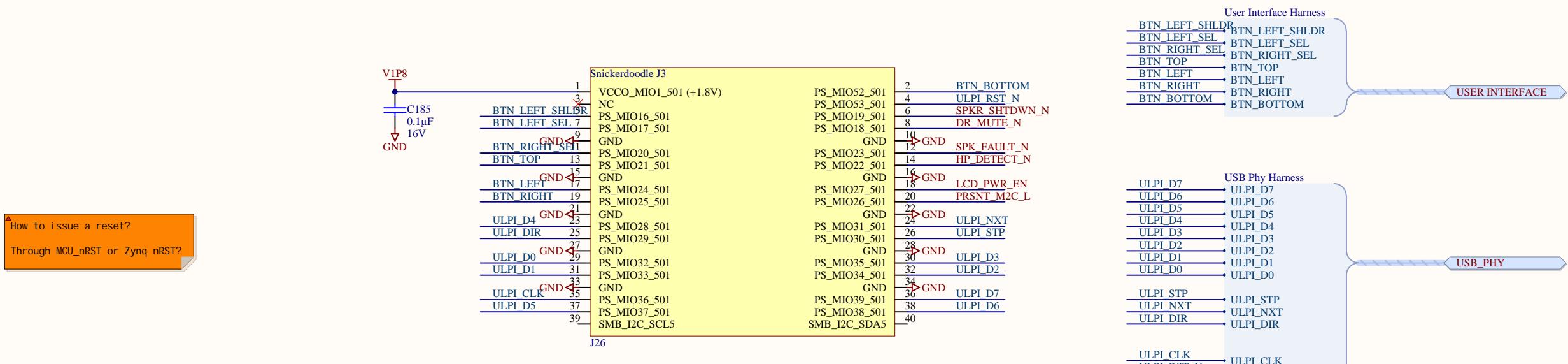
D

Not SnickerDoodle's Internal regulators for powering this board, but it would be good to make sure I2C is at the correct pullups

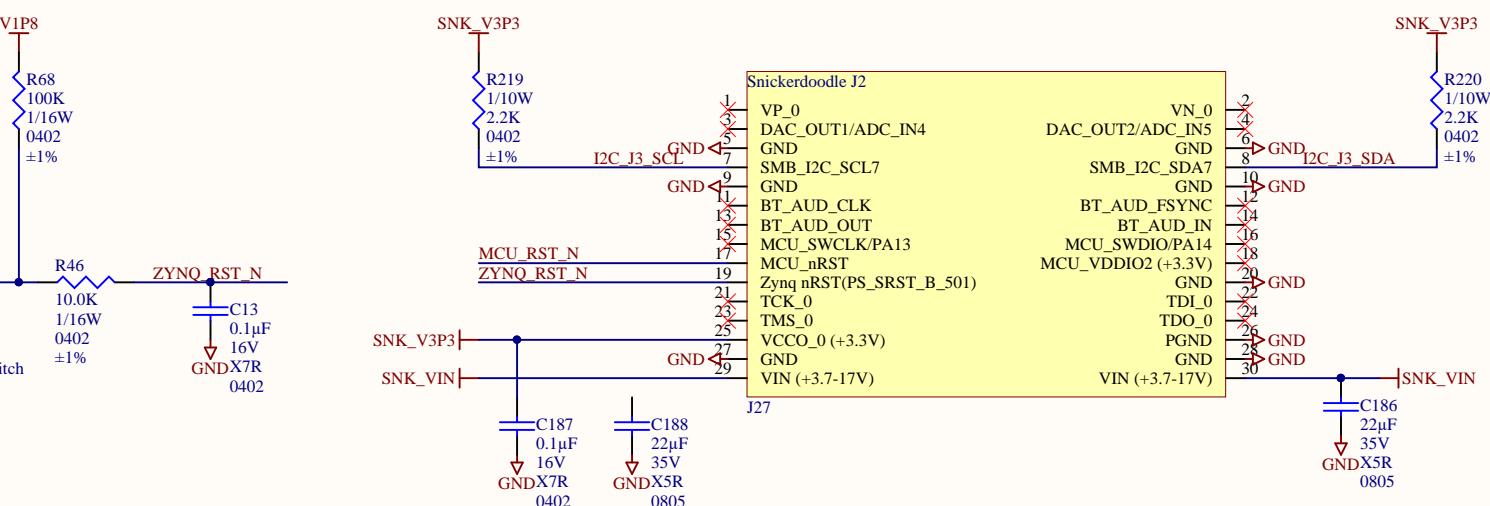
Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	Snickerdoodle Top	
Document:	Snickerdoodle.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 2 of 20



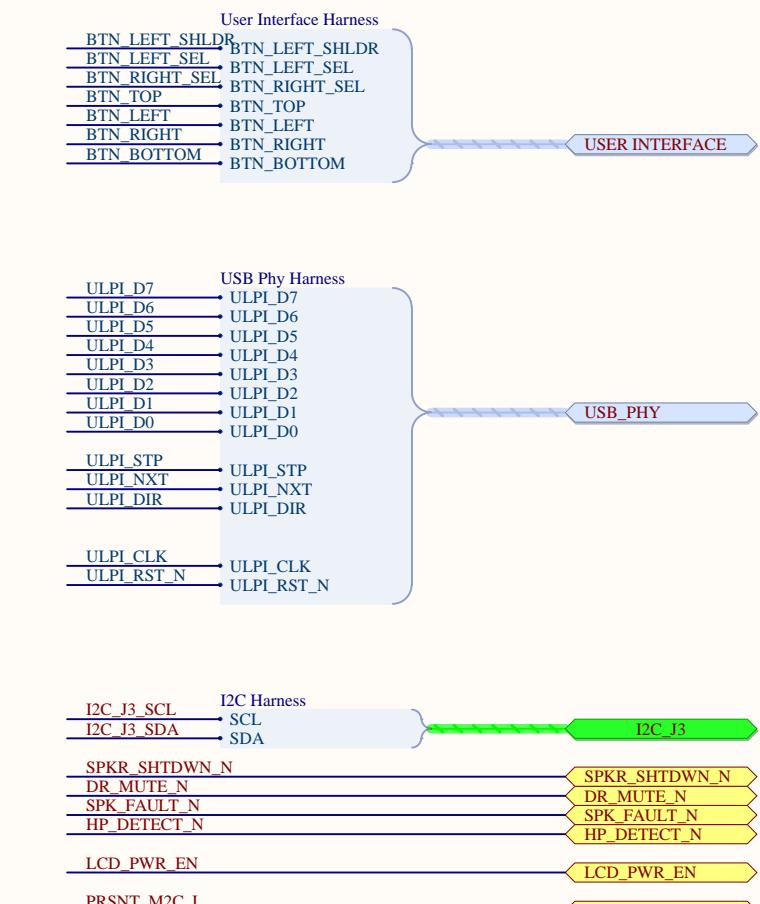
A



B



C

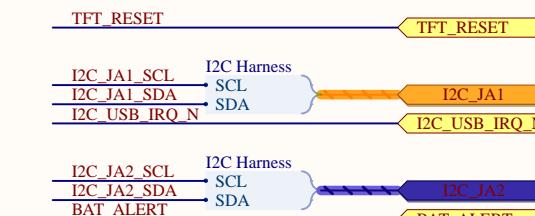
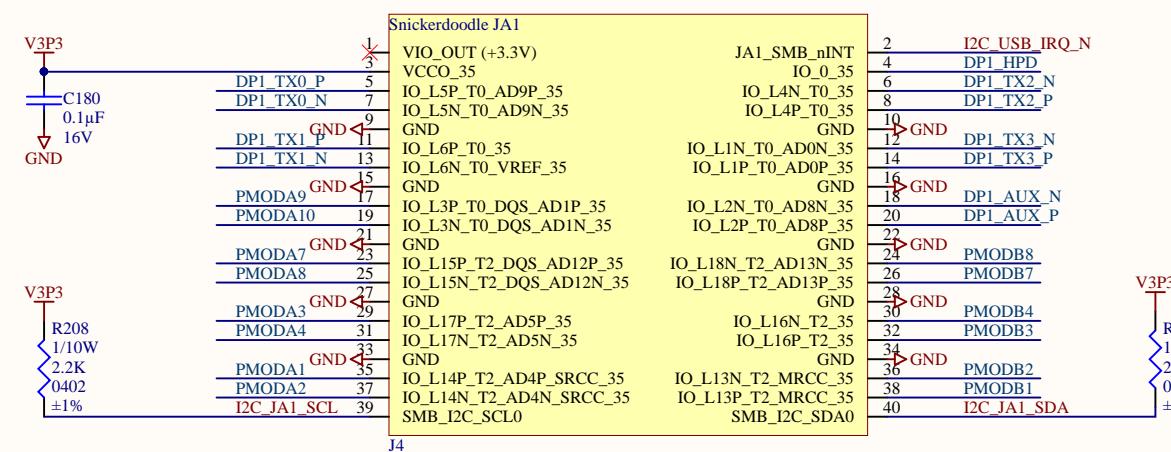


D

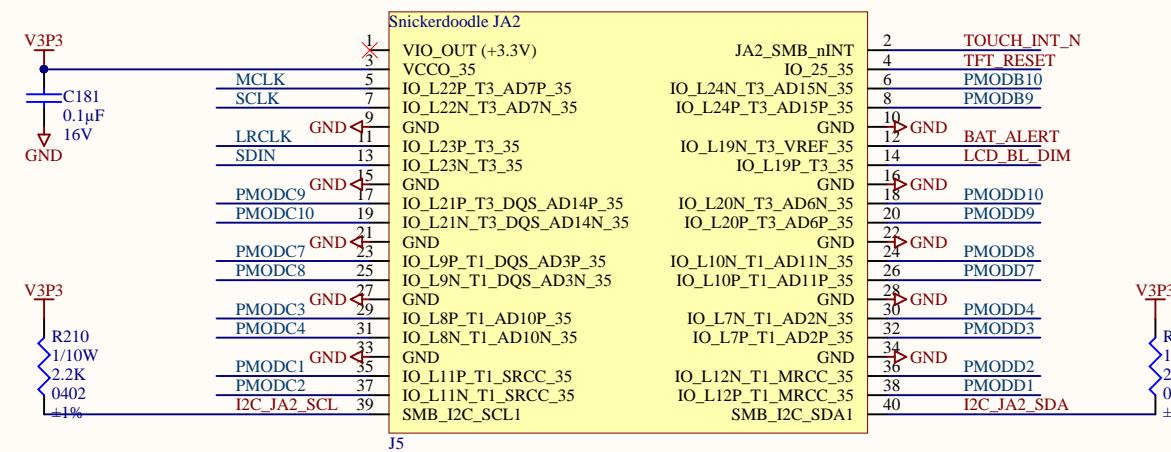
Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	Snickerdoodle PS	
Document:	Snickerdoodle PS.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 3 of 20



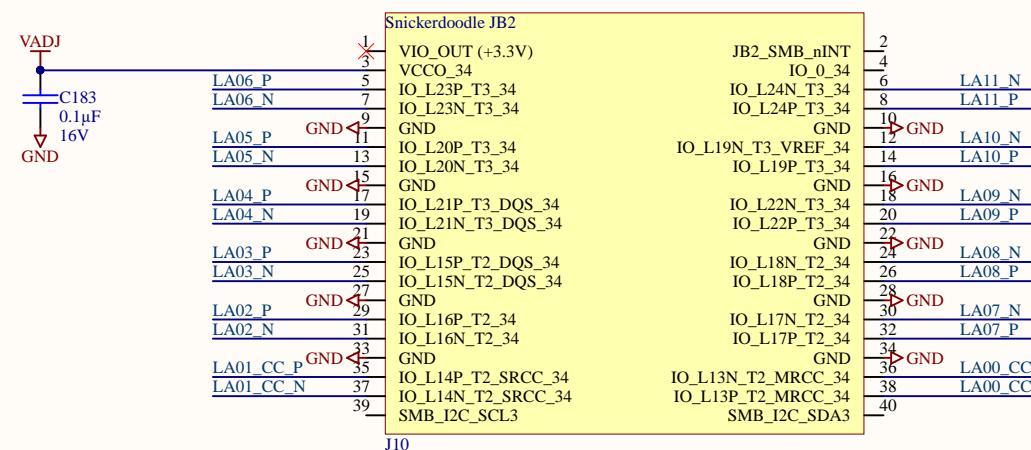
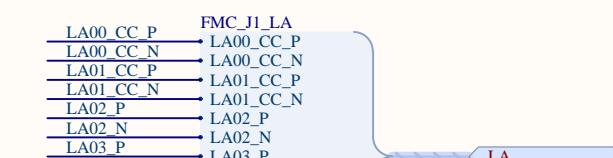
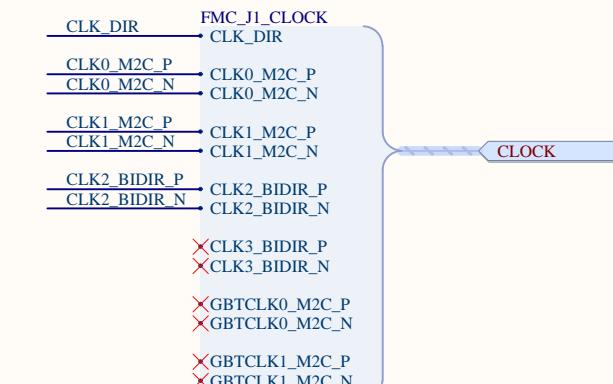
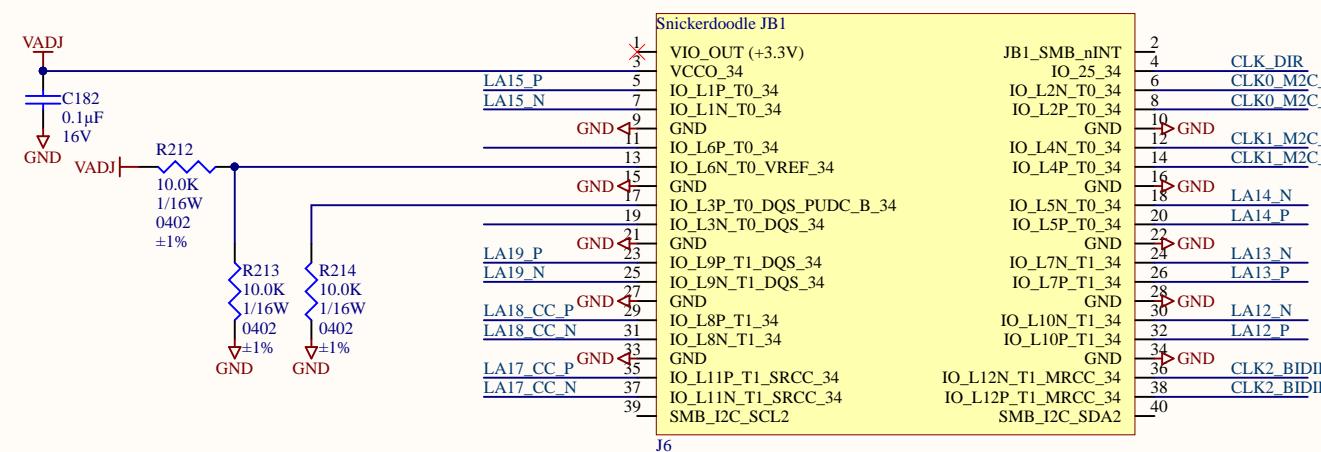
A



B



A

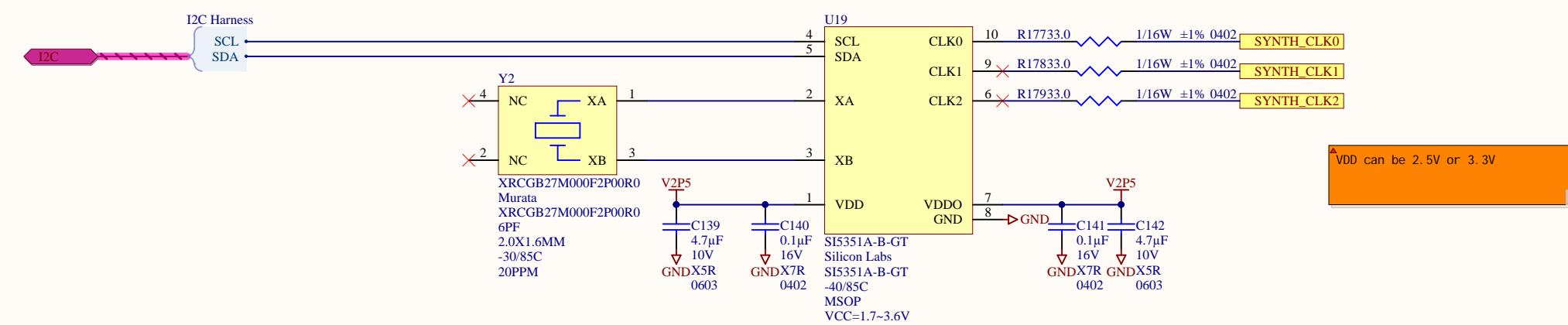


Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	Snickerdoodle JB	
Document:	Snickerdoodle FPGA JB.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	
Revision:	A	
Date:	8/16/2017	
Number:	5 of 20	



A

A



B

B

C

C

D

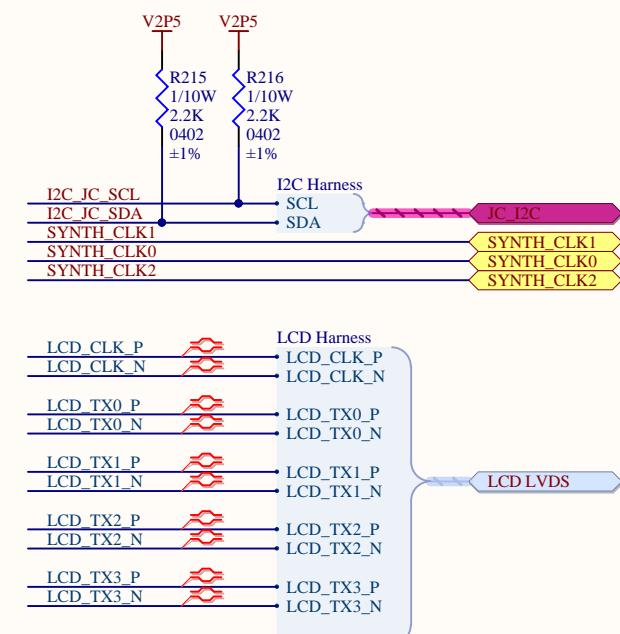
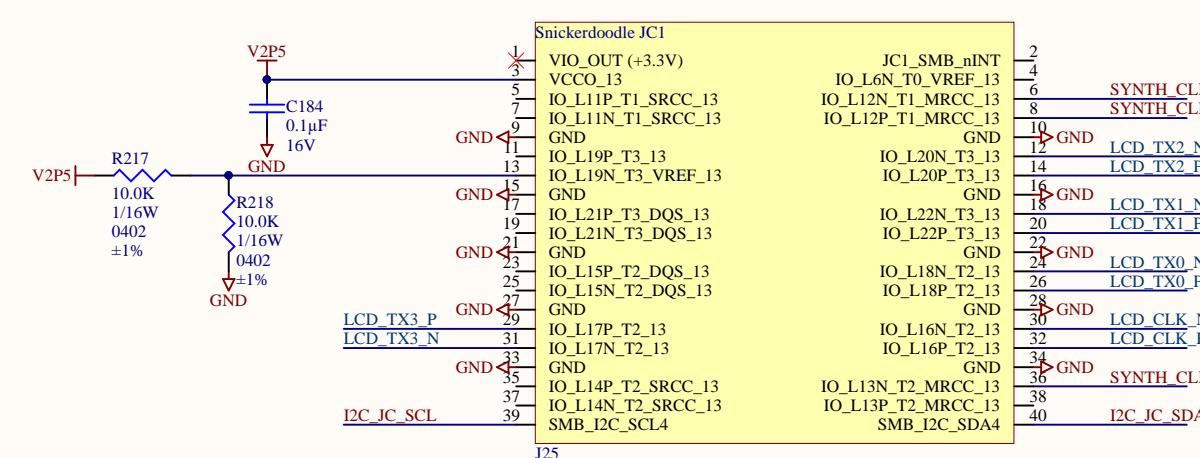
D

Project:	Project_Name	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	Clock Synthesizer	
Document:	Clock Synth.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: Rev
Date:	8/16/2017	Number: 6 of 20



A

Should I use VREF??



B

C

D

Project:	Enigma	Cospan Design
Title:	Snickerdoodle JC	<a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Document:	Snickerdoodle FPGA JC.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 7 of 20



A

A

B

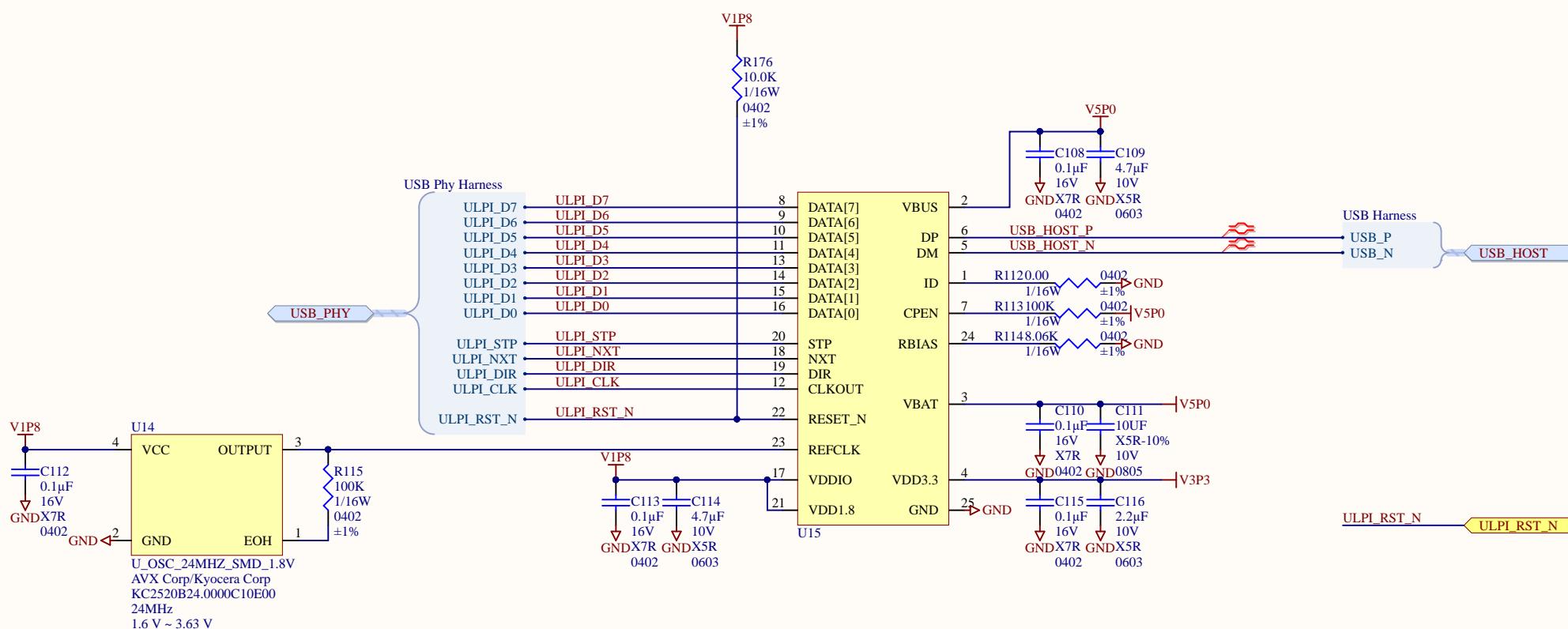
B

C

C

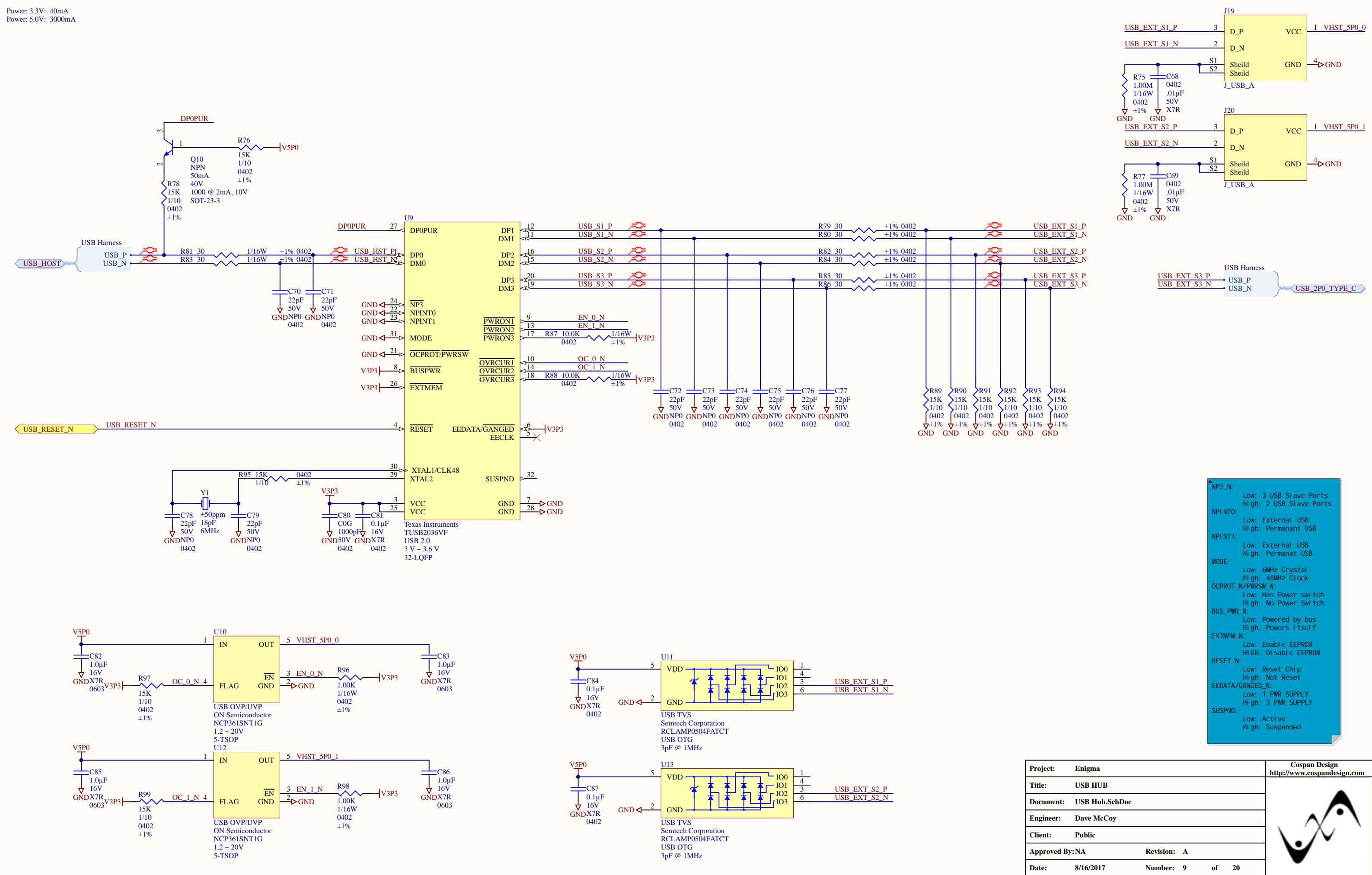
D

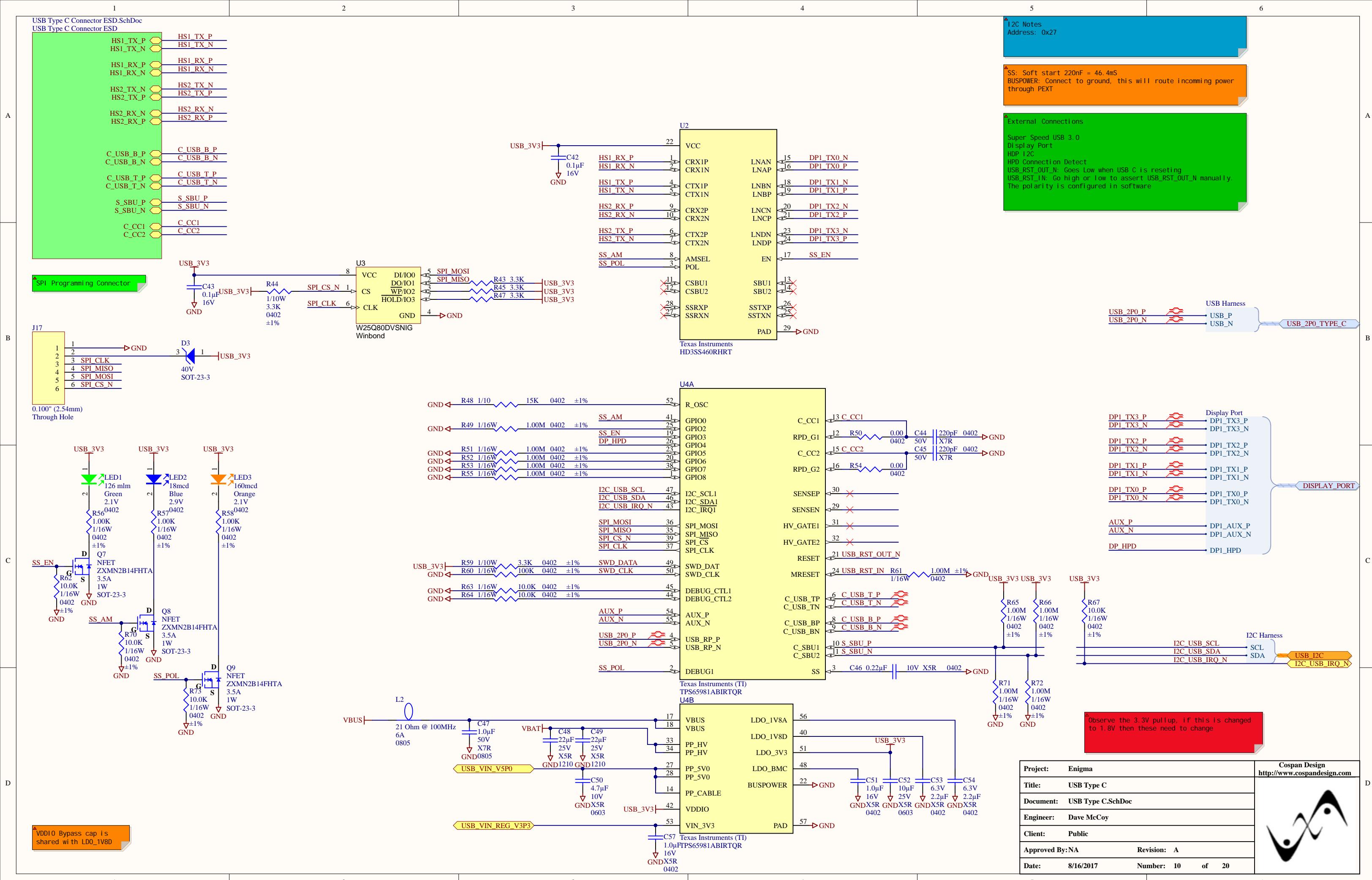
D

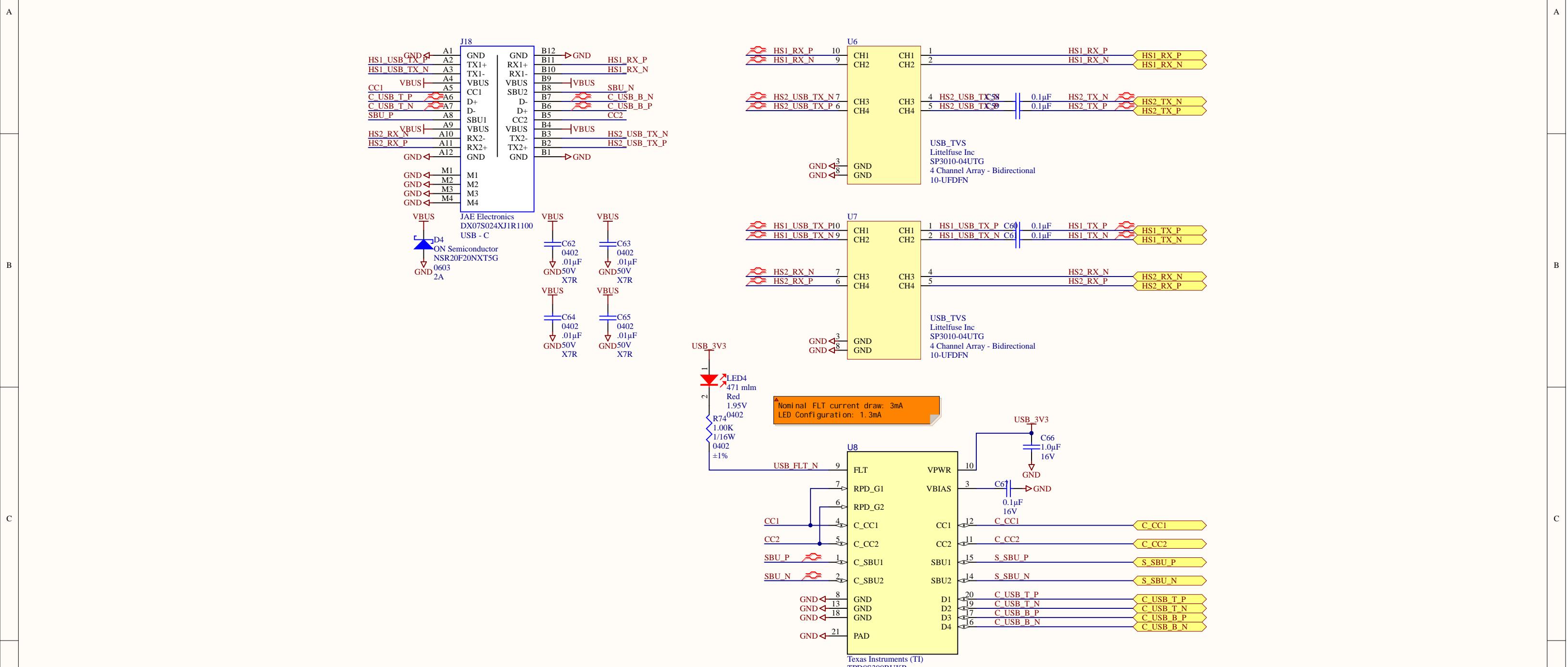


Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	USB Phy	
Document:	USB Phy.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 8 of 20



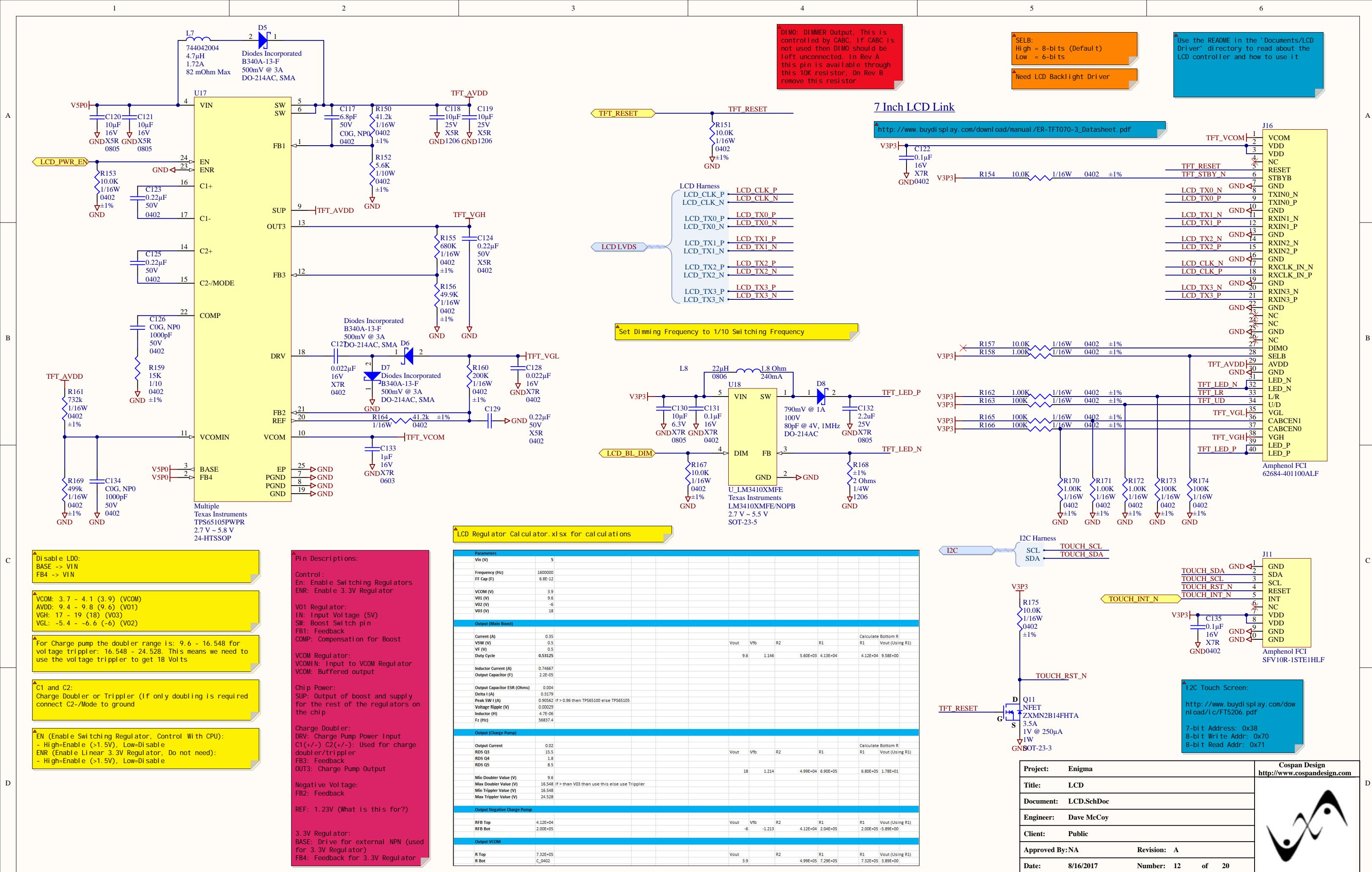




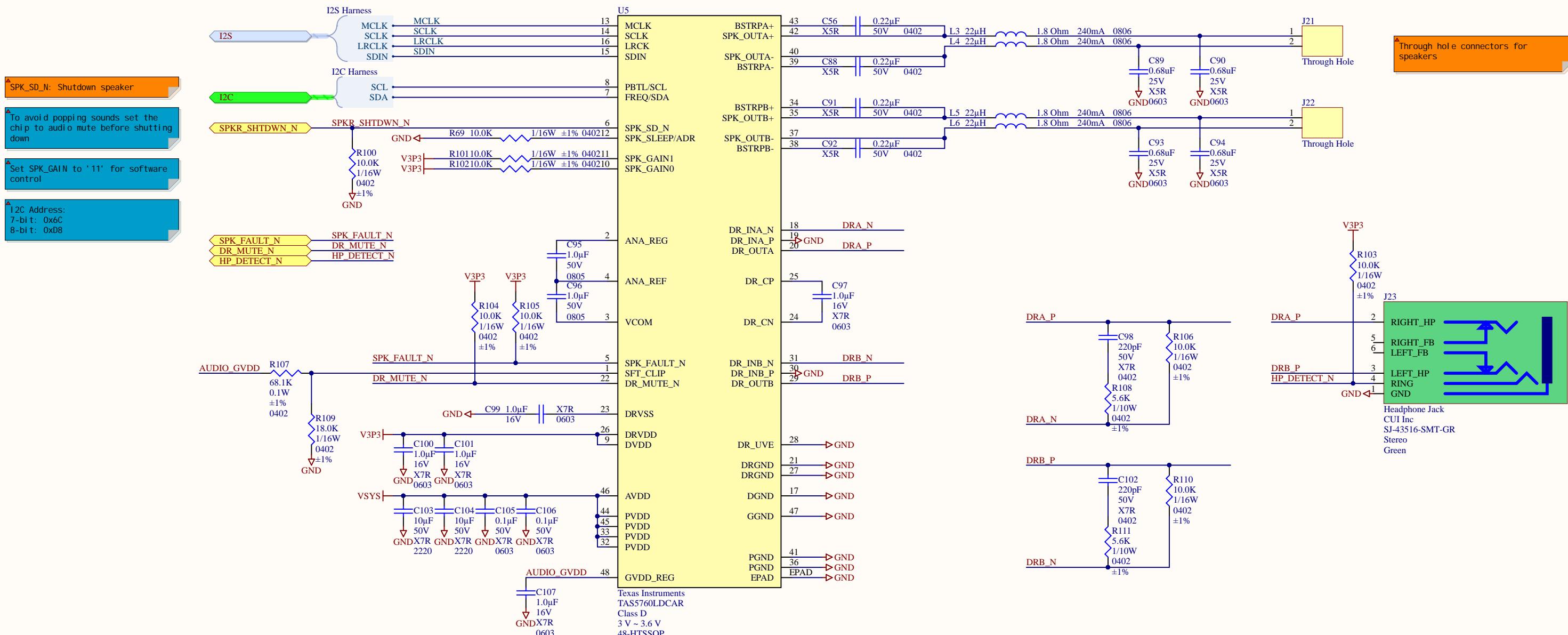


Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	USB Type C Connector	
Document:	USB Type C Connector ESD.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 11 of 20





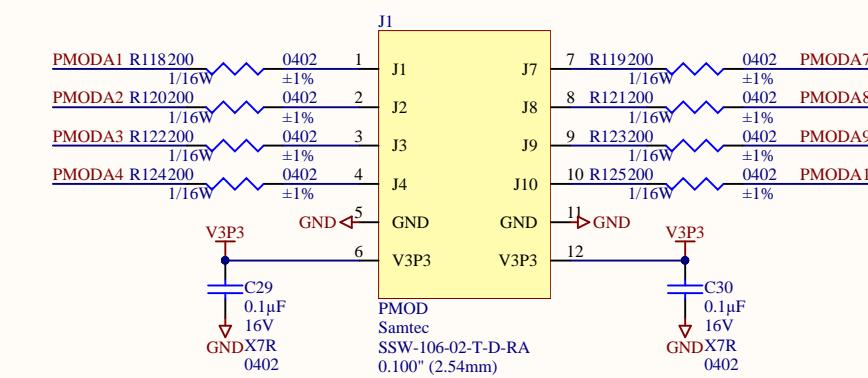
A



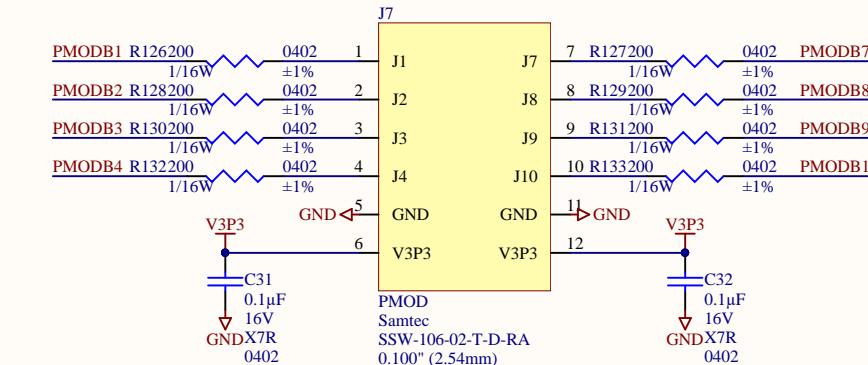
Project:	Enigma	Cospan Design
Title:	I2S Codec/Amplifier	<a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Document:	I2S Audio.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 13 of 20



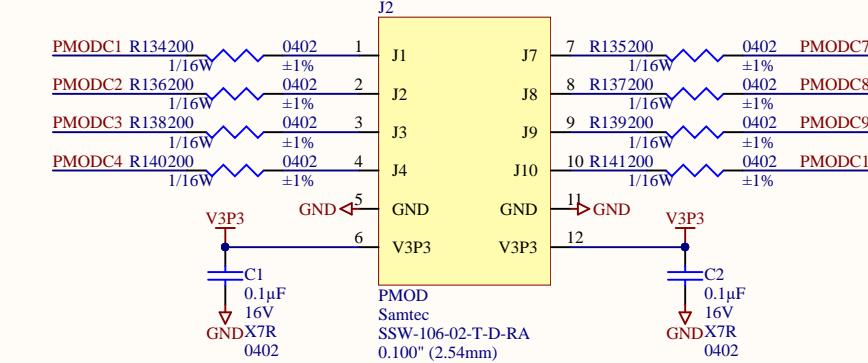
A



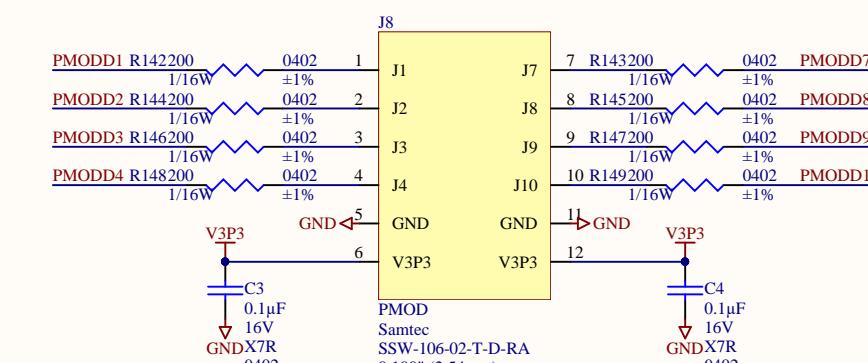
B



C

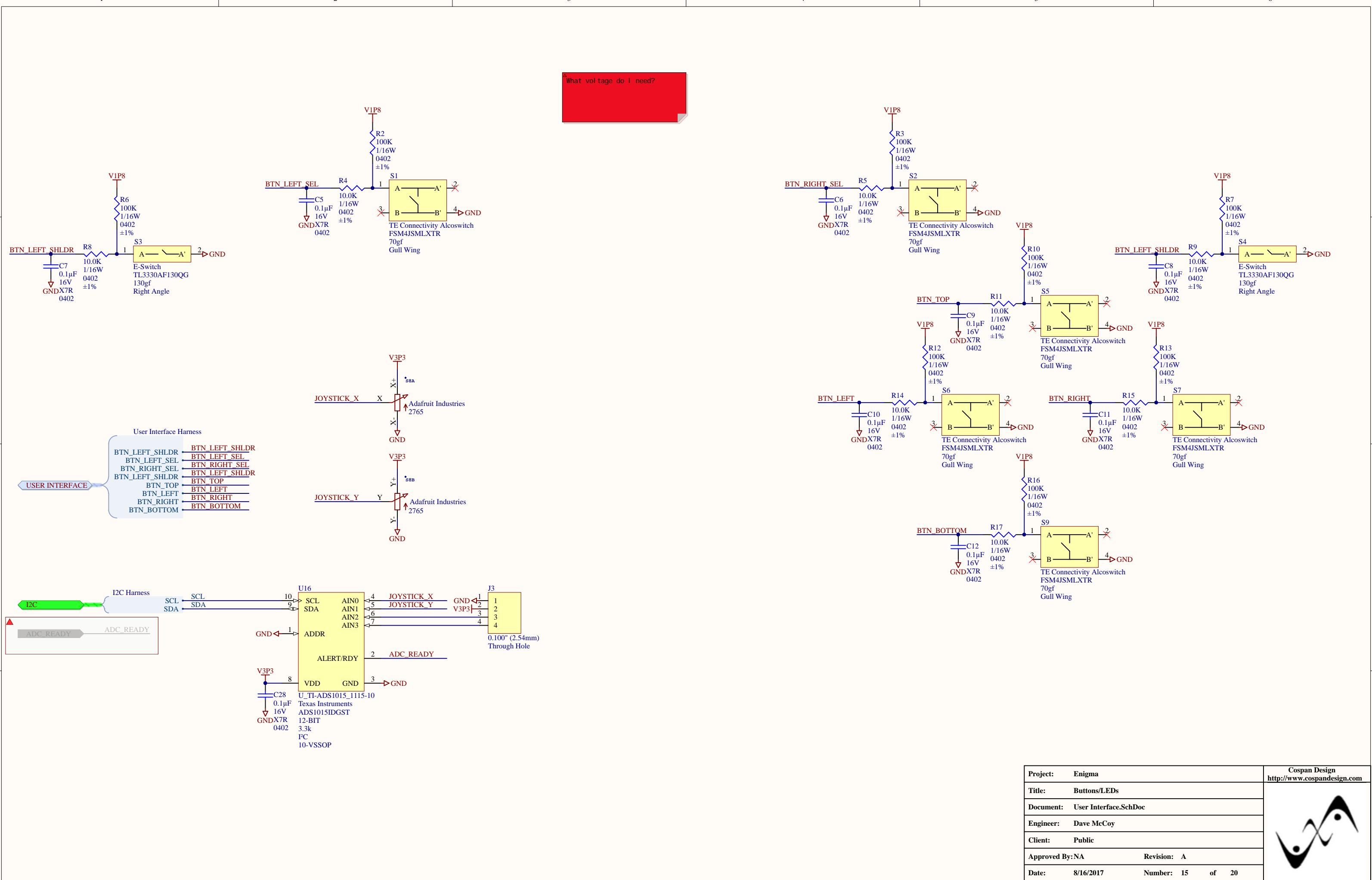


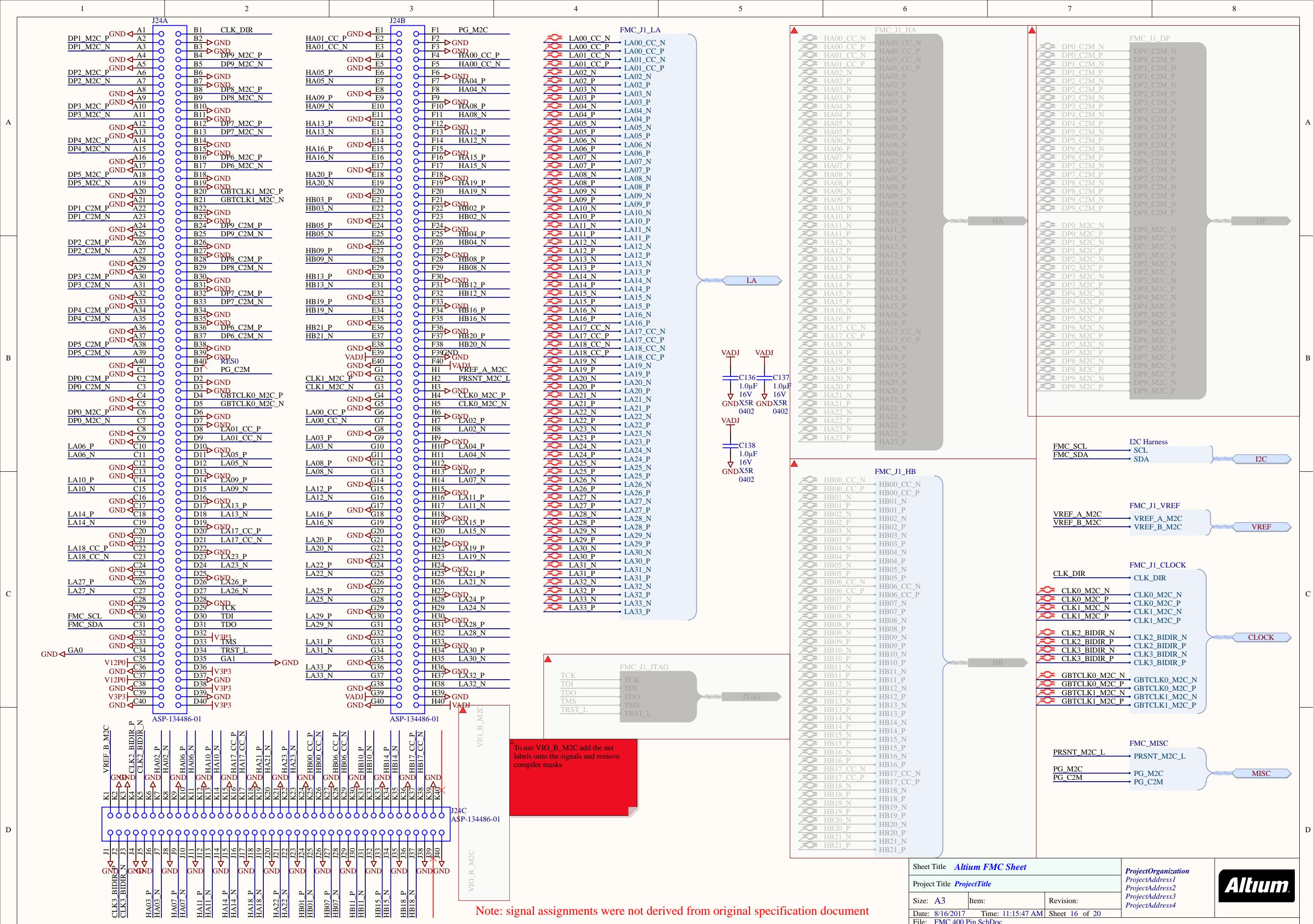
D

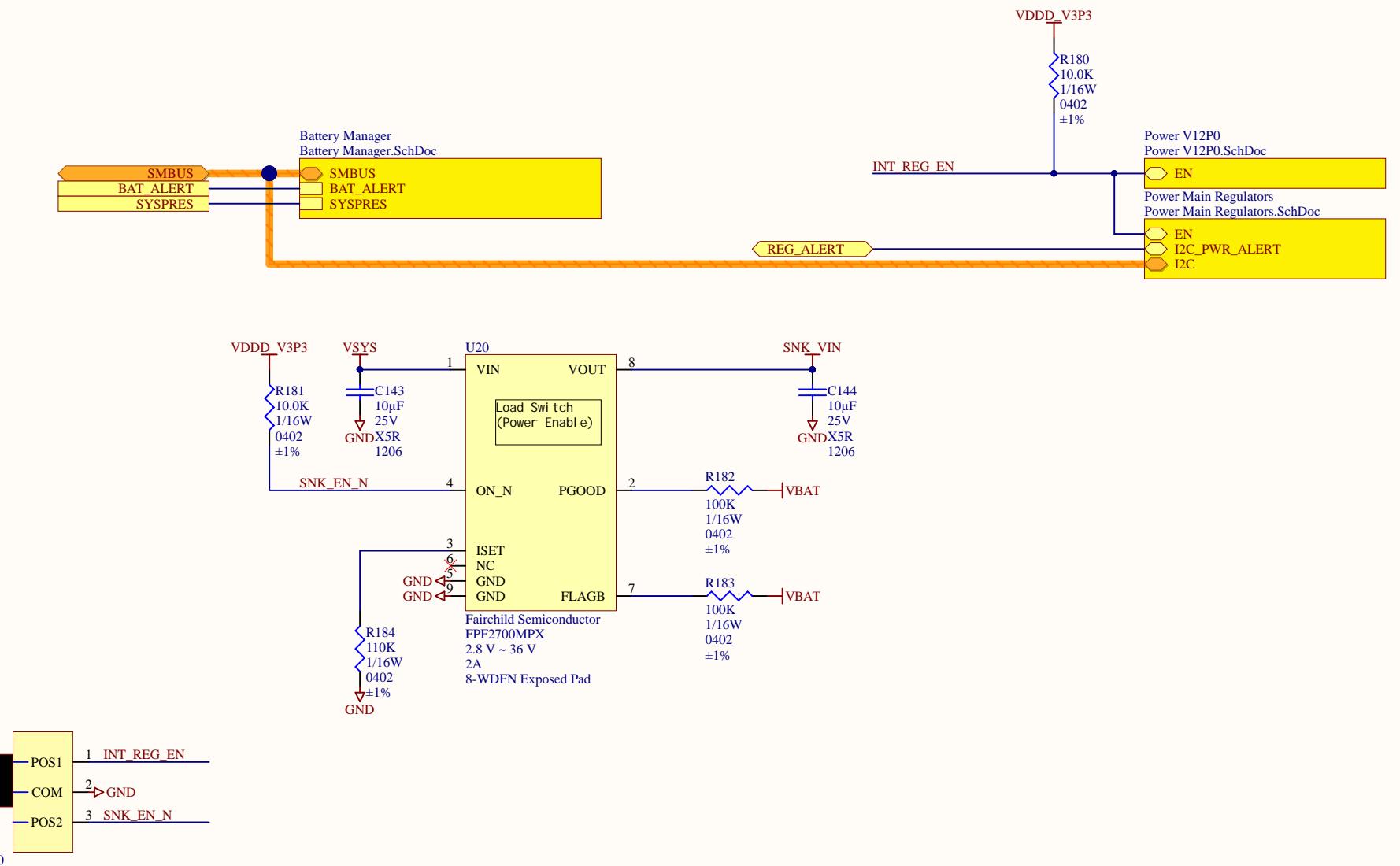


Title:	Low Speed Expansion	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Project:	Enigma	
Document:	Arduino and PMOD Connectors.SchDoc	
Engineer:	Eng	
Drawn By:	Draw	
Revision:	Rev	
Date:	7/17/2014	
Number:	14 of 20	

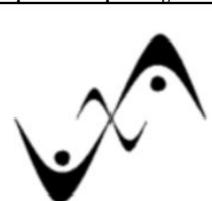


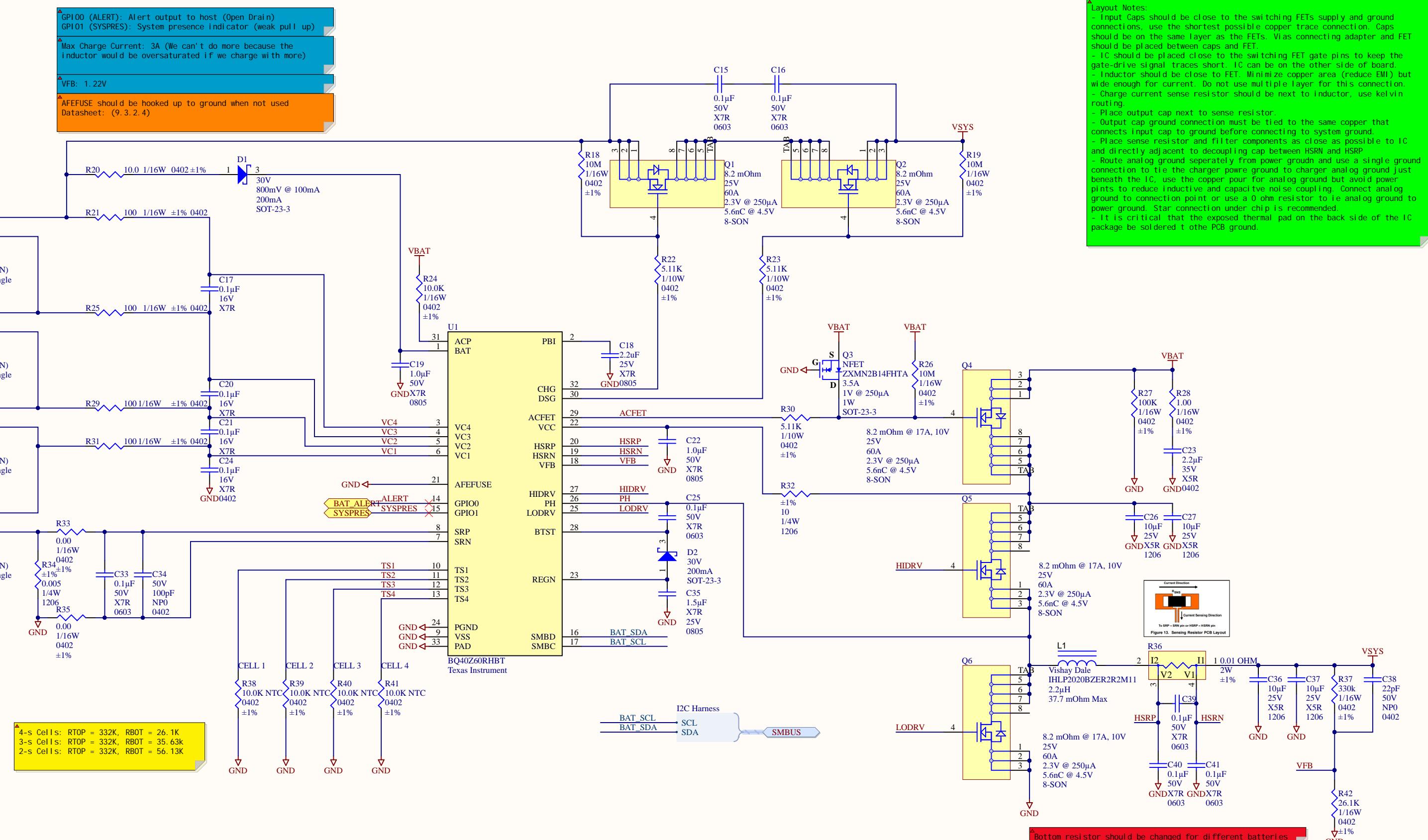




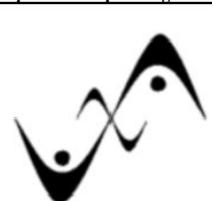


Project:	Enigma	Cospan Design
Title:	Power	<a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Document:	Power.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 17 of 20





Project:	Enigma	Cospan Design
Title:	Battery Manager	<a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Document:	Battery Manager.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 18 of 20



A

A

B

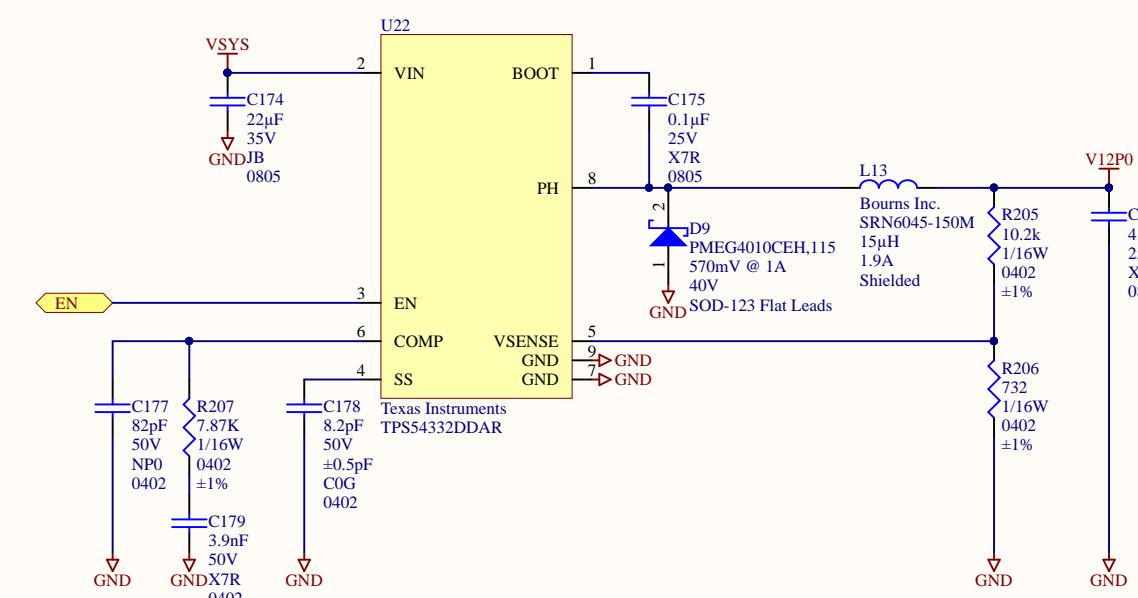
B

C

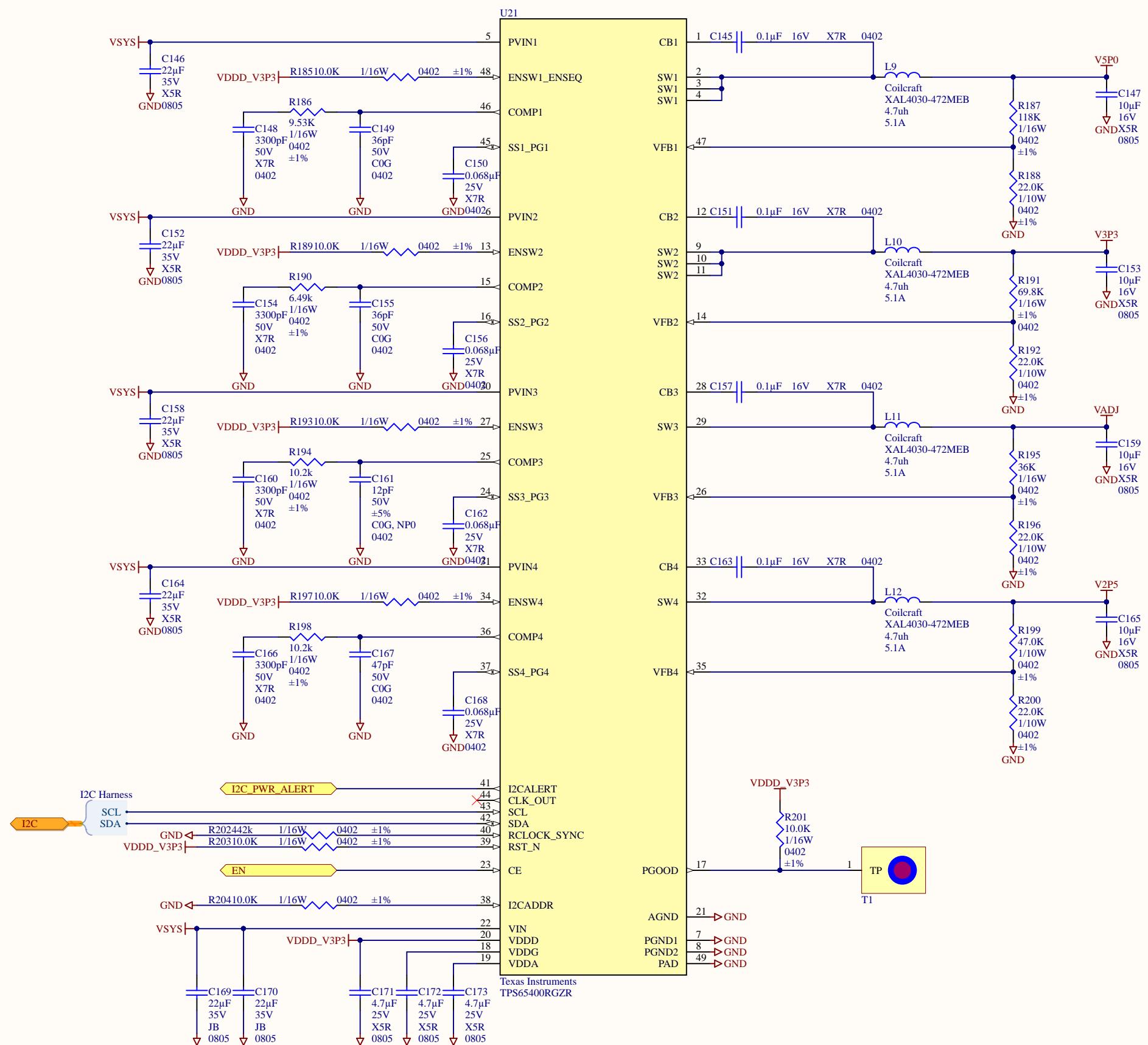
C

D

D

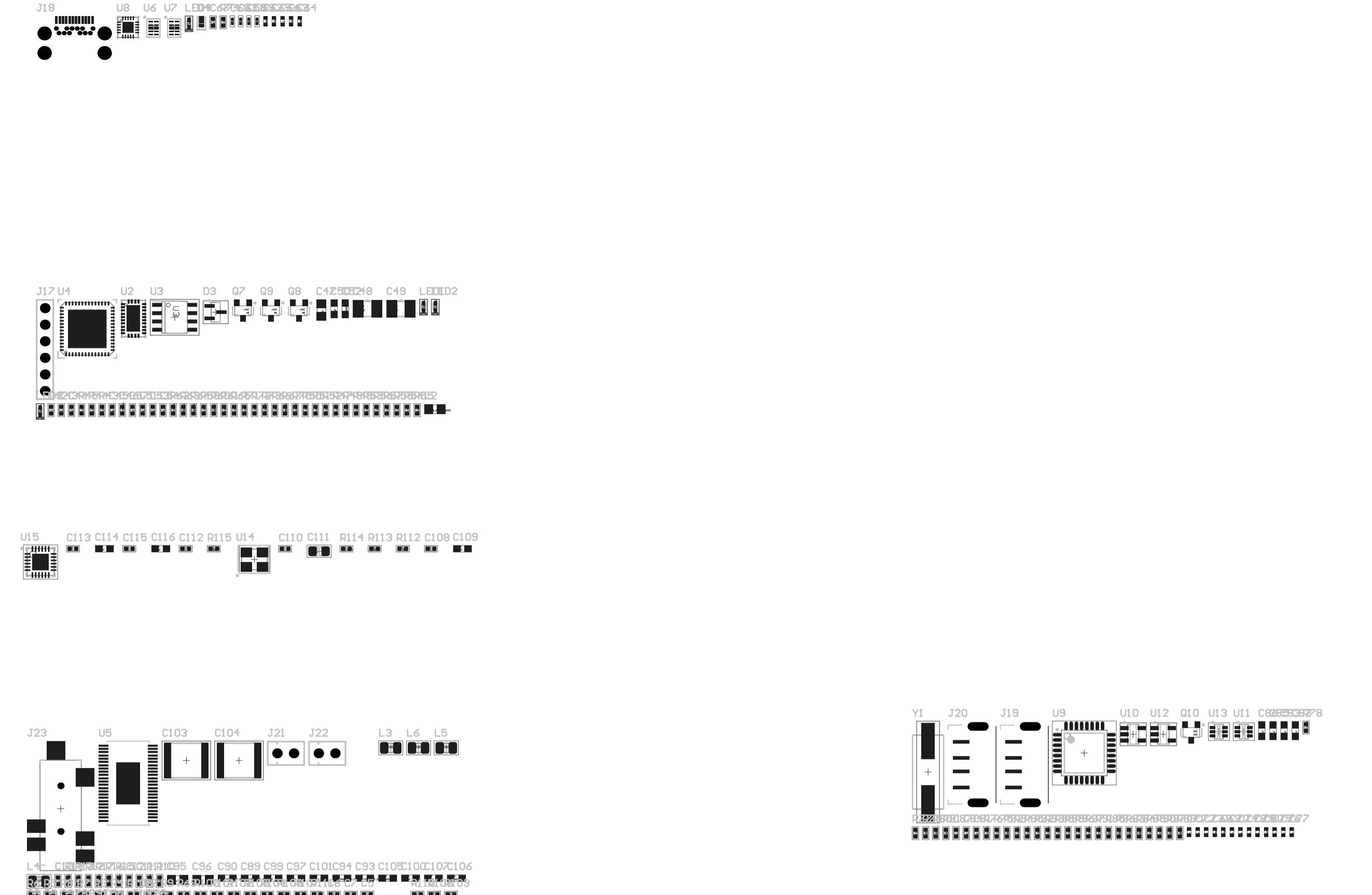
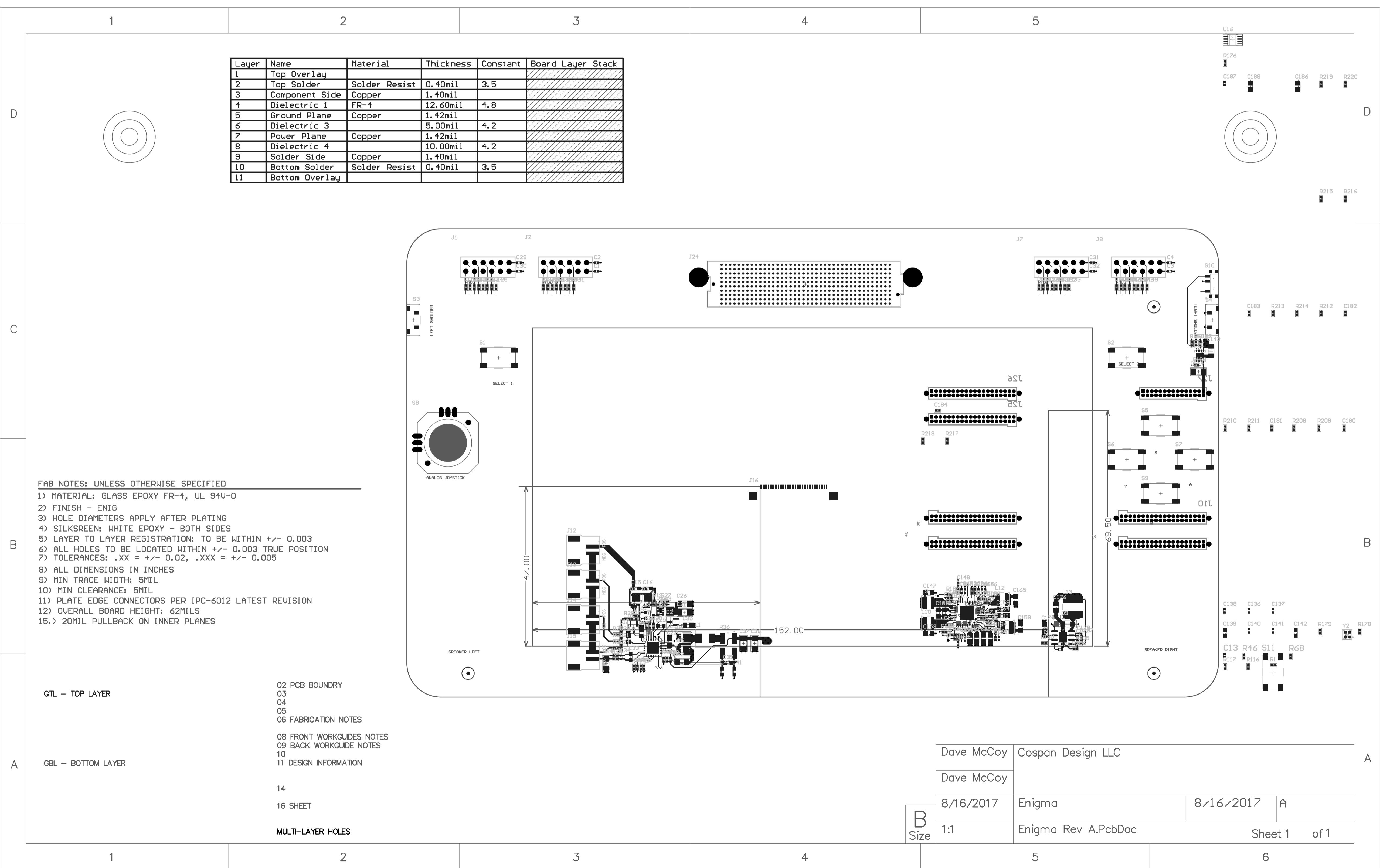


Title		
Size Tabloid	Number	Revision
Date: 8/16/2017	Sheet of	
File: C:\Users...\Power V12P0.SchDoc	Drawn By:	

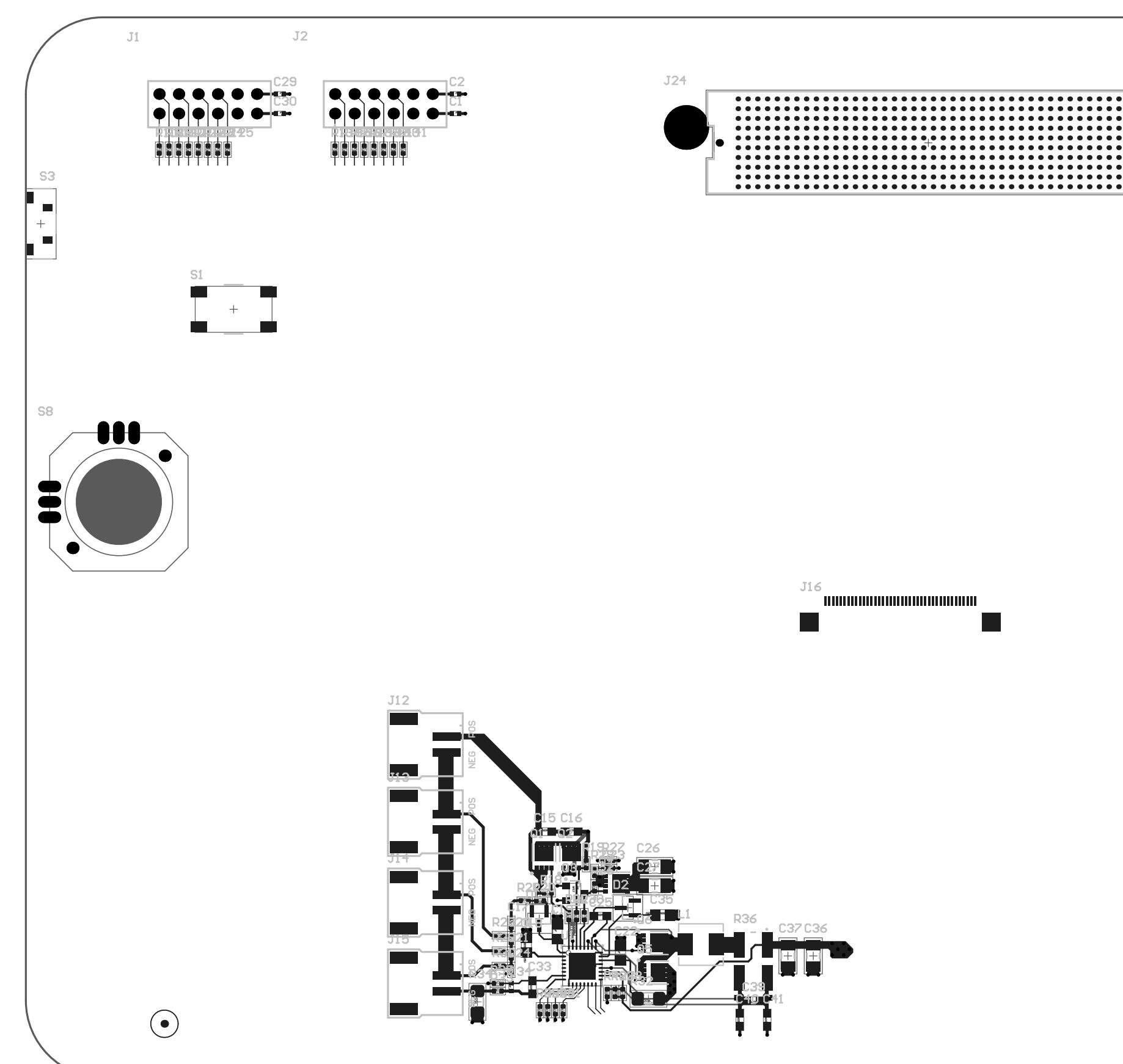


Project:	Enigma	Cospan Design <a href="http://www.cospandesign.com">http://www.cospandesign.com</a>
Title:	Main Regulator	
Document:	Power Main Regulators.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 20 of 20

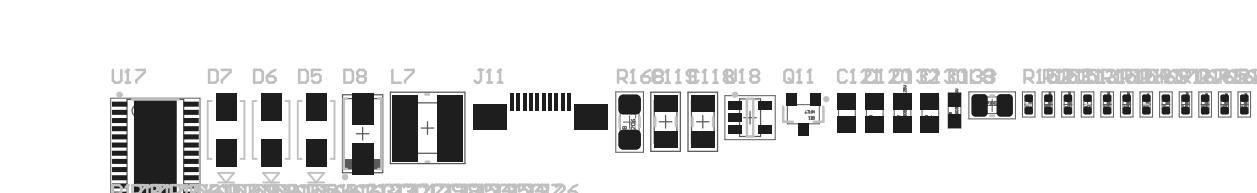
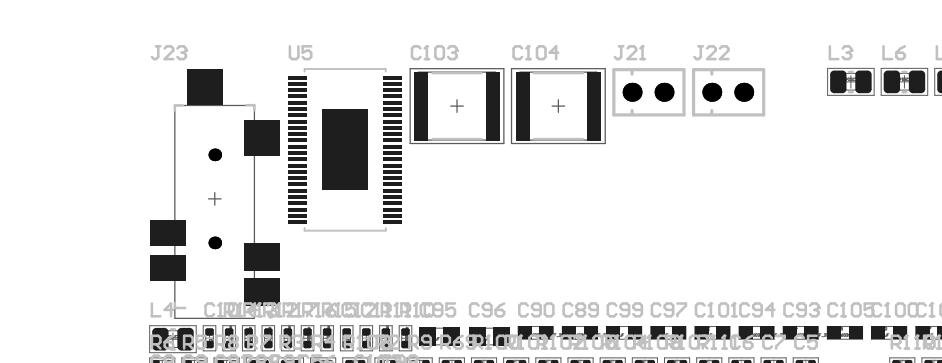
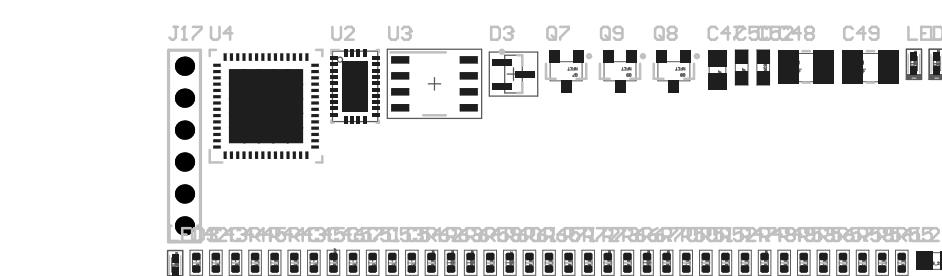
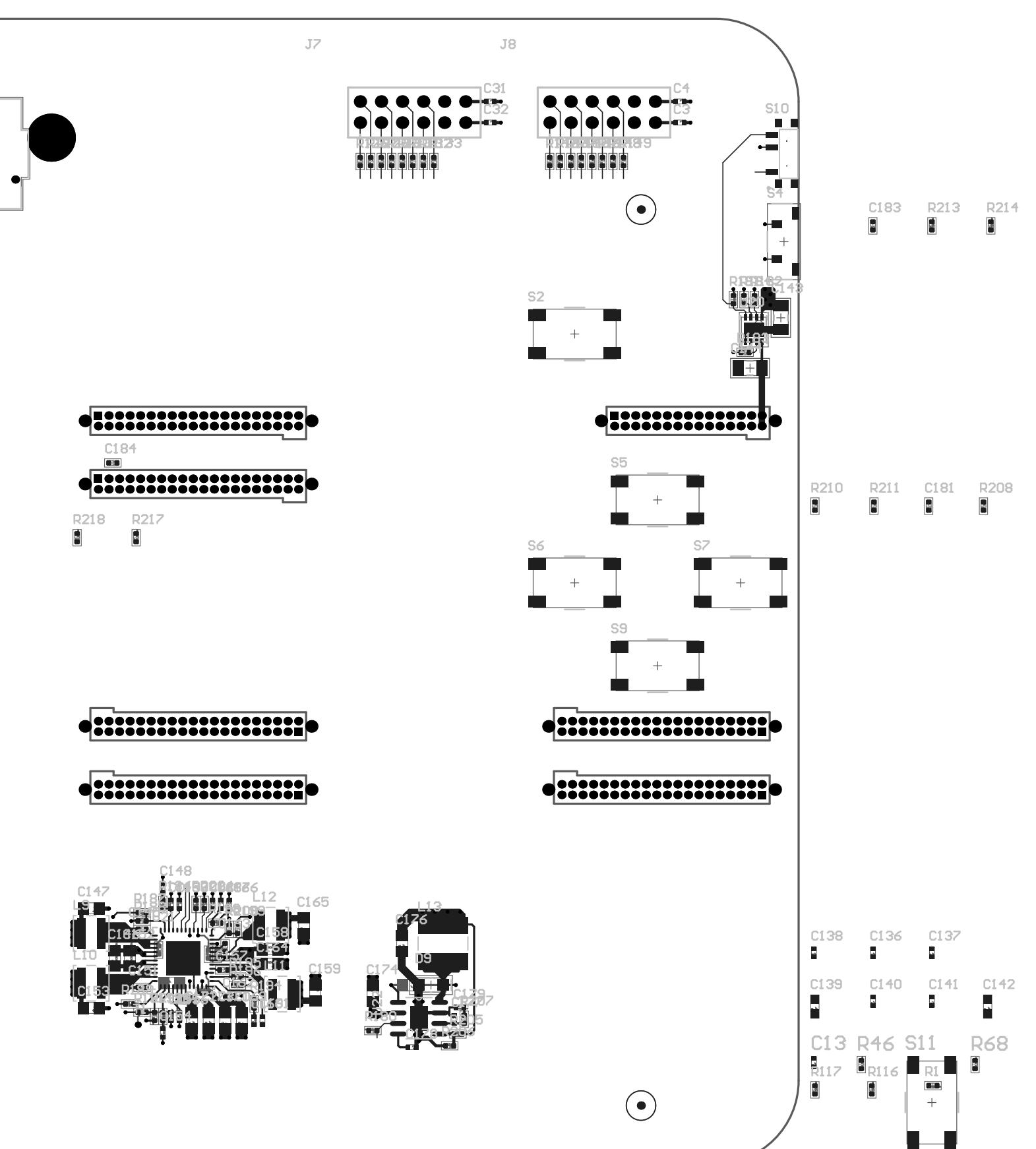




Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3		5.00mil	4.2	
7	Power Plane	Copper	1.42mil		
8	Dielectric 4		10.00mil	4.2	
9	Solder Side	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



## 02 PCB BOUNDARY



GTL – TOP LAYER

#### **GBL – BOTTOM LAYER**

