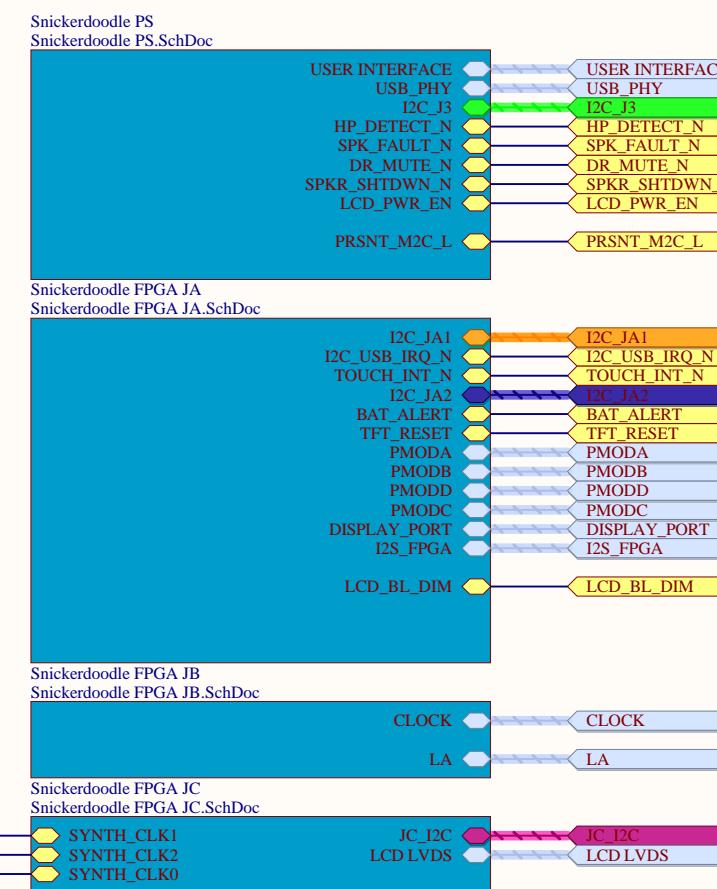


All banks are HR

A



B

A

B

C

D

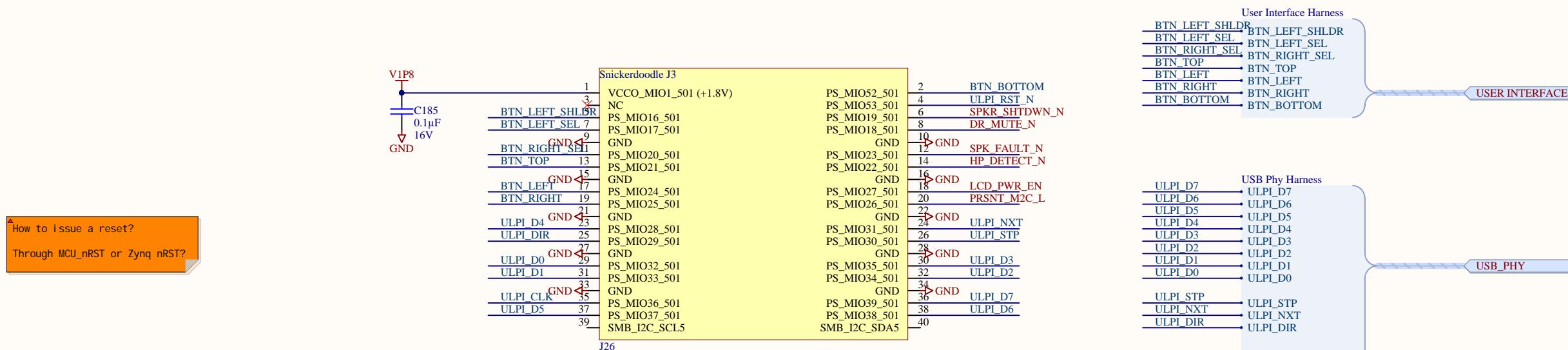
D

Not SnickerDoodle's Internal regulators for powering this board, but it would be good to make sure I2C is at the correct pullups

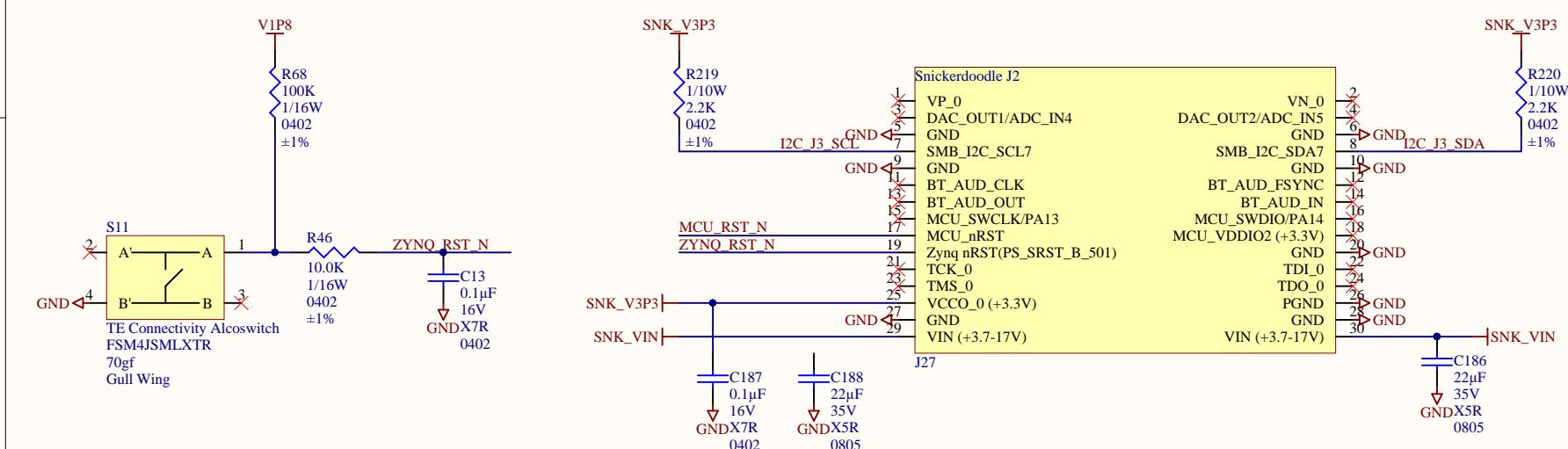
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle Top	
Document:	Snickerdoodle.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/17/2017	Number: 2 of 20



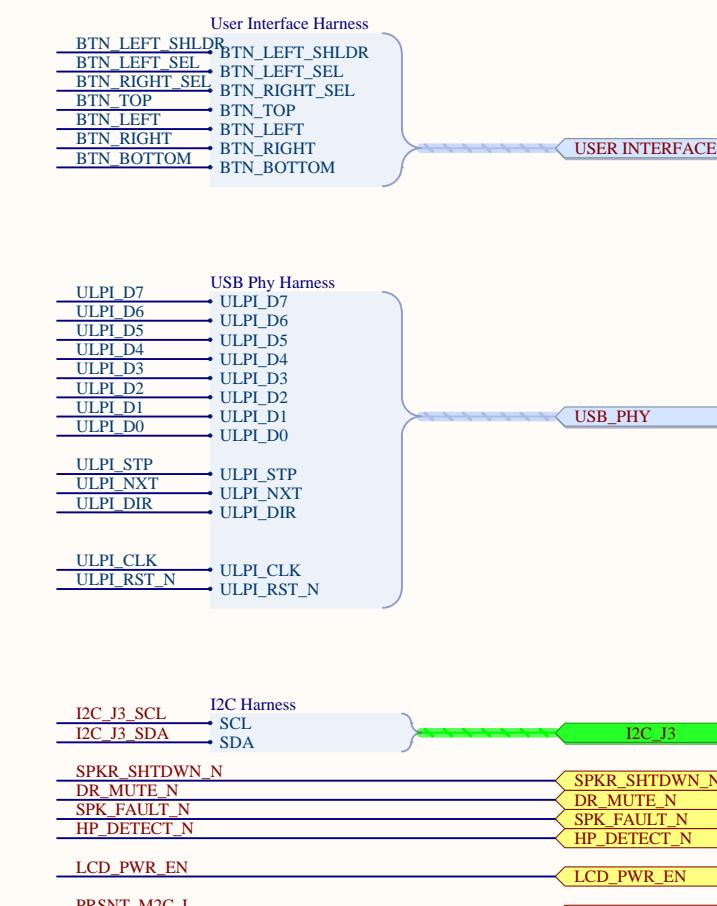
A



B



C

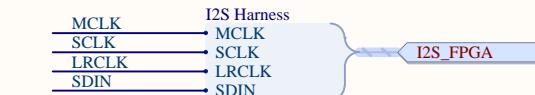
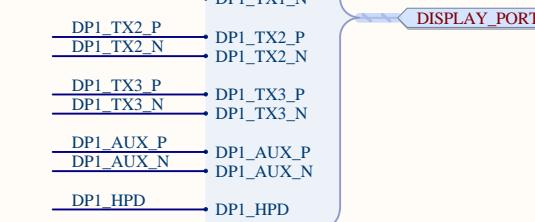
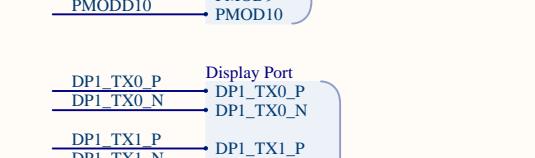
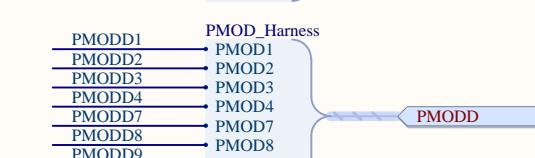
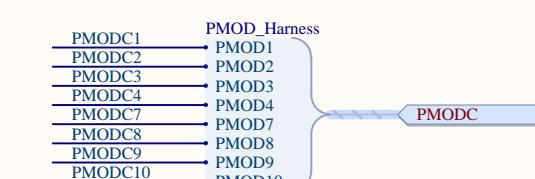
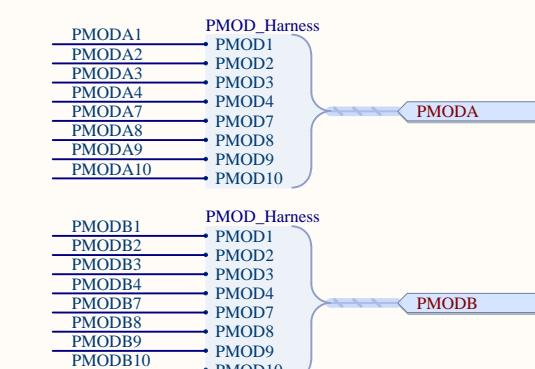
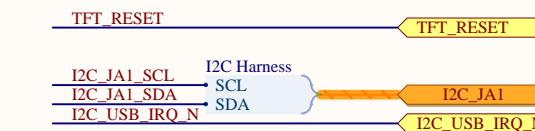
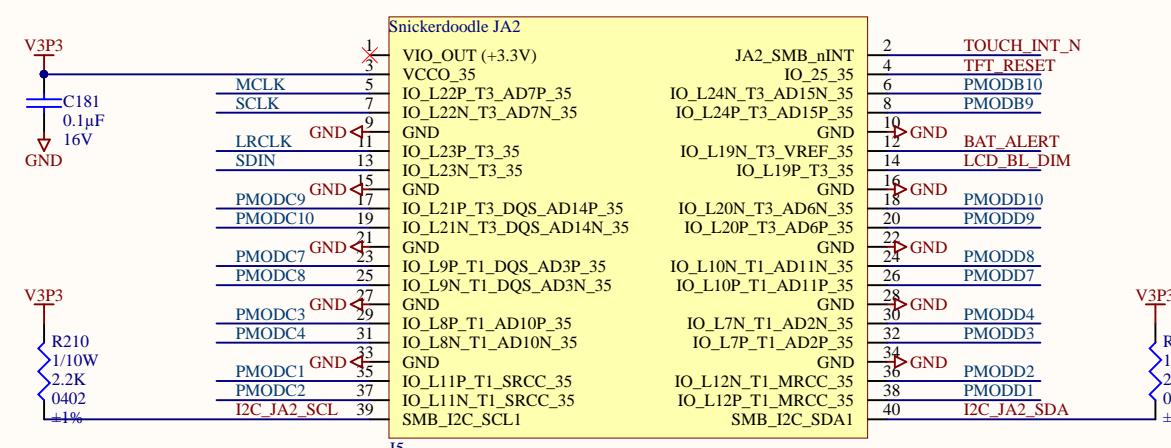
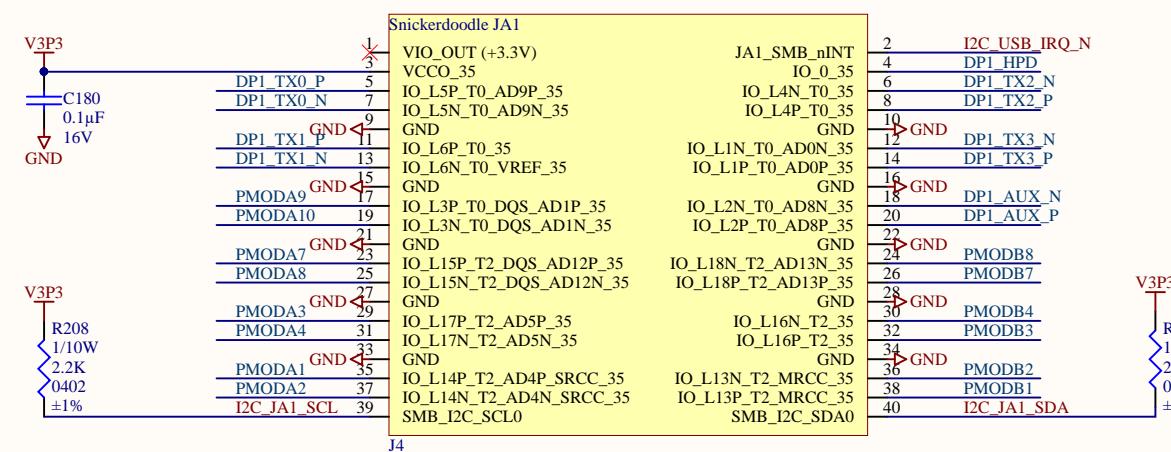


D

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle PS	
Document:	Snickerdoodle PS.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	
Revision:	A	
Date:	8/16/2017	
Number:	3 of 20	



Do I need external differential termination like on the Spartan 6 FPGAs?

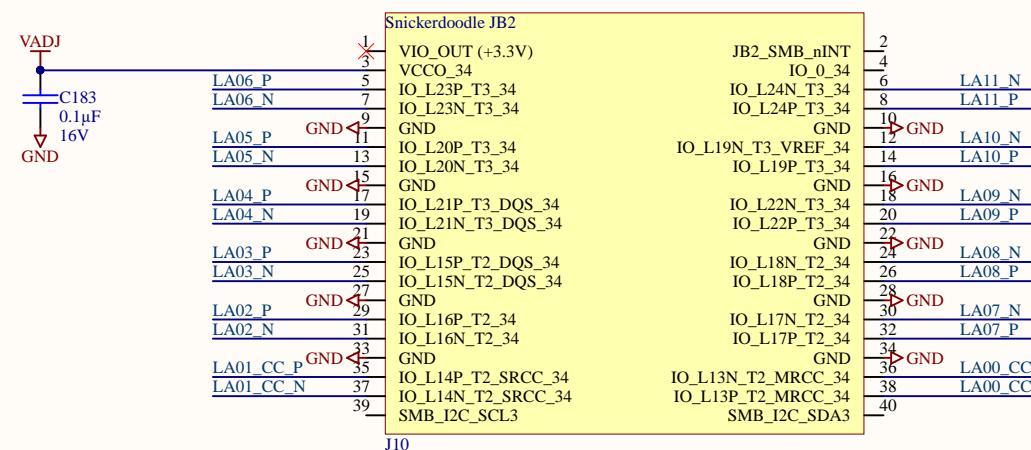
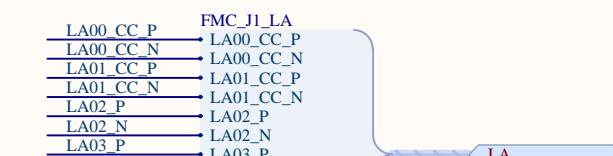
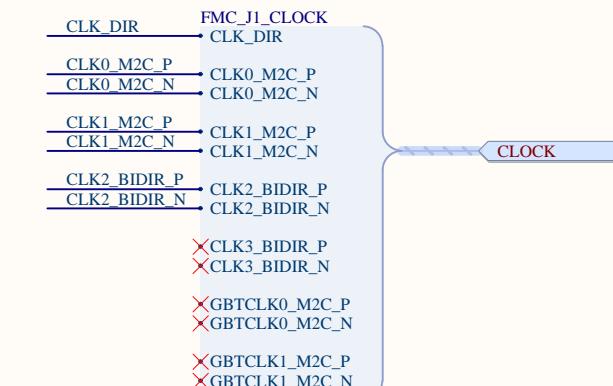
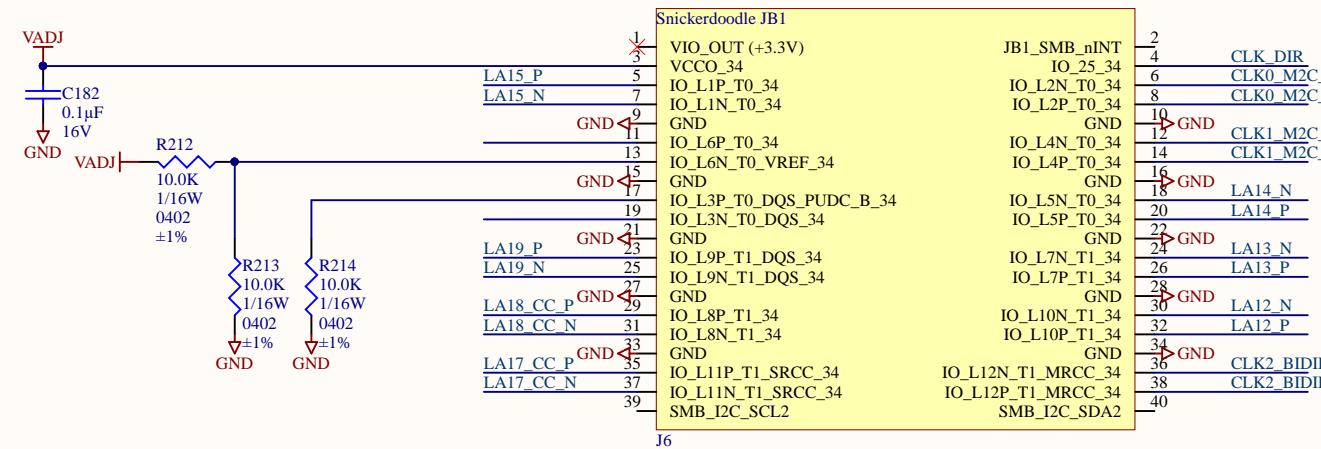


Do I need parallel termination of the Display Port Signals??

Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle JA	
Document:	Snickerdoodle FPGA JA.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/17/2017	Number: 4 of 20



A

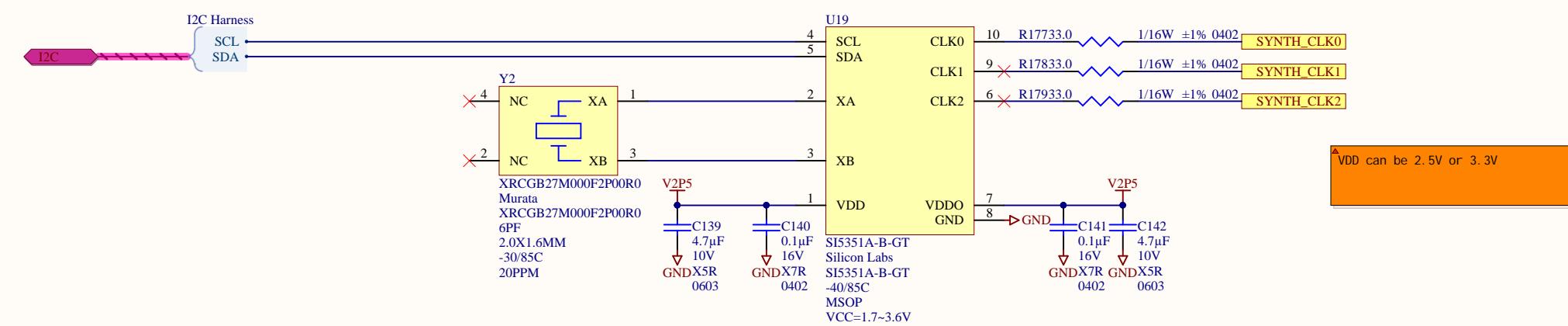


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle JB	
Document:	Snickerdoodle FPGA JB.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	
Revision:	A	
Date:	8/16/2017	
Number:	5 of 20	



A

A



B

B

C

C

D

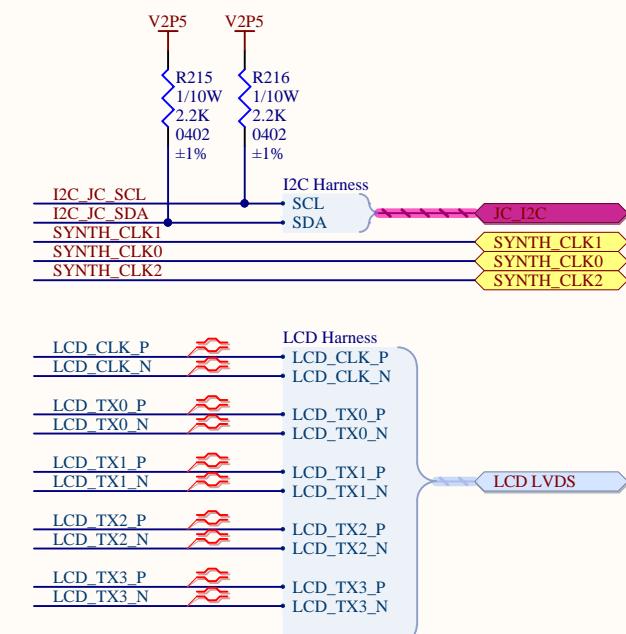
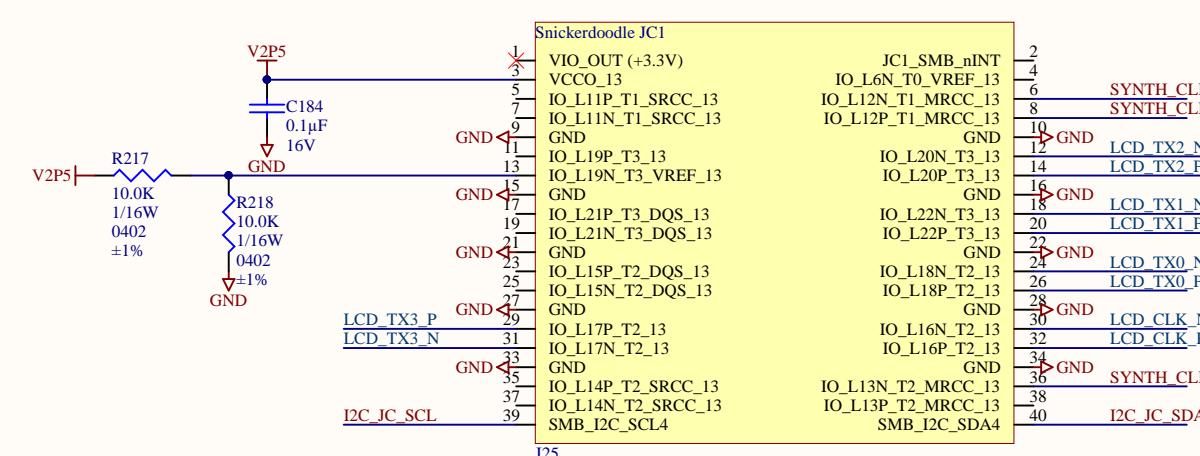
D

Project:	Project_Name	Cospan Design http://www.cospandesign.com
Title:	Clock Synthesizer	
Document:	Clock Synth.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: Rev
Date:	8/16/2017	Number: 6 of 20



A

Should I use VREF??



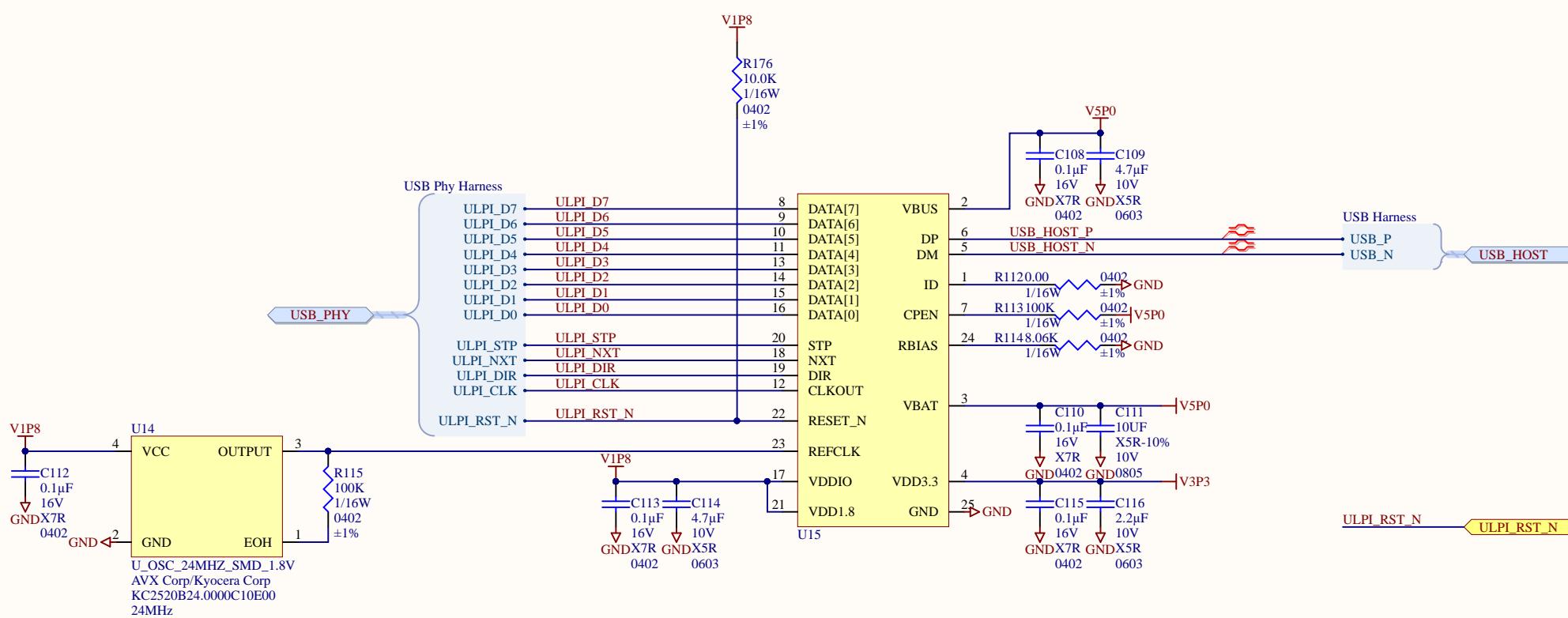
B

C

D

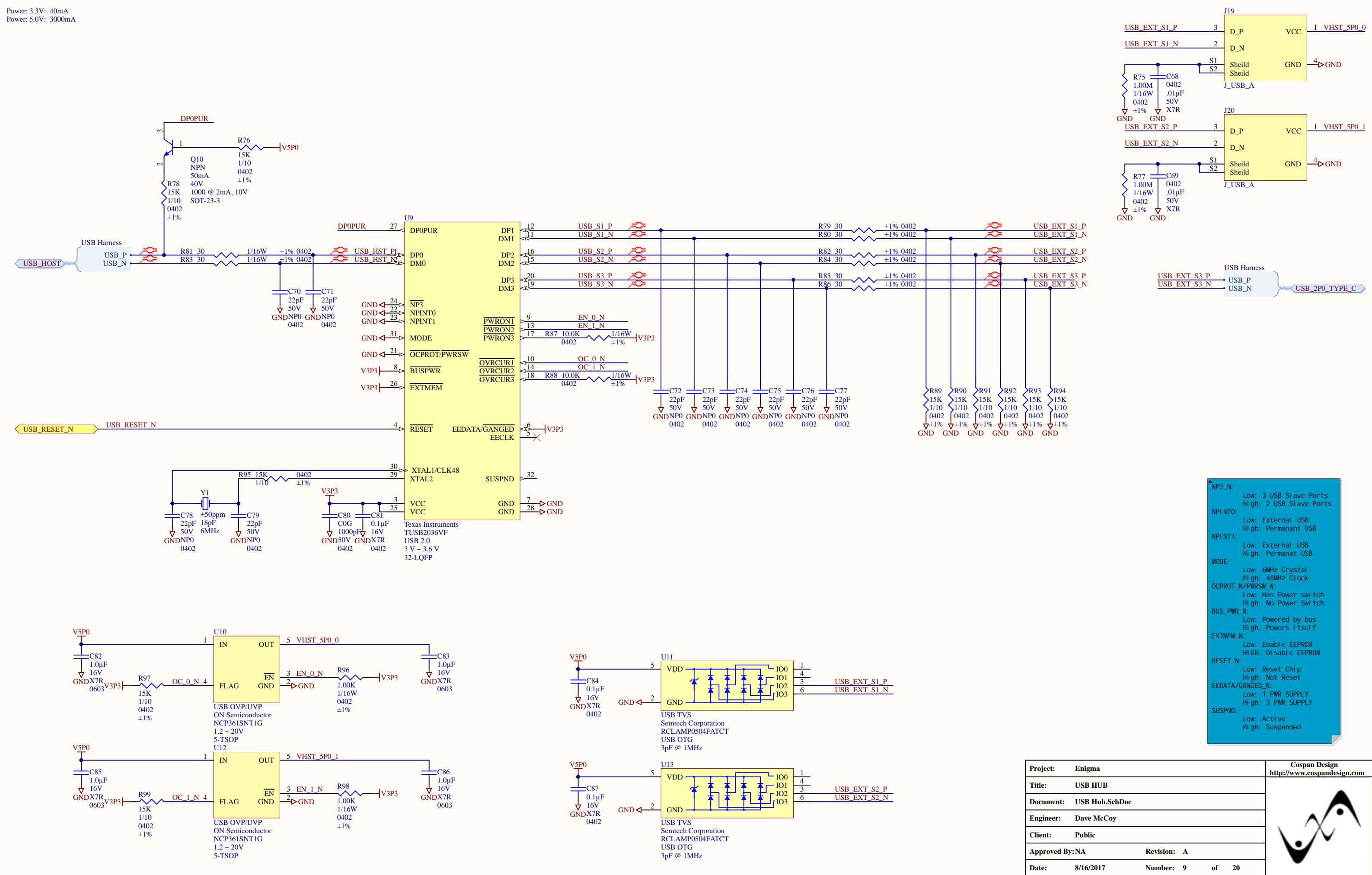
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	Snickerdoodle JC	
Document:	Snickerdoodle FPGA JC.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 7 of 20

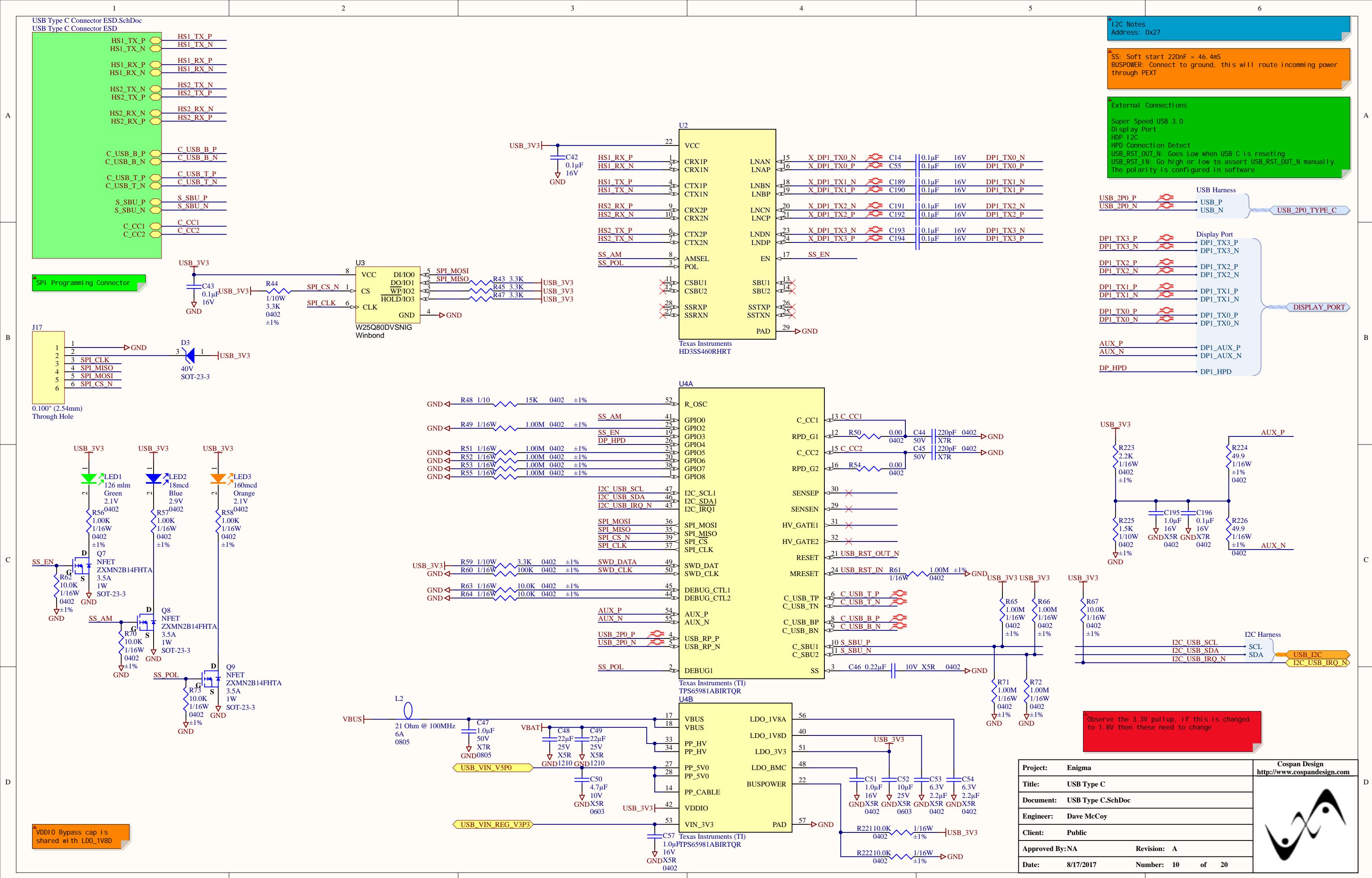


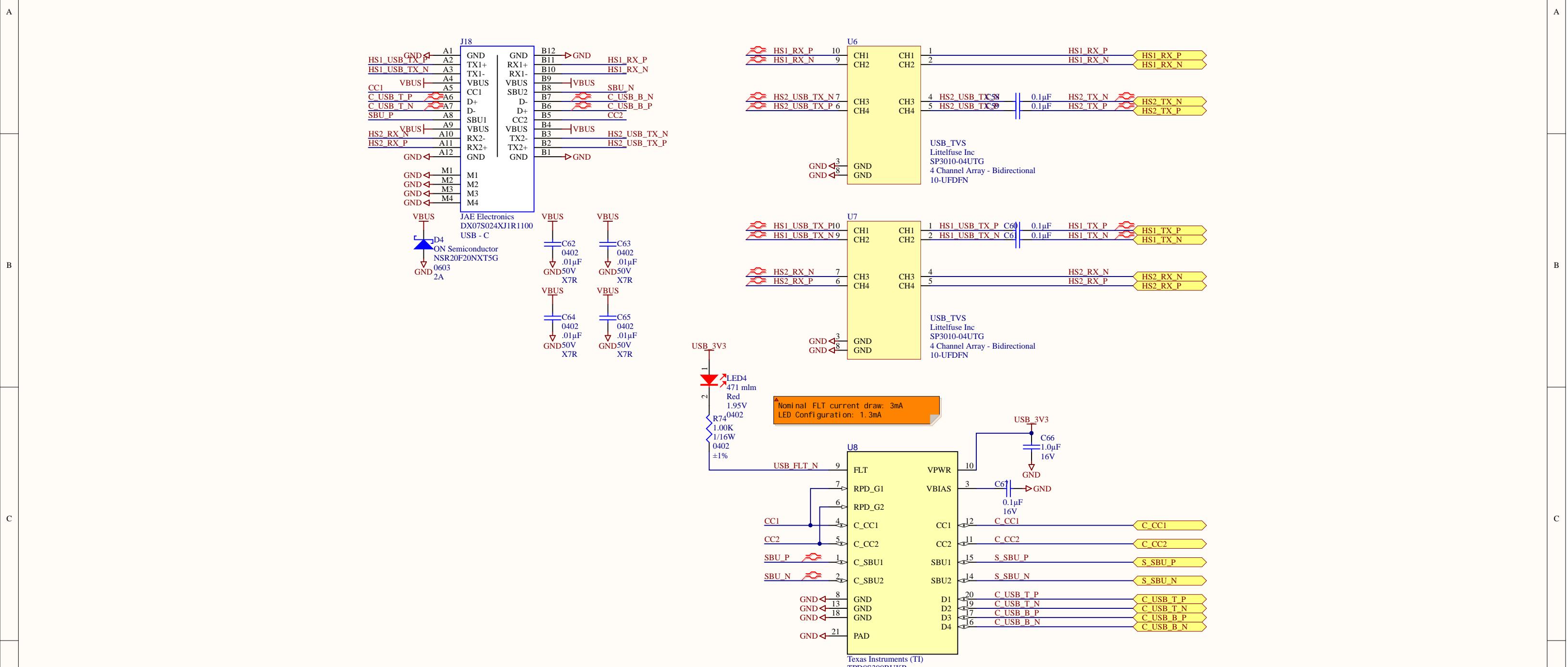


Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	USB Phy	
Document:	USB Phy.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 8 of 20



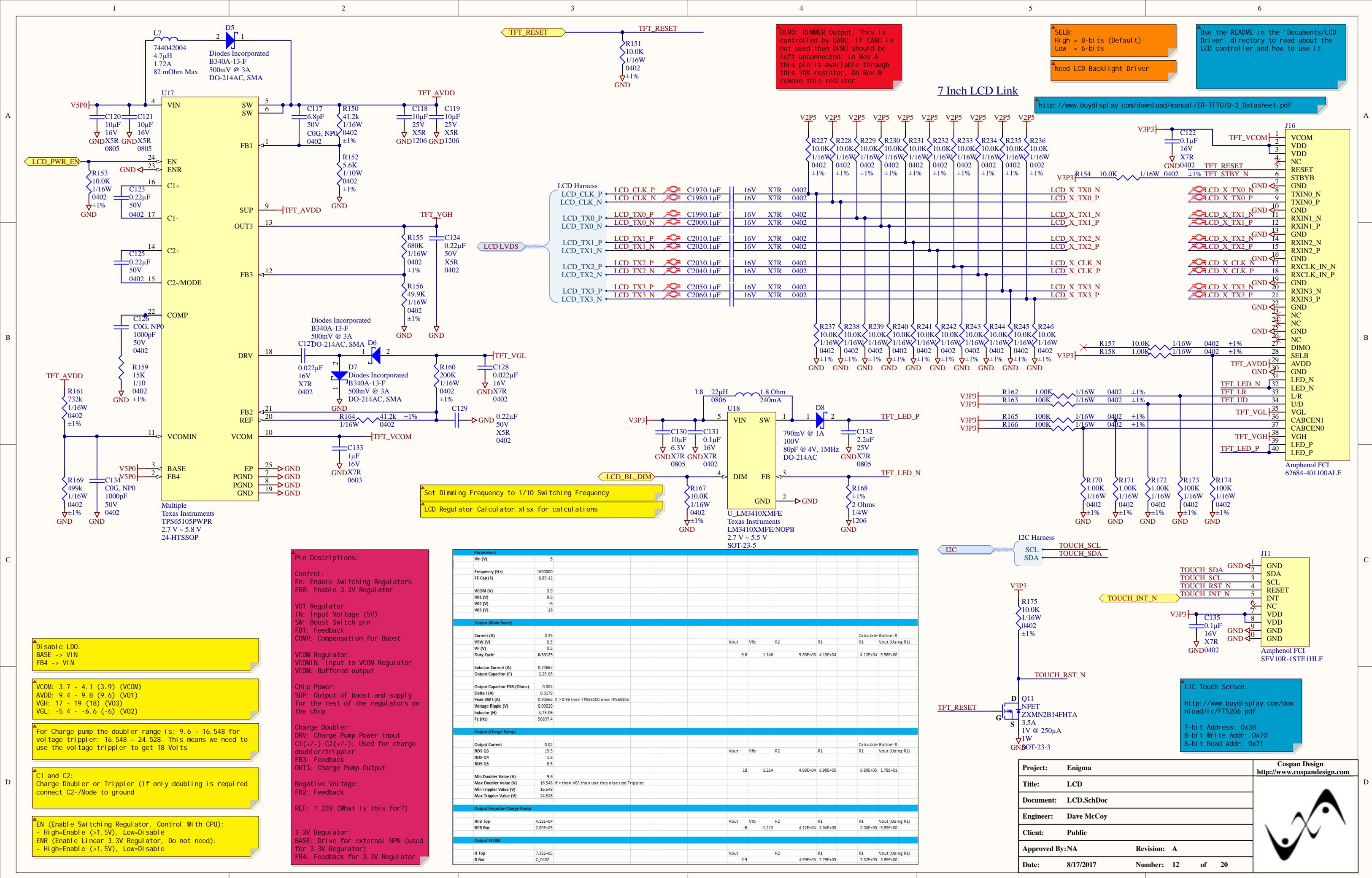


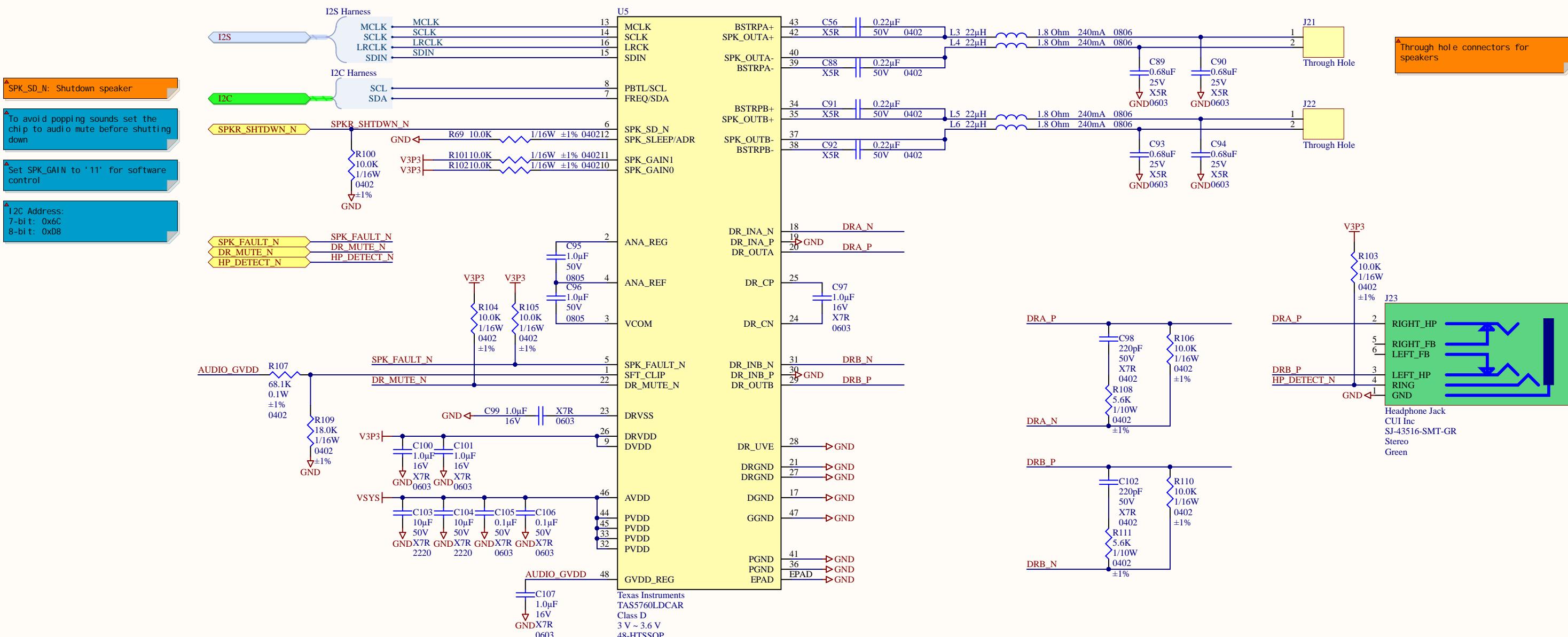




Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	USB Type C Connector	
Document:	USB Type C Connector ESD.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 11 of 20



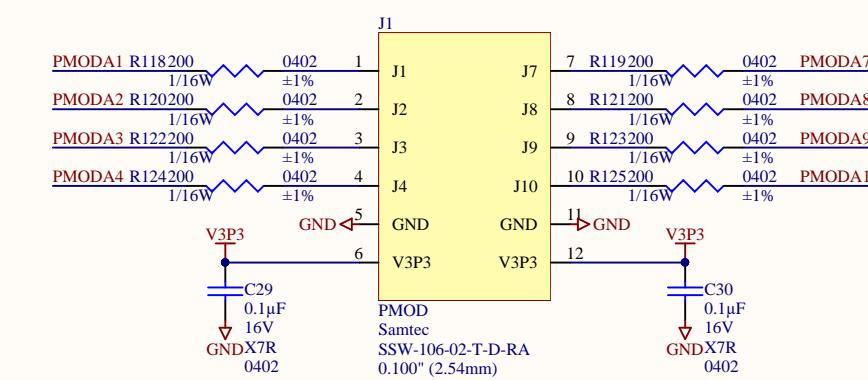




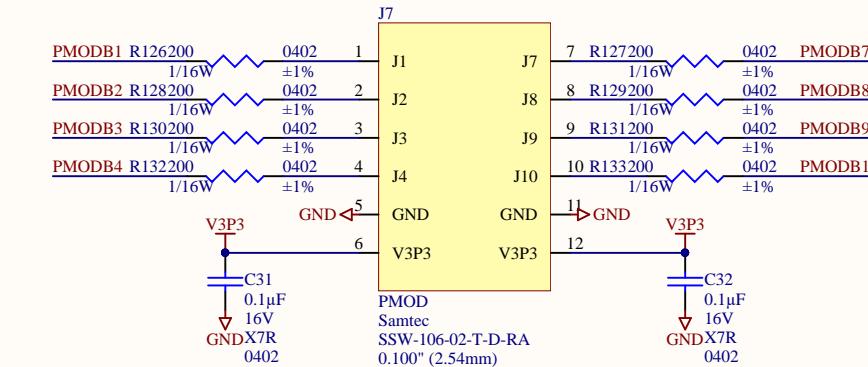
Project:	Enigma	Cospan Design http://www.cospandesign.com
Title:	I2S Codec/Amplifier	
Document:	I2S Audio.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:NA	Revision: A	
Date:	8/16/2017	Number: 13 of 20



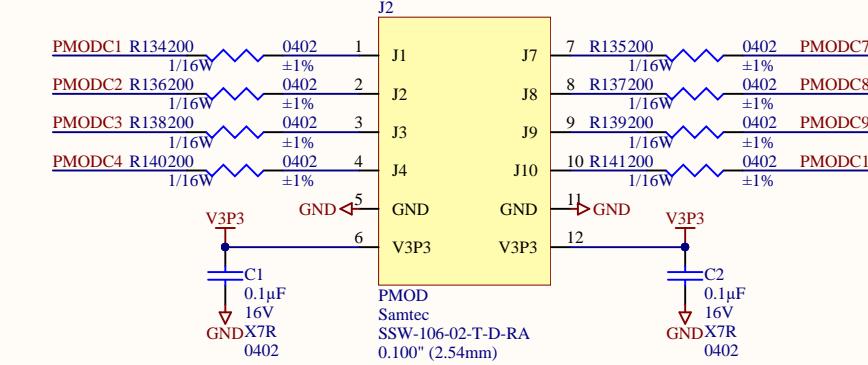
A



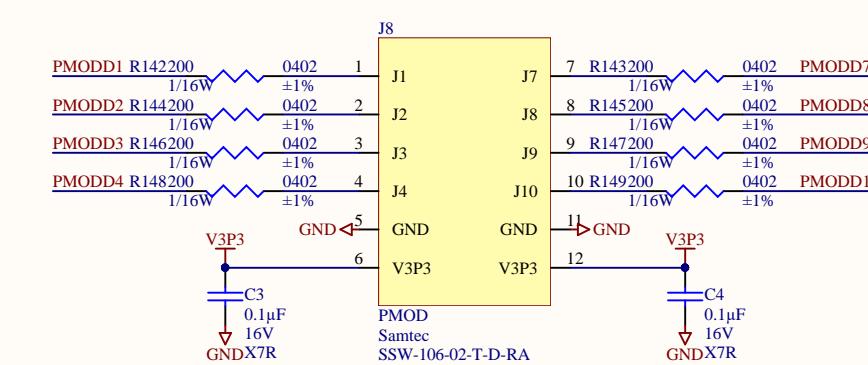
B



C

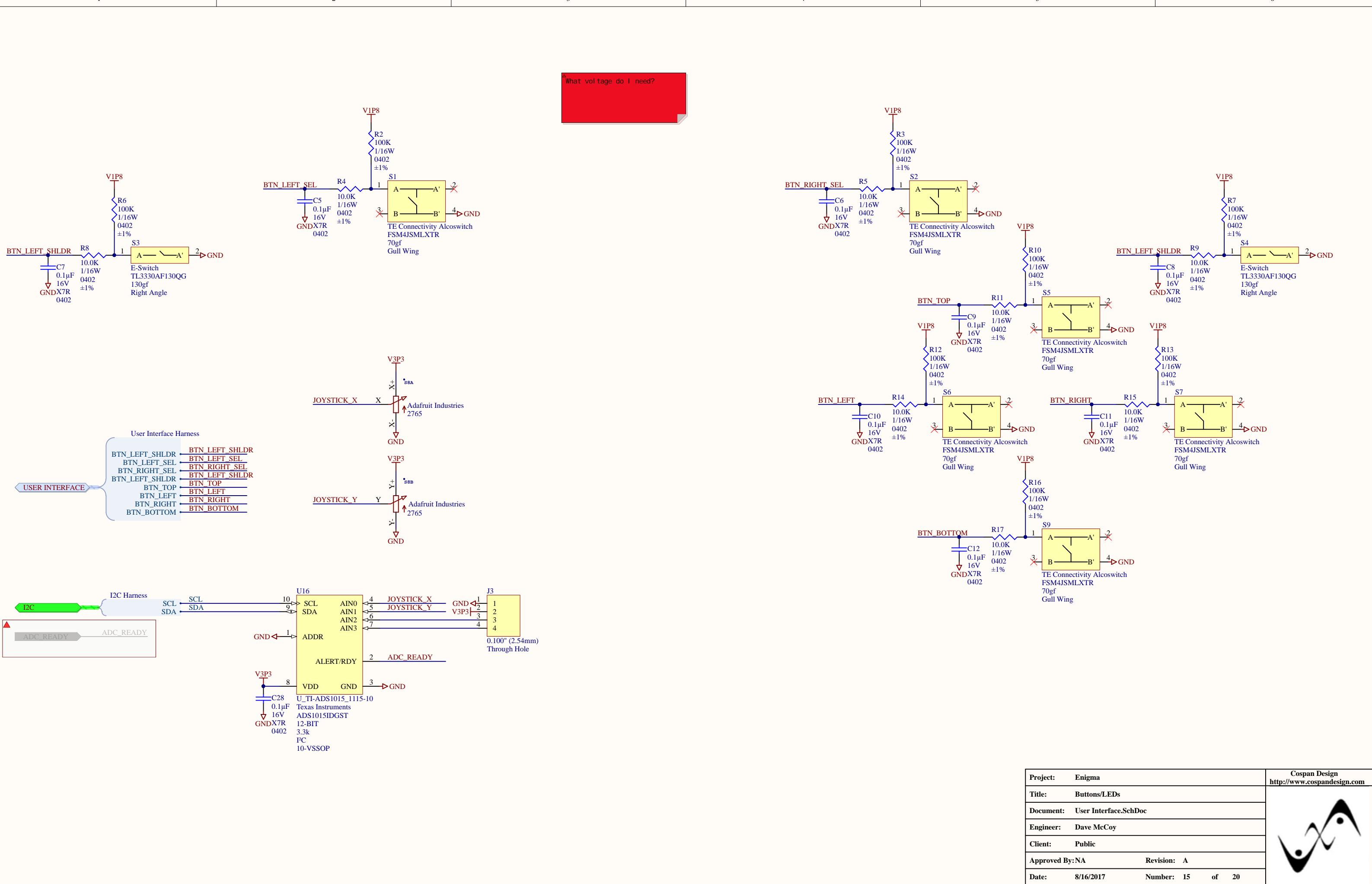


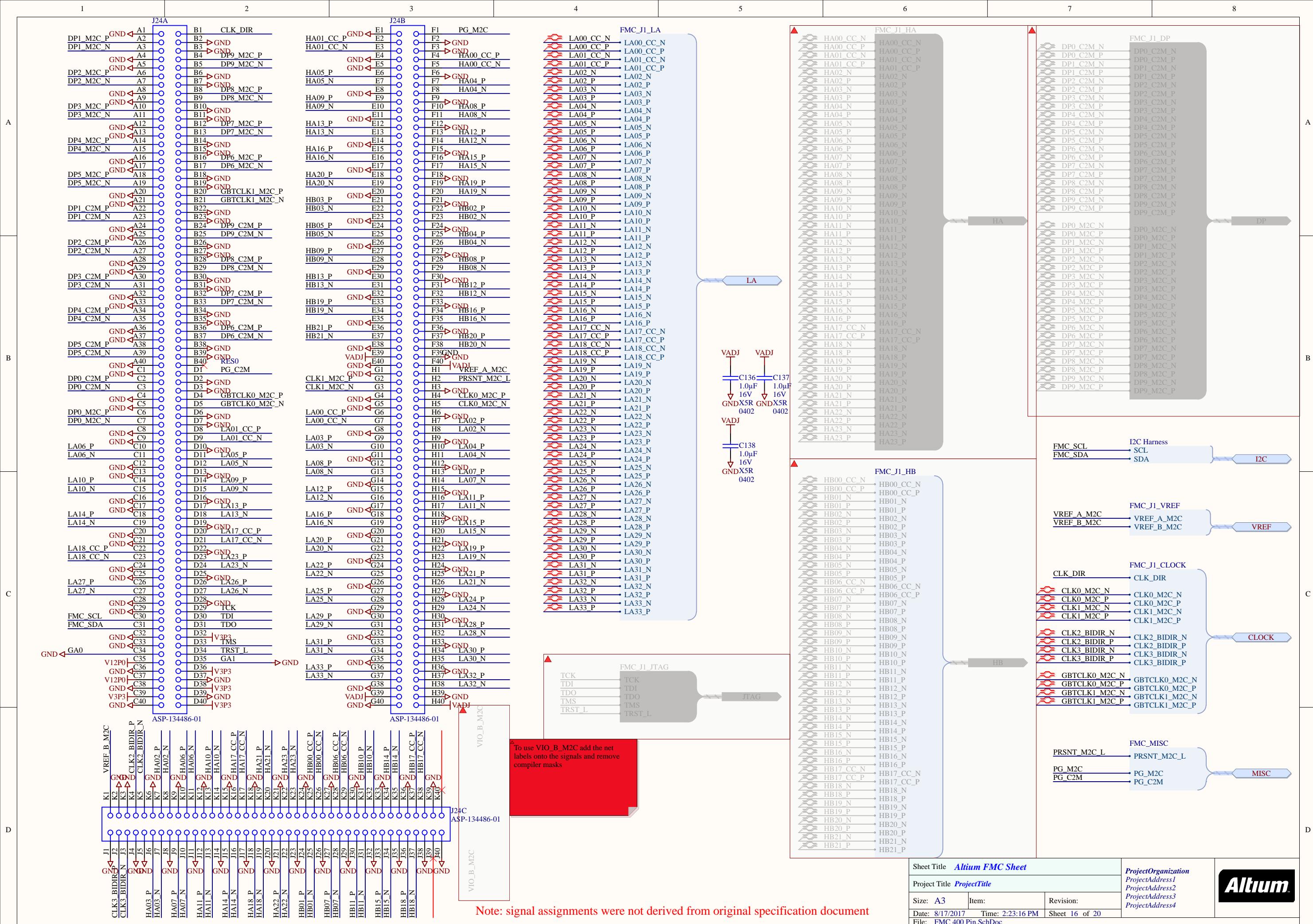
D

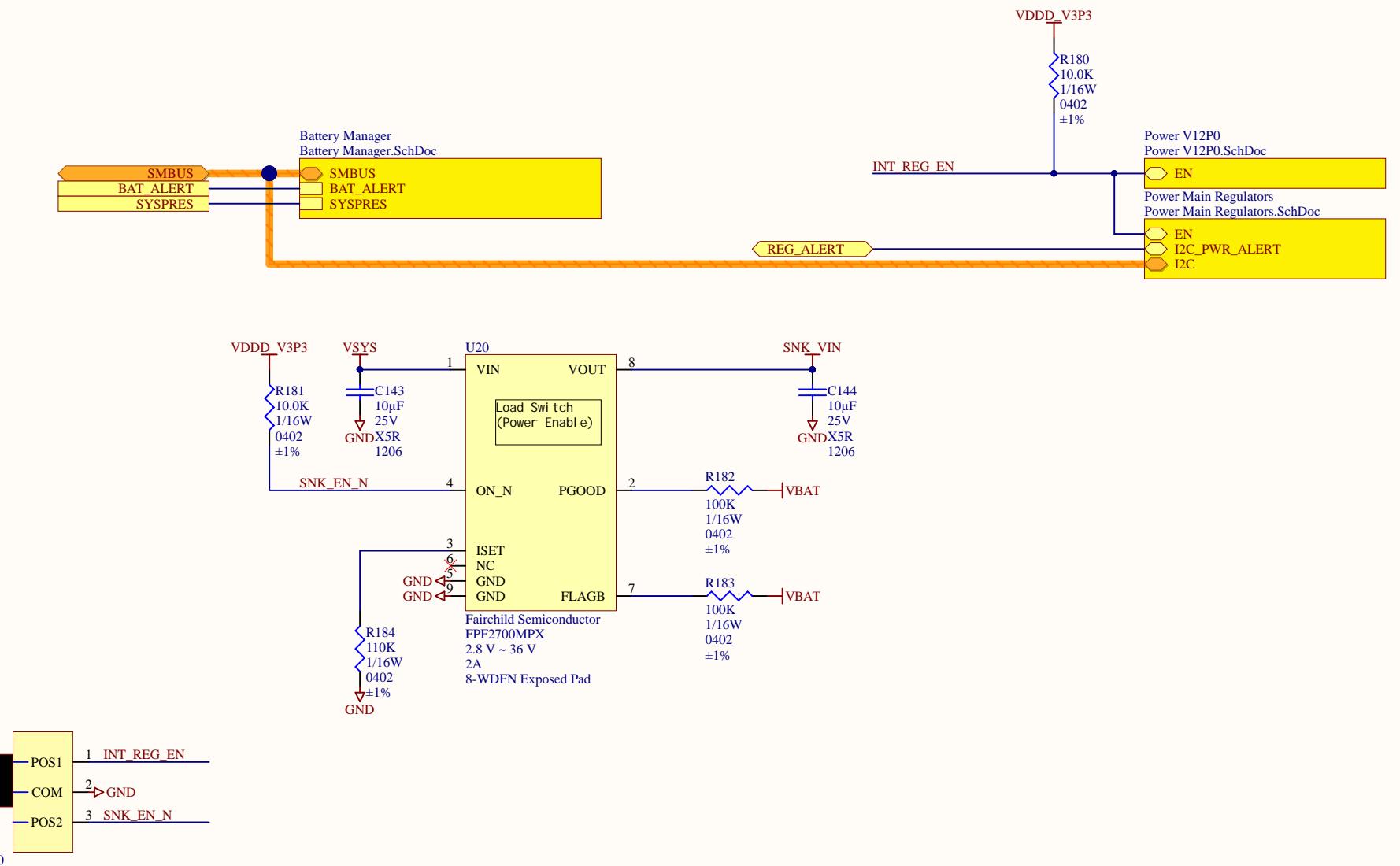


Title:	Low Speed Expansion	Cospan Design http://www.cospandesign.com
Project:	Enigma	
Document:	Arduino and PMOD Connectors.SchDoc	
Engineer:	Eng	
Drawn By:	Draw	
Revision:	Rev	
Date:	7/17/2014	
Number:	14 of 20	

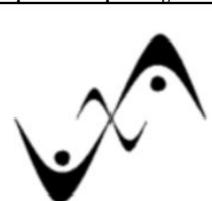




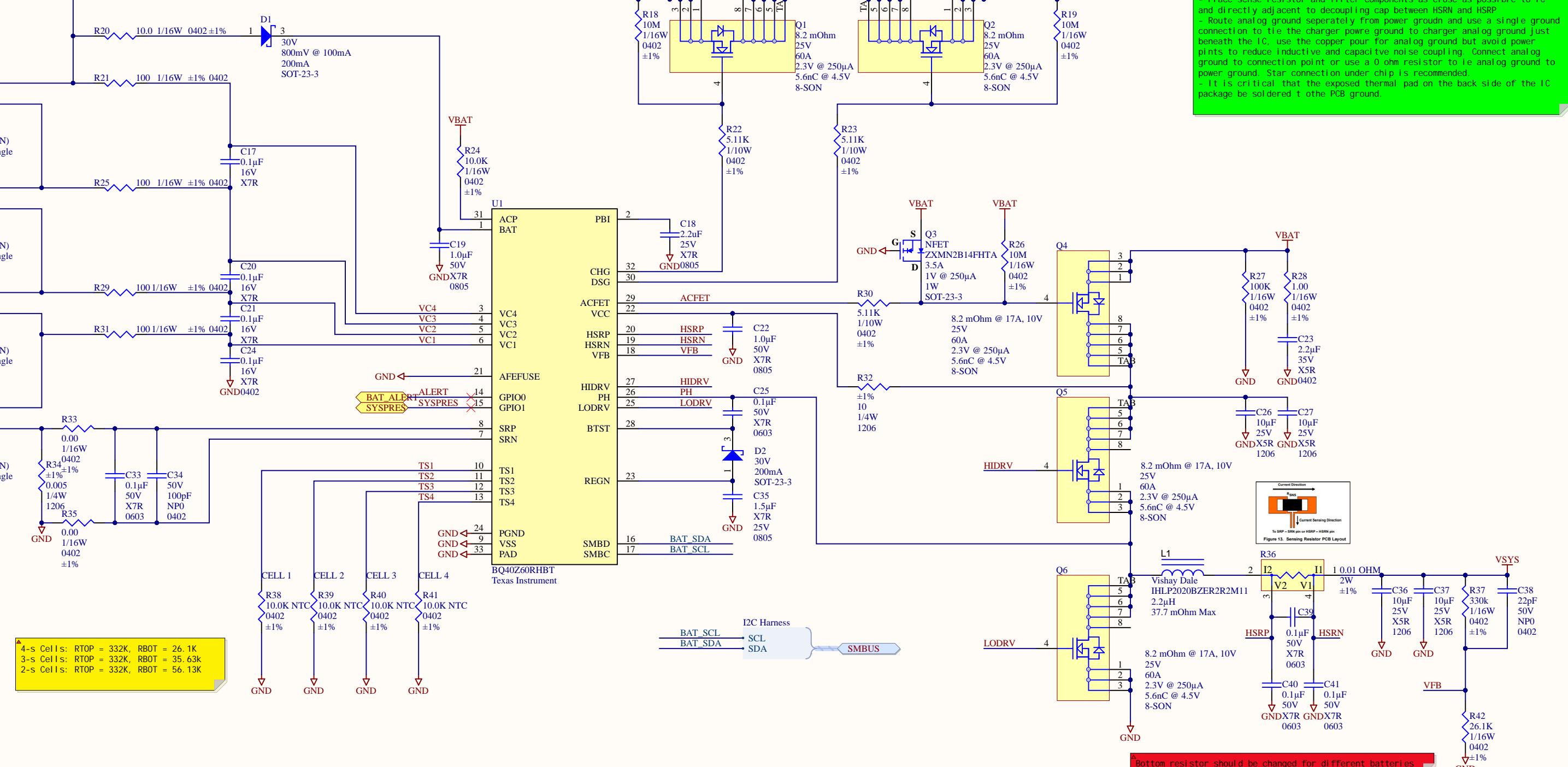




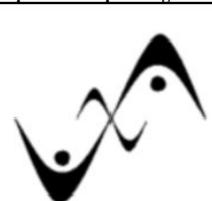
Project:	Enigma	Cospan Design
Title:	Power	http://www.cospandesign.com
Document:	Power.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 17 of 20



▲ GPI00 (ALERT): Alert output to host (Open Drain)
 ▲ GPI01 (SYSPRES): System presence indicator (weak pull up)
 ▲ Max Charge Current: 3A (We can't do more because the inductor would be oversaturated if we charge with more)
 ▲ VFB: 1.22V
 ▲ AFEFUSE should be hooked up to ground when not used
 Datasheet: (9.3.2.4)



Project:	Enigma	Cospan Design
Title:	Battery Manager	http://www.cospandesign.com
Document:	Battery Manager.SchDoc	
Engineer:	Dave McCoy	
Client:	Public	
Approved By:	NA	Revision: A
Date:	8/16/2017	Number: 18 of 20



A

A

B

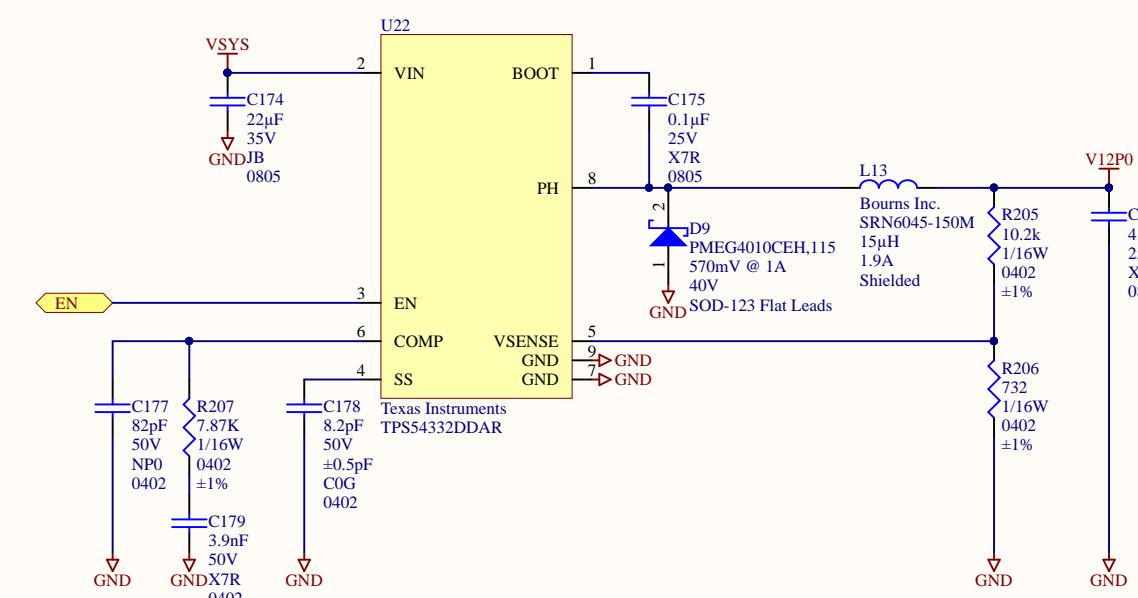
B

C

C

D

D



Title		
Size Tabloid	Number	Revision
Date: 8/17/2017	Sheet of	
File: C:\Users...\Power V12P0.SchDoc	Drawn By:	

A

All VFB can be changed through the I2C interface from 0.6 to 1.87 with a default value of 0.8V

B

C

D

I2C Slave Address:
Write: 0xD2
Read: 0x03
7-bit address: 0x69

E

F

G

H

I

J

K

L

M

N

O

P

Q

R

S

T

U

V

W

X

Y

Z

A

B

C

D

E

F

G

H

I

J

K

L

M

N

O

P

Q

R

S

T

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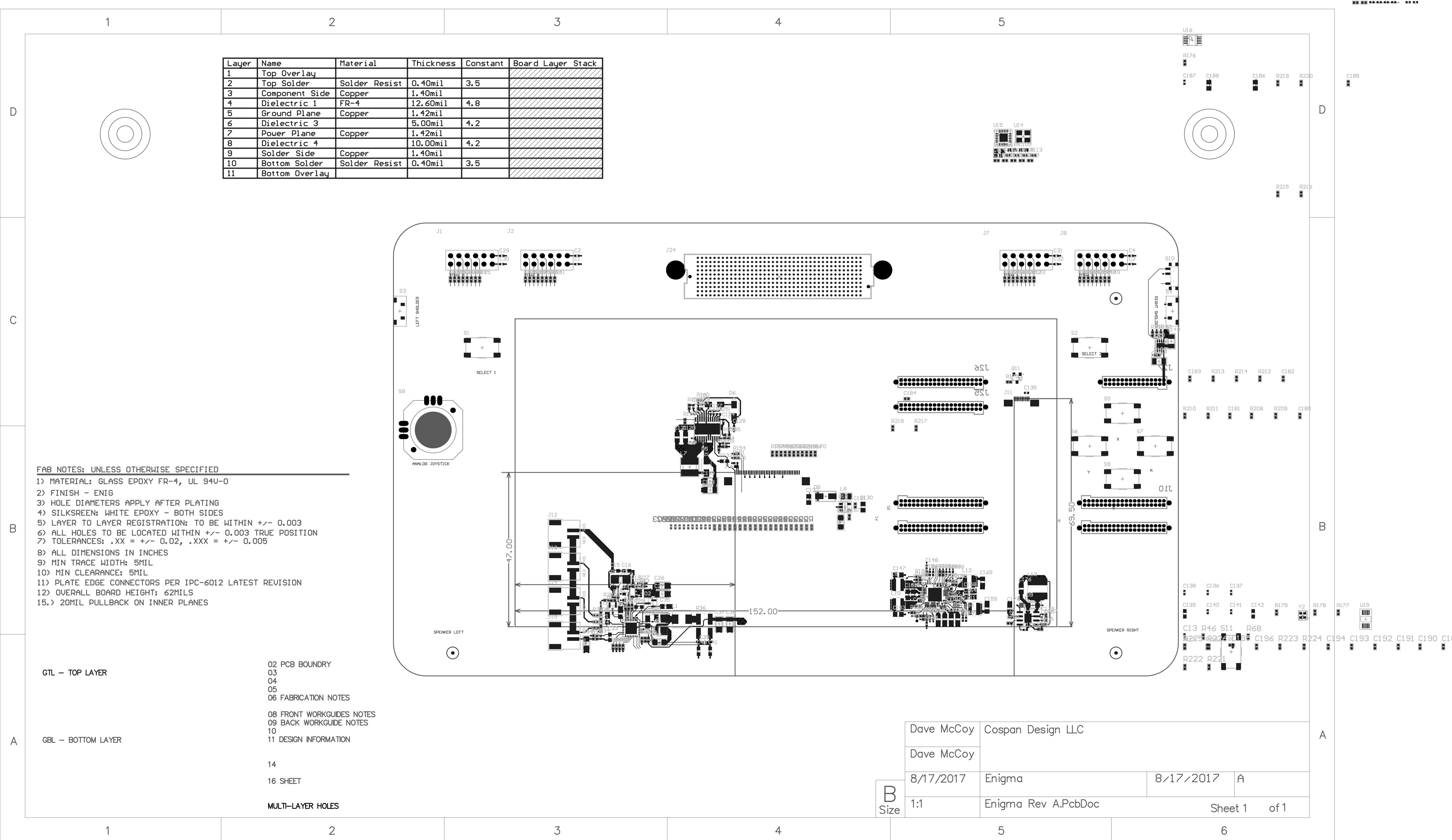
G

H

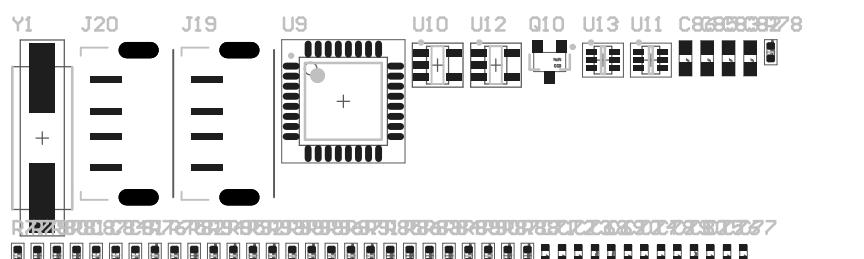
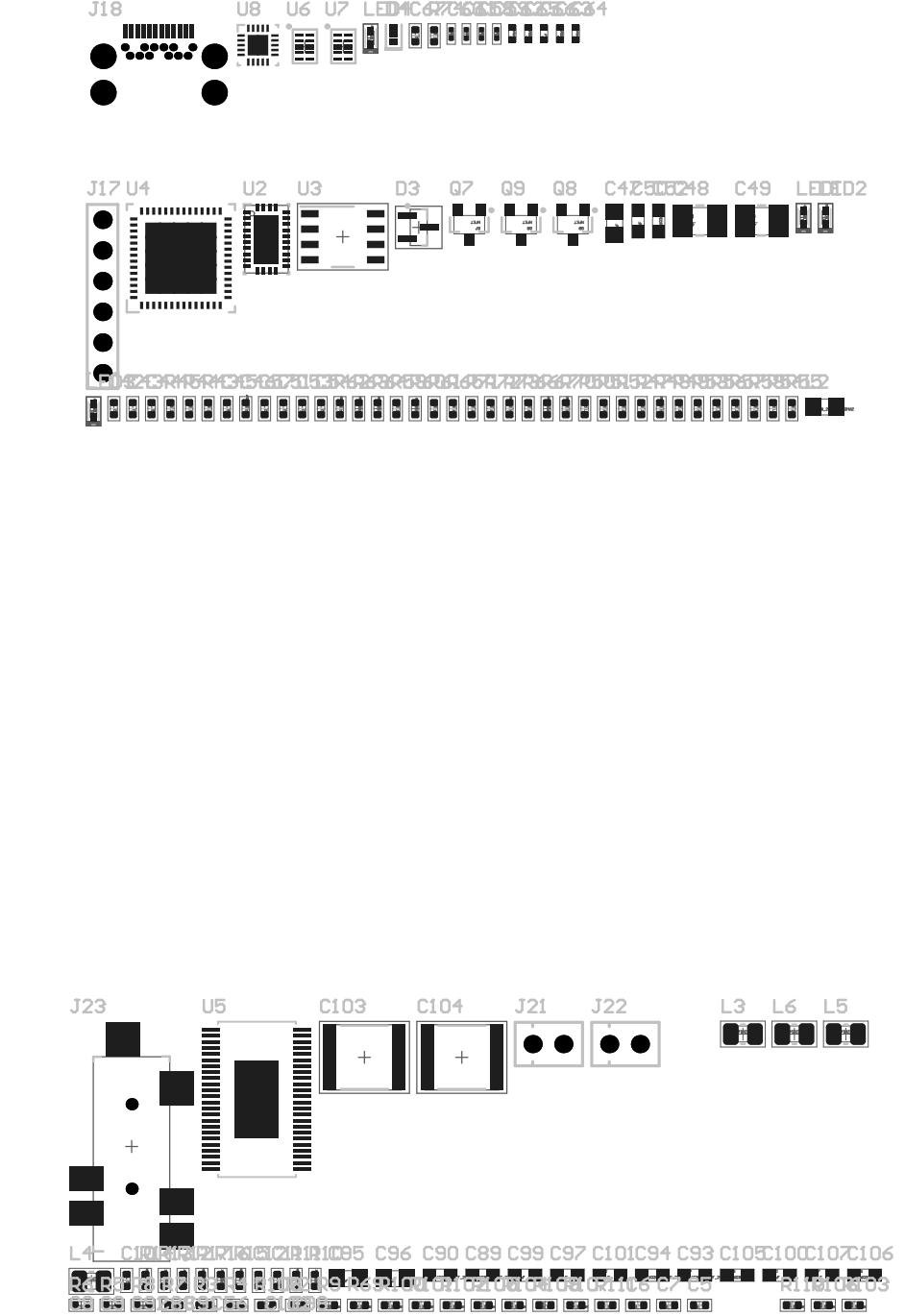
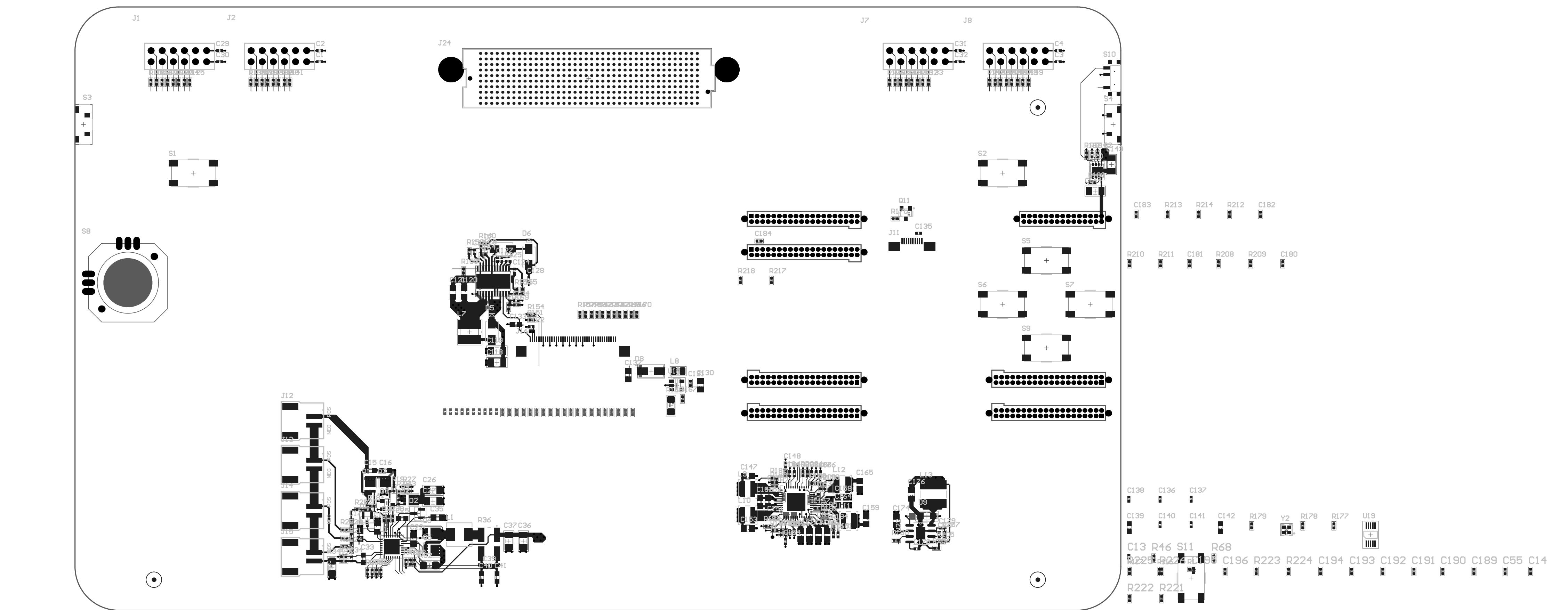
I

J

</div



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3		5.00mil	4.2	
7	Power Plane	Copper	1.42mil		
8	Dielectric 4		10.00mil	4.2	
9	Solder Side	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



GTL – TOP LAYER

GBL – BOTTOM LAYER

MULTILAYER HOLES

