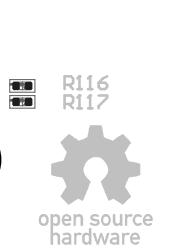


## 02 PCB BOUNDARY

## MULTI-LAYER HOLES

Snickerdoodle Carrier Board  
Enigma  
Rev: A



J7  
R99  
U12  
D126

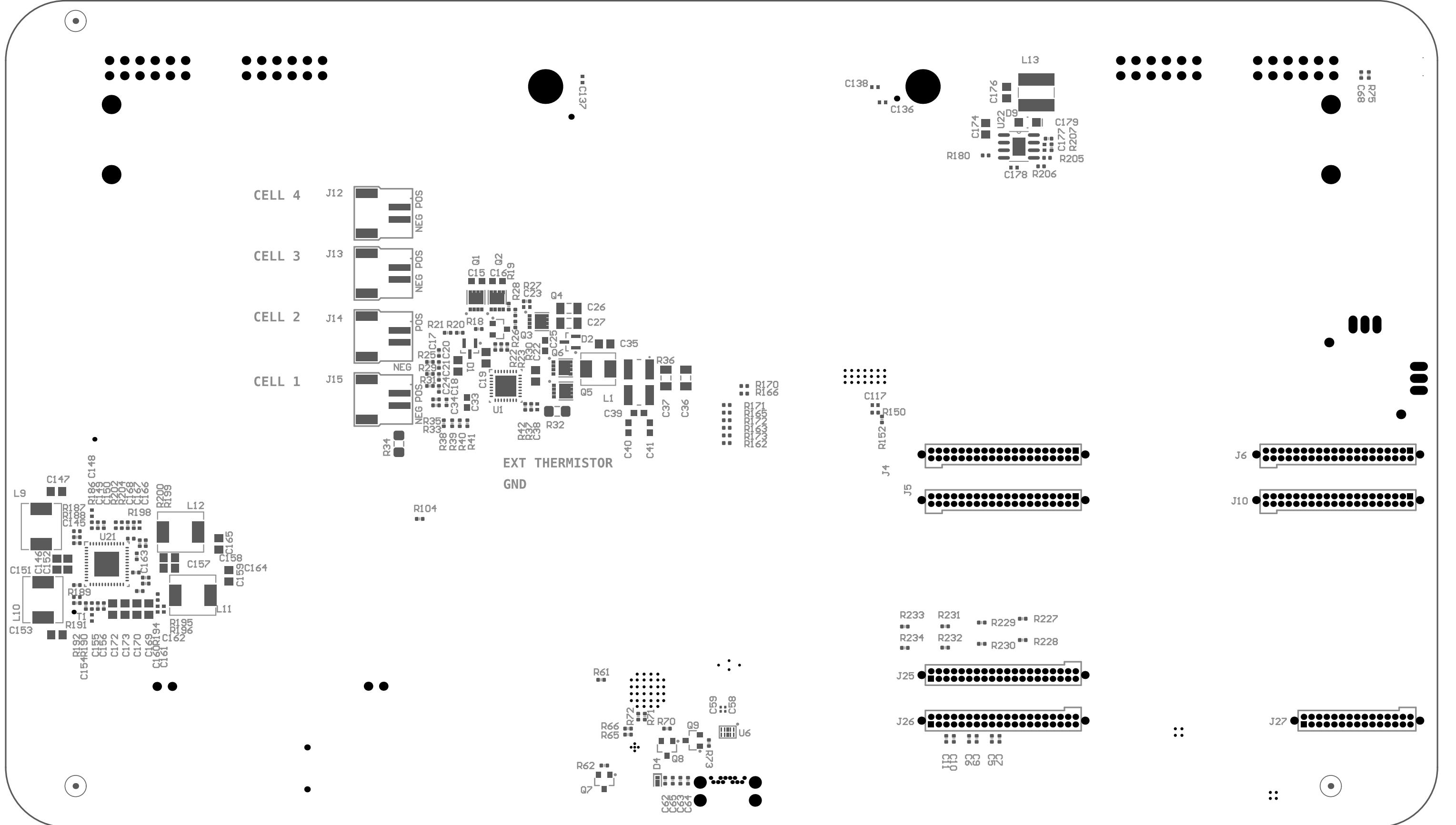
The diagram shows a portion of a printed circuit board (PCB) layout. On the left, there are two rectangular pads labeled C31 and C32, each containing four circular vias. To the right of these are two larger rectangular pads labeled C4 and C33, also with four circular vias. A horizontal line labeled J8 connects the top of C31 to the top of C32. Another horizontal line labeled J20 connects the bottom of C4 to the bottom of C33. Below C33, a vertical line labeled C86 extends downwards. To the far right, a component labeled U13 is shown with its pins connected to the PCB. On the far left, there are several small rectangular pads arranged vertically, with labels D0, D1, D2, D3, D4, D5, D6, D7, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, and R13 positioned below them.

INCH LCD CAP

+

The diagram illustrates the D100 architecture's data flow. It starts with two input images, each processed by a CNN (Convolutional Network) to produce feature maps. These feature maps are then processed by a shared backbone consisting of a ResNet-50 module followed by a Feature Pyramid Network (FPN). The FPN generates multi-scale feature maps. These are then processed by two parallel heads: one for semantic segmentation (producing a semantic map) and another for depth estimation (producing depth maps). The final outputs are the semantic map and depth maps.

U3P3  
U5PO  
U12PO  
UBAT  
VSYS



02 PCB BOUNDARY

MULTI-LAYER HOLES