**Modulul ierdna**

module ierdna (

input aral,atac,ide,icul,

output reg anao,anaid,luap

);

always @ ( ide or icul ) begin

if ( aral >= 0 ) begin

anao = icul + atac;

end

if ( aral >= 1 ) begin

anao = ide - atac;

end

if ( icul <= 0 && aral >= 1 ) begin

anaid = atac \* icul;

end

anaid = atac / icul;

luap = aral + atac + ide + icul;

end

endmodule

**Modulul ierdna\_tb**

module ierdna\_tb;

reg aral\_tb,atac\_tb,ide\_tb,icul\_tb;

wire anao\_tb,anaid\_tb,luap\_tb;

initial begin

$monitor (

$time, aral\_tb, atac\_tb, ide\_tb, icul\_tb, anao\_tb, anaid\_tb, luap\_tb );

end

initial begin

aral\_tb = 0;

atac\_tb = 0;

ide\_tb = 0;

icul\_tb = 0;

#1 aral\_tb = 1; atac\_tb = 1;

#1 aral\_tb = 0; ide\_tb = 1;

#1 aral\_tb = 1; atac\_tb = 1; ide\_tb = 1; icul\_tb = 1;

end

ierdna VasileLuNuti (

.aral(aral\_tb),

.atac(atac\_tb),

.ide(ide\_tb),

.icul(icul\_tb),

.anao(anao\_tb),

.anaid(anaid\_tb),

.luap(luap\_tb)

);

endmodule